## 13.2 A 45nm SOI-CMOS Dual-PLL Processor Clock System for Multi-Protocol I/O

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As processors emerge with multiple wireline interfaces for high-performance digital media, a common multi-protocol clock system is essential for cost and power reduction. We present a 45nm SOI-CMOS system that clocks an 8-lane processor I/O designed for PCI Express®, DisplayPort, and TMDS. Its ring-VCO PLL (RO-PLL) achieves 0.99ps rms jitter that can be reduced further to 0.55ps upon switching to its auxiliary LC-VCO PLL (LC-PLL). As seen in Fig. 13.2.1, the clock system contains the two independent frequency synthesizers, an arrangement of programmable dividers to provide the required frequencies, and clock distribution circuitry. Furthermore, design-for-test features are embedded to correct for PVT variation for optimum jitter performance and to monitor PLL bandwidth and jitter peaking.

PLLs built in ultrathin partially-depleted SOI are notoriously noisier than those built in bulk owing to floating-body noise that modulates device threshold voltage ($V_T$), which induces random jitter [1]. As such, meeting the low jitter specifications of embedded-clock protocols such as PCI-Express® can be especially challenging compared to meeting those of source-synchronous protocols, such as HyperTransport™, in which jitter tracking between transmitted data and accompanying forwarded clock facilitates higher receiver jitter tolerance.

The RO-PLL incorporates several features to minimize phase jitter and to maintain constant loop dynamics. The oscillation frequency is twice the required clock frequency for faster, lower jitter edges [2] and lower duty cycle distortion (DCD). Shown in Fig. 13.2.2, its ring-VCO stages employ narrow SOI transistors with lateral body ties depicted in Fig. 13.2.3 to help stabilize floating-body voltage noise. Our previous 45nm silicon demonstrates that employing such T-gates in the ring VCO alone suppresses phase jitter by 57% compared to using entirely floating-body devices in the PLL. An even more important noise-reduction technique is to insert source degeneration resistors in the VCO current sources. By attenuating noise arising from the highly resistive T-gate body connections, such feedback reduces phase jitter by 62%.

VCO gain (Hz/V) and tuning range tend to be naturally coupled. With larger-than-desired VCO gain translating to excessive PLL bandwidth and jitter, we decouple VCO gain and frequency tuning range by partitioning the VCO input control into a conventional path (7MHz bandwidth) and a much lower bandwidth (15kHz) path [4]. This slow path sets the *center* frequency, enabling (in our case) 75% lower VCO gain and noise sensitivity in the conventional control path. It employs a passive single-pole low-pass filter that connects to the integrating capacitor ($C_I$) of a conventional 2-pole/1-zero filter. Filtering charge pump and loop filter noise this way reduces simulated phase jitter from these sources by an estimated 70%. The otherwise long locktime, due to the slow-path time constant, can be contained to within 5µs by shorting across $R_{slow}$ during PLL exits from power-save states.

PLL bandwidth and peaking can be controlled by two digital state machines. The first automatically calibrates VCO gain at power-on. The PLL is first allowed to lock with the highest gain setting. The gain setting is subsequently decremented and the resulting control voltage is compared against a bandgap-derived reference until the control voltage reaches that reference level. The result is 43% less VCO gain variation across PVT. VCO gain calibration also reduces phase jitter by 15% since it maintains more constant VCO biasing currents. Moreover, with a more constant control voltage, reference spurs are reduced by as much as 9dB. The second state machine monitors the PLL bandwidth and jitter peaking by introducing a phase step transient in the reference clock and measuring the PLL relock time and overshoot [5]. These results may be used to determine optimal charge pump and loop filter resistor settings.

To minimize power supply-induced deterministic jitter, the PLL employs two 2.5V→1.2V regulators whose output voltage is based on a common bandgap reference. One regulator powers the sensitive analog circuits (charge pumps, loop filters, and VCOs) while the other is dedicated to the noisier digital circuits. Simulations indicate that each regulator exceeds 38dB of supply noise rejection.

The 10GHz LC-VCO (Fig. 13.2.4) is intended for 5.0Gb/s PCI Express operation, oscillating at four times the required clock frequency primarily to reduce inductor area as well as DCD. Narrow T-gate devices, with higher bandwidth floating-body connections, are used for cross-coupling and tail biasing to reduce channel noise and upconverted flicker noise respectively. Frequency is tuned using accumulation-mode thick-oxide decoupling capacitors for low series resistance and gate leakage. The LC-VCO is digitally coarse-tuned using a calibration sequence that averages across one 33kHz period at each setting to circumvent potential non-monotonicity that could arise when calibrating to a spread spectrum reference with 0.5% frequency modulation. Surrounding circuitry and noisy supply bumps are separated from the inductor to steer large switching currents away from the supply grid near the inductor in order to reduce coupling jitter magnetically into the LC tank.

The PLL was fabricated in a high-performance 45nm SOI-CMOS technology [6]. Wafers with poly-CD as well as $V_T$- and resistor-implant splits were also built. To save on mask cost to evaluate the 8-lane I/O, this design shared a reticle set with a small-footprint processor product. The I/O portion of each mask was appropriately bladed during each lithography exposure.

Typical packaged silicon results are summarized in Figs. 13.2.5 and 13.2.6 for a 2.5GHz output clock example with a 100MHz reference input. The LC-PLL frequency lock range is 8.3-11.1GHz while the RO-PLL locks across a much wider range of 1.0-8.5GHz. Measured phase noise was integrated from 1MHz to 1.25GHz to arrive at an rms jitter of 0.55ps and 0.99ps for the LC- and lower-Q RO-PLL respectively with corresponding reference spurs at -61.8 and -58.4dBc. Both designs show a 6.6MHz closed-loop bandwidth with peaking not exceeding 0.54dB. In-band spurs are common to both PLLs and attributed to noise in the off-chip switching regulator that powers the reference clock distribution. Silicon area is 0.277mm$^2$ with supply decoupling capacitors dominating the floorplan and the inductor occupying only 4% of the total area. The LC- and RO-PLL dissipate 24mA and 28mA respectively from a 2.5V nominal supply in which the majority of power is actually consumed in the digital circuits. By bypassing the bandgap output, the supply voltage can be reduced to 1.8V to lower the regulator output to 0.9V and the 28% power reduction incurs only 14% penalty in RO-PLL jitter. The 2.5V supply voltage, however, is dictated by non-PLL processor system requirements.

*References:*

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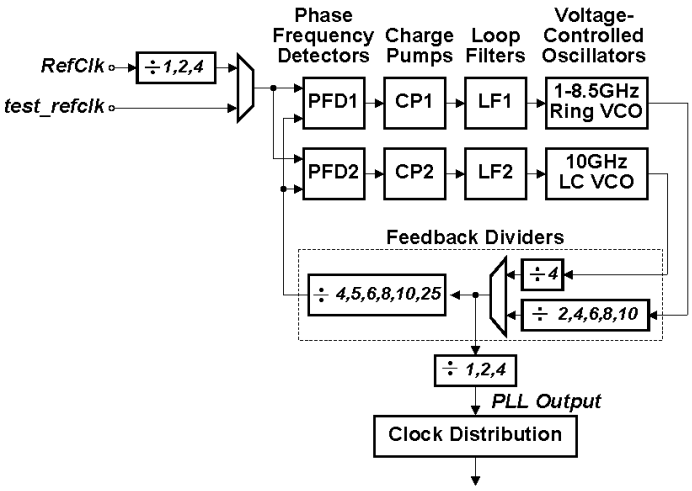


Figure 13.2.1: Block diagram of multi-protocol I/O clock system.

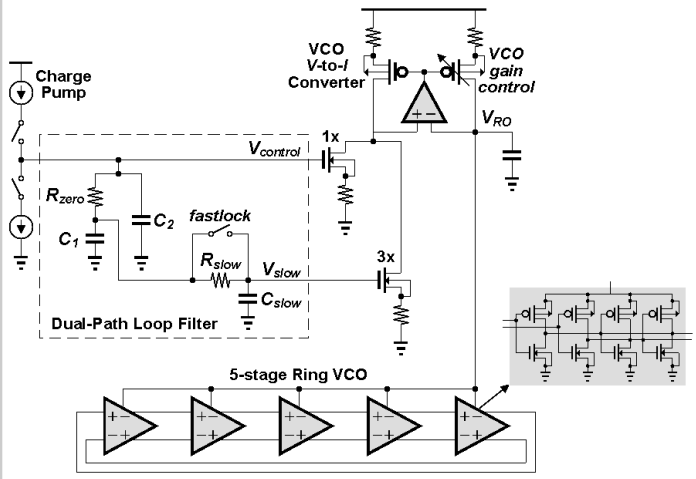


Figure 13.2.2: Schematic of ring-PLL dual-path loop filter and VCO.

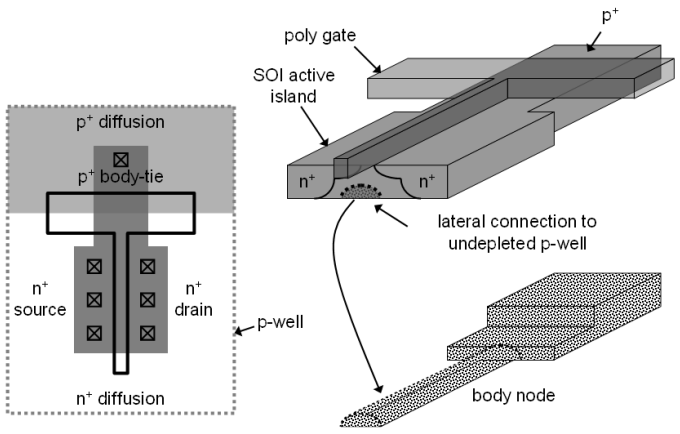


Figure 13.2.3: Body-tied nFET (T-gate) in partially-depleted SOI technology.

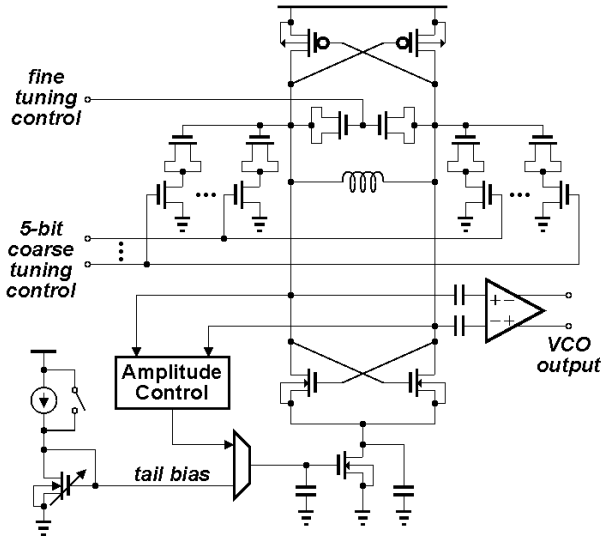


Figure 13.2.4: Schematic of LC-VCO.

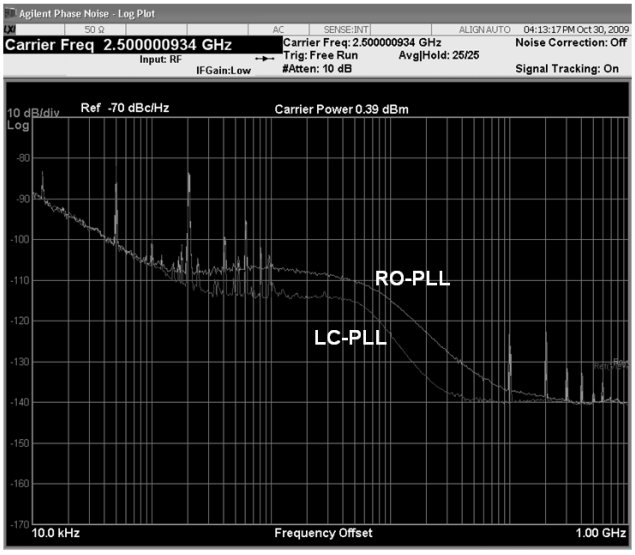


Figure 13.2.5: Measured phase noise (Agilent N9020A).

| Parameter | | RO-PLL | LC-PLL |
|---|---|---|---|
| Technology | | 45nm SOI-CMOS (36nm $L_{gate}$) | |
| Silicon Area | Total | 0.277mm$^2$ (388μm×715μm) | |
| | Inductor | 0.012mm$^2$ (120μm×104μm) | |
| Frequency Lock Range | | 1.0–8.5GHz | 8.3–11.1GHz |
| Output RMS Jitter (1MHz–1.25GHz) | | 0.99ps | 0.55ps |
| Phase Noise | At 1MHz Offset | –106.6dBc/Hz | –112.1dBc/Hz |
| | At 10MHz Offset | –114.9dBc/Hz | –123.4dBc/Hz |
| Reference | At 100MHz Offset | -58.4dBc | -61.8dBc |
| Jitter Transfer | -3dB Bandwidth | 6.6MHz | 6.6MHz |
| | Peaking | 0.41dB | 0.54dB |
| Static Phase Offset | | 16ps | 6.4ps |
| Supply Consumption | Current | 28mA | 24mA |
| | Voltage | 1.8–2.7V (2.5V nom) | |

Figure 13.2.6: Performance summary.

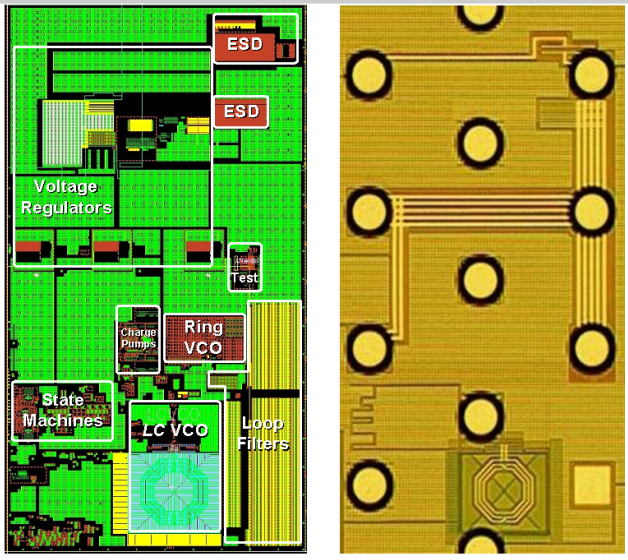


Figure 13.2.7: Die floorplan (left) and micrograph (right).


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