Constant-Current Threshold Voltage Extraction in HSPICE for Nanoscale CMOS Analog Design

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ABSTRACT

We present a substantially enhanced HSPICE feature that extracts MOSFET threshold voltage (V_T) based on the constant-current definition universally adopted by fabs to measure, specify, and monitor V_T. With simulated V_T now conveniently correlated to measurement, this capability enables faster design of robust analog circuits in cutting-edge CMOS technologies where voltage margins are critically limited and only predictive models, subject to periodic retargeting, are available during design. The feature was developed and evaluated using a 32-nm technology model and subsequently introduced in the 2009.09 HSPICE release. Operating point, DC, AC, and most importantly transient analyses are supported for industry-standard BSIM4, BSIMSOI4, and PSP MOSFET models.

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1. Introduction

The threshold voltage (V_T), defined fundamentally as the gate voltage at which a strongly inverted surface layer forms for channel conduction, is one of the most important parameters of a metal-oxide-semiconductor field-effect transistor (MOSFET). Yet the equation-based V_T computed by a circuit simulator such as HSPICE often does not match well to silicon measurement. This discrepancy is attributed to the difficulty of measuring the condition of strong inversion, especially in the presence of short-channel effects resulting from dimensional scaling of FETs [1], [2]. As an example, for a 32-nm minimum channel length device with linear V_T of 0.35 V, a drain voltage increase of 1.0 V will reduce the magnitude of V_T by 0.14 to 0.18 V, leading to markedly different V_T values in linear and saturation regions of operation. Supply voltage has also scaled to maintain device reliability, constraining FETs to operate with much less gate voltage overdrive (gate voltage in excess of V_T) particularly in analog designs where devices are typically biased into saturation for current source behavior. For a 1.0-V supply (V_{DD}), worst-case overdrives as low as 50 mV are sometimes necessary to support a stack of three devices across process as well as operating supply voltage and temperature corners. Finally, the use of predictive models to support design activity concurrent with process technology development has become a popular means of achieving faster product time to market, especially for cutting-edge processor ICs with long design times [3]. In this design environment, the extrapolative nature of device models requires modeling teams and circuit designers to respond quickly to periodic shifts in manufacturable technology targets. These realities raise the critical need for a circuit simulator to provide silicon-correlated V_T quickly and conveniently in order to facilitate rapid design of robust analog circuits with accurate operating margins.

This paper presents a substantially enhanced HSPICE feature that extracts V_T based on the constant-current method typically used in fabs to measure, specify, and monitor V_T. The feature was jointly developed by Synopsys, Advanced Micro Devices, and GLOBALFOUNDRIES. First, we summarize the device fundamentals of a basic long-channel MOSFET and its evolution with scaling so we can appreciate the non-idealities in a modern-day device and complexities in modeling V_T. Next, we cover the equation presently used by HSPICE to compute V_T to highlight the difficulty of physically measuring the V_T condition. We then review common silicon V_T measurement techniques and explain why the constant-current approach, despite its limitations, has become widely adopted in practice. Subsequently, we introduce the HSPICE `.OPTION IVTH` feature to extract the constant-current V_T, explain its usage, and provide a brief evaluation using a predictive BSIMSOI4.0 model of a 32-nm technology.

2. The Nanoscale MOSFET

The gate length of a state-of-the-art MOSFET has already scaled below 30 nm for early production. For decades, each new technology node has enjoyed increasing chip performance from relentless refining of the basic MOSFET to maintain its general behavior despite aggressive scaling. To appreciate the complexities in a modern-day device and the corresponding complexities in modeling V_T, we provide a tutorial of how the MOSFET physical structure has progressed to overcome scaling challenges.

Consider the basic *n*-type long-channel MOSFET with a uniformly doped *p*-type body of dopant concentration N_A [4], [5] as shown in Figure 1. The simplest depiction of a MOSFET is a 3-terminal voltage-controlled switch where the controlling gate terminal is electrically isolated from the body by an insulating silicon-dioxide-based dielectric. The gate voltage (V_{GS}) dictates if electron current can flow from source to drain. If V_{GS} falls below V_T, then the switch is off and no current can flow. If V_{GS} exceeds V_T, then the switch turns on and current will flow for some applied V_{DS}. The optional fourth or body terminal can be used to force V_{BS} to a known value to provide stable, noise-resilient transient control of V_T; this terminal is explicit in a bulk technology but absent in a silicon-on-insulator (SOI) technology [6].

Going further, we start with the MOSFET in the off state. At some offset voltage V_{FB} (flatband voltage) which depends on materials properties of the MOS system, the silicon surface directly beneath the gate oxide exhibits a uniform hole concentration of N_A and hence a surface potential (ϕ_s) relative to intrinsic silicon that is equal to the body potential (ϕ_b)

$$\phi_b = \frac{k_B T}{q} \ln \frac{N_A}{n_i} . \tag{1}$$

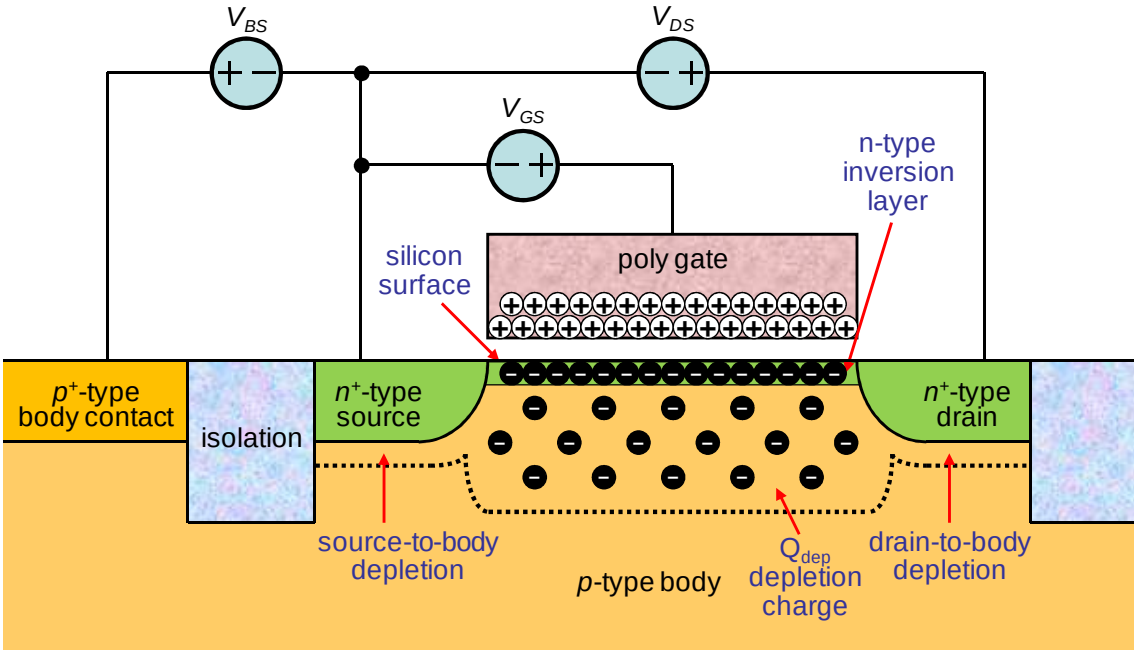

Figure 1 – Cross-section of basic *n*-type long-channel bulk MOSFET.

Here, k_B is Boltzmann's constant, T is absolute temperature, q is electronic charge, and n_i is the intrinsic concentration of electron and holes at temperature T. In this flatband condition, the silicon surface is *p*-type and forms rectifying *p*-*n* junction diodes with the n^+-type source and drain. If $V_{DS} > 0$, no appreciable current will flow along the silicon surface since the drain junction is always reverse-biased.

As we make V_{GS} more positive, the surface becomes less *p*-type and eventually inverted or *n*-type where electron concentration begins to exceed hole concentration. Continuing to increase V_{GS}, we come to invert the surface so heavily that the induced surface electron concentration is equal to the hole concentration in the body far away from the surface ($\phi_s = -\phi_b$). In this strong inversion or threshold condition, the corresponding V_{GS} is

$$V_T = V_{FB} + 2\phi_b + \frac{Q_{dep}}{C_{ox}} \tag{2}$$

where Q_{dep} is the total accompanying depleted charge (per unit gate area) in the body required for the surface to reach strong inversion, and C_{ox} or gate oxide capacitance (per unit gate area) is the ratio of gate dielectric permittivity (ε_{ox}) to gate dielectric thickness (T_{ox}). With an *n*-type surface connecting the n^+ source and drain, current can now readily flow with $V_{DS} > 0$ just like in a resistor. To reach threshold, the applied V_{GS} must move ϕ_s by ϕ_b to first reach the onset of inversion plus another ϕ_b to finally reach strong inversion. In the process, the accompanying depleted charge in the body generates a voltage drop across the gate oxide which must be supported by V_{GS}. This is illustrated in the electron energy band diagrams of Figure 2.

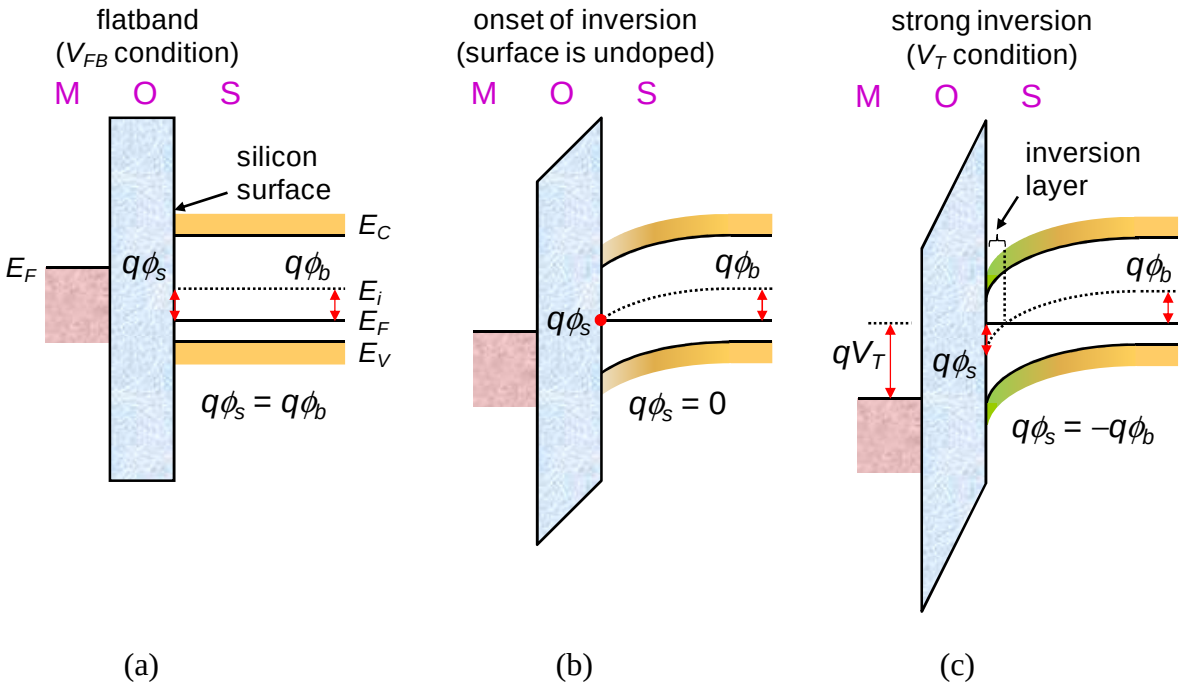

Figure 2 – MOS energy band diagram at (a) flatband, (b), onset of inversion, and (c) threshold.

The resulting source-to-drain current (I_{DS}) in the linear ($V_{GS} - V_{DS} > V_T$) and saturation ($V_{GS} - V_{DS} < V_T$) regions of operation are respectively given by

$$I_{DS} = \mu_N C_{OX} \frac{W}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \quad \text{and} \tag{3}$$

$$I_{DS} = \frac{1}{2}\mu_N C_{OX} \frac{W}{L}\left(V_{GS} - V_T\right)^2 \tag{4}$$

where μ_N is electron mobility, and W and L are respectively effective channel width and length.

Short-channel effects result when L is reduced so substantially that the source and drain depletion regions facing each other become significant fractions of the body charge that must be depleted to invert the silicon surface [7], [8]. Since these depletion regions exist independent of V_{GS}, they will reduce V_T as L scales down and constitute a loss of gate control over surface inversion. Furthermore, the V_T reduction is exacerbated by an increasing V_{DS} which widens the drain depletion region, an effect commonly known as drain induced barrier lowering (DIBL). Another drawback of L scaling is dramatic increases in channel electric fields resulting in velocity saturation of charge carriers (electrons and holes in *n*- and *p*-channel MOSFET respectively) which degrades carrier mobilities. The higher fields result from V_T and supply voltages not scaling as aggressively in proportion with L in order to avoid excessive subthreshold leakage [9].

Since the 180-nm node, the MOSFET structure of Figure 3 has become ubiquitous for mitigating short-channel effects.

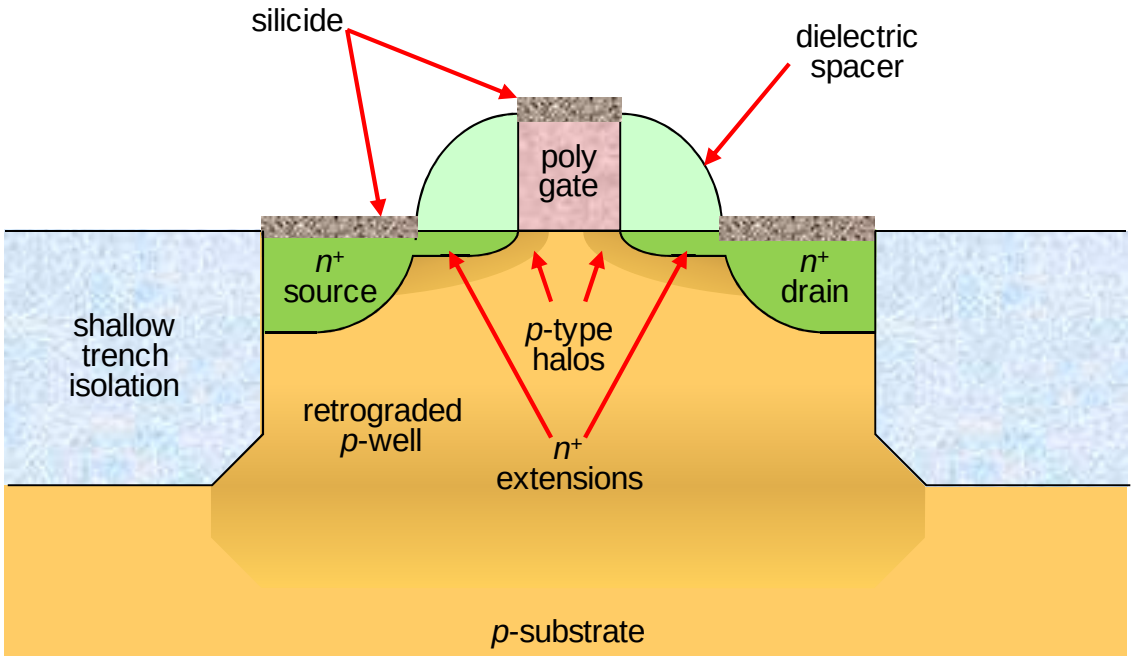

Figure 3 – N-channel MOSFET structure with halos and source/drain extensions.

First, the structure enables shallow high-tilt halo implants, self-aligned to the gate, to be incorporated under the edges of the gate to locally raise the body dopant concentration. Since the depletion region width of a one-sided p-n^+ junction

$$w \propto \frac{1}{\sqrt{N_A}} \quad , \tag{5}$$

the higher local doping of the halos pushes back the source/drain depletion regions away from each other. Moreover, as the doping is not increased throughout the length of the channel, V_T is not significantly increased. Second, by creating shallow n-type source/drain extensions to contact the channel, the source and drain depletion charge near the channel is contoured away from the region under the gate, thereby enabling more gate control. Although shallower junctions result in higher series resistance which degrades I_{DS}, the resistance is minimized by shortening the extensions with dielectric spacers that enable another self-aligned implant to form much deeper source/drain regions away from the extensions. Furthermore, the source/drain (as well as polysilicon gate) surfaces are typically strapped with a conductive refractory silicide to further reduce source/drain (and gate) resistance.

Better control of channel charge can be achieved with the controlling gate charge in closer proximity to the channel. As such, thinning T_{ox} has been effective for many technology nodes until direct gate tunneling contributed significant leakage current at 1 to 2 nm thickness. When T_{ox} scaling dramatically slowed down at the 90-nm node, the industry began introducing mechanical strain techniques to improve I_{DS} [10]. Since silicon is piezoelectric, as little as 1% crystalline strain along the channel will increase carrier mobilities by several times – electrons favor tensile while holes favor compressive strain. The strain is induced by intentionally surrounding the channel with stressors (material regions with built-in stress) such as nitride capping liners and embedded silicon-germanium (e-SiGe) source/drain [11]. As strain techniques become less effective with further scaling, high-ε_{ox} (high-K) gate dielectrics such as hafnium oxides are replacing conventional silicon oxides at the 45- and 32-nm nodes [12], [13], enabling C_{ox} to resume increasing without furthering the gate leakage penalty – higher ε_{ox} enables a thicker T_{ox} to reduce tunneling leakage while still increasing C_{ox}. With T_{ox} scaling also limited by high-resistivity polysilicon gate depletion, integrating high-ε_{ox} dielectrics necessitates polysilicon replacement with a metal gate material. The metal-gate/high-ε_{ox} system exhibits thermal stability issues and has inspired novel integration schemes such as replacement-gate for improved manufacturability.

With halos making the lateral source-to-drain body doping non-uniform, the vertical doping profile away from the silicon surface is also not uniform. The vertical doping is, in fact, retrograded with higher body or well doping deep beneath the silicon surface to prevent latch-up and provide better device isolation from underlying substrate noise and adjacent devices. These deep implants are commonly followed by a shallow surface implant to overcome the retrograded background doping for tighter V_T control.

The increased transistor density enabled by scaling has also made several layout proximity effects more pronounced starting at the 130-nm node. From the 250-nm node, chemo-mechanical polishing (CMP) has been used to form trenches filled with silicon dioxide for device isolation. Shallow trench isolation (STI) has since been enabling finer gate lithography since the reduced

surface topography resulting from CMP mitigates less depth of focus that comes with higher resolution printing. Unfortunately, the deposited oxide stress and oxide-to-silicon thermal expansion mismatch transfer compressive mechanical stress to the silicon islands. The result, known as the LOD effect [14], is degraded electron and enhanced hole mobilities where the extent of mobility change depends on the gate proximity to the surrounding STI. Another proximity effect is the well-proximity effect [15]. With tall photoresist needed to mask deep well implants, ion scattering off the resist sidewalls increases channel doping and consequently raises the magnitude of V_T. This effect is most pronounced for channels that are closest to the edges of well resist. For 65-nm nodes and beyond, V_T is also prone to similar layout proximities arising from mobility-enhancement stressors [16] although industry-standard MOSFET models are yet to incorporate these effects.

Although much of the preceding has focused on mitigating short-channel effects, narrow-channel effects also exist. For relatively narrow W (below 0.4 µm in 32-nm technology), V_T will either increase or decrease monotonically as W decreases. Although the classic narrow-width effect describes V_T as increasing in magnitude with decreasing W in obsolete LOCOS-isolated devices, the polarity of narrow-width V_T shifts in cutting-edge technologies is the result of complex competing phenomena specific to process integration choices. Furthermore, for similar reasons, these effects are not necessarily correlated between NMOS and PMOS.

We conclude with a micrograph of a 32-nm MOSFET illustrated in Figure 4. Compared to its long-channel ancestor, the modern-day MOSFET is the culmination of many evolutionary improvements that address device scaling effects. The electrical impact of these improvements must be accurately captured in a compact model of the MOSFET for that model to be usable.

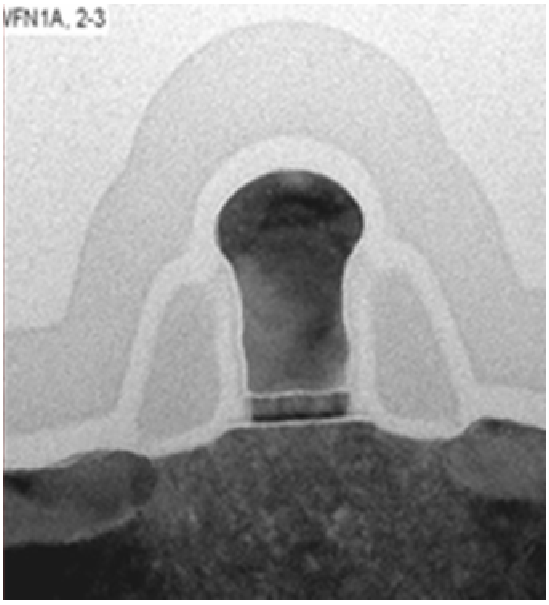

Figure 4 – Cross-sectional micrograph of 32-nm SOI-CMOS transistor with 30 nm L_{gate} [13].

3. Existing V_T Extraction in HSPICE

The current V_T reported by HSPICE (in the LV9 output template parameter [17]) is calculated using

$$
\begin{aligned}
V_T &= VTH0 + \left(K_{1ox}\cdot\sqrt{\Phi_s - V_{BSeff}} - K1\cdot\sqrt{\Phi_s}\right)\sqrt{1+\frac{LPEB}{L_{eff}}} - K_{2ox}V_{BSeff} \\
&+ K_{1ox}\left(\sqrt{1+\frac{LPEB}{L_{eff}}}-1\right)\sqrt{\Phi_s} + \left(K3 + K3B\cdot V_{BSeff}\right)\frac{TOXE}{W_{eff}^{'}+W0}\Phi_s \\
&- \left[\frac{DVT0W}{\cosh\left(DVT1W\frac{L_{eff}W_{eff}^{'}}{l_{tw}}\right)-1} + \frac{DVT0W}{\cosh\left(DVT1\frac{L_{eff}W_{eff}^{'}}{l_t}\right)-1}\right]\frac{V_{bi}-\Phi_s}{2} \\
&- \frac{ETA0 + ETAB\cdot V_{BSeff}}{\cosh\left(DSUB\frac{L_{eff}}{l_{t0}}\right)-1}\frac{V_{DS}}{2} - n\frac{k_BT}{q}\ln\left\{\frac{L_{eff}}{L_{eff}+DVTP0\left[1+\exp\left(-DVTP1\cdot V_{DS}\right)\right]}\right\}
\end{aligned}
\tag{6}
$$

which comes from the industry-standard BSIM model [18]. See [18] for a description of the parameters. With so many nanoscale MOSFET complexities, it should be surprising that a closed-form equation for V_T can even be formulated. However, Equation (6) starts with *VTH0*, the uniformly-doped long-channel V_T at V_{BS} = 0 given by Equation (2), and adds phenomenological fitting parameters to account for:

- Body effect (V_T increase when V_{BS} < 0 in NMOS and V_{BS} > 0 in PMOS),
- Short-channel effect including DIBL,
- Narrow-width effect,
- Non-uniform lateral doping due to halo implants,
- Non-uniform vertical doping due to surface implant and retrograded well doping,
- LOD effect from STI compressive stress, and
- Well proximity effect from implant mask scattering.

As such, this equation-based V_T still defines V_{GS} where an inversion layer forms in the channel region. Many higher order effects are described behaviorally for faster simulator computation.

One practical limitation of Equation (6) is that process technology advances, such as inclusion of new stressors, will introduce new V_T dependencies. Since the modeling effort can only capture these effects following silicon observation, an equation-based V_T model will always lag in its ability to correlate to new silicon even if silicon measurement could extract V_T marking the onset of strong inversion, which the following section will show is *not* the case.

4. Overview of V_T Measurement Techniques

We proceed to summarize popular past and present techniques for measuring V_T.

Linear and Quadratic Extrapolation Methods

We extract the linear V_T by sweeping I_{DS} vs. V_{GS} at some low V_{DS} value (typically 50 mV) and fixed V_{BS} such that the device directly enters its linear region upon turning on [19]. We then draw a tangent line to the measured curve at V_{GS} corresponding to the peak transconductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{7}$$

as shown in Figure 5(a) and extrapolate this line to the V_{GS} axis to determine the intercept V_{GS0}. Applying Equation (3), we obtain

$$V_{Tlin} = V_{GS0} - \frac{V_{DS}}{2}. \tag{8}$$

The peak-g_m condition is not fundamental but chosen simply to obtain a unique intercept given a gradual cutoff-to-linear subthreshold transition while minimizing series resistance effects.

We extract the saturation V_T by sweeping $\sqrt{I_{DS}}$ vs. V_{GS} at some fixed high value of V_{DS} (typically V_{DD}) and fixed V_{BS} such that the device enters saturation upon turning on. This method is known as quadratic extrapolation since the square-law relationship of Equation (4) is assumed [19]. For the same reason as above, we draw a tangent line to the measured curve at V_{GS} corresponding to peak $\partial\sqrt{I_{DS}}/\partial V_{GS}$ as shown in Figure 5(b) and extrapolate this line to the V_{GS} axis to determine the intercept V_{GS0}. Applying Equation (4), we obtain

$$V_{Tsat} = V_{GS0}. \tag{9}$$

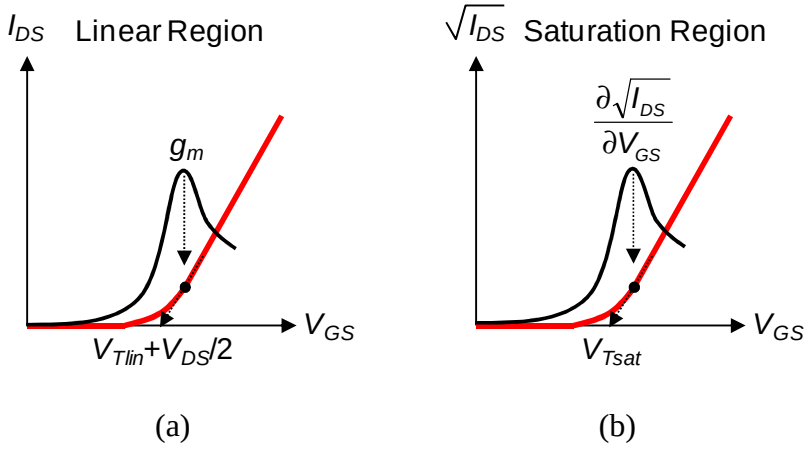

Figure 5 – Extrapolation method of V_T measurement in (a) linear and (b) saturation regions.

These methods rely on ideal long-channel behavior and clearly assume that Equations (3) and (4) hold in the linear and saturation regions respectively. Unfortunately, the assumptions break down in short-channel devices where velocity saturation effects are dominant and thereby invalidate the use of I_{DS} and $\sqrt{I_{DS}}$ vs. V_{GS} plots to extrapolate V_{GS0} consistently. Hence, these methods are no longer applicable despite popularity in past decades.

Constant-Current Method

We sweep log I_{DS} vs. V_{GS} and choose V_{DS} for either linear or saturation operation as shown in Figure 6 [20], [21]. V_{BS} is also held constant. V_T is simply defined as V_{GS} when I_{DS} matches some user-specified current threshold $I_0 \times W_{drawn} / L_{drawn}$

$$V_T = V_{GS}\Big|_{I_{DS}=I_0\times\frac{W_{drawn}}{L_{drawn}}} . \tag{9}$$

I_0 is typically between 50 and 500 nA. Since W_{drawn} and L_{drawn} are drawn layout dimensions, no auxiliary measurements are needed to extract effective W and L. The constant-current method is a fast, simple, and consistent method for extracting linear and saturation V_T as well as DIBL:

$$DIBL = V_{Tlin} - V_{Tsat} . \tag{10}$$

This method is undoubtedly the most practical and widely used today for measuring, specifying, and monitoring V_T. It does not assume any particular I_{DS} relationship such as Equations (3) and (4). I_0 can be user- and/or process-specific and can evolve with process technology advances. As such, the key limitation is the lack of an obvious physical connection between the chosen I_0 and the onset of strong inversion. However, this shortcoming invariably exists in all other measurement methods since the threshold condition fundamentally cannot be determined as ϕ_s and ϕ_b are not electrically measurable quantities.

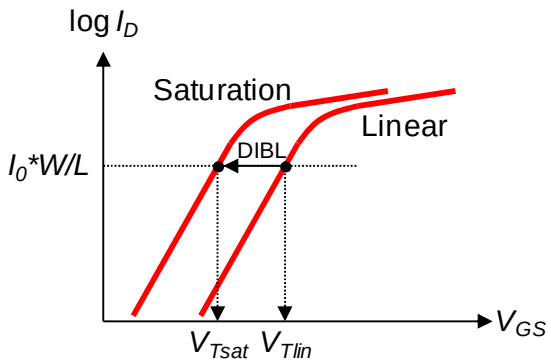

Figure 6 – Constant-current method of V_T measurement.

Other Methods

The reader is referred to [19] for a summary of other techniques, such as the transconductance change method. They are not discussed here as they require complex extractions and are impractical for routine V_T measurements.

5. HSPICE `.OPTION IVTH` Usage

Introduced in the 2009.09 release, HSPICE simulations now compute constant-current V_T the exact same way V_T is measured in the fab. This `.OPTION IVTH` feature is supported for Levels 54 (BSIM4), 69 (PSP100), and 70 (BSIMSOI4) MOSFET models. Shown below is the relevant excerpt from the 2009.09 *HSPICE® Reference Manual: Commands and Control Options* [22].

> **.OPTION IVTH**
> Invokes a constant-current threshold voltage probing and characterization function for BSIM4 models.
> **Syntax**
> `.OPTION IVTH=val | IVTHN=val | IVTHP=val`
> **Description**
> Specifies the ivth constant drain terminal current density, to be multiplied by the ratio of transistor width (W) and length (L). The value must be greater than zero to enable the function; the `IVTH` option should always be set to a positive value for both PMOS and NMOS. `.OPTION IVTH` has been enhanced to support HSPICE BSIM4 (level 54), BSIMSOI4.x (level 70) and PSP (level 69). `.OPTION IVTHN` and `IVTHP` support NMOS and PMOS, respectively.
> **Note:** The `val` should be a constant.
> In OP analysis, a constant-current-based `vth` is reported in the OP output. In addition, the element region operation check and Vod output are based on the new `vth`. During transient or DC analysis, a template output of LX142 accesses the new `vth` value. `LX142(m*)` or `ivth(m*)` could be used for the new `vth` output. This methodology is based on the monotony Id/Vgs curve.

At each evaluation instance, HSPICE determines V_{GS} that makes I_{DS} equal the current threshold based on V_{GS}, V_{DS}, and V_{BS} at that instant. The current threshold is `IVTHN*W/L` for NMOS, `IVTHP*W/L` for PMOS, or `IVTH*W/L` for the case `IVTHN=IVTHP`. If I_{DS} cannot reach that threshold, e.g., in the case when $V_{DS} = 0$, HSPICE reports $V_T \approx 0$, e.g., 10^{-29}. Depending on the type of analysis performed, evaluation instance refers to the operating point itself in a `.OP` analysis, a point along a particular voltage or current sweep in a `.DC` analysis, a single frequency in a `.AC` analysis, or a specific moment in time in a `.TRAN` analysis. The constant-current V_T result is accessed by probing the `LX142` output template as documented in the 2009.09 *HSPICE® Reference Manual: MOSFET Models* [17].

Name	Alias	Description	MOSFET Level
vth	LV9	Threshold voltage (bias dependent)	All
ivth(m*)	LX142 (m*)	New vth output, based on the monotony Id/Vgs curve obtained through .OPTION IVTH; ivthn and ivthp support NMOS and PMOS, respectively	54, 69, 70

As an example, the following HSPICE input deck statements specify a constant-current threshold of 100 nA × W_{drawn} / L_{drawn} for both NMOS and PMOS in a transient analysis:

```
.OPTION IVTHN=100e-9 IVTHP=100e-9
.OPTION BYPASS=0
.PROBE TRAN LX142(m*)
```

Since `IVTHN=IVTHP` in this example, we can alternatively declare:

```
.OPTION IVTH=100e-9
.OPTION BYPASS=0
.PROBE TRAN LX142(m*)
```

Adding `.OPTION BYPASS=0` [22] is presently required for reliable `.TRAN` simulation results in the 2009.09 release.

6. Evaluation of New Feature

We validated the functionality of `.OPTION IVTH` using a predictive BSIMSOI4.0 MOSFET model (Level 70) for a 32-nm partially-depleted SOI technology [13]. Both floating-body and body-tied devices [23], [24] were tested. A floating-body MOSFET does not have an explicit body terminal while a body-tied MOSFET mimics a bulk MOSFET using the lateral body connection shown in Figure 7.

Simulations compared the constant-current-based `LX142` vs. equation-based `LV9` with

```
.OPTION IVTHN=300e-9 IVTHP=70e-9
.OPTION BYPASS=0
.PROBE [DC|AC|TRAN] LX142(M*) LV9(M*)
```

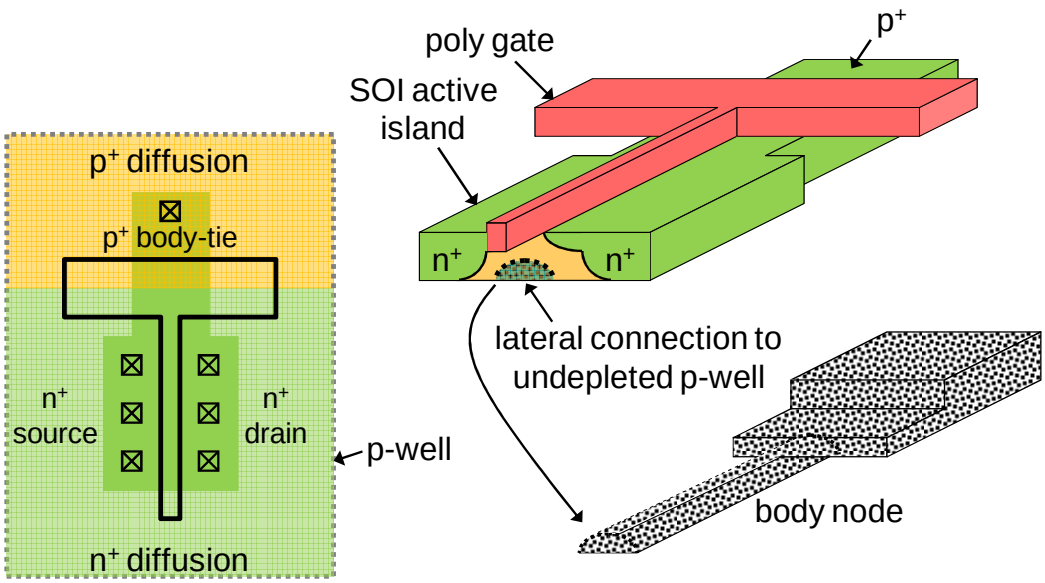

Figure 7 – Body-tied NMOS in partially-depleted SOI technology [24].

Constant-current thresholds of 300 nA × W_{drawn} / L_{drawn} for NMOS and 70 nA × W_{drawn} / L_{drawn} for PMOS were chosen for consistency with fab measurements. In our test examples, we simulated floating-body NMOS and PMOS with W_{drawn} / L_{drawn} = 2 × 1 µm / 40 nm:

```
Mn  drainn gaten sourcen vnsub TNSSFR w=1 l=0.04 m=2
Mp  drainp gatep sourcep vpsub TPSSFR w=1 l=0.04 m=2
```

Here, the source nodes (`sourcen` and `sourcep`) and substrate nodes below the SOI buried oxide (`vnsub` and `vpsub`) were grounded. `TNSSFR` and `TPSSFR` refer to our SOI device model names. Multiple (two) fingers were declared to verify that the constant-current thresholds were correctly multiplied by `m`.

During co-development, initial testing demonstrated expected functionality in `.OP`, `.DC`, and `.AC` analyses which was mostly adequate for device modeling needs. Further testing revealed that the feature needed to be extended to `.TRAN` analyses. Most analog/mixed-signal design effort relies primarily on transient simulations that are only occasionally complemented by `.OP`, `.DC`, and `.AC` analyses.

DC Verification of `.OPTION IVTH` *Functionality*

To illustrate that `.OPTION IVTH` did indeed extract the constant-current V_T as described in Figure 5, we performed DC sweeps of V_{DS} from 0.0 to 1.0V at V_{GS} of 0.05 and 1.00 V to extract V_{Tlin} and V_{Tsat} respectively. Results are shown in Figures 8(a) and 8(b). The V_T values reported by `LX142` did indeed match the NMOS and PMOS V_{Tlin} and V_{Tsat} extracted at current thresholds of 15 and 3.5uA respectively.

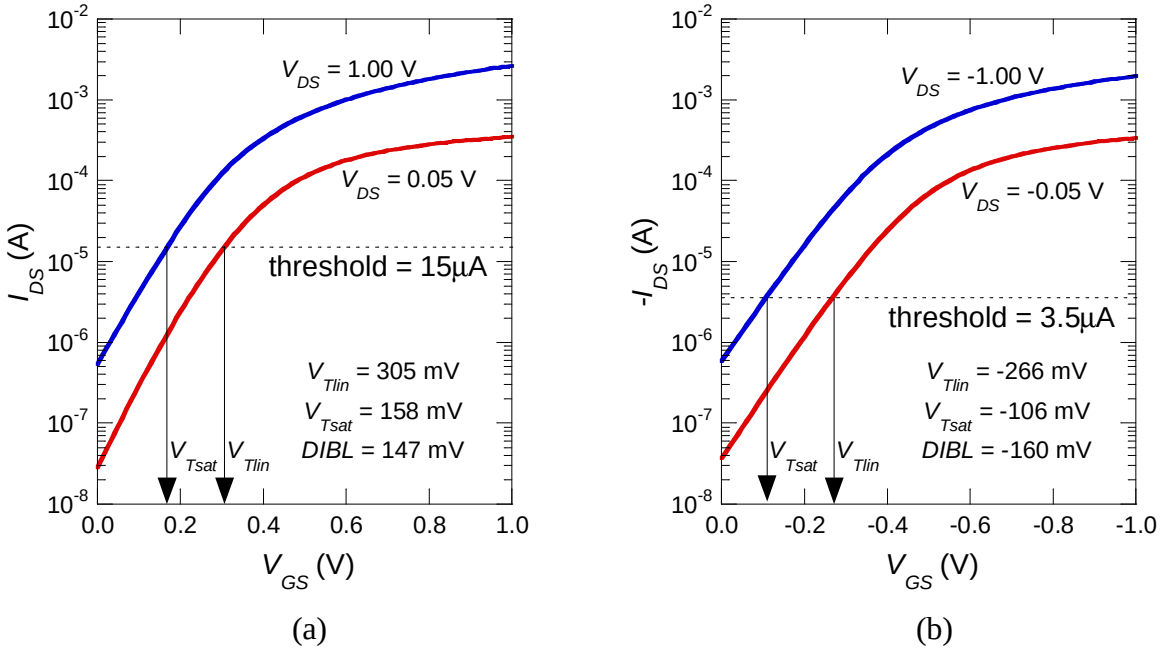

Figure 8 – `.DC` simulation to extract constant-current V_T for SOI (a) NMOS and (b) PMOS.

Transient Test Case 1: V_{DS} Ramp at Fixed V_{GS}

We ramped the magnitude of V_{DS} from 0.5 to 0.9 V with magnitude of V_{GS} fixed at 0.6 V. Results are shown in Figure 8. Notice that the NMOS and PMOS magnitudes of `LX142` are 125–136 mV and 214–226 mV lower than the respective magnitudes of `LV9`. Naturally, we expect some discrepancy between NMOS and PMOS since `IVTHN` ≠ `IVTHP` but the differences between `LX142` and `LV9` are clearly significant especially in low-V_{DD} design. This clearly demonstrates the difficulty to match `LV9` from simulations to silicon measurement. Notice also that the polarity of PMOS `LV9` is incorrectly positive while the polarity of `LX142` accurately reflects the device type (positive for NMOS and negative for PMOS). Not surprisingly, $|V_T|$ decreases with increasing $|V_{DS}|$ due to DIBL. For a V_{DS} change of 0.4 V, the 56 and 66 mV $|V_T|$ reductions for NMOS and PMOS respectively are in line with expectation.

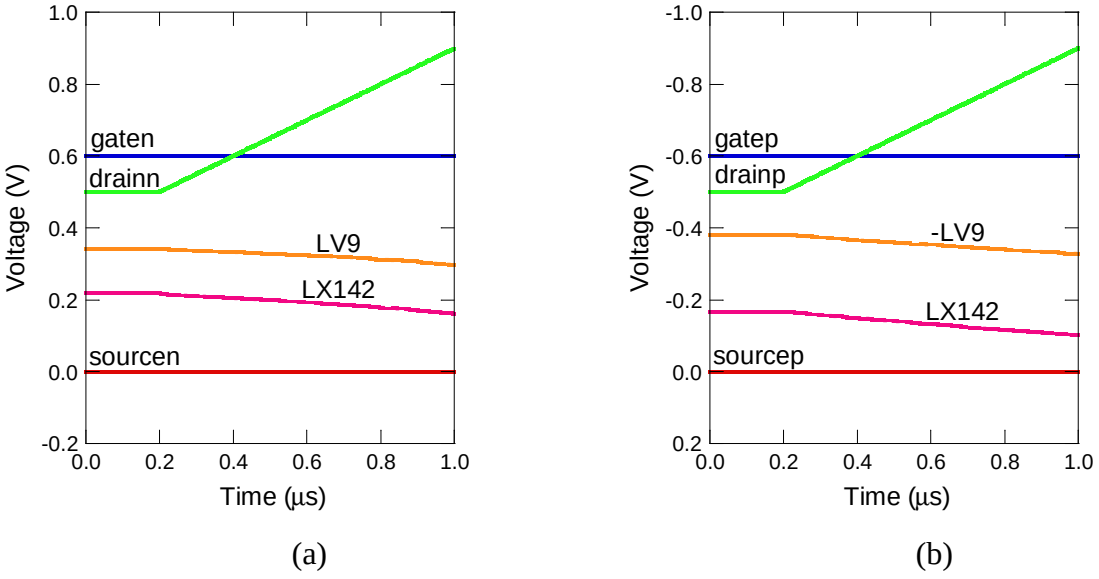

Figure 9 – . TRAN simulation of V_{DS} ramp at fixed V_{GS} for SOI (a) NMOS and (b) PMOS.

Transient Test Case 2: V_{GS} Ramp at Fixed V_{DS}

We ramped the magnitude of V_{GS} from 0.0 to 1.0 V with magnitude of V_{DS} fixed at 0.5 V. Results are shown in Figure 9. Since V_{DS} was fixed to preclude V_T shifts related to DIBL, one would expect no V_T change as V_{GS} was ramped. Upon closer inspection, we notice the `LX142` magnitudes reduce by 6.8 and 36.3 mV for NMOS and PMOS respectively during the 1.0-V V_{GS} ramp. When the V_{GS} ramp rate was reduced by 10×, the respective V_T shifts were reduced to 5.6 and 17 mV. So the V_{GS} transient ramp was capacitively coupling to the floating body of each device, thereby raising the body potential slightly and lowering the magnitude of V_T (reverse body effect) [25]. We additionally confirmed this observation by repeating a similar test using the body-tied devices of Figure 7 in which the body connection was shorted to the device source to pin the body voltage. As expected, no `LX142` shifts were observed as V_{GS} was ramped.

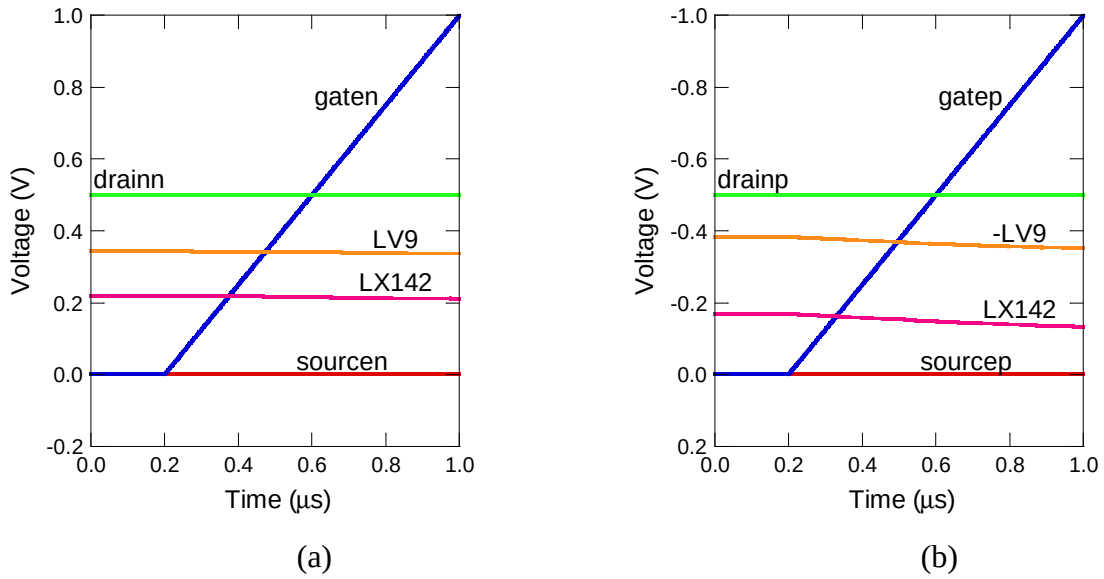

Figure 10 – `.TRAN` simulation of V_{GS} ramp at fixed V_{DS} for SOI (a) NMOS and (b) PMOS.

Transient Simulation Runtime

We conducted a brief evaluation of simulation runtime to assess the impact of using `.OPTION IVTH`. Since `.OP`, `.DC`, and `.AC` simulation runtimes are seldom of concern, we concentrated on `.TRAN` simulations. Our test circuit was a bandgap voltage reference similar to [26] since bandgap references have extensive analog content and designing one would especially benefit from `.OPTION IVTH`. As seen in Table 1, there was a significant impact on runtime when `.OPTION BYPASS=0` was enabled which forced more computation at each time step. However, this option is presently compulsory to ensure reliable `LX142` results. Further HSPICE development is needed to remove the `.OPTION BYPASS=0` requirement.

Table 1 – Impact of `.OPTION IVTH` on simulation runtime.

.OPTION IVTH	.OPTION BYPASS	Normalized Simulation Runtime
Disabled	Default	1.0
Enabled	Default	1.2
Enabled	0	2.3

7. Conclusions

We have presented an HSPICE feature that extracts MOSFET V_T the same way it is measured in the fab using the constant-current approach, enabling circuit designers and modeling engineers to compare simulated to measured V_T conveniently and directly. Such correlation has become increasingly critical given the necessarily limited gate overdrives in low-voltage analog design and the pervasive usage of predictive models for faster time to market. Although the constant-current measurement does not have an obvious physical connection to the fundamental definition of V_T, it is the practical technique of choice owing to its measurement simplicity in dealing with short-channel effects and other device non-idealities. Hence, it is prudent that circuit simulators offer a convenient way to provide this extraction of V_T.

The full feature has been introduced in the 2009.09 release of HSPICE and supports `.OP`, `.DC`, `.AC`, and `.TRAN` analyses with Level 54 (BSIM4), 69 (PSP100), and 70 (BSIMSOI4) MOSFET models. The feature is specified using

`.OPTION IVTHN=`*`val1`* `IVTHP=`*`val2`*

for fab- and technology-specific I_{DS} thresholds of *`val1`*`*W/L` for NMOS and *`val2`*`*W/L` for PMOS. The extracted V_T is reported in the `LX142` output template. This feature is especially important in `.TRAN` simulations since the majority of analog/mixed-signal simulations are really `.TRAN` analyses occasionally complemented by `.OP`, `.DC`, and `.AC` analyses. Since `.TRAN` simulations are by far the most runtime-intensive, we request optimization of the HSPICE engine so that `.OPTION IVTH` can operate reliably without `.OPTION BYPASS=0`.

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9. References

[1] R. Dennard, F. Gaensslen, H.-N. Yu, L. Rideout, E. Bassous, and A. LeBlanc, "Design of ion-implanted MOSFETs with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. SC-9, no. 5, pp. 256–268, Oct. 1974.

[2] G. E. Moore, "No exponential is forever but 'forever' can be delayed," in *IEEE Int. Solid-State Circuits Conf.* (San Francisco, CA), pp. 20–23, Feb. 2003.

[3] L. Bair, "Process/product interactions in a concurrent design environment," in *Proc. IEEE Custom Integrated Circuits Conf.* (San Jose, CA), pp. 779–782, Sep. 2007.

[4] D. L. Pulfrey and N. G. Tarr, *Introduction to Microelectronic Devices*. Englewood Cliffs, NJ: Prentice-Hall, 1989, ISBN 0-13-488107-9.

[5] R. F. Pierret, *Semiconductor Device Fundamentals*. Reading, MA: Addison-Wesley, 1996, ISBN 0-201-54393-1

[6] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. 3rd ed. New York, NY: Springer, 2004, ISBN-10 1402077734.

[7] H. S. Lee, "An analysis of the threshold voltage for short-channel IGFETs," *Solid-State Electron.*, vol. 16, pp. 1407–1417, 1973.

[8] L. D. Yau, "A simple theory to predict the threshold voltage of short channel IGFET," *Solid-State Electron.*, vol. 17, pp. 1059–1063, 1974.

[9] J. McPherson, "Reliability trends with advanced CMOS scaling and the implications for design," in *Proc. IEEE Custom Integrated Circuits Conf.* (San Jose, CA), pp. 405–412, Sep. 2007.

[10] S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-process-induced strained-Si: extending the CMOS roadmap," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1010–1020, May 2006.

[11] V. Chan, K. Rim, M. Ieong, S. Yang, R. Malik, Y. W. Teh, M. Yang, and Q. Ouyang, "Strain for CMOS Performance Improvement," in *Proc. IEEE Custom Integrated Circuits Conf.* (San Jose, CA), pp. 667–674, Sep. 2005.

[12] K. Mistry *et al*., "A 45nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging," in *IEEE Int. Electron Device Meeting Tech. Dig.* (Washington, DC), pp. 247–250, Dec. 2007.

[13] M. Horstmann, A. Wei, J. Hoentschel, T. Feudel, T. Scheiper, R. Stephan, M. Gerhadt, S. Krügel, and M. Raab, "Advanced SOI CMOS transistor technologies for high-performance microprocessor applications," in *Proc. IEEE Custom Integrated Circuits Conf.* (San Jose, CA), pp. 149–152, Sep. 2009.

[14] R. A. Bianchi, G. Bouche, and O. Roux-dit-Buisson, “Accurate modelling of trench isolation induced mechanical stress effect on MOSFET electrical performance,” in *IEEE Int. Electron Device Meeting Tech. Dig.* (San Francisco, CA), pp. 117−120, Dec. 2002.

[15] T. B. Hook, J. Brown, P. Cottrell, E. Adler, D. Hoyniak, J. Johnson, and R. Mann, “Lateral ion implant straggle and mask proximity effect,” *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1946–1951, Sep. 2003.

[16] A. Sultan, J. Faricelli, S. Suryagandh, H. van Meer, K. Mathur, J. Pattison, S. Hannon, G. Constant, K. Kumar, K. Carrejo, J. Meier, R. O. Topaloglu, D. Chan, W. Hahn, T. Knopp, V. Andrade, B. Gardiol, S. Hejl, D. Wu, J. Buller, L. Bair, A. Icel, and Y. Apanovich, “CAD utilities to comprehend layout-dependent stress effects in 45 nm high-performance SOI custom macro design,” in *IEEE Int. Symp. Quality of Electronic Design* (San Jose, CA), pp. 442–446, Mar. 2009.

[17] Synopsys HSPICE® Reference Manual: MOSFET Models. Version C-2009.09, Sep. 2009.

[18] W Yang, M. V. Dunga, X. Xi, J. He, W. Liu, K. M. Cao, X. Jin, J. J. Ou, M. Chan, A. M. Niknejad, and C. Hu, *BSIM4.6.2 MOSFET Model User's Manual*, Regents Univ. California, Berkeley, CA, 2008.

[19] D. K. Schroder, *Semiconductor Material and Device Characterization.* New York, NY: Wiley-Interscience, 1990, ISBN 0-471-51104-8.

[20] H. G. Lee, S. Y. Oh, and G. Fuller, “A simple and accurate method to measure the threshold voltage of an enhancement-mode MOSFET,” *IEEE Trans. Electron Devices*, vol. ED-29, no. 2, pp. 346–348, Feb. 1982.

[21] X. Zhou, K. Y. Lim, and D. Lim, “A simple and unambiguous definition of threshold voltage and its implications in deep-submicron MOS device modeling,” *IEEE Trans. Electron Devices*, vol. 46, no. 4, pp. 807–809, Apr. 1999.

[22] Synopsys HSPICE® Reference Manual: Commands and Control Options. Version C-2009.09, Sep. 2009.

[23] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. Ko, and C. Hu, “A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation,” in *IEEE Int. Electron Device Meeting Tech. Dig.* (San Francisco, CA), pp. 809–812, Dec. 1994.

[24] D. M. Fischette, A. L. S. Loke, M. M. Oshima, B. A. Doyle, R. Bakalski, R. J. DeSantis, A. Thiruvengadam, C. L. Wang, G. R. Talbot, and E. S. Fang, “A 45nm SOI-CMOS dual-PLL processor clock system for multi-protocol I/O,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers* (San Francisco, CA), pp. 246–247, Feb. 2010.

[25] S. Krishnan and J. G. Fossum, “Grasping SOI floating-body effects,” *IEEE Circuits and Devices Mag.*, vol. 14, no. 4, pp. 32–37, Jul. 1998.

[26] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, May 1999.

