OEB-SPS&CS

You are invited to an IEEE Meeting on
Thursday, Oct. 25, 2012

Title: # Decisions, decisions… Multi-core, GPGPU or FPGA for data-intensive computing?

Speaker:	**Maya Gokhale**, Lawrence Livermore National Laboratory
Date:	Thursday, October 25, 2012
Time:	Presentation from 12:30 PM – 1:30 PM
Cost:	No charge
Place:	Livermore Valley Open Campus (LVOC) – Bldg. 6475 Lawrence Livermore National Laboratory Greenville Road, Livermore, CA Building 6475 is located south of the Eastgate Drive entrance off of Greenville Road. Follow signs to the HPC Innovation Center. The building is located behind the UNCLE Credit Union.
RSVP:	**Please make a reservation by Oct. 24** by e-mailing Brock Beauchamp (brockb@ieee.org)

Meeting Description:

Data intensive applications developers find a bewildering variety of parallel hardware, software tools, and libraries from which to build high bandwidth solutions. For the highest performance (and highest pain) specialized or programmable hardware (i.e. FPGA) may be required, but for an increasing body of use cases, commodity programmable processors are viable, especially for signal and image processing needs. In this talk, I will describe the landscape of hardware alternatives from FPGAs to many-core programmable processors, software and productivity tools that promise to transform your processing pipeline from block diagram to hardware with a few clicks of the mouse, and our experience with mapping machine learning analytics algorithms onto multi-core processors, GPGPU, and FPGA.

This abstract was prepared under the auspices of the Department of Energy by Lawrence Livermore National Laboratory under Contract DE-AC52-07NA27344 (LLNL-ABS-586712)

About the Speaker:

Maya Gokhale is a computer scientist in the Computation Directorate of LLNL. Her career spans research conducted in academia, industry, and National Labs, most recently Los Alamos National Laboratory. Maya received a Ph.D. in Computer Science from University of Pennsylvania in 1983. Her current research interests include data intensive architectures and reconfigurable computing. Maya is co-recipient of three patents related to memory architectures for embedded processors, reconfigurable computing architectures, and cybersecurity; an R&D 100 award for a C-to-FPGA compiler; and an Intelligence Community Award. She is co-author of more than one hundred technical publications. Maya is a member of Phi Beta Kappa and a Fellow of the IEEE.