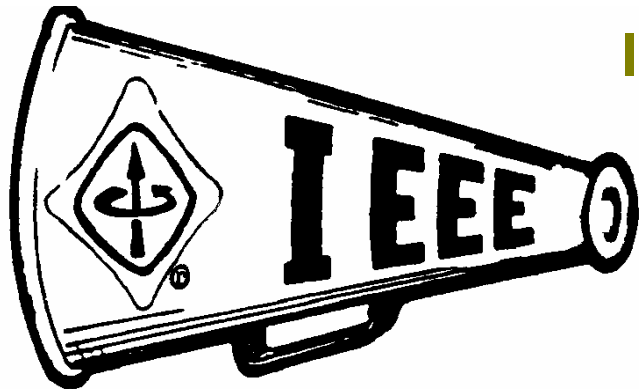


The Valley Megaphone



Newsletter of the
**IEEE – Institute of Electrical and
Electronic Engineers, Inc.
Phoenix Section**

April 2003, Volume XVII, Number 4

Executive Committee

Past Chair

Charles A. Smith, 480-814-6617
Smith@ieee.org

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James E. Drye, 480-413-5685
Jdrye@ieee.org

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George Karady, 480-965-6569
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Mike Andrews, 480-991-1619
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Membership

Open

Student Activities

Keith E. Holbert, 480-965-8594
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This Issue of Valley Megaphone Features:

Contacts and Links

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Volunteer Needed for Membership Chair

IEEE Phoenix section is seeking nomination for membership chair for 2003. Being an officer helps you to improve your leadership skills in addition to serve the local technical community, network with colleagues both at local and national level. It is also a stepping stone for getting involved in national level technical organizations. If you are interested or you know someone that is interested in this opportunity, please contact section chair James E. Drye at 480-413-5685 or Jdrye@ieee.org. You must be an active member of IEEE for this position.

Executive Committee contd..

Awards

Vasu Atluri, 480-554-0360
vpatluri@ieee.org

Inter-Society

Mike Andrews, 480-991-1619
m.andrews@ieee.org

Web Master

Chandan K. Das, 480-554-1300
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Comm & Signal Processing

Junshan Zhang, 480-727-7389
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diane@fuseki.com

Consultants Network (PACN)

Paul Everett, 480-706-4753
peverett@ieee.org

CPMT Society

Rao Bonda, 480-413-6121
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EMC Society

Harry Gaul, 480-441-5321
Harry.gaul@ieee.org

.....Contd... on page 2

The Valley Megaphone is the newsletter of the Phoenix Section of the Institute of Electrical and Electronics Engineers. It is published monthly, September through June. The publication reaches about 4000 members. Submit articles, advertisements, and announcements to Dongming He at the above email address. Deadline for announcements and advertisements is the third Friday of the month prior to publication.

Advertising Rates: Full page: \$200, 3/4page: \$125, 1/2 page: \$75, 1/3 page:\$50,1/4 page:\$25. Change of address/email? Call toll free 1-800-678-IEEE. Please allow 6-8 weeks. Section Web Page is : <http://www.ieee.org/phoenix>



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IEEE ANNOUNCEMENTS

Chapters & Branches

[Contd.. from page 1](#)

Power Engineering Society
Chuck Russell, 602-236-0975
csrussell@srpnet.com

Waves & Devices Society
Bruce Kim, 480-965-3749
bruce.kim@asu.edu

GOLD
Vasu Atluri, 480-554-0360
vpatluri@ieee.org

Student Branches

ASU Engineering Student Branch
Chair: Maziar Brumand
Maziar.Brumand@asu.edu
Advisor: Tony Rodriguez, 480-965-3712
aar@asu.edu

ASU Computer Society Chapter
Chair: Kalyan Chamarthi
Kalyan.c@asu.edu
Advisor: Joseph Urban, 480-965-3374,
joseph.urban@asu.edu

ASU Engr. Tech Student Branch
Chair: Esaki Soundarajan
Esaki.Soundarajan@asu.edu
Advisor: Dr. Raji Sundararajan, 480-727-1507
Raji@asu.edu

DeVry Student Branch
Chair: Chris Leno, chrisleno@ieee.org
Advisor: Gary Bryan, 602-870-9222
gebryan@devry-phx.edu

DeVry Computer Society Student Branch
Chair: Christopher Roan, chris_roan@computer.org
Advisors: Terri Barnes, 602-870-9222
tbarnes@devry-phx.edu, Diane Smith
602-870-9222, dianesmith@devry-phx.edu

NAU Engineering Student Branch
Chair: Lamont Serbousek lgs6@dana.ucc.nau.edu
Advisor: Peter Blakey, 928-523-3493
Peter.Blakey@nau.edu

NAU Computer-Society Student Branch
Chair: Billy Olsen, wdo@dana.ucc.nau.edu
Advisor: Phil Mlsna, 928-523-2112
Phillip.Mlsna@nau.edu

Embry-Riddle Student Branch
Chair: Brook Heiling, bheiling@heitek.biz
Advisor: Steve Chadwick, 928-777-6980
chadw202@erau.edu

Embry-Riddle Computer Society Student Branch
Chair: Andrew Soroker, sorok3b8@erau.edu
Advisor: Susan Gerhart, (928) 777-3882
gerharts@erau.edu

IEEE Senior Member and Fellow Grades

All IEEE Phoenix Section Members interested in getting nominated to Senior Member or Fellow Grade, please contact Vasu Atluri by telephone at (480) 554-0360 or by email at vpatluri@ieee.org. Please refer to www.ieee.org for more information related to senior member and fellow grades.

IEEE Phoenix Section Graduate of the Last Decade (GOLD) Affinity Group

Volunteers are needed to serve as officers for IEEE Phoenix Section Graduate Of the Last Decade (GOLD) Affinity Group. Volunteers should be active IEEE members from IEEE Phoenix Section who have obtained their first professional degree, preferably a Bachelor of Science in Engineering, within last decade. If interested, please contact Vasu Atluri by telephone at (480) 554-0360 or by email at vpatluri@ieee.org. Please refer to www.ieee.org for more information related to GOLD Affinity Group.

Consultants Network Announcement

The next meeting of the IEEE Phoenix Area Consultants Network will be held on Thursday, April 10 at Monti's La Casa Vieja at the southwest corner of Mill Ave and Rio Salado Parkway in Tempe. Networking and the social hour begin at 6:30 with dinner starting about 7 PM. Ed Mischen will present the program "Intellectual Property, Part 2 – Trade Secrets and Patents". This is very useful information for all of us whether we are independently employed or have day jobs. Ed is a very good speaker, and his Part 1 presentation in February was very well received. The two presentations are independent, and Part 1 (which was on trademarks and copyrights) is NOT a prerequisite for Part 2. Everyone is welcome. If you want to skip dinner, just come around 8 for the program. There is no charge for the program, and dinner is only \$10. Please let us know by sending an email to peverett@everettinfrared.com if you are planning to come so that we can make sure that Monti's sets aside a large enough room for us. We had such a big crowd last month that we had a minor overflow problem.

The Network will have its annual family picnic in May and will not have a regular dinner meeting. We will be back at Monti's in June with a presentation by Bruce Johnson on "Electric Windmills".



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COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Encapsulated Processors for 10 GHz and Beyond

Bob Carroll

Chief Technology Officer, Primarion, Inc. Tempe AZ

ABSTRACT

Process technology keeps advancing at a pace that may put a 10 GHz processor in our hands by 2005-2007 timeframe. But, there is a number of system related technology scaling issues that we need to deal with, before a 10GHz processor system becomes a reality. Large and fast transient current demands from the 10 GHz processor, whose operating voltage and noise margin will be much lower than the prevalent levels, will demand a whole new power delivery system based on a wide-band power architecture. Also, system performance will be limited by the inefficiencies of the traditional I/O interconnect structure that lacks the required bandwidth and robustness to keep up with the increasing core speeds. Chip-to-chip optical interconnects will be the alternative technology that may enable us to utilize the benefits of the 10 GHz technology to their fullest potential. An encapsulated processor with integrated power delivery and optical I/O is the way to go for reaching 10 GHz and beyond. This talk will be on the enabling technologies that will help us reach this goal and will discuss the packaging design challenges on the way.

BIOGRAPHY

Bob Carroll is the Chief Technology Officer of Primarion, the semiconductor company that develops technologies to bring fiber to processors for communicating at the speed of computing. Before becoming the CTO, Bob was the Vice President of Engineering at Primarion, overseeing the development of all Primarion wideband power and optical datacom technologies and products. Before joining Primarion, Bob has served as Director of Communications and Networking, at MITRE Corporation, and Director of Microelectronics prior to that. Bob also managed Hughes Aircraft Company's Advanced Circuit Development where he led the design of high-performance mixed signal products.

Date: Tuesday, April 15th, 2003.
Location: Motorola, 2100 E. Elliot Rd., Tempe, AZ (Group Conference Room). (Entrance to the facility through the main (south) lobby by the flagpoles. You will be escorted to the Conference Room.)
Time: 5:30-6:00 p.m. - Social/Refreshments; 6:00-7:00 p.m. - Presentation; 7:00 p.m. Dinner
IEEE members & non-members are welcome. Refreshments, pizza & soda provided by CPMT Society Phoenix Chapter.

For more information, please call any of the following officers:

Mali Mahalingam, Motorola (480) 413-5368	Rao Bonda, Motorola (480) 413-6121
Eric C. Palmer, Intel (480) 554-8710	Sam Karikalan, Primarion (602) 659-4634
Ravi Sharma, Microchip (480) 792-7920	Vasu Atluri, Intel (480) 554-0360



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COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Bruce Freyman of Amkor Technology receives IEEE CPMT Society's "Electronics Manufacturing Technology Award"



IEEE CPMT Society announces that Mr. Bruce Freyman (Amkor Technology, Chandler, AZ) is the recipient of the "Electronics Manufacturing Technology Award" for the year 2003. This award is given yearly to recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society. The CPMT Society has chosen Mr. Freyman for this award to recognize his pioneering work in developing the PBGA package and for his vision and drive in making the PBGA package and its format commercially successful.

Bruce serves as Corporate Vice President of Product Operations at Amkor Technology, the world's largest subcontract assembler of I.C. packages and the world's largest manufacturer of ball grid array (BGA) packages. He is the co-inventor and co-developer of the overmolded plastic ball grid array and holds 13 patents pertaining to array packaging technology.

Bruce has spent over twenty years in the semiconductor packaging business; the last ten years have been with Amkor. Prior to joining Amkor, Bruce was I.C. Packaging Manager at Motorola's Communications Sector, Plantation, FL. He led the Motorola team of engineers and scientists that developed the first plastic ball grid array (PBGA) and implemented the technology into hand-held communications equipment. Bruce was responsible for developing an outside packaging source for the first plastic ball grid array which was initially called an Over Molded Pad Array Carriers (OMPAC). This effort was a first in introducing PBGA's into portable products.

Bruce left Motorola to join Amkor Technology to commercialize Motorola's OMPAC (now called PBGA) technology. He negotiated with Motorola for the first commercial license for OMPAC technology in 1993. Subsequently, he led the group at Amkor who installed the first high volume PBGA capacity that enabled the entry of the PBGA into widespread usage for ASICs, graphics chips, and chipsets in the P.C. industry. Bruce and the Amkor Sales Team were the first messengers of PBGA technology at virtually every major semiconductor company in the world during 1993 and 1994. Bruce is responsible for Amkor's product and business management, corporate research and development, worldwide test, and process engineering groups. Prior to his current assignment with Amkor, Bruce managed Amkor's Laminate Packaging Group including the plastic ball grid array, Chip Array™ and *fle*XBGA™ product families.

Bruce holds a Masters in Business Administration and a B.S. in Chemical Engineering.

For information about this and the other IEEE CPMT Awards, please visit the CPMT Society website, www.cpmt.org.

Rao Bonda, Ph.D.

Chair, Awards and Recognition

IEEE Components, Packaging and Manufacturing Technology Society



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COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Dennis Olsen receives IEEE CPMT Society's "Outstanding Contribution Award"



IEEE CPMT Society announces that Dr. Dennis Olsen (Consultant and Motorola retiree, Scottsdale, AZ) is the recipient of the "David Feldman Outstanding Contribution Award" for the year 2003. This award is given yearly to an individual for outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial direction. The CPMT Society has chosen Dr. Olsen for this award to recognize his exceptional service to the CPMT Society and his outstanding contributions to electronic materials and packaging.

As a member and officer in several IEEE organizations, Dennis served with distinction since joining the IEEE CPMT in 1983. For over two decades, he has demonstrated his leadership in IEEE CPMT and in electronic materials, assembly and packaging technologies. While representing Motorola's Semiconductor Products Sector, he held leadership roles in both industry-sponsored organizations and university-industrial programs and consortia for electronics packaging research. In Motorola, he earned the recognition as a "Distinguished Innovator" and received the "Patent of the Year Award" in 1993. His patents covered a broad spectrum of electronic packaging, ranging from a state-of-matter patent for a lead-free solder alloy to a probe card for -testing unencapsulated semiconductors for known-good-die applications. His work in semiconductor packaging included the development of assembly processes for low cost manufacturing of diodes, small signal transistors, and silicon power products; and the management of the process and packaging R&D for advanced packaging applications, such as hybrid power modules, flip-chip bonded microcontrollers, TAB bonded bipolar ASIC devices, and packaging integrated pressure sensors.

Dennis organized the Phoenix IEEE CPMT Chapter and was elected as the first Chapter Chair. Under his leadership, the CPMT Chapter became the most active IEEE chapter in the Phoenix Section by establishing strong technical programs and successful educational workshops. In the Phoenix Section of the IEEE, he served as Membership Chair, Secretary, and Vice Chair during 1993-95. In the IEEE CPMT Society, he was elected to the Board of Governors in 1985 and 1988, and was Vice President of Administration between 1990 and 1994. He was elected President of the IEEE CPMT Society in 1994.

Since his retirement from Motorola in 1998, Dennis has worked as a consultant for solder interconnections used in optical and power products and electrical motor connectors, and as a visiting scientist in the Microelectronics Group at the Institute for Materials Research and Engineering (IMRE) in Singapore.

For information about this and the other IEEE CPMT Awards, please visit the CPMT Society website, www.cpmt.org.

Rao Bonda, Ph.D.
Chair, Awards and Recognition
IEEE Components, Packaging and Manufacturing Technology Society



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COMPUTER SOCIETY ANNOUNCEMENT

The Computer Society's second meeting of the year was great success. Sixty three (63) people came to hear Randy Brown's great talk on Communication Trends and Technologies. Thank you, to all the people who supported the Computer Society by attending the meeting and helping get out the word about the meeting. If you have not made it to a Computer Society meeting this year, mark your calendar, we hope to see you April 22.

On Tuesday April 22, Rajeev Arora will discuss Java and E-collaboration. Electronic communications today are based a two way voice telephone system that was started in the late 1800s and one way television broadcasts that were started in the late 1940s. E-mail is the web analog of telephone and HTTP is the web analog for TV. Rajeev sees totally new paradigms. He will talk about "Instant Meeting" a collection of new technologies for sharing: whiteboards, documents, voice, and notes over vast distances. The Tuesday April 22 will be held at DeVry University (2149 West Dunlap Ave, Phoenix, Arizona 85021 (1 mile east of I-17 on Dunlap, SE corner of 22nd Ave and Dunlap). More information is posted on our website (www.ieee.com/phoenix/compsociety). Print out a flyer and post it at work.

IEEE Senior Members - Only 3% of the Phoenix Computer Society members are Senior Members. Nation wide, 10% of The IEEE are Senior Members. We are starting an initiative to double the number of Phoenix Computer Society Senior Members. Being a IEEE Senior Member does not raise or lower you annual dues. It is a recognition by your professional peers in the IEEE of your experience and accomplishments. When the IEEE elevates you to a Senior Member, the National IEEE sends a letter to your employer so they can share your recognition and you receive a wood plaque. Many IEEE Senior Members choose list their recognition in on their resume/CVs. To become an IEEE Senior Member you need ten (10) years of professional engineering experience. Education counts toward the 10 years (3 years for a BS, 4 for MS, and 5 for PhD). At least five of those years must demonstrate significant achievements. Walking on water or winning the Noble Prize would definitely demonstrate significant achievement. Not there yet? Don't worry! In reality most software engineers with 10 to 12 years engineering experience, have been performing significant achievements for the last five years. Please see the IEEE page for overall information <http://www.ieee.org/organizations/rab/md/smprogram.html>. See the Phoenix Computer Society web page www.ieee.org/phoenix/compsociety for more details. If you have more than ten years of experience as a software engineer, you should consider being elevated to an IEEE Senior Member. The first step is yours. Please contact my self (either at an IEEE Computer Society meeting or by e-mail (Bob.Bianca@computer.org)) or any Computer Society officer. We are ready to review your experience statement, nominate you (serving as one reference), and help you contact two other IEEE Senior Members to serve as references.

Jobs – Discussions with members at our recent meetings indicate the economy is tough and a number of members are looking for jobs. We have members with many years of excellent experience and a new crop of graduating students. Based on a discussion at the Phoenix Section Executive Committee meeting we are adding a page on our web site with pointer to open jobs. If you or your employer have an opening for the software engineer or other computer professionals, send us (Bob.Bianca@computer.org) a twenty five word blurb (job title or micro description, contact (name, e-mail, or phone), and pointer to your web page for more information). We will list the blurb for 45 days, so please send an update each month and tell us to remove it when the job is filled). Note: if you work for a large company, your company has policies on who can list jobs, for your protection please go through you management and/or HR department. Your hiring managers and HR reps are welcome to come to Networking Hour at the beginning of each Computer Society meeting to meet members.



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Development of Oxides on Silicon by Molecular Beam Epitaxy

Ravi Droopad

Motorola Labs, Physical Sciences Research Laboratories,
7700 S River Parkway, Tempe AZ 85284

Tel: (480) 755 5358, ravi.droopad@motorola.com

Abstract

One of the main problems facing the semiconductor industry to the continuing reduction in the size of Si CMOS devices, is the scaling of the gate dielectric. Presently, SiO₂ is being used but at a thickness below 20 Å it suffers from high tunneling leakage current and reliability problems. Alternative high-k materials to replace SiO₂ need to be developed as soon as possible. The alkaline earth oxides such as barium strontium titanate (Ba_xSr_{1-x}TiO₃) and LaAlO₃ have a substantially higher dielectric constant than SiO₂ and are ideal candidates for gate dielectrics. Because of their higher dielectric constant a physically thicker layer can yield an equivalent oxide thickness of <20 Å, thereby eliminating the leakage problems experienced with ultra-thin SiO₂. These oxides also exhibit ferroelectric behavior and their use as the gate dielectric on Si can be exploited in the realization of a single transistor memory element.

In this presentation I will present our approach in depositing gate quality oxide layers on silicon with low leakage and effective oxide thickness <10 Å using molecular beam epitaxy. Growth of crystalline perovskite oxide layer proceeds with a 45° rotation of the lattice with respect to the silicon lattice. Extensive atomic simulations have been used to determine the structure of the oxide/Si interface which was subsequently confirmed by high resolution transmission electron microscopy studies. Electrical measurements on capacitors fabricated on wafer using platinum gate electrodes demonstrated leakage as low as 10⁻⁸ A/cm² with interface state densities in the mid 10⁻¹⁰ cm⁻² eV⁻¹. Results on MOSFET devices fabricated using SrTiO₃ as the gate insulator will also be presented.

Biography

Ravi Droopad obtained his PhD in 1989 at Imperial College of Science, Technology and Medicine working on the growth of Sb-based narrow gap semiconductors by MBE. He spent 6 years at ASU as a research scientist developing growth processes for GaAs-based for high speed optoelectronic device applications. Since 1995 he has been with Motorola Labs responsible for the development of novel growth processes for GaAs-based RF electronic devices. More recently he has been working on the integration of oxides on silicon for gate dielectric applications. He has published over 75 refereed journal articles and has 20 patents issued.

Date: April 17, 2003

Location: Arizona State University, Main Campus, Gold Water Center (GWC) Room 487

Enter the facility through the main (south) lobby and take the elevator to the fourth floor. The conference room is on your right. See <http://www.asu.edu/map/> for more details.

Time: 5:30-6:00pm Social/Refreshments, 6:00-7:00pm Presentation, 7:00pm Dinner (pizza & soda are being provided by the WAD Phoenix Chapter)

For more information, please call Bruce Kim (Chapter Chair) at (480) 965-3749



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Ultrasound: An Unexplored Tool For Blood Flow Visualization And Hemodynamic Measurements

K. Kirk Shung

Department of Biomedical Engineering, 500 Olin Hall,
University of Southern California, Los Angeles, CA 90089-1451

Abstract

Ultrasonic scattering by blood has been studied both theoretically and experimentally for many years for the purpose of a better characterization of the performance of ultrasonic Doppler flow and imaging devices. In the course of these investigations it became clear that ultrasonic scattering from blood or echogenicity of blood is critically related to the hematological and hemodynamic properties of blood. It can be affected by hematocrit, plasma protein concentration, flow rate and flow cycle duration, to name just a few parameters. The experimental efforts have been paralleled by theoretical developments that successfully predict many experimental observations.

An unexpected conclusion from this work is that ultrasound appears to be a totally unexplored and ignored tool for blood flow visualization and hemodynamic measurements. Two unique hemodynamic phenomena that have never been reported in the hemodynamic literature have been observed: the black hole, a low echogenic zone in the center stream of whole blood flowing in a blood vessel under steady flow and the collapsing ring, an echogenic ring appearing near the periphery of a vessel at the beginning of a flow cycle, converging toward the center, and eventually collapsing during pulsatile flow. They are believed to be resulted from the spatial and temporal variations of the shear rate in the blood stream. With the recent technical advances including standard B-mode, color Doppler, power Doppler, and B-flow imaging, clinical reports of observing similar phenomena in vivo on human patients begin to appear. These are exciting evidences to showcase the viability and effectiveness of ultrasound as a tool for blood flow visualization and quantitative measurements of hemodynamic parameters.

BIOGRAPHY

K. Kirk Shung obtained a B.S. in electrical engineering from Cheng-Kung University in Taiwan in 1968, a M.S. in electrical engineering from University of Missouri in 1970 and a Ph.D. in electrical engineering from University of Washington in 1975. He is a fellow of the IEEE, the Acoustical Society of America and the American Institute of Ultrasound in Medicine. He is a founding fellow of the American Institute of Medical and Biological Engineering. He has served for two terms as a member of the NIH Diagnostic Radiology Study Section. He is the distinguished lecturer for the IEEE UFFC society for 2002-2003. He was elected an outstanding alumnus of Cheng-Kung University in 2001. Dr. Shung has published more than 160 papers and book chapters. He is the author of a textbook "Principles of Medical Imaging" published by Academic Press in 1992. He co-edited a book "Ultrasonic Scattering by Biological Tissues" published by CRC Press in 1993. Dr. Shung's research interest is in ultrasonic transducers, high frequency ultrasonic imaging, and ultrasonic scattering in tissues

Date: April 21, 2003

Location: Arizona State University, Main Campus, Gold Water Center (GWC) Room 487

Time: 5:30-6:00pm Social/Refreshments, 6:00-7:00pm Presentation, 7:00pm Dinner (pizza & soda are being provided by the WAD Phoenix Chapter)

For more information, please call Bruce Kim (Chapter Chair) at (480) 965-3749.



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CLOCK SIGNAL ANALYSIS JITTER SEMINAR

Wed April 23, 2003
Fiesta Inn 2100 S. Priest, Tempe, AZ

Clock Signal Analysis

This Full Day seminar provides detailed and up to date technical information about the clock signal from generation to distribution, design issues and fundamentals, test, and measurement issues and solutions.

The session will be held Wednesday April 23, 2003 at the:

Fiesta Inn and Conference Center
2100 S. Priest, Tempe, Arizona.

Attendees will receive a full packet of information at the session to include a CDROM with all presentations from all speakers. Coffee is served in the morning, and luncheon is provided at the session.

You may pre-register with an *early bird discount* (\$50.00 off of the *at the door fee*) for this session at our site at www.timing-is-everything.com. Registration on site at the door is \$495.00 for the session, so take advantage of the early bird discount via the web. Plan to arrive early at 8:30am for coffee. The session starts at 9am, and runs thru 5pm.

Heavy emphasis is placed on

- Device specifications
- Design and Layout
- Test and Measurement
- Interpretation of the results

Guest speakers at this session include:

John Claiborne	EDA Tools and Issues
William Gervasi	The Charge Transfer Model, (an enhancement to Tsetup/Thold)
Tektronix Corporation	High Performance Digitizers
	Probing Solutions
LeCroy Corporation	Jitter analysis integrated software
	PLL Bandwidth measurements

Please take time to review our website at www.timing-is-everything.com and register by selecting the **STORE** button, or contact:

Steven Sillyman at 602-992-8866 (voice) or sillyman@att.net.



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IEEE PHOENIX SECTION SCHOLARSHIPS

**Applications Due Wednesday, May 14, 2003
Awardees Announced June 4, 2003**

Institute of Electrical & Electronics Engineers

Entering Freshman Scholarship	IEEE Student Member Scholarship
<ul style="list-style-type: none"> • Four \$250 Scholarships per year • For incoming college freshmen who enroll electrical engineering related fields • Must attend a university in the Phoenix Section (<i>i.e.</i>, ASU, DeVry, Embry-Riddle, or NAU) during 2003-04 and join IEEE • Approved majors are Electrical Engineering, Computer Systems Engr., Electr. Engr. Technology, or Computer Engr. Technology <p>Scholarship Application Requirements</p> <ul style="list-style-type: none"> • Application form with general information and qualifications including: <ul style="list-style-type: none"> ○ financial aid statement, and ○ one-page personal statement of attainments, interests and goals • Official transcripts of all high school work • SAT and/or ACT scores • Recommendation letters (optional, but helpful) 	<ul style="list-style-type: none"> • Two \$1,000 Scholarships per year • For full-time undergraduates who are members of IEEE • Must attend a university in the Phoenix Section during 2003-04 (<i>i.e.</i>, ASU, DeVry, Embry-Riddle, or NAU) • Approved majors are Electrical Engineering, Computer Systems Engr., Electr. Engr. Technology, or Computer Engr. Technology <p>Scholarship Application Requirement</p> <ul style="list-style-type: none"> • Application form with general information and qualifications including: <ul style="list-style-type: none"> ○ financial aid statement, and ○ one-page personal statement of attainments, interests and goals • Official transcripts of all college work • Recommendation letters (optional, but helpful)

For Application Forms or Further Information Please Contact:

Dr. Keith Holbert
holbert@asu.edu
(480) 965-8594

Send Completed Application Materials to:

Dr. Keith Holbert
Electrical Engineering Department, MS 5706
Arizona State University
Tempe, AZ 85287-5706