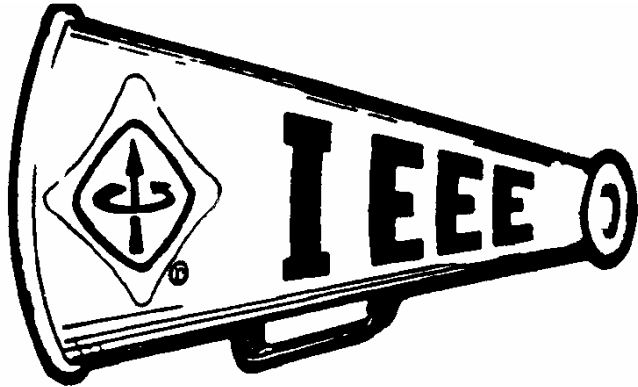


The Valley Megaphone



Newsletter of the
**Institute of Electrical and
Electronics Engineers, Inc.**
Phoenix Section
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This Issue of The Valley Megaphone Features:

Contacts:

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IEEE Phoenix Section Executive Committee meeting minutes can be found at: <http://www.ieee.org/phoenix>

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The Valley Megaphone is the newsletter of the Phoenix Section of the Institute of Electrical and Electronics Engineers. It is published monthly, usually September through June. The publication reaches about 4000 members. Submit articles, advertisements, and announcements to Eric Palmer at the above email address. Deadline for announcements and advertisements is the third Friday of the month prior to publication.

Advertising Rates: Full page: \$200, 3/4page: \$125, 1/2 page: \$75, 1/3 page: \$50, 1/4 page: \$25. Change of address/email? Call toll free 1-800-678-IEEE. Please allow 6-8 weeks. Section Web Page is: <http://www.ieee.org/phoenix>



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IEEE ANNOUNCEMENTS

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Embry-Riddle Computer Society

Advisor:



Website Design and Optimization Ben Marcus, ETA Engineering

Thursday, June 9, 2005

Networking begins at 6:30 p.m.

Dinner begins at 7:00 p.m.

Date: Thursday, June 9, 2005

Time: Networking begins at 6:30 p.m.
Dinner begins at 7:00 p.m.

Place: Denny's Restaurant
3315 N. Scottsdale Rd.
Scottsdale, Arizona 85251

Speaker: Ben Marcus does web design at ETA Engineering. He will give us ideas on how to improve a firm's website for a stronger web presence.

Directions: From Highway 101 and Indian School Road, go west. Turn left on Scottsdale Road and head south. It is at the southeast corner of Scottsdale and Osborn Roads, just south of downtown Scottsdale.

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Networking the World™

IEEE ANNOUNCEMENTS



Digital Image Processing

SPEAKER: Gary Mastin

DATE: 6:00 PM, Wednesday June 8, 2005

LOCATION: DeVry University, 2149 West Dunlap Ave, Phoenix, Az 85021 (1 mile east of I-17 on Dunlap, SE corner of 22nd Ave and Dunlap). Networking will be in the Courtyard (6-7PM with light meal), presentation at 7PM.

Free, Everyone is welcome. Please tell others about this meeting.

Digital image processing has found broad utility, especially in engineering and scientific endeavors. Gary Mastin will provide insight into how digital image processing has been applied to interesting problems from his work at Sandia National Laboratories and at Lockheed Martin. Among the applications to be presented will be the analysis of launch imagery associated with the Space Shuttle Columbia disaster.

Dr. Gary Mastin is a principal engineer with Lockheed Martin IS&S in Goodyear, Arizona, where he is an algorithm development lead. Gary has considerable experience in synthetic aperture radar (SAR) image formation and parallel architectures for signal processing. Prior to working for Lockheed Martin, Dr. Mastin worked at Sandia National Laboratories in Albuquerque, New Mexico. He was part of a small Sandia team that provided digital image processing consulting across the laboratories. Sandia applications included shock physics, accelerator physics, nuclear weapons safety, physical chemistry, and a few unique activities with the FBI and Defense Intelligence Agency.

See www.ieeecs.com, for more information.

Contact Bob Bianca (Bob.Bianca@Computer.Org)

Fall: Wednesdays September 14, October 12, November 9, December 14



Networking the World™

IEEE ANNOUNCEMENTS



Institute of Electrical and Electronics Engineers, Inc. Phoenix Section

Components, Packaging and Manufacturing Technology Society Chapter
&

Waves and Devices Chapter

PRESENT AN ALL-DAY WORKSHOP ON

Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications

Date: Thursday, November 10th, 2005

Time: 7:00 A.M. – 5:00 P.M.

Location: Arizona State University, Tempe, Arizona – ASU Memorial Union (Arizona Room)

Abstract

The one-day workshop will focus on device, interconnect and packaging challenges for next generation computing and communication applications. Participants will hear from leading contributors from industry, academia and the national labs. Long-range technology roadmaps will be reviewed and state-of-the-art processor, memory, and mixed-signal technologies will be addressed. Chip, package, and board-level interconnect issues will be discussed. Key materials, process, and performance challenges for physically realizing the required devices, interconnects and packaging will be presented. Market trends in computing and communications are within the scope of the workshop as well. A panel discussion on the future of computing and communications will bring closure to the day's workshop. Vendors representing the entire supply chain of chip, package, and board will display their products and services.

Topics

- ? **System & Architecture:** Future computing approaches (local vs. net-centric, personal & server computer); convergence of computing and communication; advances in processor technology such as multi-core, high-bandwidth buses and advanced drivers/receivers; memory/processor integration; SoC partitioning, modeling, and testing challenges/issues.
- ? **Materials & Processing:** ITRS roadmap for CMOS technology; Moore's law/prognosis in the context of the next few technology nodes; BEOL processing (low-k/Cu, ultra low-k/Cu); advances in memory technologies.
- ? **Simulation & Modeling:** Simulation for advanced devices; EM simulation in RF circuit/module/package design; signal noise analysis for SoC.
- ? **Advanced Packaging:** New packaging technologies, especially flip-chip, lead-free, 3D interconnect, multi-chip, and RF modules.
- ? **Special Topics:** Signal integrity; power delivery and distribution; cooling/thermal management.
- ? **Panel discussion on the future of computing and communications.**



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