



**SAN FRANCISCO BAY AREA
NANOTECHNOLOGY COUNCIL**

Noon Time Seminar – Tuesday, October 20, 2009



Co-Sponsored by IEEE SCV Electron Devices Society

Title: Opportunities and Challenges with Graphene Production and Application

**Speaker: Xiaogan Liang, Ph.D, Researcher, The Molecular Foundry,
Nanofabrication Facility, Lawrence Berkeley National Laboratory**

Date: Tuesday October 20, 2009

Time: Registration & light lunch 11:30am. Presentation & Q/A 12:00 to 1pm

Location: National Semiconductor Bldg E-1 CMA Room. 2900 Semiconductor Drive, Santa Clara, CA

Directions: See attached pages.

Cost: IEEE Members and Students \$5. Non-Members \$10

Please RSVP at our website: www.ieee.org/nano

Talk Abstract:

Recently, graphene has been extensively studied as a material for making future electronic device. In comparison with conventional semiconductors graphene exhibits exceptional properties, such as pronounced ambipolar effect, high carrier mobility, a stable 2D crystal structure, and potential to realize ballistic transport at room temperature. In comparison with other graphitic nanostructures (e.g. nanotube and fullerene), graphene is more compatible with state-of-the-art silicon technology. Potential electrical and electronic applications include bio/chemical sensors, semiconductor devices, transparent conductors, and energy conversion/storage devices, etc.

However, two of the challenges for scale-up applications are incorporating graphene over large areas and patterning nanostructures to achieve desirable electronic characteristics. Several approaches have been attempted to produce graphene for large area electronics, including epitaxial growth on catalytic metals, thermal decomposition of SiC, solution-based deposition, and mechanical cleavage, etc. At the same time, efforts have been made to tailor graphene sheets into nanoscale features (e.g. nanoribbons). At LBNL, we developed a novel nanotransfer-printing route to address these two challenges simultaneously. With this method, we have successfully demonstrated the printing of graphene features ranging from 18 nm to 100 μm . Furthermore, working transistors have been fabricated by using the patterned graphene nanolines. Such a method could be used for constructing graphene-based integrated circuits and quantum devices in the future.

Speaker Biography:

Dr. Xiaogan Liang is currently working at The Molecular Foundry, Nanofabrication Facility, Lawrence Berkeley National Laboratory. His current research interests are focused on nanoimprint lithography, graphene-based electronics, nanofluidics, block copolymer self-assembly, and photovoltaics. Dr. Liang has coauthored 16 journal publications and more than 15 conference presentations, and has 4 pending patents. Xiaogan Liang is the member of Sigma Xi and IEEE.

Dr. Liang obtained a BS in Physics from Peking University, a MS in Condensed Matter Physics from Chinese Academy of Sciences, and a Ph.D. in Electrical Engineering from Princeton University.

Directions To National Semiconductor Campus

□ Address: Building E Auditorium, 2900 Semiconductor Dr., Santa Clara, CA 95051

□ If heading South on Lawrence Expressway from Highway 101:

✖1a: Turn RIGHT (west) onto **Kifer Road**.

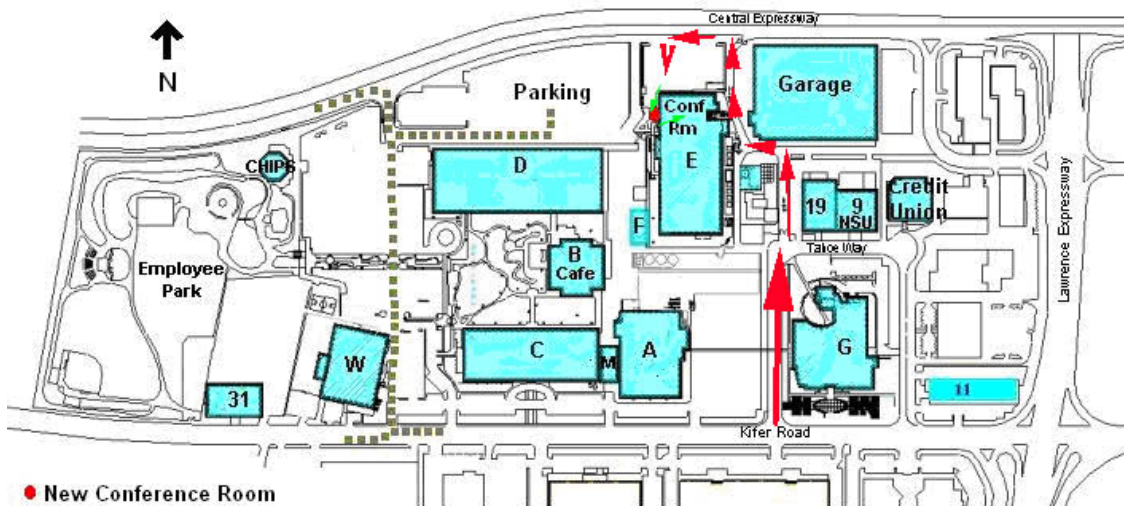
□ If heading North on Lawrence Expressway from El Camino Real:

✖1b: Turn LEFT (west) onto **Kifer Road**.

□ Then:

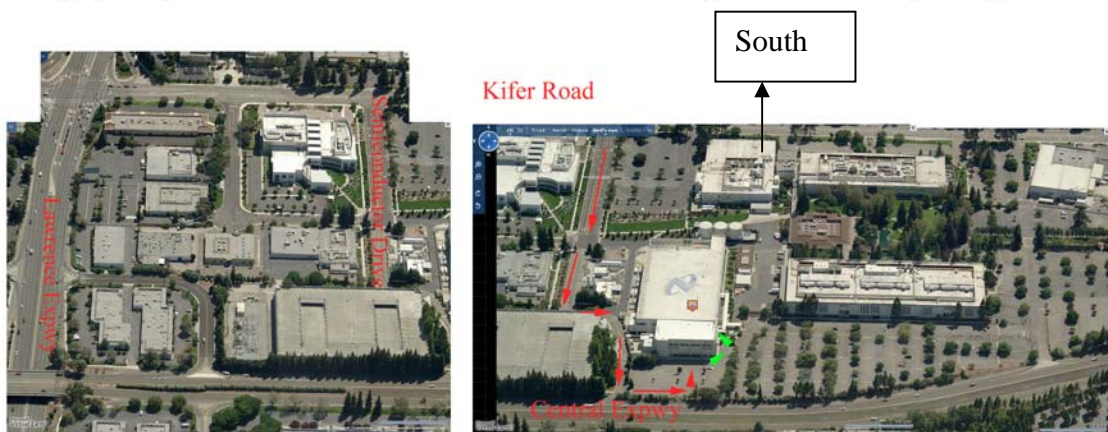
✖2: Turn RIGHT (north) at First Stop Light onto 2900 Semiconductor Drive

✖3: See National Semiconductor Campus Map below (follow red arrows to park; follow green arrows to walk to auditorium entrance).

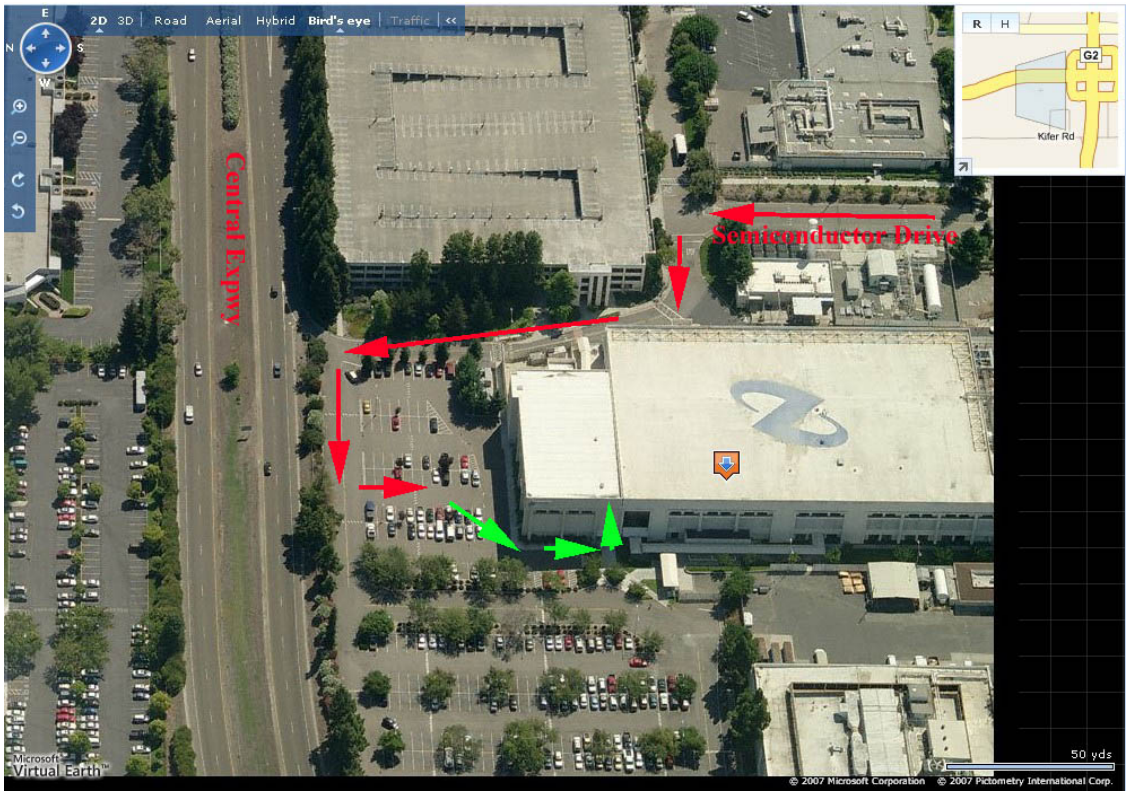


● New Conference Room
(Enter through Bldg E Lobby)

■ Bldg E parking is accessible from both directions of Kifer and driving east on Central Expressway.



Aerial photos looking southward.



Aerial photos looking eastward.