High Performance Computing
Union of Software and Reconfigurable Logic

Ivo Bolsens, Senior Vice President and CTO
October 2010

Xilinx at a Glance

- **Worldwide leader in programmable solutions**
  - Founded in 1984
  - $1.8B in revenues in FY ’10
  - ~3,100 employees worldwide
    - 1,300 in San Jose
  - 20,000+ customers worldwide
- **+50% PLD market segment share**
  - Larger than all competitors combined
- **Diversified customers and markets**
- **Excellent financial scorecard**

Why Programmable Logic?

Xilinx Provides Standard Parts

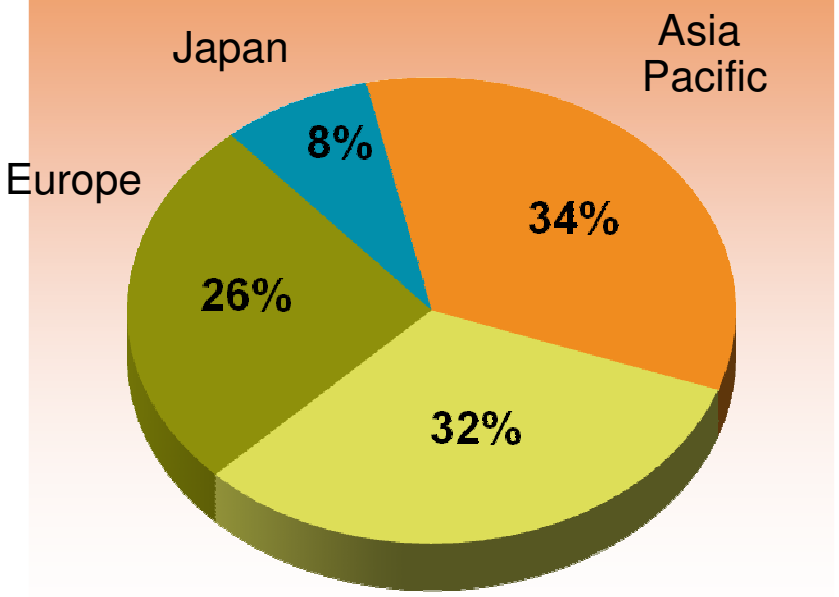
- Faster time-to-market and volume production
- Modifications made quickly through software
- Low inventory risk for customers
- Field programmability
- No up front NRE (Non-recurring Engineering)

The Benefits of FPGAs vs. Asics are Similar to
Digital Photography vs. 35mm Film

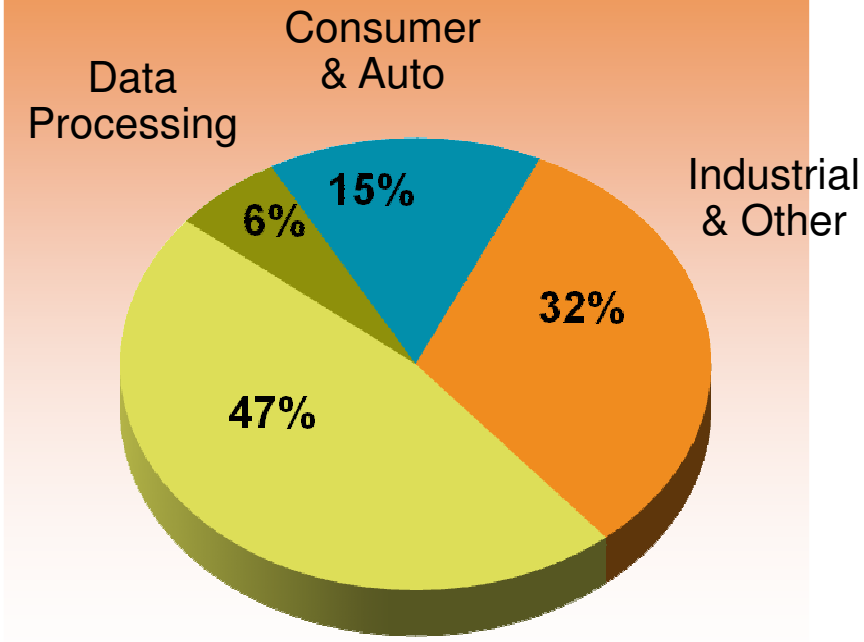
Xilinx Revenue Breakdown

Q2 Calendar Year 2010

Revenue by Geography



Revenue by End Market



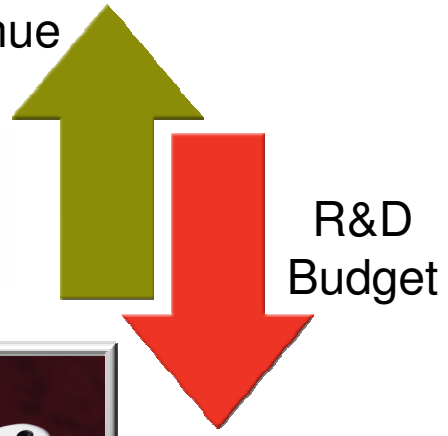
Source: Xilinx, Inc.

Challenging, Changing Markets

Hyper-connectivity and mobility

Fickle, fragmented markets

How System Companies Must Adapt



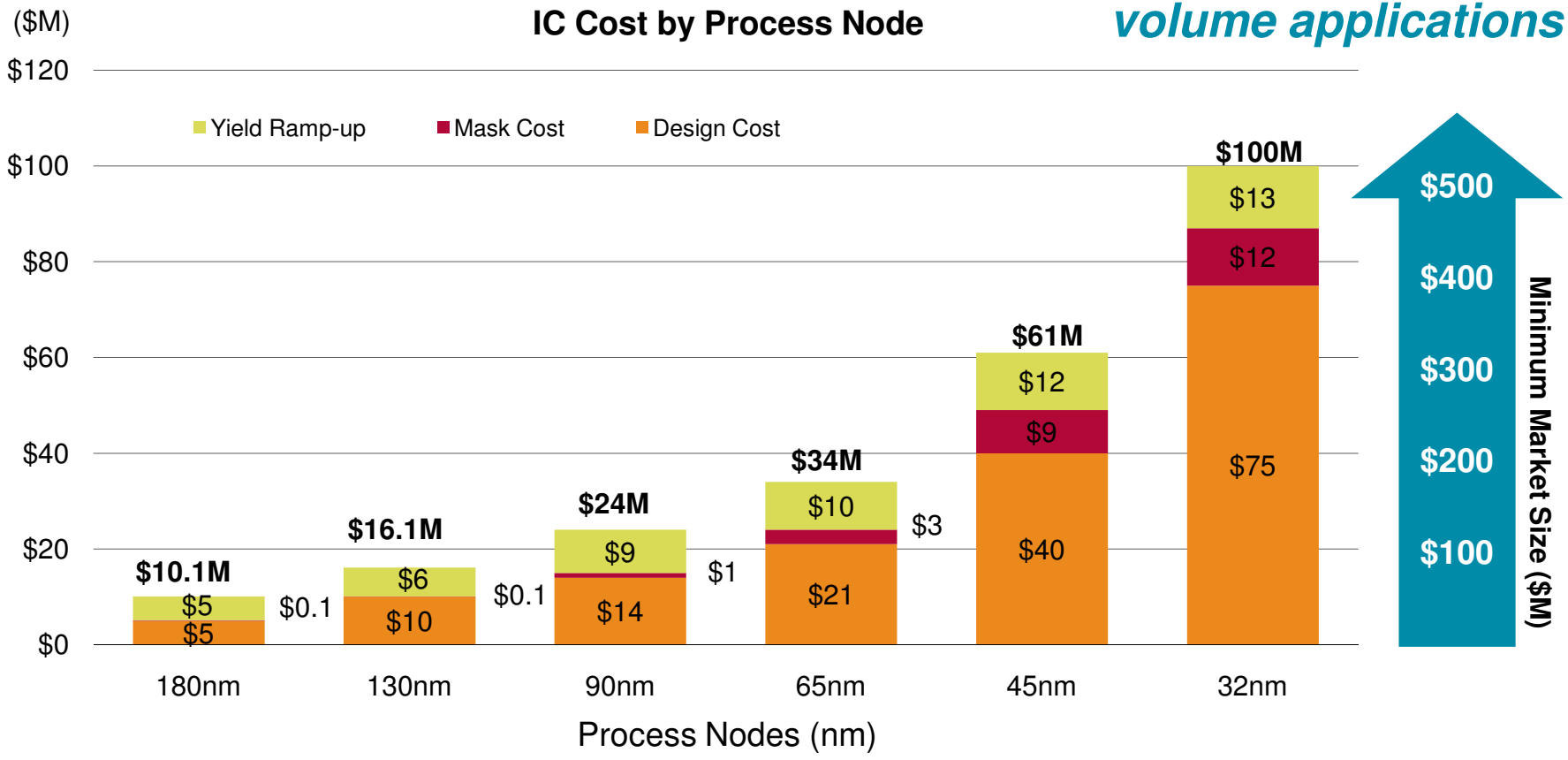
Do more with less ▪ **Improve engineering productivity**

Reduce risk profile ▪ **Build-in flexibility**

Focus on Core competencies ▪ **Differentiate or die**

Design Cost Challenges

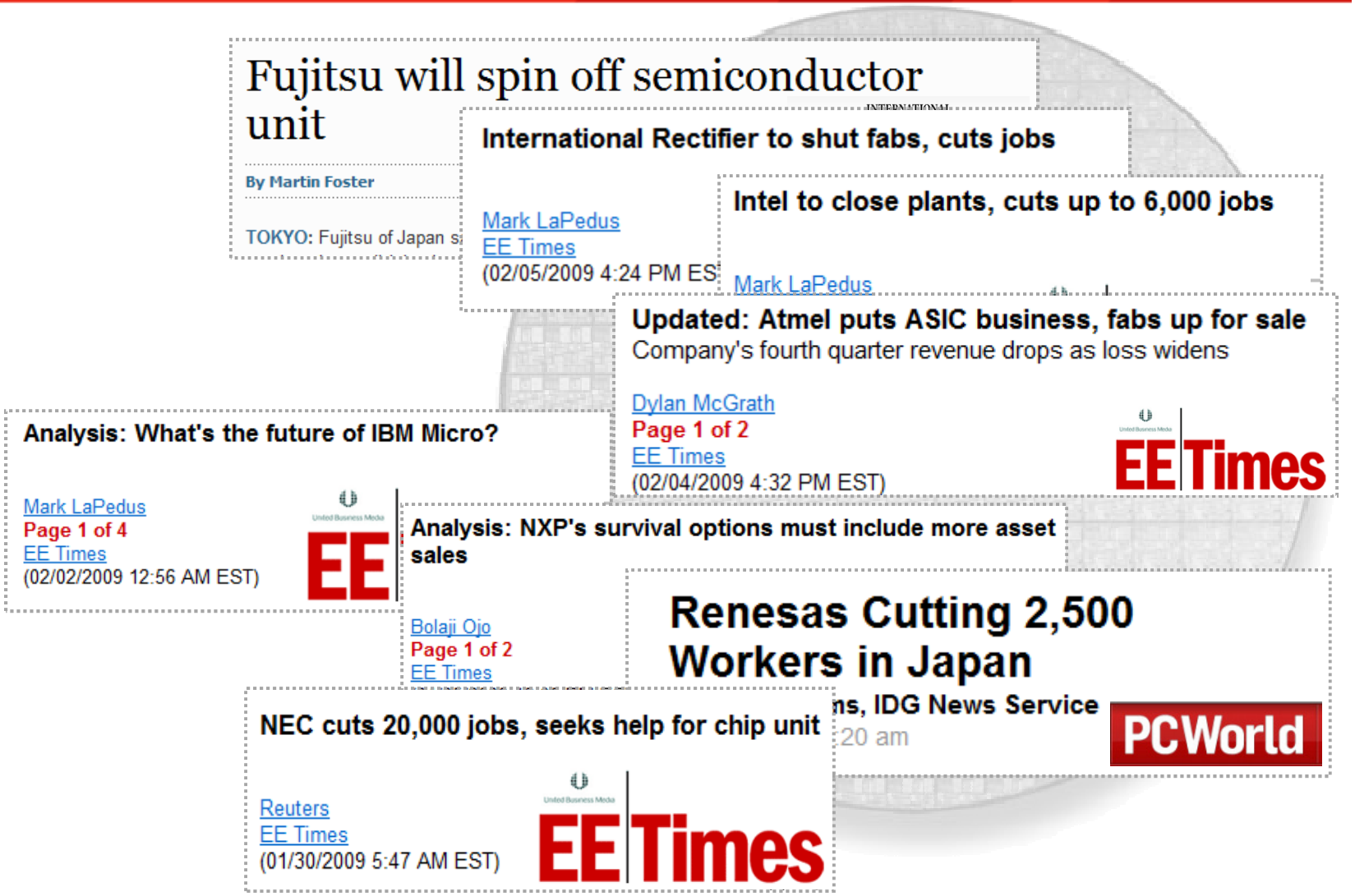
Narrow Focus to high volume applications



Source: GSA, Chartered and Synopsys

XILINX

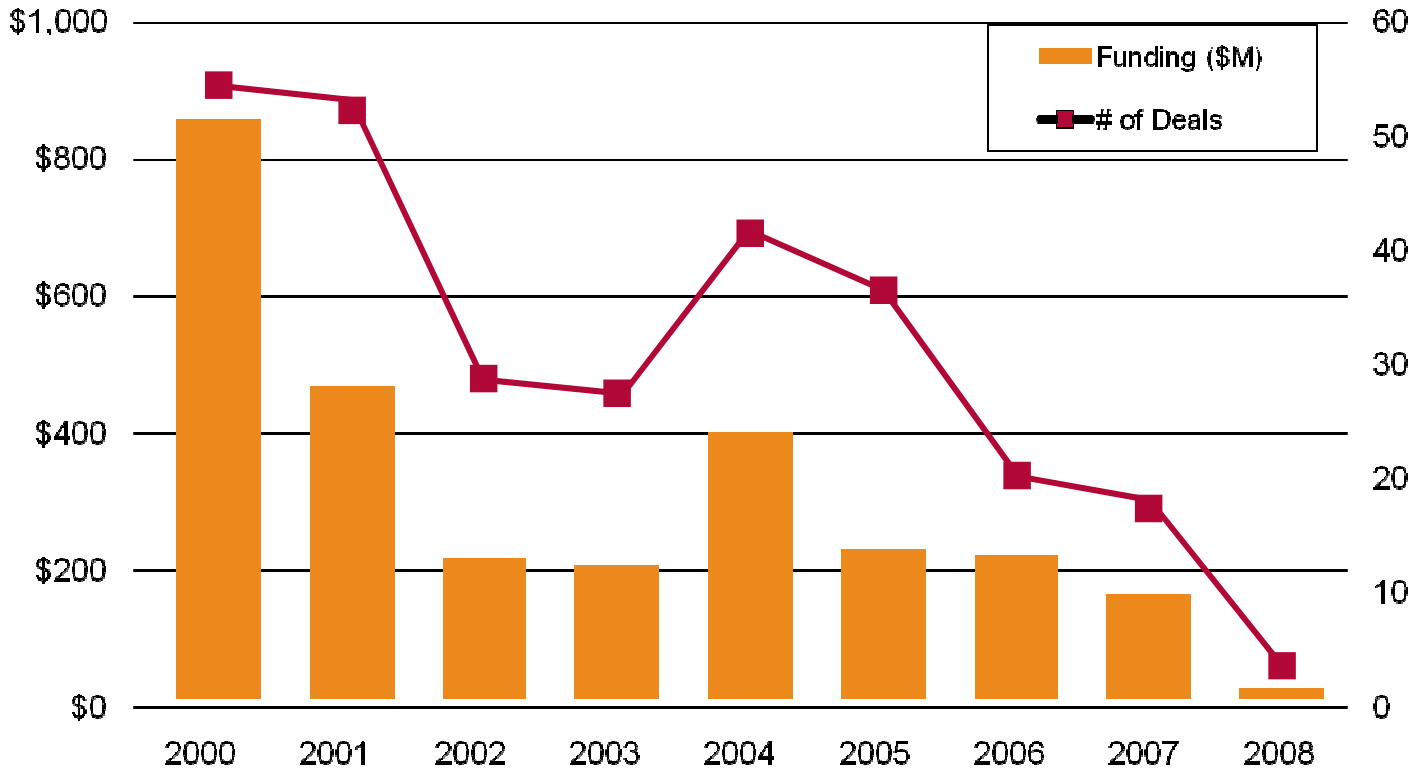
Semiconductor Companies are Challenged



Source: GSA

Startup Challenges

Funding Has Vanished



- **Round-A funding [$ amount] declined 82% from 2000-2007**
- **Only 2 chip companies received Round-A funding in 2008, totaling $12M**

Source: GSA

Startup Challenges

EE Times

Rick Merritt
Page 1 of 4
EE Times
(06/22/2009 2:52 PM EDT)

August Capital, Partner
Andy Rappaport

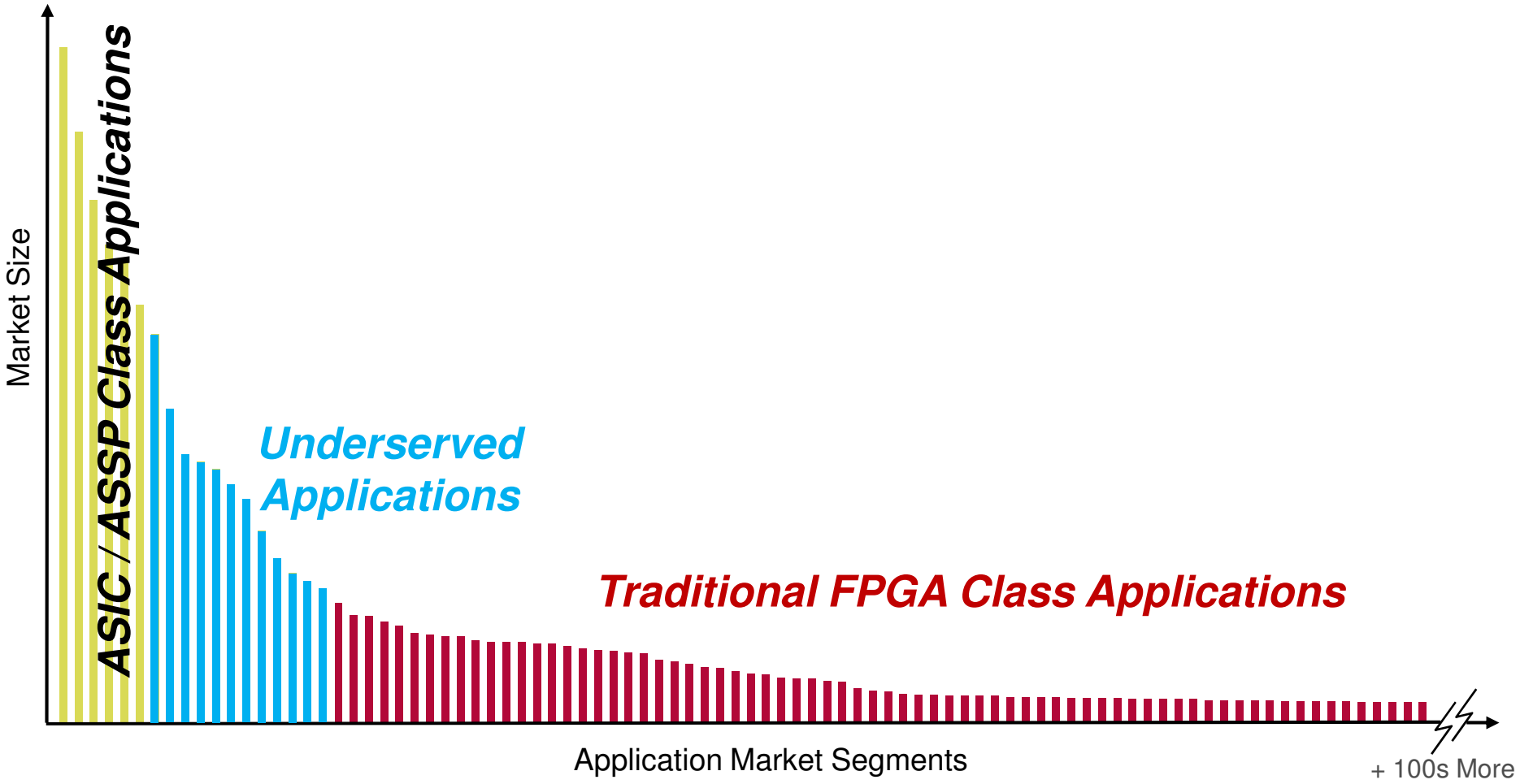
Sequoia Capital, Partner
Mark Stevens

"These days it's very *difficult to build a fabless company making a device with any digital complexity for less than $100 million*, and a number have exceeded 200 million" A Rappaport
"The problem came when we looked at the volume required vs. the cost of running the company"
"We said, 'hold on these equations don't solve." – A Rapport commenting on T-Zero semiconductor

Stevens estimated it takes $40–$100 million and six to eight years to get a major chip startup to a breakeven point. "That's much larger than it was in the '80's or even the '90's,"
"the IPO window has been largely shut for semiconductor startups for most of this decade,"
"When you put nearly $100 million in a company and someone buys it for $200 million, if you're lucky, the math doesn't work,"

"The Tzero story likely will be repeated more than a hundred times over the next few years as investors slash through a decade of over-investments in semiconductor startups." Rick Merritt, EETimes

FPGA Opportunity Is Growing



New FPGA Powered Infrastructure Opportunities

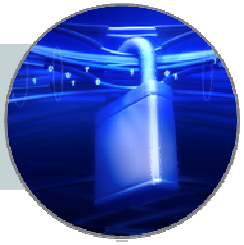
Smart Grid

Communications

Automotive Infotainment

Green IT

Surveillance

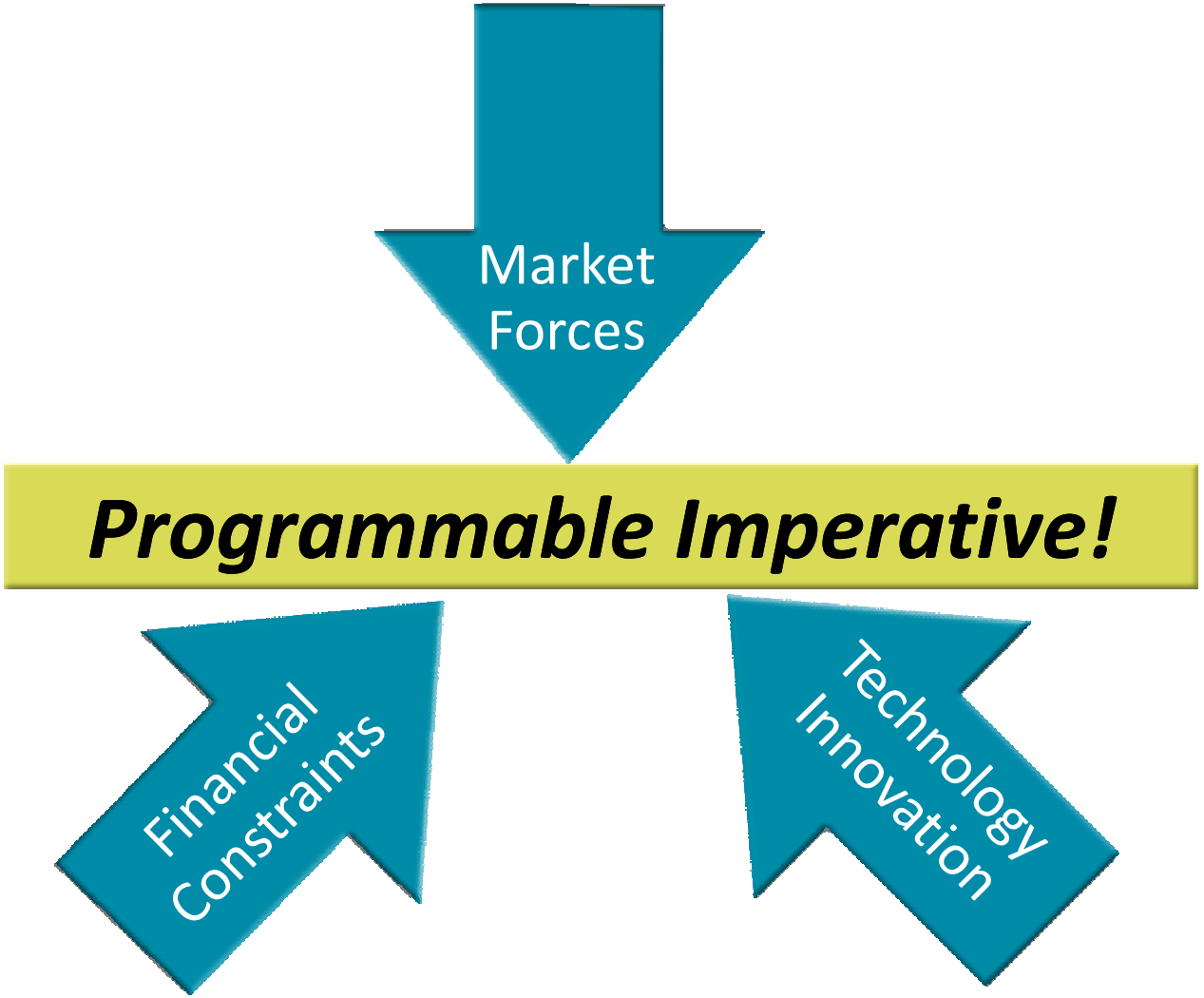


Intelligent Video

Cloud Computing

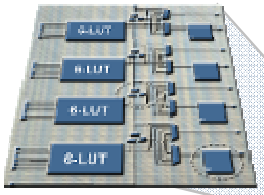
Security Infrastructure

Now Is the Time for Programmable Platform

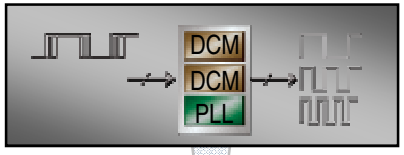


FPGA Platform : “Virtual Foundry”

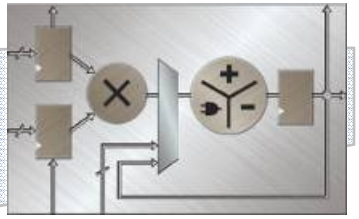
2M Logic Cells
6-LUT architecture



Clocking Flexibility
DCM (precision synthesis)
+ PLL (Low jitter)



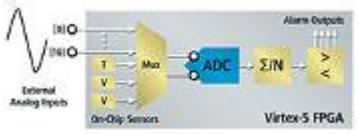
4K DSP datapaths
> 2.4 Tera MACC



Embedded Memory
65MBit

VIRTEX 7

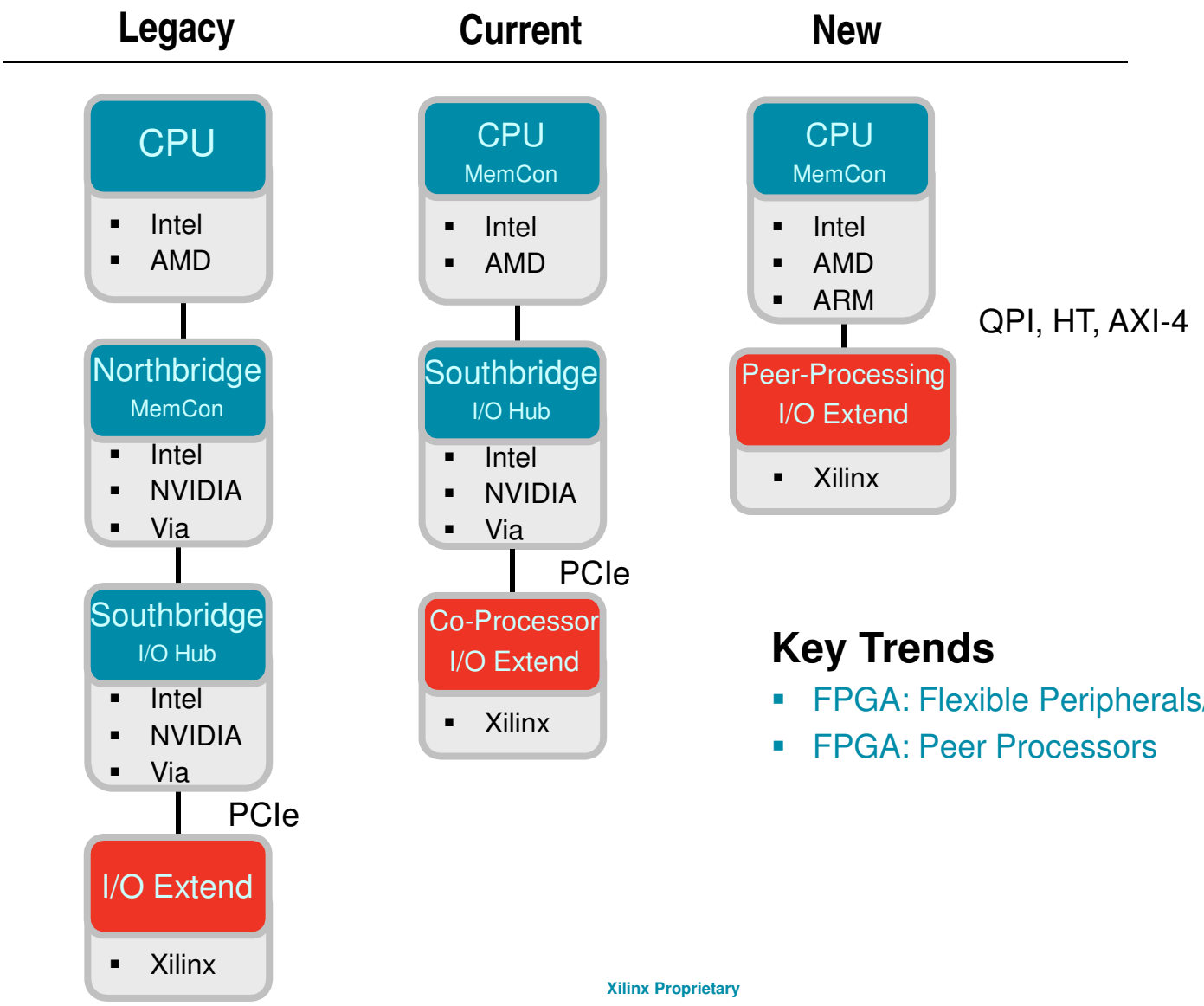
PCI Express Gen3
Integrated x8
End-point/Root



Integrated Reliability
Temp/PowerMonitor

Optimized Serial IO Power & Performance
Upto 28 Gigabit/sec Transceivers

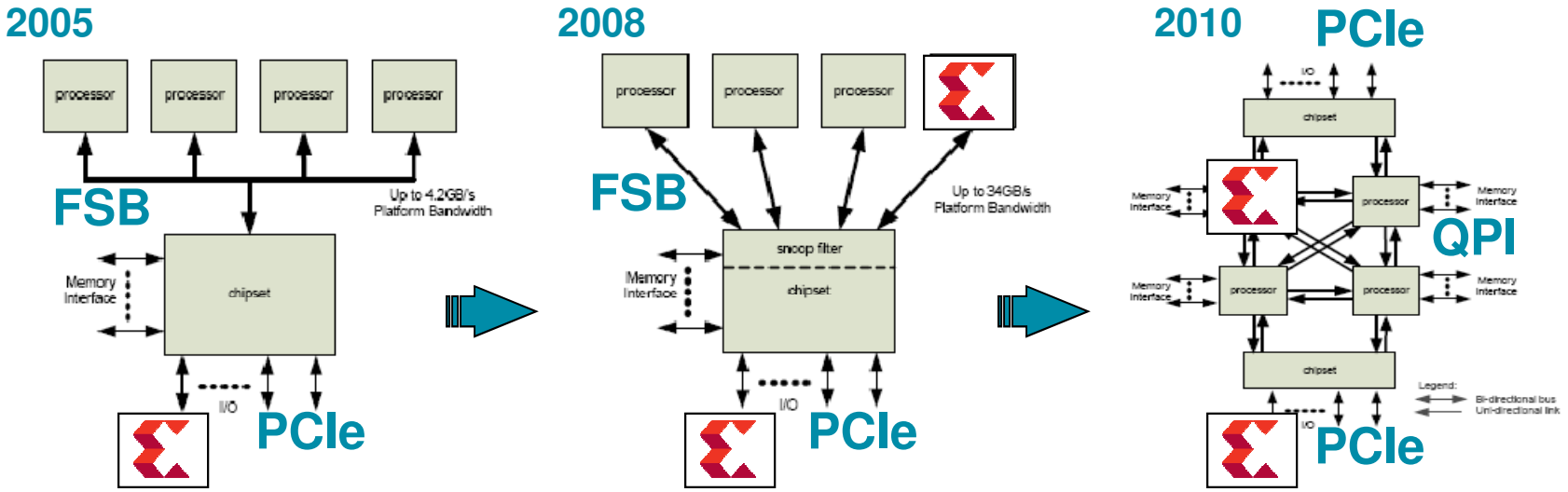
Platform Architecture : Processor + FPGA Platforms



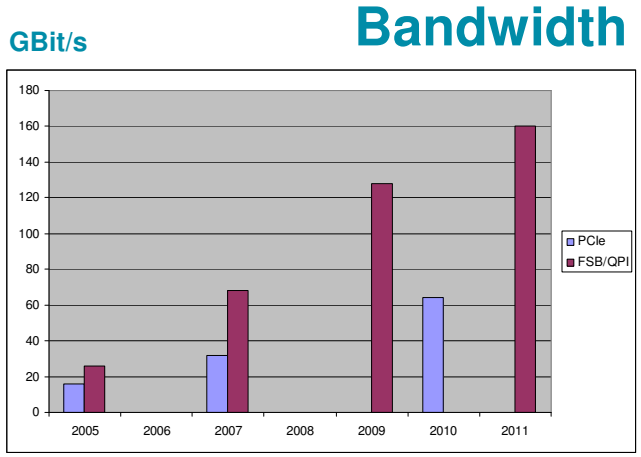
Key Trends

- FPGA: Flexible Peripherals/Accelerators
- FPGA: Peer Processors

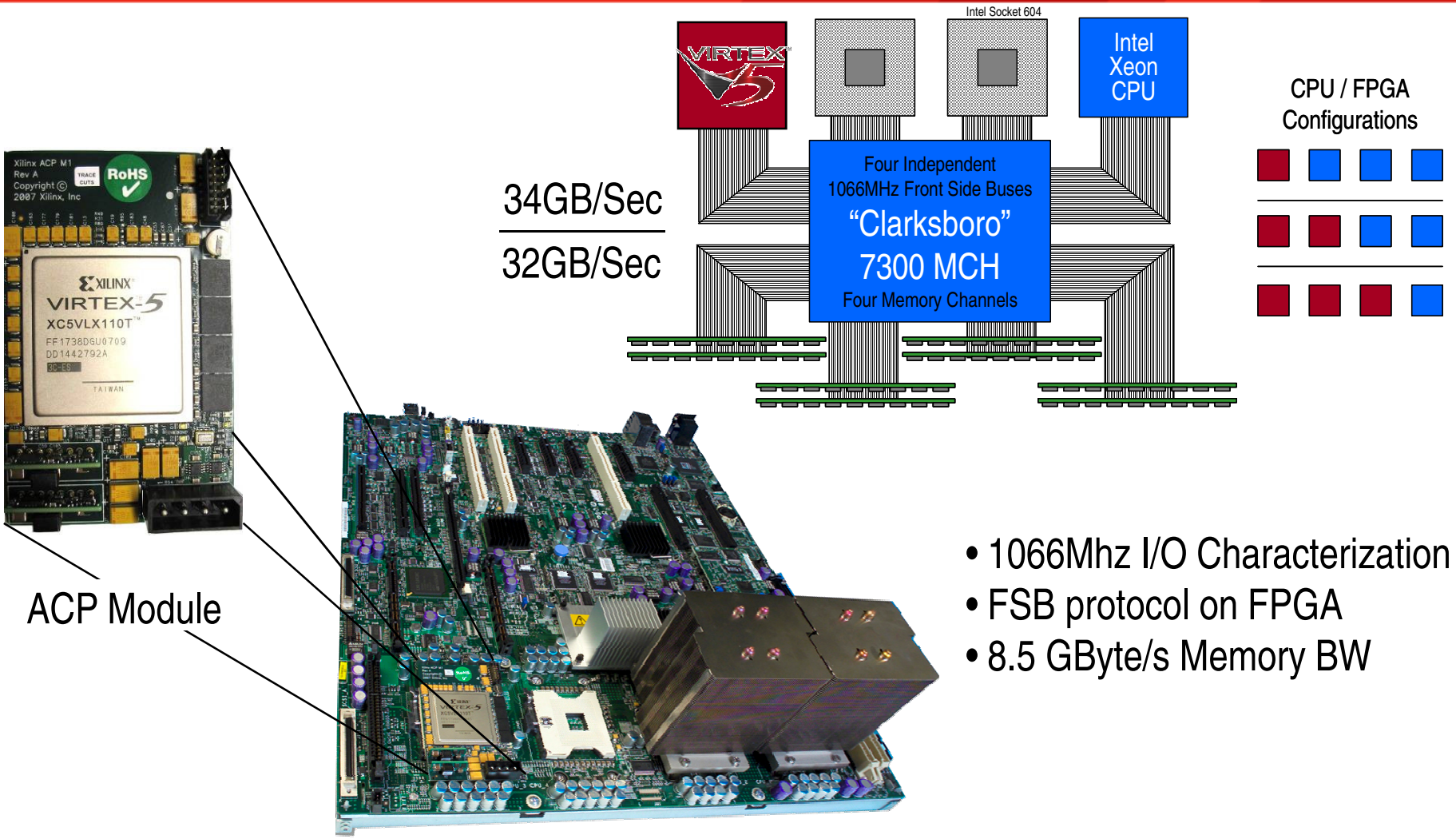
System Interconnect



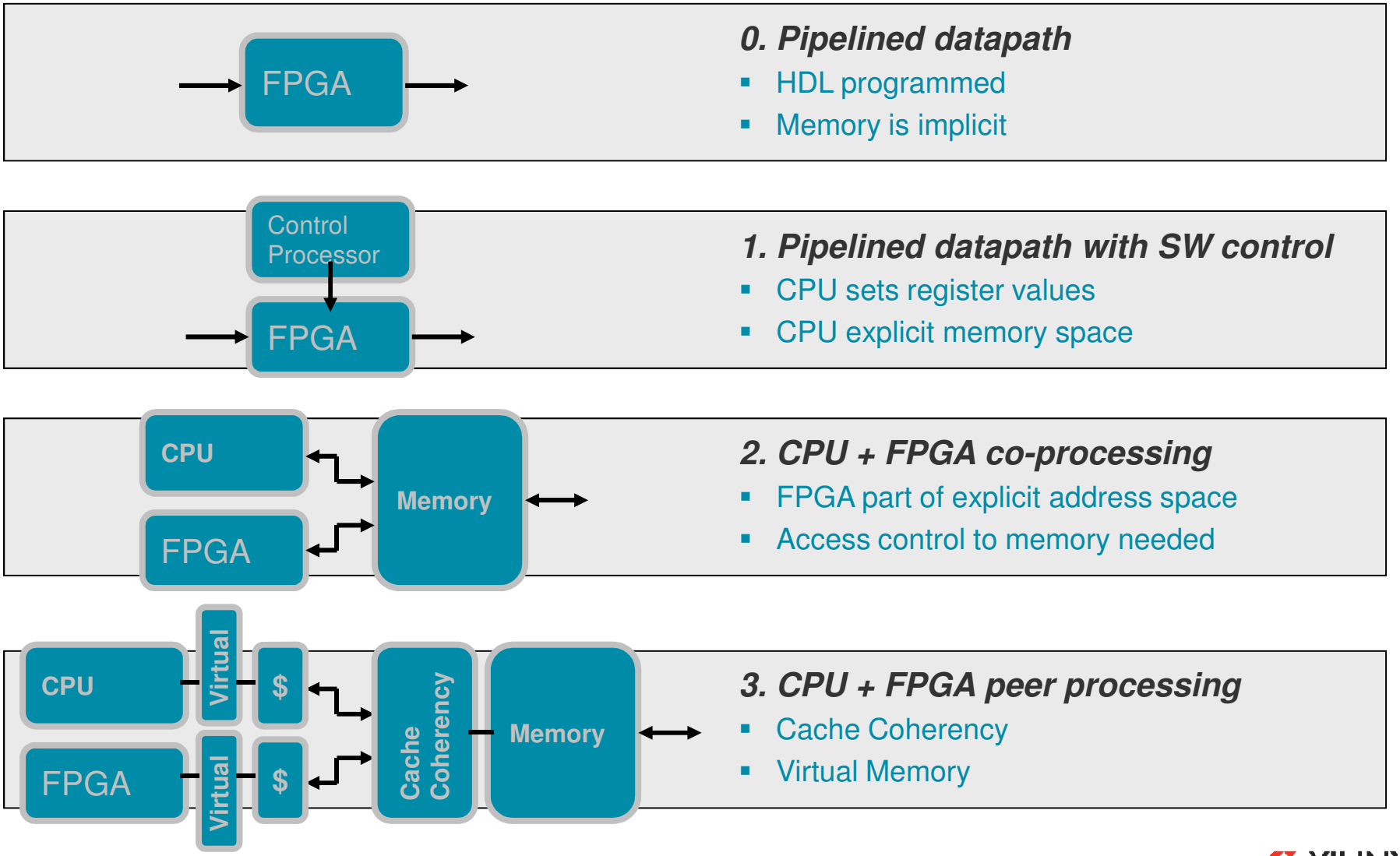
Equal BW: FSB vs PCIe	FSB/QPI: 2x PCIe BW
PCIe IO Device	In-Socket Accelerator
Cache Flush	Direct Cache Access
Device Driver Call	Shared Memory Function



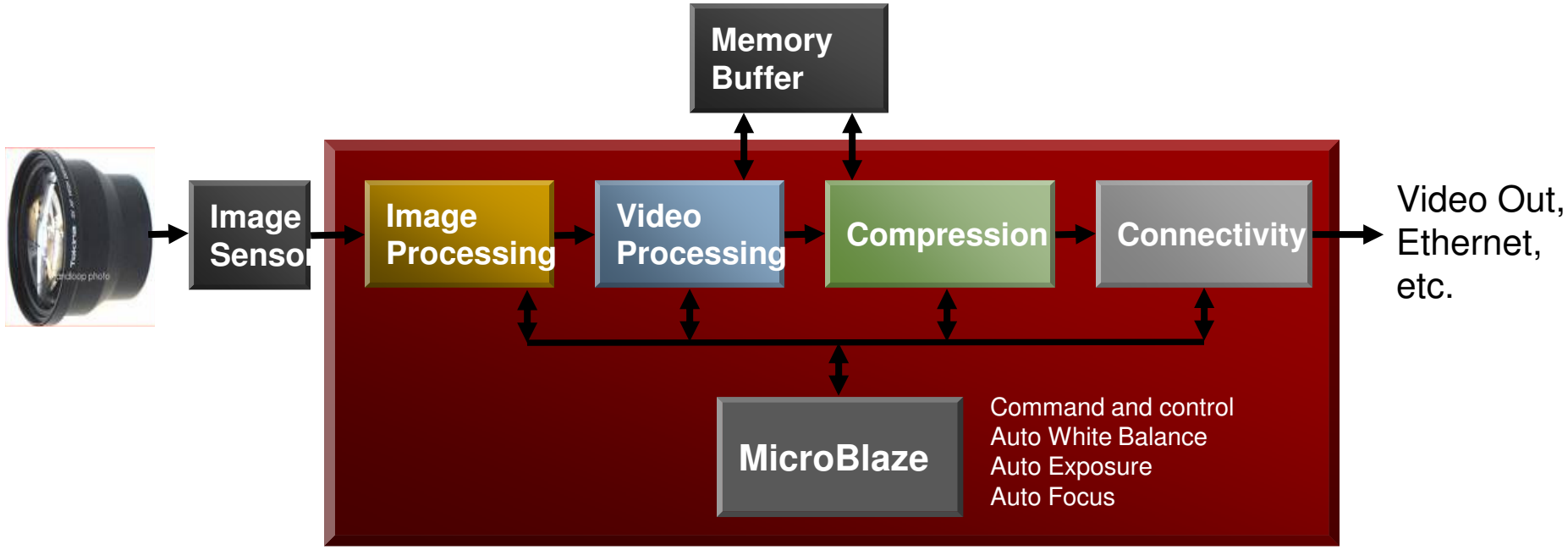
Heterogeneous Multi-Processor



FPGA Use Models

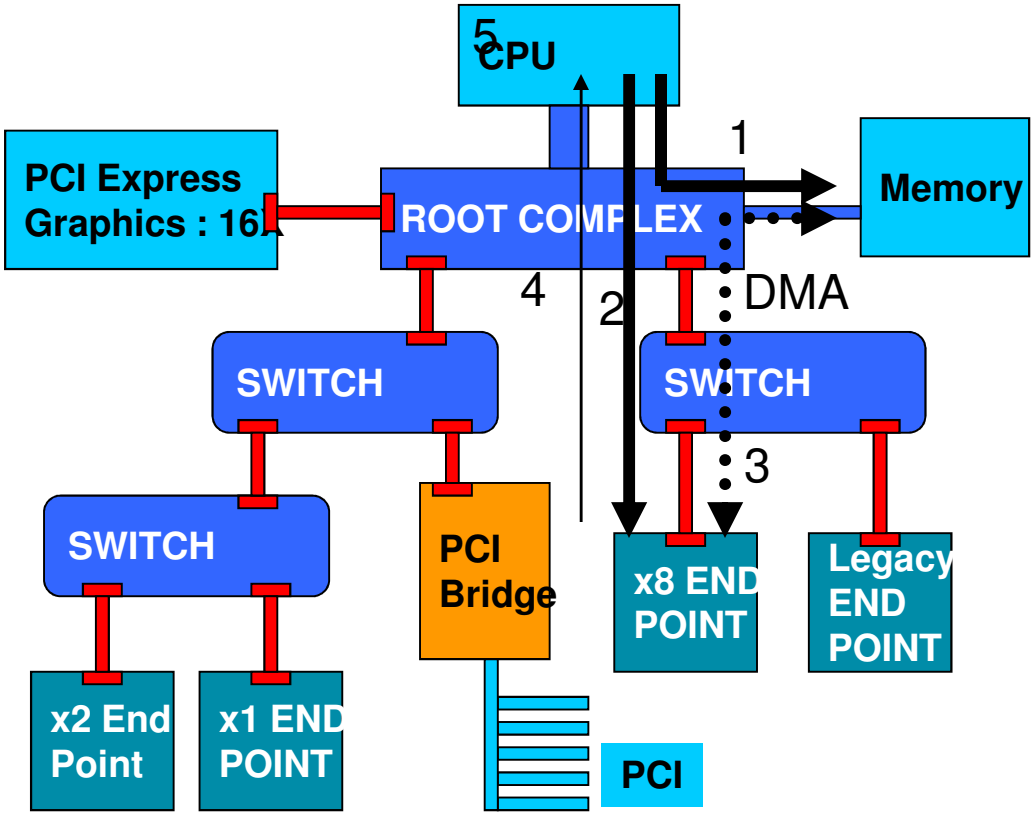


Use Model 1 : Image and Video Processing Pipe



- RTL design and IP blocks for the Pipe: pixel rate processing
- Microblaze : control program and some image contents based settings

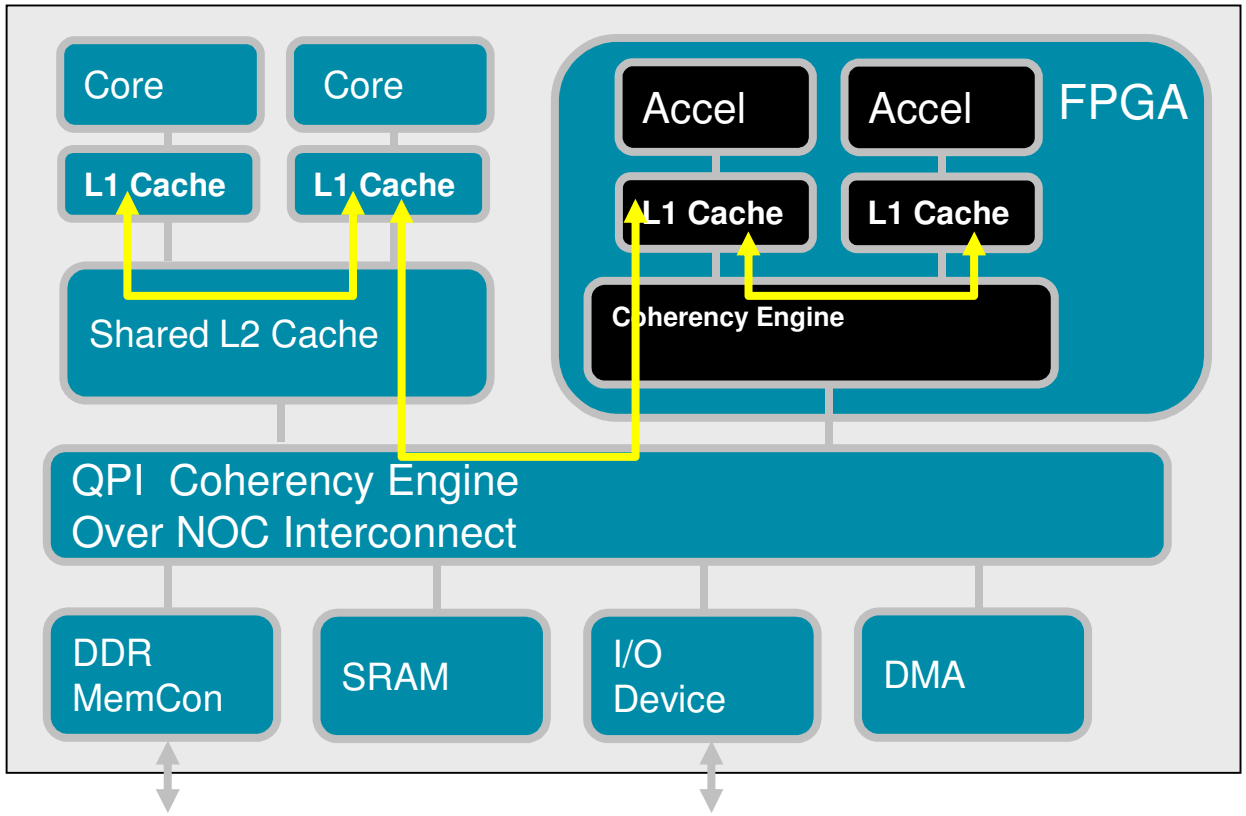
Use Model 2 : Explicit Memory Management



- 1. flushSourceToMem()
- 2. setupDMA()
- 3. HW Process()
  - A. if DMA'event …
  - B. DMAreadFromMainMem()
  - C. HWcomputeProcess()
  - D. DMAwriteToMainMem()
- 4. SignalDoneIRQ()
- 5. waitForHWDone()
- 6. rebuildCacheFromMem()

Model 3 : CPU + FPGA Peer Processing

Shared Memory with Coherency



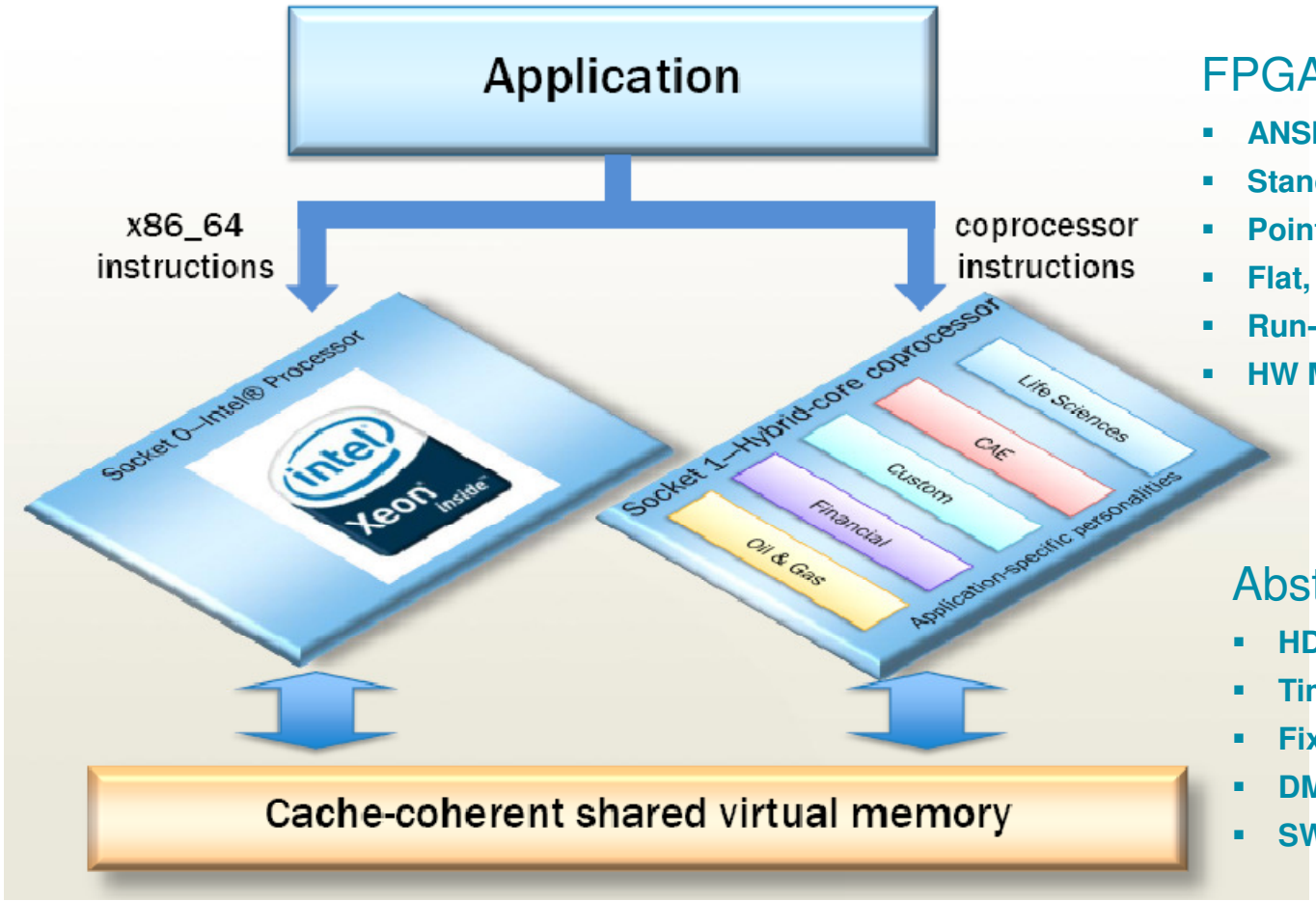
Capabilities

- Coherent Caches for HW
- Coherent Caches for SW
- Coherency Management

Coherency Benefits:

- **Peer Processing**: Direct Cache-2-Cache data movement
- **Latency**: Very low latency access to CPU (FPGA) data
- **Usability**: No SW cache flush needed

Shared Memory Programming on FPGAs:
Convey HC-1 *(2008)*



FPGA Accelerators Today:

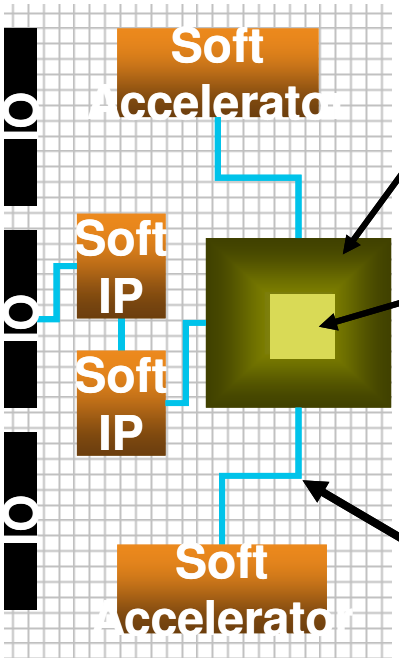
- ANSI C Programming
- Standard C Compilers
- Pointers
- Flat, Virtual Memory
- Run-Time Scheduler
- HW Managed Memory Consistency

Abstracted Away:

- HDL Design
- Timing Closure
- Fixed, Static Scheduling
- DMA Engine Programming
- SW Managed Memory Regions

Source: Convey Computer, 2008

Processor-Centric, Embedded ARM, AMBA-AXI



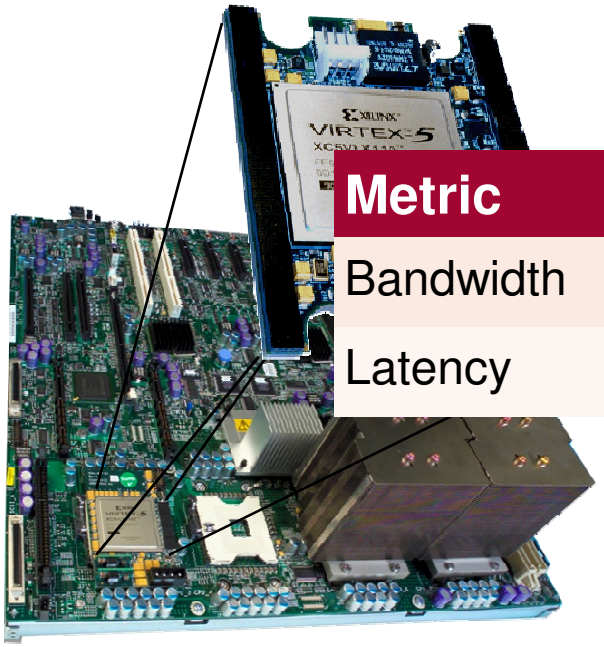
- Processor system available at power-up
- Ease-of-use programming for SW developers
- SoC approach w/dedicated IP, pins + FPGA extension

- Industry's best 32-bit processor roadmap
- Low power, performance, volume leader
- ARM Connected Community

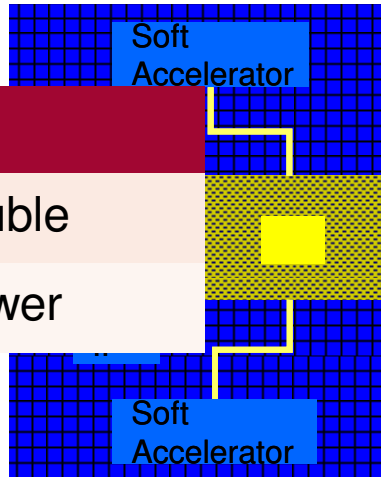
nnect

- Open standard optimized for data throughput
- Supports multiple outstanding transactions
- Uni-directional improves gate count & timing
- Symmetrical interfaces enables Hybrid Computing

Embedded Opportunity



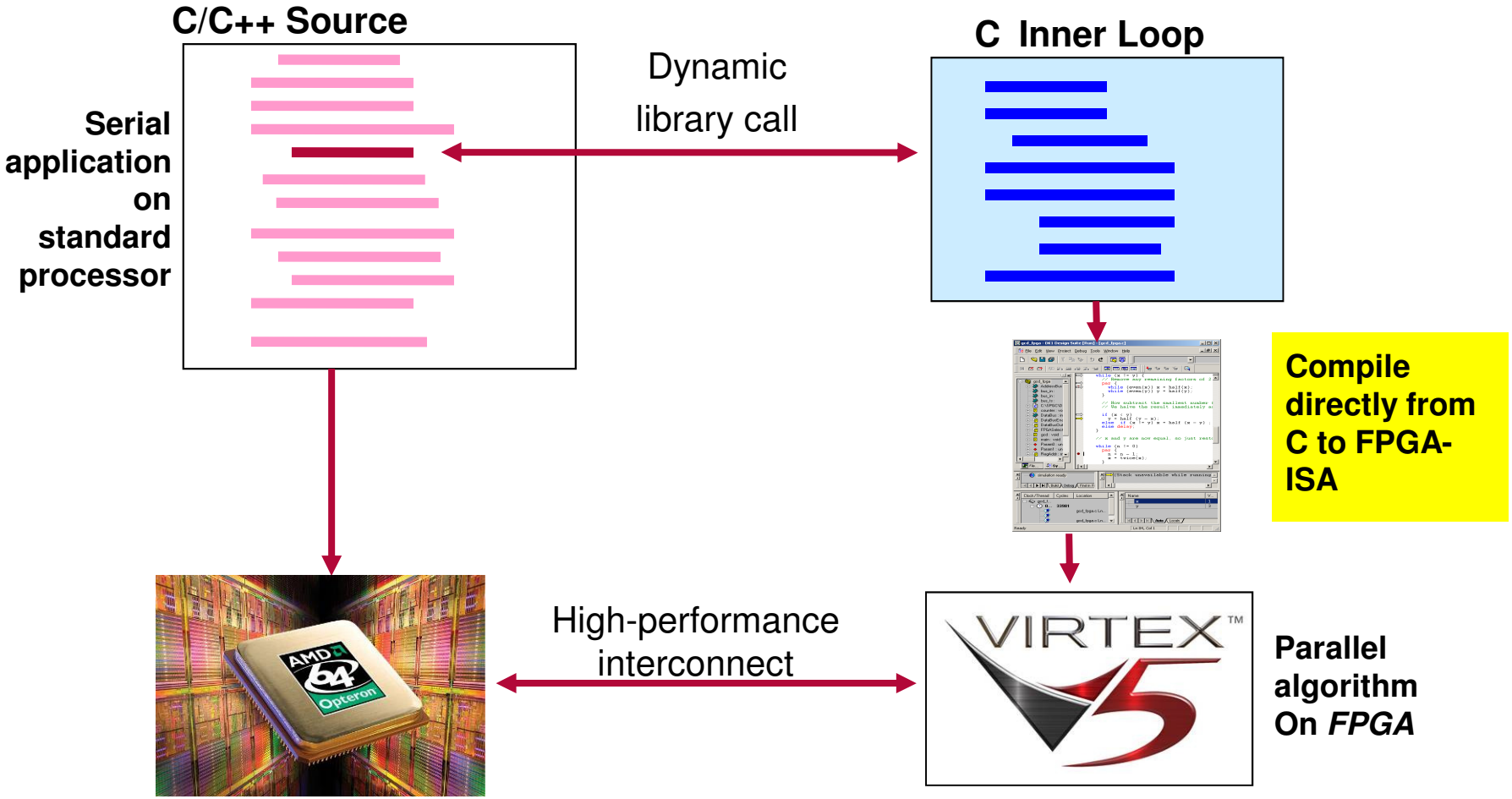
Metric	
Bandwidth	> Double
Latency	4x lower



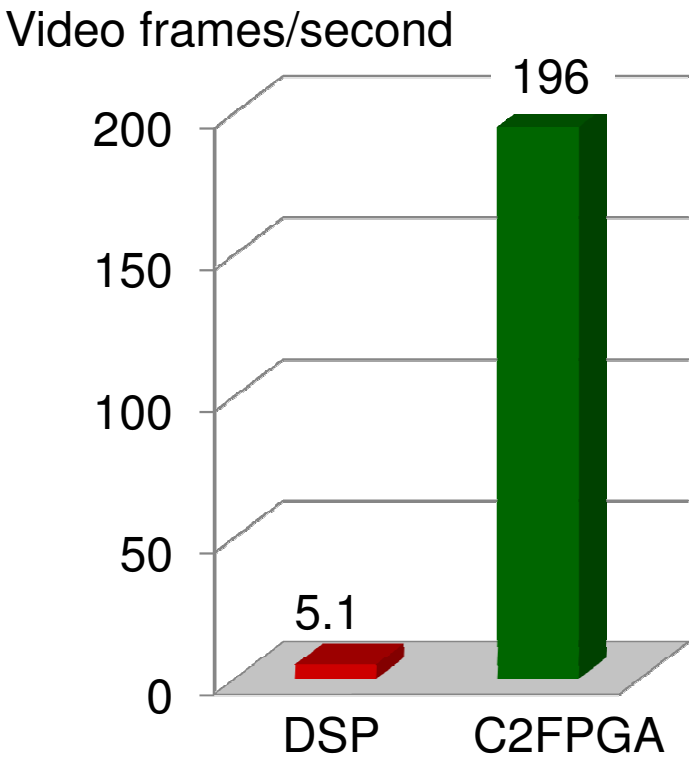
EPP

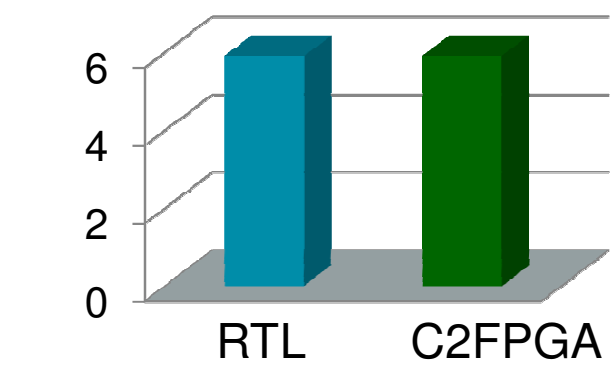
Major Leap in Cost and Performance

High Level Programming : C2FPGA



From C Algorithm to FPGA Implementation



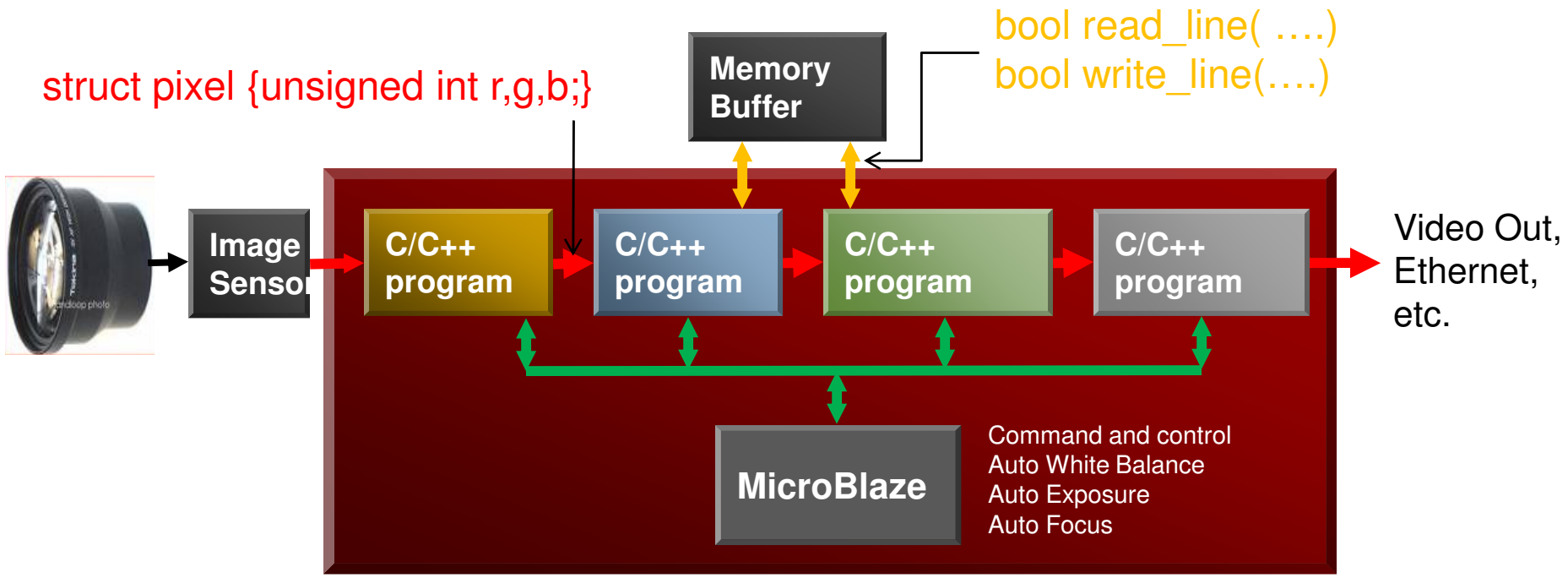


FPGA: >38 times better performance than DSP video processor

QOR: C2FPGA equal to or better than RTL synthesis

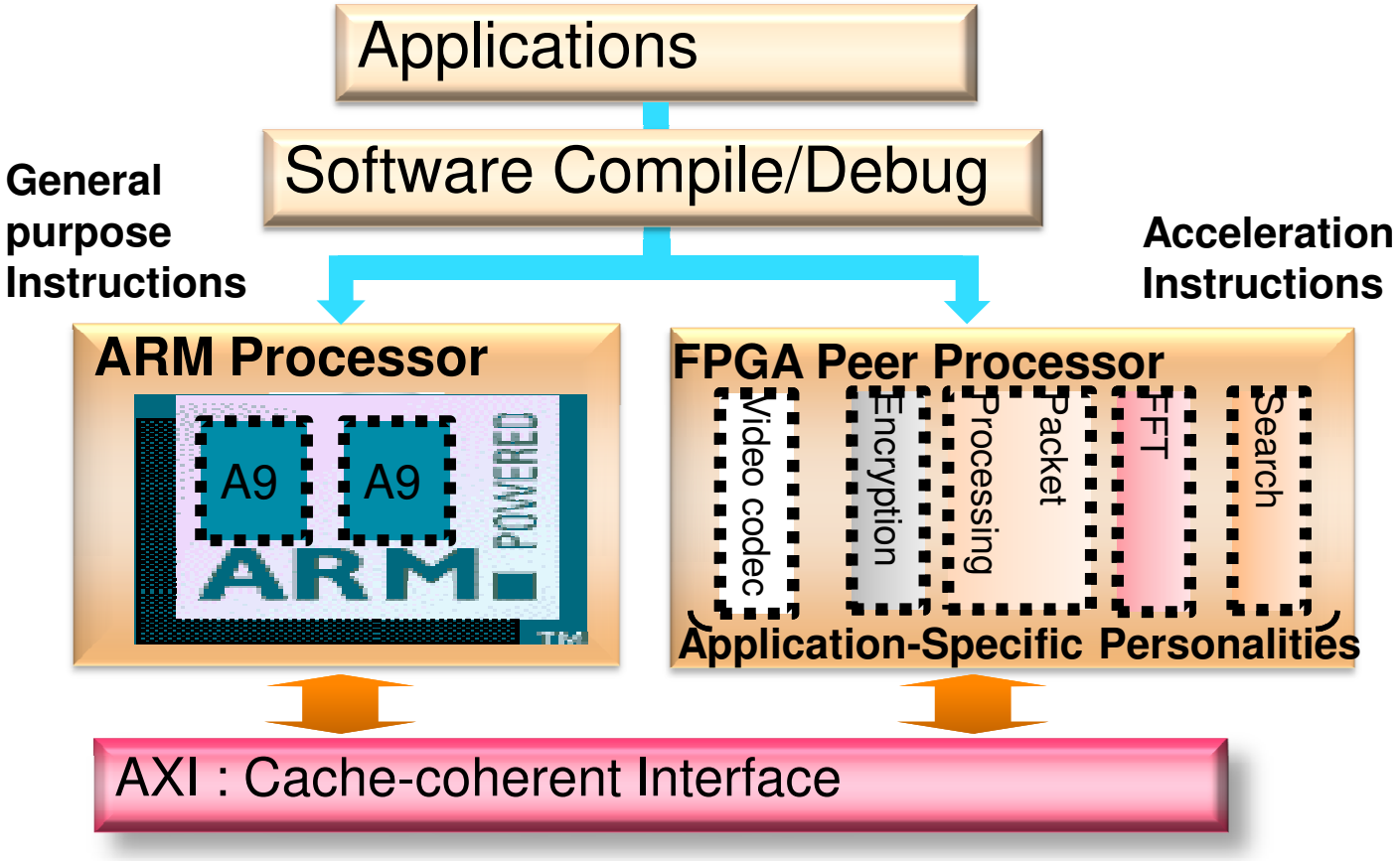
Ease-of-use: C2FPGA 2x fewer lines of C code than DSP processor

Next: C programs on a Video Design Platform



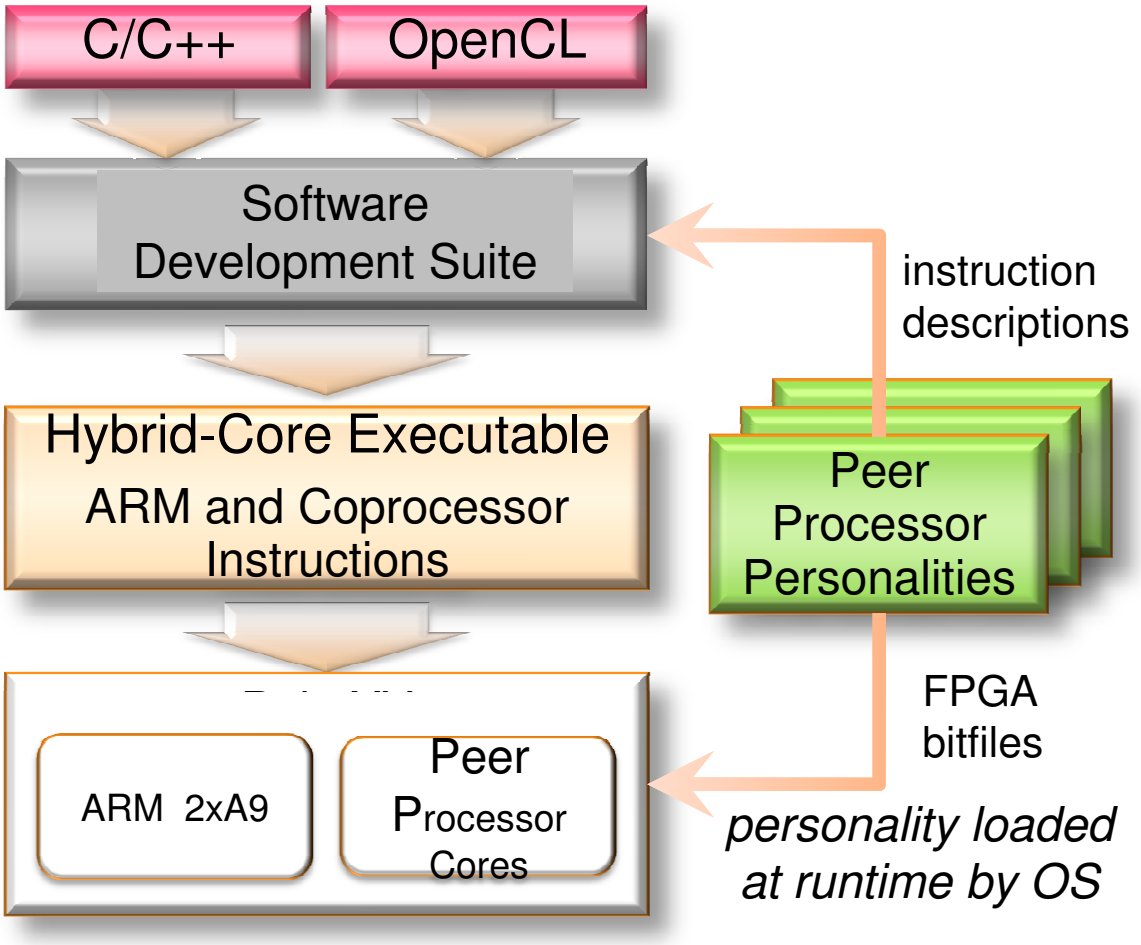
- C/C++ programs on streams of pixels,
- Cooperating program on the Microblaze, e.g. coefficient tables
- Guaranteed performance on abstract interfaces

EPP Opportunity : Software Flow



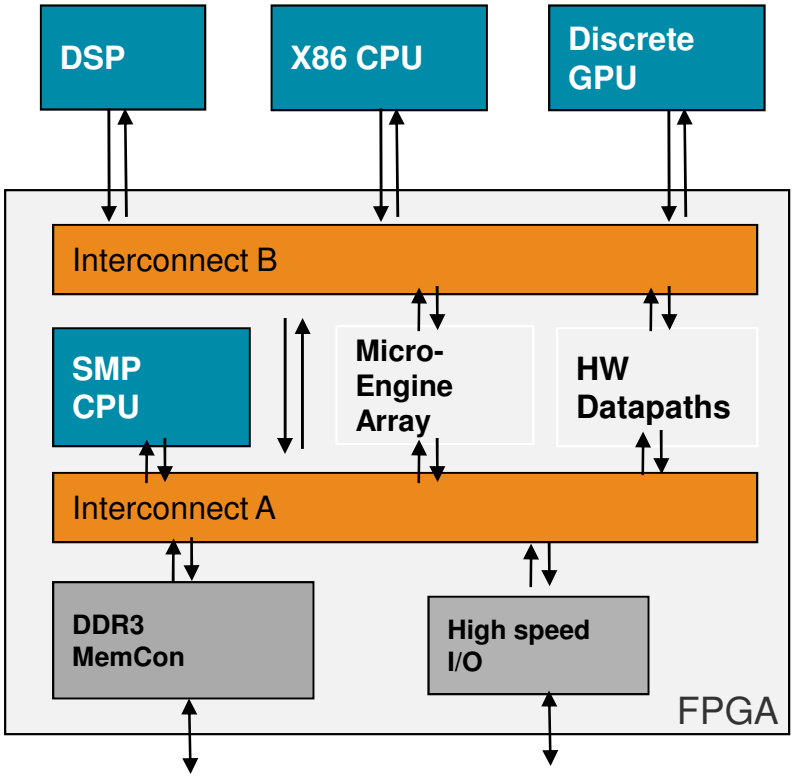
Hybrid Multi-core Platform

Hybrid Multi-Core Programming Model



The Programmable Processing Platform

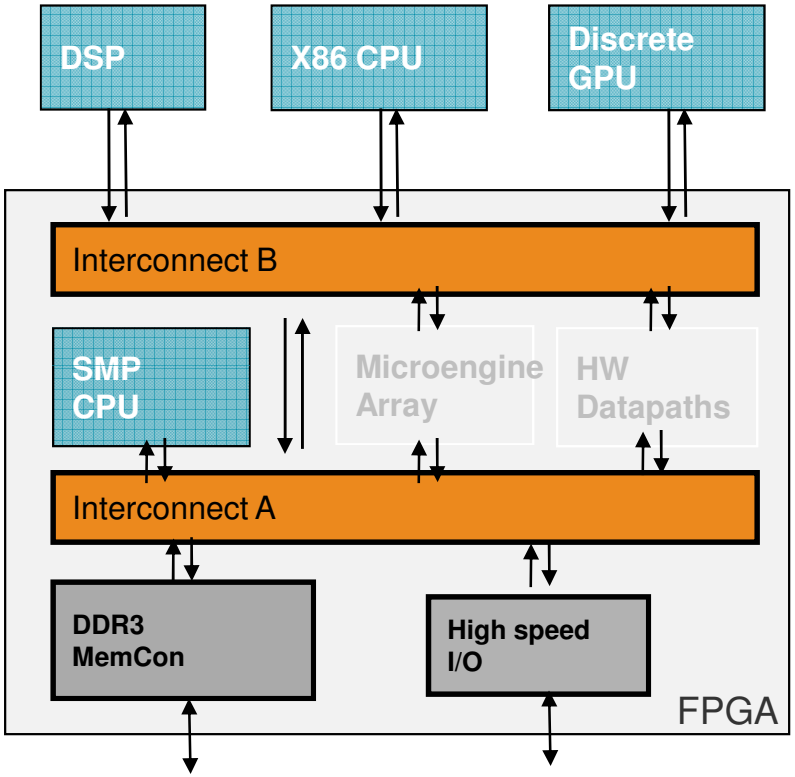
A heterogeneous multicore



- **Application processors**
  - Hard core and soft core
  - External and embedded
  - Caches and large memory space
  - Unified shared memory
  - Full OS support
- **Streaming micro-engines**
  - Configurable (soft) vector cores
  - Tiny memory footprint
  - Many, distributed, memories
  - Compute kernels, no OS
- **Fixed function datapaths**
  - C to Gates generated
  - HDL coded
  - Library IP component

FPGAs provide a rich set of mapping options for complex algorithms and communication patterns

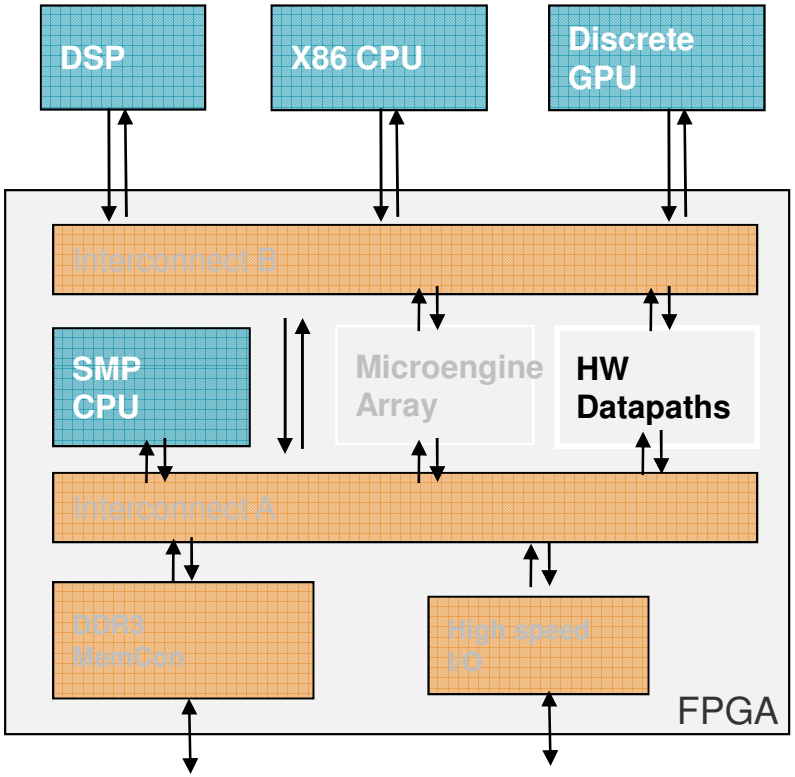
Pre / Post Bitstream Programming
Interconnect



- **Pre bitstream programmable**
  - Buffer sizes
  - Arbitration schemes
- **Post bitstream programmable**
  - Relative port priorities
  - Routing tables

A correctly tuned interconnect is crucial to minimize the inevitable bottlenecks of feeding processors and processing engines

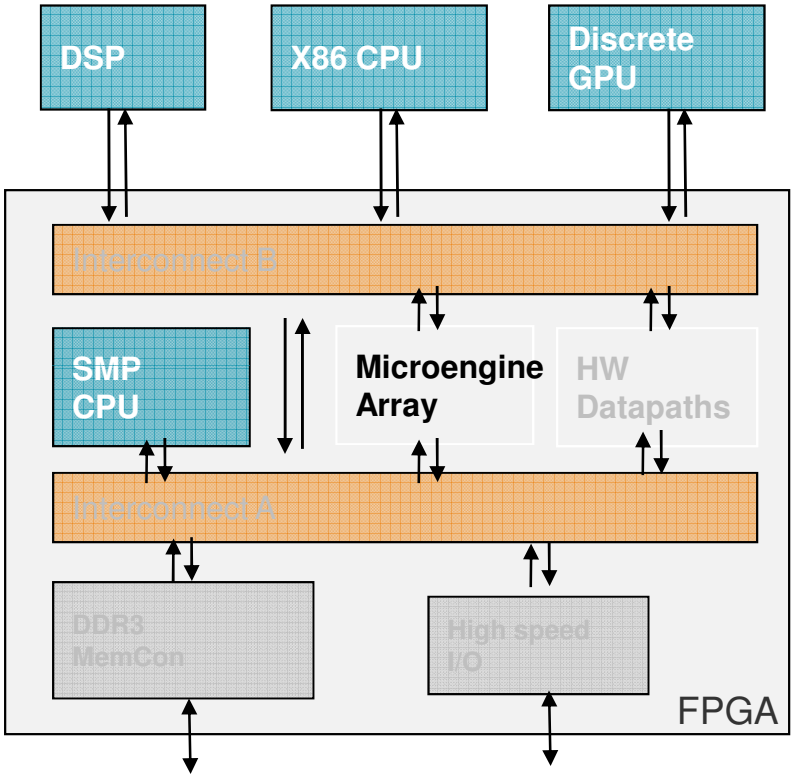
Pre / Post Bitstream Programming
Hardware Datapaths



- **Pre bitstream programmable**
  - C program synthesized
  - Parameters passed in at compile time
- **Post bitstream programmable**
  - Contents of RAMs modifiable

A well built hardware datapath will always outstrip its single core software equivalent

Pre / Post Bitstream Programming
Microengine Array



- **Pre bitstream programmable**
  - Topology of engines
  - Number and type of engines
  - Memory hierarchy
- **Post bitstream programmable**
  - Load kernels into engines
  - Load datasets into memory hierarchy

Most multi-cores are only "post bitstream" programmable

Conclusions

- **If FPGA technology did not exist today, you had to invent this**
- **FPGA will be at the heart of future :**
  - DSP processing
  - Packet processing
  - Embedded computing
- **Enabling technology for high end computing**
  - Silicon roadmap
  - Intimate integration CPU and FPGA
  - Programming flow


XILINX®
Thanks!