Fundamentals of EMI

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Three Basic Elements of EMC

- EMI source
  - Emission
  - Conduction
    - Conductive
    - Low, Middle & High Frequency
  - Space & Field
    - Capacitive
    - Low & Middle Frequency
    - Inductive
    - High Frequency
    - Radiative
  - Coupling process
  - Low, Middle & High Frequency
  - LC Resonance
  - High Frequency

Immunity

EMS
Controlling EMI

EMI source

Coupling process

Conduction

Conductive

EMI Filters

Capacitive

Inductive

Radiative

Space & Field

Shields

EMI Filters

Shields

Shields

Shields

Low & Middle Frequency

LC Resonance

High Frequency

EMS

Immunity

High-Performance EDA
PCB Noise Sources

- **Intentional Signals**
  - Emissions from intentional signals include loop-mode and common-mode sources.

- **Unintentional Signals** (more than 90% of EMI)
  - Emissions from unintentional signals include common-mode, crosstalk coupling to I/O traces (both PCB and IC level), power planes, and above board structures.

*Reference from “PCB Design for Real-World EMI Control,” Bruce Archambeault*
Intentional Signals

- Focus on Clock and High Speed Signals
  - Stripline not necessarily better than Microstrip
  - Examine Clock Harmonics

- Common Mode Conversion
  
  \[ SCD_{11} = 0.5 \times (S_{11} - S_{13} + S_{31} - S_{33}) \]
  
  \[ SCD_{21} = 0.5 \times (S_{21} - S_{23} + S_{41} - S_{43}) \]
Unintentional Signals

- Crosstalk is a big concern
  - Beware the low speed nets; use post-layout analysis to scan for unintended coupling
  - Coupling may be direct, through intermediate metal or even from plane cavities
- Common mode will always exist
  - Don’t neglect the overall plane impedance
Loop Mode & Common Mode Noise

A PC Board & Cables

A Driver & Receiver

A victim device

Loop mode current

by AC Analysis of Q3D Extractor

Differential mode current flows --- Loop
Common mode current flows --- Open

We can see Common mode current is more serious than Normal mode.
Antenna theory

- A Differential mode current flow
- A Common mode current flow

Loop antenna theory
Dipole antenna theory

\[ E = \frac{131.6 \times 10^{-16} (f^2 AI) \sin \theta}{r} \]

\[ E = \frac{4\pi \times 10^{-7} (fIl) \sin \theta}{r} \]

A : area of the loop
r : distance

Illustration of a loop antenna
Illustration of a dipole antenna

FCC B level  Mag. E limit : 40dBuV/m @ 3m
Mag. E( Loop antenna) : 20mA
Mag. E( Dipole antenna) : 8uA
EMC Design Flow

**Impedance Analysis**
Ensure a low impedance as seen by active parts

**Resonance Analysis**
Change stackup, plane cutouts and decoupling as necessary

**Signal Extraction**

**Emissions Analysis**

**Enclosure Simulation**
Decoupling Capacitor

- Decoupling Capacitor on Package
- On-chip Pwr/Gnd
- Ball Bonding
- Wire Bonding
- Ball Bonding
- Power/Ground
- Chip
- Via
- VRM
- Package P/G Network
- PCB P/G Network
- Bulk Capacitor Near VRM
Decoupling Impedance of PDN

- Bare PCB
- 0.01uF
- 0.1uF
- 1uF
- 10uF
- Total PDN
Plasma Screen Example

Changed Return Path
- Widened section of GND plane
- Added decoupling Capacitors

Old model

New model

Impedance test port near C3,4,5
Impedance Plot

Impedance: Old model

Impedance: New model
EMI Test Results: Old model

CISPR spec.
EMI Test Results : New model

<table>
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<th>#</th>
<th>X Axis</th>
<th>Amplitude</th>
<th>Pk</th>
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<td>33.28 dBµV</td>
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<td>28.93 dBµV</td>
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<td>726 MHz</td>
<td>29.52 dBµV</td>
<td>10</td>
<td>163 MHz</td>
<td>24.62 dBµV</td>
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EMC Design Flow

- Impedance Analysis
  Ensure power planes do not resonate in critical locations

- Resonance Analysis
  Change stackup, plane cutouts and decoupling as necessary

- Signal Extraction

- Emissions Analysis

- Enclosure Simulation
Managing Resonances

Even though resonances ALWAYS exist, you don’t need to excite them:

- Keep them away from Clock harmonics
- Examine Via Transitions
- Avoid routing near splits
- Move discrete parts
EMC Design Flow

- Impedance Analysis
- Resonance Analysis
- Signal Extraction
- Emissions Analysis
- Enclosure Simulation

Ensure signals meet required bandwidth
Change routing as necessary
Image Plane Violations

- Always Consider Return Current Path

- Capacitor bridging the moat to transfer RF currents between partitions

- RF current return path

- Signal Trace

- Moat or slot in ground plane
EMI Reduction using Ferrites

- Insert High Q Ferrite
- Insert Low Q Ferrite
- Without Ferrite

Internal Clock Line
EMI Test Results
Clock Distortion
Clock Distortion
Clock Distortion
Clock Distortion
EMC Design Flow

- Impedance Analysis
- Resonance Analysis
- Signal Extraction
- Emissions Analysis

Ensure EMI is at acceptable level
Optimize previous three simulations
Real Drivers as Noise Source

MaxE Radiated from PCB

PCB Data-Line Source spectrum
Near-Fields

Low |Z| at 50 MHz

High |Z| at 137 MHz
EMC Design Flow

- Impedance Analysis
- Resonance Analysis
- Signal Extraction
- Emissions Analysis

Test performance of different enclosures

Iterate design as necessary
Linking EMI Source with Shield

A noise analysis by SIwave

A excitation source

SIwave to HFSS
HFSS to HFSS

A ECU analysis by HFSS

A EM analysis by HFSS
A noise source and a cable

310 MHz
Impedance
Peak on PCB

A cable
Conclusions

- It’s easiest to control EMI at it’s source
  - Prevents Emission and Self Interference
- EMC is comprised of good PI and SI
- Simulating throughout the design cycle can help you avoid trouble in the chamber