Designing a Multilayer PCB Stackup to Balance Signal Integrity Against Manufacturability and Reliability

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THE CHANGING WORLD OF PCB FABRICATION

• At the outset of PCB fabrication PCBs were:
  − Single sided
  − Single layer
  − Had no vias
  − Dealt with clock speeds of 100 KHz
  − Had components with no more than four leads

• As technology has advanced speeds have increased to the present where PCBs:
  − Can have as many as 50 layers
  − Can have components on both sides
  − Have data paths as high as 28 Gb/S
  − Have components with as many as 2400 leads
  − May have both buried and blind vias as well as through hole
PCB PARAMETERS OF CONCERN

- At the outset of PCB fabrication, the concerns were:
  - Accurate etching of 20 mil (.51 mm) wide traces
  - Drilling unplated holes 40 mils in diameter
  - Insuring traces and pads adhered to PCB during soldering

- PCB fabrication concerns of today are:
  - Accurate etching of traces as narrow as 3 mils (76 microns)
  - Drilling holes as small as 8 mils (.254 mm) and plating them
  - Aligning as many as 50 layers to each other
  - Maintaining impedance accuracy
  - Minimizing path loss
  - Creating interplane capacitance
  - Minimizing signal degradation from irregular glass weaves
  - Minimizing cross talk
OBJECTIVES

• Review how stackups are usually done.
• Discuss deficiencies in this method.
• Outline the increased demands on PCB stackups created by faster, denser electronics.
• Examine possible ways to construct a multilayer PCB.
• Examine materials choices.
• Discuss impedance and how to calculate it.
• Examine methods for determining that the final PCB has the correct cross section and impedance.
• Look at some typical stackups and the documentation needed to insure they are correctly fabricated.
WHAT IS STACKUP DESIGN?

Stackup design is the arranging of the signal and power layers of a PCB to meet the electrical and mechanical performance needs of a specific design.

Historically, the primary electrical requirements have been a controlled impedance in the signal layers and enough copper in the plane layers to deliver DC power to the circuits mounted on the PCB.

The primary mechanical requirements have been mechanical stability and ability to withstand soldering and rework.
TRADITIONAL DESIGN APPROACH

• In most cases, PCB stackup design has traditionally been done by each PCB fabricator to exploit the materials and processes it has in place.

• Because of this, a given design may have as many stackups as there are fabricators manufacturing it.

• Initially, the primary concerns were manufacturability and reliability, followed closely by cost.

• As IC speeds increased, the need for controlled impedance was added.

• Most design engineers did not know how to design for a specific impedance.

• As a result, PCB fabricators had to acquire the ability to calculate impedance in order to achieve correct impedance.
DEFICIENCIES WITH TRADITIONAL DESIGN APPROACH

• Impedance calculation is an electrical engineering problem.

• The strengths of PCB fabricators are:
  – Plating
  – Lamination
  – Etching
  – Drilling

• Electrical engineering is not part of that skill set.

• Even so, many fabricators have learned to calculate impedance. (The skill level at each fabricator varies widely.)

• Times have changed and impedance is only one of the electrical requirements that are important in a stackup.

• Crosstalk and interplane capacitance are two other parameters that have been added to the stackup requirements.
REQUIREMENTS FOR A HIGH PERFORMANCE PCB

• Provide enough signal layers to allow successful routing of all signals to signal integrity rules.

• Provide enough power and ground layers to meet needs of the PDS (Power Delivery System).

• Trace widths, spacing and dielectric thickness that meet both impedance and cross talk goals.

• Spacing between power and ground planes that results in adequate plane capacitance while complying with breakdown voltage rules.

• Use of materials that are readily available and comply with assembly requirements.
MULTILAYER PCB MATERIALS

- The three main components that make up a multilayer PCB are:
  - Copper foils
  - Cured laminate with copper foil on both sides
  - Uncured glass/resin sheets called prepreg that will serve as the “glue” during lamination.

- Copper foils are available in many thicknesses. The three main thicknesses are ½ ounce, 1 ounce and 2 ounce with ½ ounce being the dominant thickness. (1 ounce copper is 1.4 mils thick or 36 microns.)

- Laminates and prepreg come as sets from each material supplier. Both are known by their thicknesses and the styles of glass weave used in their makeup. For a given material type such as FR408 there is a wide selection of laminates coupled with a much smaller selection of prepreg styles. Laminates can have any combination of foil thicknesses on each side, but the most commonly have the same thickness copper on both sides.
## A TYPICAL LAMINATE DATA SHEET

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Courtesy of Isola Corporation. This table is for Isola IS620i low loss laminate.
### A TYPICAL PREPREG DATA SHEET

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Courtesy of Isola Corporation. This table is for Isola IS620i low loss prepreg.
MULTILAYER FABRICATION PROCESS

1. Create inner layers details by etching signal and plane layers on adjacent pairs of copper foils on a piece of laminate.

2. Stack inner layers with alternating layers of prepreg.

3. Add foil to outside of stack.

4. Press/laminate stack.

5. Process laminated stack through the outer layer processing steps (drilling, plating, etching and masking).

6. Route PCB from process panel.

7. Test finished PCB to net list.
Foil lamination is the most common method for creating a multilayer PCB.
ALTERNATE PCB FABRICATION METHOD

Cap lamination is the original method for creating a multilayer PCB. It is more expensive than foil lamination. When materials such as Rogers RO4350 are used between L1 and L2 this method is required.
The use of blind and buried vias is often called buildup or HDI construction. It is clearly more expensive than either foil or cap lamination when the same number of layers are involved and is used only when through hole technology is not possible.
CHOOSING A FABRICATOR AS A DESIGN PARTNER

• As can be seen from previous slides, PCB stackup design is a combination of manufacturing engineering and electrical engineering.

• Successful stackup design required close cooperation between electrical engineers and fabrication engineers.

• Therefore, it is advisable for the design engineer to seek out a fabricator whose capabilities are in line with the complexity of the PCB being designed. (This means that the traditional method of allowing purchasing to select fabricators on a price basis will no longer work.)

• Once this alliance is established, the design engineer needs to propose a stackup that meets the electrical requirements and have it reviewed by the fabricator for feasibility.
### TYPES OF SIGNAL LAYERS

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Signal layers on the outside of a PCB are called surface microstrip (L1 and L10 above). Signal layers embedded in the dielectric with a plane on only one side are buried microstrip (L2 and L9 above). Signal layers between two planes are stripline layers (L5 and L6). These can be centered between the planes or offset as shown above.
ALTERNATE WAYS TO STACK LAYERS

OPTION 1

6 SIGNAL LAYERS, ONLY ONE
PLANE PAIR

GOOD FOR ROUTING SIGNALS
POOR FOR POWER DISTRIBUTION

P = Prepreg  L = Laminate
Long bars are plane layers and short bars are signal layers.
SELECTING AN IMPEDANCE

• Common transmission line impedances for PCBs are:
  • 28-33 ohms as specified for Rambus®
  • 50 ohms as used with ECL and other fast logic
  • 62-65 ohms as used with the PCI bus
  • 72-75 ohms as used with video signals.
  • 100 ohm differential- just two 50 ohm lines in a PCB
MULTIPLE IMPEDANCES IN A SINGLE PCB

• It is very difficult to design a PCB stackup for more than one impedance.

• One example is a PCB with a PCI bus and ECL or GTL.

• ECL and GTL require 50 ohms. PCI is usually specified at 62 or 65 ohms.

• Trying to put two different trace widths in the same layer is difficult and sometimes, impossible.

• Designing a stackup with signal layers of different impedances is possible.

• Getting the wiring space correct for each impedance is difficult resulting in some signal layers that are poorly used, others crowded.
IS IT POSSIBLE TO MAKE ALL IMPEDANCES THE SAME?

• Making all of the transmission line impedances the same greatly reduces stackup complexity.

• Making all the transmission line impedances the same greatly reduces design complexity.

• Is it possible to make all impedances the same?

• If so, what impedance?

• 50 ohms is the most common impedance for cables, testers and PCBs.

• Let’s see if it is possible to make all signals 50 ohms.
CAN ALL TECHNOLOGIES WORK WITH 50 OHM TRANSMISSION LINES?

• All currently available logic technologies are capable of operating with 50 ohm transmission lines.

• What about the PCI bus? This bus works fine with 50 ohm impedance transmission lines. (See reference 1.)

• What about 100 ohm differential pairs? Diff pairs are really just two 50 ohm lines. (See reference 2.)

• What about 72 ohm video interfaces? These normally connect to cables that exit the PCB. Placing the driver or receiver close to the connector, so the length of mismatched 50 ohm trace is very short solves this problem without requiring a 72 ohm trace on the PCB. (Simulation will verify this.)

• Yes, one impedance will work and the best values is 50 ohms.
SELECTING LAMINATES

• Laminate systems are commonly made using “E” glass for the woven reinforcement.
• Laminate systems are known by their resin systems.
• There are a wide range of resin systems to choose from.
• Some of these resin systems are listed on the next slide.
• Each resin system was formulated to meet a particular application.
• The merits of many of them are discussed in Chapter 5 of reference 21.
POTENTIAL LAMINATE SYSTEMS

- Epoxy based systems (sometimes called FR4)
- Polyimide
- PPO- Polyphenylene Oxide
- PPE- Polyphenylene Ester
- BT- Bismalamine Triazine.
- CE- Cyanate Ester
- Phenolic cured epoxy
- Cyanate Ester modified epoxy
- Filled Phenolic cured epoxy
## PROPERTIES OF SOME COMMON PCB LAMINATES

<table>
<thead>
<tr>
<th>Material</th>
<th>$T_g$</th>
<th>$e_r^*$</th>
<th>Tan(f)**</th>
<th>DBV(V/Mil)</th>
<th>WA %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Epoxy Glass (FR-4)</td>
<td>125C</td>
<td>4.1</td>
<td>0.02</td>
<td>1100</td>
<td>0.04</td>
</tr>
<tr>
<td>Multifunctional EG (FR-4)</td>
<td>145C</td>
<td>4.1</td>
<td>0.022</td>
<td>1050</td>
<td>0.14</td>
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<tr>
<td>Tetrafunctional EG (FR_4)</td>
<td>150C</td>
<td>4.1</td>
<td>0.022</td>
<td>1050</td>
<td>0.13</td>
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<tr>
<td>Nelco N4000-6 Hi Tg FR-4</td>
<td>170C</td>
<td>4.0</td>
<td>0.012</td>
<td>1300</td>
<td>0.10</td>
</tr>
<tr>
<td>Getek (Megtron 4)</td>
<td>180C</td>
<td>4.1</td>
<td>0.011</td>
<td>1100</td>
<td>0.12</td>
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<tr>
<td>BT Epoxy Glass</td>
<td>185C</td>
<td>4.1</td>
<td>0.023</td>
<td>1350</td>
<td>0.20</td>
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<tr>
<td>Nelco 4000-13SI</td>
<td>210</td>
<td>3.3</td>
<td>0.009</td>
<td>1400</td>
<td>0.09</td>
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<td>Cyanate Ester</td>
<td>245C</td>
<td>4.0</td>
<td>0.01</td>
<td>800</td>
<td>0.70</td>
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<tr>
<td>Rogers RO4350</td>
<td>280C</td>
<td>3.5</td>
<td>0.004</td>
<td>780</td>
<td>0.04</td>
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<tr>
<td>Polyamide Glass</td>
<td>285C</td>
<td>4.1</td>
<td>0.015</td>
<td>1200</td>
<td>0.43</td>
</tr>
<tr>
<td>Teflon Glass</td>
<td>N/A</td>
<td>2.2</td>
<td>0.002</td>
<td>450</td>
<td>0.01</td>
</tr>
</tbody>
</table>

* Measured at 2 GHz with a resin content of 55%.
** This is loss tangent, an expression of how much signal is lost in the dielectric.

$T_g$ = Glass Transition Temperature
DBV= Dielectric breakdown voltage.
WA = Water Absorption, more than 0.25% results in PCBs that fail leakage tests.
All materials reinforced with woven glass.

Notice that a 5 mil thickness of any glass reinforced material has a dielectric breakdown voltage approaching or exceeding 5000 volts.
CONSIDERATIONS WHEN SELECTING A LAMINATE SYSTEM

- Lead free assembly
- Halogen free materials
- Ability to withstand high temperatures
- Need for low dielectric loss
- Sensitivity to single source materials
- Need to prototype one place and produce another
- Cost and price
**OBTAINING LAMINATE INFORMATION**

- First choice for laminate information is the laminate manufacturer.
- Second choice is fabricators.
- The amount of information held by fabricators varies from virtually none to very complete data sets.
- Type of information needed is:
  - Dielectric constant vs. frequency for each laminate and prepreg
  - Dielectric loss vs. frequency for each laminate and prepreg
  - Types of glass cloth used in each laminate and prepreg
  - Copper foil roughness needed for good adhesion.

Some laminate supplier web sites:
- [www.isola-group.com](http://www.isola-group.com)
- [www.parknelco.com](http://www.parknelco.com)
- [www.rogerscorp.com](http://www.rogerscorp.com)
HOW THIN SHOULD LAMINATE AND PREPREG BE?

- As can be seen on slides 8 and 9, laminate and prepreg is available in thicknesses as thin as 2 mils (51 microns).

- Some specialty materials are available as thin as 1 mil (25 microns) and 0.5 mil (13 microns).

- The principal consideration when selecting thin laminates and prepregs is the breakdown voltage requirement of the design.

- For most products intended for the Telco market this is 1500 volts.

- Most commercially available laminates have breakdown voltages around 1000 volts per mil of thickness (25 microns). This would make it unwise to use materials thinner than 2 mils.
EFFECTS OF GLASS WEAVE ON FAST DIFFERENTIAL SIGNALS

• If the distribution of glass in the dielectric is not uniform it can result in variations in impedance and velocity along the length of a trace.

• When differential signals travel over loose weave glass, one member of the pair may be faster than the other resulting in skew and data errors.

• Variations in impedance along a trace can result in unwanted reflections that degrade the signal amplitude.

• This effect can be pronounced on signals of 2.4 Gb/S and higher.
GLASS STYLES OR WEAVES

• The glass used as reinforcement in PCB materials is available as random glass and woven glass.

• Random glass has not proved to be sufficiently stable for use in precision PCBs.

• Woven glass is the reinforcement of choice for nearly all PCBs. (There are woven non-glass cloths available at high price premiums.)

• Woven glass is available in a wide variety of styles. The next slide shows some of them. The “standard construction” columns on slides 8 and 9 show many of them. Page 109 of reference 4 shows more examples.)

• Certain glass weaves can have undesirable effects on very high speed signals. (References 5, 7, 9 & 10)
SOME REPRESENTATIVE GLASS STYLES

106

WIRE IS 3.5 MILS IN DIAMETER

1080

2113

3313
Impedance variation is due to variation of dielectric constant. This also causes velocity to vary, resulting in differential skew in differential pairs.
SELECTING THE PROPER COPPER FOIL THICKNESS

• Copper foils are available in a variety of thicknesses. They are rated in ounces. One ounce copper is 1.4 mils (36 microns) thick. ½ ounce 0.7 mils (18 microns) etc.

• Thicker copper is more difficult to etch and process. Thinner copper has less conductivity.

• Thickness may differ between signal and power layers.

• For etching reasons, it is desirable to use the same thickness copper on both sides of a piece of laminate.

• If one side of a piece of laminate is a signal layer and the other a power plane, which should dominate?
SIGNAL LAYER THICKNESS

• Nearly all signal layers in modern designs have signals fast enough that skin effect loss and skin depth determine how thick the signal traces need to be.

• “Skin effect” is the behavior of current flow in conductors at high frequencies where the current flows near the surface of a conductor rather than all the way through it. (See reference 12.)

• When frequencies are high enough that the current is penetrating less than half the thickness of the conductor, making that conductor any thicker is of no value.

• For etching uniformity it is useful to make signal layers as thin as possible. (1/2 ounce being a good compromise).
SKIN DEPTH VS. FREQUENCY

Notice that at 1 GHz, skin depth is 2 microns or 80 micro inches. Trace layers thicker than ½ ounce copper do not help above this frequency.

Therefore, ½ ounce signal layers are ”good enough” for high speed signals.
COPPER SURFACE ROUGHNESS

• There has been much concern over the roughness of the copper surface and its effect on loss at high frequencies.

• The graph below depicts loss due to roughness from smooth copper to the roughest used in lamination.

• At 5 GHz (10Gb/S) loss varies 0.1 db per inch from roughest to smoothest. It is desirable to use smooth copper finish.
Two PCBs built at two different fabricators using the same materials and the same stackup yield different losses due to differing surface roughness done during processing. Copper roughness has been left to each fabricator. With the advent of 10 Gb/S and higher signal paths, this is no longer allowable. Test structure is 7" Daughterboard made from FR408HR, 13" backplane made from Megtron 6 and 7" daughter board made from FR408HR. Only daughter boards were changed.
INSURING UNIFORM LOSS FROM LOT TO LOT

• The two PCBs in the previous slide were build from the same artwork and material by two different fabricators.

• They differ only in the roughness of the copper as finished by each fabricator.

• Copper roughness, by fabricator, varies substantially. Why?

• Until recently, the only driving force for copper roughness has been to insure delamination does not occur.

• Fabricators with prior experience with delamination tend to be aggressive with their roughening step.

• In order to insure uniform loss from this operation it is necessary to call out copper roughness maximums on fabrication drawings.
CROSS SECTION OF TWO PCBS ON PREVIOUS SLIDE

Supplier #1 Oxide

Supplier #2 Oxide

Poor Loss

Good Loss
PROBLEMS WITH ROUGHNESS SPECIFICATIONS

• At the present time, there are no standards for specifying copper roughness.

• There are several designators such as low profile, but each copper supplier uses the term differently.

• It appears there is no activity underway to develop a reliable roughness standard.

• At present, the only reliable way to control copper roughness is to determine the minimum copper roughness required to assure delamination does not occur and put this requirement on the fabrication drawing.

• The proper place to obtain the copper roughness spec. is the laminate manufacturer.
BASIC COPPER CONDUCTIVITY

- The chart below illustrates DC resistivity of copper traces by foil thickness and trace width.
- This data is useful for calculating trace width for DC signals.
TRADING OFF TRACE WIDTH VS. OVERALL PCB THICKNESS

• Skin effect loss in traces is primarily a function of frequency and outer surface layer area of the trace.

• To minimize skin effect loss it is tempting to select the widest trace that will fit between pins of components.

• In order to maintain a 50 ohm impedance the height above the nearest plane must be increased, making the overall PCB thick. This also increases overall cost.

• Traces farther away from planes also have higher crosstalk.

• Making traces wide reduce skin effect loss, but has undesirable side effects. (higher crosstalk, thicker PCBs, more cost)
AN EXAMPLE OF SKIN EFFECT AND DIELECTRIC LOSS IN A SIGNAL PATH

Dielectric loss dominates the loss problem for current technologies. Changing dielectric is much better than using wider traces.
TRACE WIDTH CONCLUSIONS

- From the previous slide, varying trace width from 5 mils (127 microns) to 10 mils (254 microns) reduces skin effect loss at 2.5 GHz (5 Gb/S) approximately 1 db for 33” (84 cm) long trace.

- Changing trace width from 5 mils to 10 mils results in a PCB that is often twice as thick. (This makes cost go up and plating more difficult.)

- Changing from a lossy dielectric to a less lossy dielectric has a much bigger impact on overall loss.

- To minimize overall loss and maximize manufacturability, it is wise to use lower loss laminate and minimize trace width. (My standard trace width is 5 mils (127 microns, even at 10 Gb/S).)
DECIDING WHETHER TO USE “LOW LOSS” LAMINATE SYSTEM

- In this context low loss means low dielectric loss.

- Dielectric loss in a path is a function of path length and operating frequency.

- In order to determine whether a low loss laminate is needed for a particular application it is necessary to employ an analytical tool to model the proposed path.

- As always, the results of any analysis should be verified by constructing a test circuit to validate them.

- From experience designing many “high speed” PCBs, I have found that most products do not need low loss laminates.
SELECTING PLANE COPPER THICKNESS

• When pairing plane layers with signal layers across a piece of laminate, it is wise to use the same copper thickness on both sides to insure etching is uniform on both sides.

• For impedance control reasons, it is desirable to mate every signal layer with a plane.

• From previous slides it was shown that ½ ounce in signal layers is the best choice.

• Is ½ ounce copper good enough for plane layers? Depends on the current flow and allowable voltage drop in the planes. (Chapter 33 in reference 3 discusses how to perform this analysis.)

• In most cases, ½ ounce planes are satisfactory.
POWER PLANE CAPACITANCE

• A key component of any high performance PCB is the capacitance formed by adjacent power and ground layers.

• This high quality (low inductance) capacitance is necessary to support the very fast switching transients associated with driving single ended transmission lines and the rapidly changing IC core supply currents.

• The amount of plane capacitance needed is calculated as part of the PDS design.

• Once the amount of plane capacitance is known, the plane area and separation needed to achieve that capacitance can be designed into the stackup.

• In some cases it may be necessary to have more than one plane pair to support a given power supply voltage.
POWER PLANE CAPACITANCE vs. DIELECTRIC THICKNESS
DIELECTRIC CONSTANT = 4.1 (FR-4)

\[ C \text{ in } \text{pF/SQIN}, \quad t \text{ is thickness in mils} \]

SOLID PLANES

PLANE WITH 30% AREA LOSS
TYPICAL OF SMT PCBs
There are two basic methods for calculating impedance. They are:

- Equations
- Field solvers

All equations are partial solutions that are accurate over a narrow range of variables.

Field solvers employ Maxwell’s equations to precisely calculate impedance for any geometry and are more accurate than any of the equations.
FOUR BASIC TYPES OF PCB TRANSMISSION LINES

NOTE: VARIABLES ABOVE CORRESPOND TO THOSE USED IN THE IMPEDANCE EQUATIONS IN THIS COURSE.
AN IMPEDANCE EQUATION FOR SURFACE MICROSTRIP

\[ Z_0 = \frac{79}{\sqrt{e_r + 1.41}} \ln \left( \frac{5.98H}{0.8W + T} \right) \]

- \( e_r \) = RELATIVE DIELECTRIC CONSTANT
- \( H \) = HEIGHT OF TRACE ABOVE PLANE
- \( W \) = TRACE WIDTH
- \( T \) = TRACE THICKNESS
- \( Z_0 \) = TRACE IMPEDANCE IN OHMS

Any dimension system is applicable

NOTE: VALID FOR 5 < \( w \) < 15 MILS

\( e_r \) value is that obtained from velocity measurements made with a TDR.

A more precise calculation can be obtained using a 2D field solver which the author recommends.
BURIED MICROSTRIP IMPEDANCE EQUATION

\[ Z_0 = \text{TRANSMISSION LINE IMPEDANCE (OHMS)} \]
\[ H = \text{HEIGHT OF LINE ABOVE POWER PLANE} \]
\[ W = \text{TRACE WIDTH} \]
\[ T = \text{TRACE THICKNESS} \]
\[ e_r = \text{RELATIVE DIELECTRIC CONSTANT} \]

Valid for \(5 < W < 15\) mils, valid for any dimension system
Assumes at least 5 mils of dielectric lying on top of trace.

\[ Z_0 = \left( 43.037 \ln \frac{H}{W} \right) + 5.048 \left( \frac{T}{W} \right) + \frac{106.76}{1.09 \sqrt{e_r}} \]

A more precise calculation can be obtained using a 2D field solver which the author recommends.
ASYMMETRIC STRIPLINE IMPEDANCE EQUATION

- $Z_0 =$ TRANSMISSION LINE IMPEDANCE
- $B =$ TRACE TO PLANE SPACING
- $C =$ TRACE PLANE TO TRACE PLANE SPACING
- $T =$ TRACE THICKNESS
- $W =$ TRACE WIDTH
- $e_r =$ relative dielectric constant of insulator
- FOR $C = 0$, equation applies to centered stripline
- Valid for $5 < W < 15$ mils

$$Z_0 = 80 \left[ 1 - \frac{B}{4(B+C+T)} \right] \ln \left[ \frac{1.9(2B+T)}{(0.8W+T)} \right]$$

A more precise calculation can be obtained using a 2D field solver which the author recommends.
SOME 2D FIELD SOLVERS FOR IMPEDANCE CALCULATIONS

• Hyperlynx Linsym- Does whole cross section at once,
• Polar Instruments Si9000b- Can do whole cross section at once. Most used by fabrication shops.
• Cadence PCB SI- Does whole cross section at once.
• Applied Simulation Technologies RLGC.
• ADS by Agilent (also 3D)
• HFSS by Ansoft (Also 3D)
R, L, C TRANSMISSION LINE MODEL

O - R - L - R - L - R - L - R - L - R - L - O

I   I   I   I
C   C   C   C
I   I   I   I
P   P   P   P

O = END OF LINE     R = RESISTANCE PER UNIT LENGTH
P = PLANE           L = INDUCTANCE PER UNIT LENGTH
C = CAPACITANCE PER UNIT LENGTH

Model assumes a plane of negligible inductance and resistance.

The following equations permit one to calculate the reactance of capacitors and inductors as a function of frequency.

\[ X_C = \frac{1}{2\pi fC} \]
\[ X_L = 2\pi fL \]

\( X_C = \text{Capacitive Reactance} \)
\( X_L = \text{Inductive Reactance} \)
THE IMPEDANCE EQUATION

\[ Z_0 = \text{CHARACTERISTIC IMPEDANCE OF LINE} \]
\[ L_0 = \text{INDUCTANCE PER UNIT LENGTH} \]
\[ C_0 = \text{CAPACITANCE PER UNIT LENGTH} \]
\[ R_0 = \text{RESISTANCE PER UNIT LENGTH} \]
\[ G_0 = \text{TRANSCONDUCTANCE PER UNIT LENGTH} \]

\[ Z_0 = \sqrt{\frac{R_0 + j\omega L_0}{G_0 + j\omega C_0}} \quad Z_0 = \sqrt{\frac{L_0}{C_0}} \]

Exact Equation             Simplified Equation

As capacitance is added to a transmission line (example: periodic loads) the impedance goes down. Note that impedance is independent of length and frequency.

These equations are useful only when there is a ready means for determining values per unit length.
THE CONTROL SCREEN FOR THE HYPERLYNX 7.0 FIELD SOLVER
CADENCE PCB SI FIELD SOLVER

SpecctraQuest Fieldsolve Impedance Calculator

<table>
<thead>
<tr>
<th>Ech Sublayer</th>
<th>Type</th>
<th>Thickness</th>
<th>Dielectric Constant</th>
<th>Loss Tangent</th>
<th>Shield</th>
<th>Line Width</th>
<th>Impedance</th>
<th>Coupling Type</th>
<th>Spacing</th>
<th>Differential Impedance</th>
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<tr>
<td>1</td>
<td>SURFACE</td>
<td>5.6 MIL</td>
<td>1</td>
<td>0</td>
<td>EDGE</td>
<td>6.500 MILE</td>
<td>50.138 ohm</td>
<td>EDGE</td>
<td>6.000 MILE</td>
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</tr>
</tbody>
</table>

Total Thickness: 10.4 MIL

Stripline Layer Dielectric: [Determined Automatically]

Dielectric Constant: [ ]

Loss Tangent: [ ]

Differential Mode: [ ]
THE CONTROL SCREEN FOR THE POLAR INSTRUMENTS Si8000/SB200

POTENTIAL ERRORS IN IMPEDANCE CALCULATIONS

- There are several places errors can creep into impedance calculations. Among these are:
  - Equation inaccuracy
  - Incorrect dielectric constant for laminate
  - Tool precision
  - Bad assumptions by fabrication houses
  - From experience, it has been demonstrated that field solvers are capable of calculating impedance to an accuracy of less than 1%.
COMPARING FIELD SOLVER RESULTS TO EQUATION RESULTS
FIELD SOLVER vs. EQUATIONS

EQ SMS
EQ BMS
EQ CSL
FS SMS
FS BMS
FS CSL

Er = 4, Th = 1.4 mils, Height = 5 mils

SMS = Surface microstrip, EMS = embedded microstrip, CSL = centered stripline
WHAT IS RELATIVE DIELECTRIC CONSTANT, $e_r$?

• Relative dielectric constant, $e_r$, is a measure of the affect an insulator has on the capacitance of a pair of conductors as compared to the same conductor pair in a vacuum.

• The dielectric constant of a vacuum is 1. All materials have dielectric constants higher than 1.

• A common method for measuring $e_r$ is the parallel plate method at 1 MHz. A more useful method for transmission line design is signal velocity in the dielectric.
AN EQUATION FOR CALCULATING $e_r$ USING VELOCITY MEASURED WITH A TDR

- $C =$ SPEED OF LIGHT, .0118 INCH/pSEC
- $V =$ MEASURED PROPAGATION VELOCITY

$$\sqrt{e_r} = \frac{C}{V}$$

NOTE: All dielectrics slow electromagnetic waves down according to the above formula.

Note: As will be seen later, $e_r$ varies with frequency in most PCB materials.
RELATIVE DIELECTRIC CONSTANT vs. FREQUENCY
FOR VARIOUS LAMINATES

FOR RESIN CONTENT OF 42%
EXCEPT ** AT 55%

NOTE: MOST LAMINATES USED IN MULTILAYER PCBs AVERAGES ABOUT 55% RESIN CONTENT.
Materials Comparison

- Dielectric constant ($\varepsilon_r$) vs. frequency

Morgan, Chad & Helster, Dave, “The Impact of PWB Construction on High-Speed Signals” DesignCon99.

Courtesy AMP Circuits and Design 3/99
DIELECTRIC CONSTANT AS A FUNCTION OF GLASS TO RESIN RATIO

DIELECTRIC CONSTANT FOR FR-4 TYPE MATERIALS AS A FUNCTION OF GLASS TO RESIN RATIO

NOTE: THESE VALUES ARE FOR A 1MHz TEST FREQUENCY. AT HIGHER FREQUENCIES, THE ENTIRE CURVE WILL SHIFT DOWNWARD.

USUAL RANGE OF $e_r$ FOR MULTILAYER PCBs

PURE RESIN HAS AN $e_r$ OF APPROX 3.4 AT 1 MHz

RELATIVE DIELECTRIC CONSTANT $e_r$

PERCENT RESIN CONTENT
# SOME PROPERTIES OF HI Tg “FR-4” LAMINATE

Data courtesy of NELCO

<table>
<thead>
<tr>
<th>Thickness</th>
<th>Construction</th>
<th>Resin Content</th>
<th>$\varepsilon_r @ 1$ MHz</th>
<th>$\varepsilon_r @ 1$ GHz</th>
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<tr>
<td>.002</td>
<td>1 x 106</td>
<td>69.0%</td>
<td>3.84</td>
<td>3.63</td>
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<tr>
<td>.003</td>
<td>1 x 1080</td>
<td>62.0%</td>
<td>4.00</td>
<td>3.80</td>
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<tr>
<td>.004</td>
<td>1 x 2113</td>
<td>54.4%</td>
<td>4.19</td>
<td>4.00</td>
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<tr>
<td>.004</td>
<td>1 x 106 + 1 x 1080</td>
<td>57.7%</td>
<td>4.11</td>
<td>3.91</td>
</tr>
<tr>
<td>.004</td>
<td>1 x 2116</td>
<td>43.0%</td>
<td>4.54</td>
<td>4.37</td>
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<tr>
<td>.005</td>
<td>1 x 106 + 1 x 2113</td>
<td>52.8%</td>
<td>4.24</td>
<td>4.05</td>
</tr>
<tr>
<td>.005</td>
<td>1 x 2116</td>
<td>51.8%</td>
<td>4.26</td>
<td>4.08</td>
</tr>
<tr>
<td>.006</td>
<td>1 x 1080 + 1 x 2113</td>
<td>52.2%</td>
<td>4.25</td>
<td>4.06</td>
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<tr>
<td>.006</td>
<td>1 x 106 + 1 x 2116</td>
<td>50.8%</td>
<td>4.29</td>
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<tr>
<td>.006</td>
<td>2 x 2113</td>
<td>43.5%</td>
<td>4.52</td>
<td>4.35</td>
</tr>
<tr>
<td>.007</td>
<td>2 x 2113</td>
<td>49.6%</td>
<td>4.33</td>
<td>4.14</td>
</tr>
<tr>
<td>.008</td>
<td>1 x 7628</td>
<td>44.4%</td>
<td>4.49</td>
<td>4.32</td>
</tr>
<tr>
<td>.010</td>
<td>2 x 2116</td>
<td>51.8%</td>
<td>4.26</td>
<td>4.08</td>
</tr>
<tr>
<td>.014</td>
<td>2 x 7628</td>
<td>38.8%</td>
<td>4.69</td>
<td>4.53</td>
</tr>
</tbody>
</table>

Under construction, the three or four digit number refers to the glass weave type.
IMPEDANCE ACCURACY

• In order to achieve accurate impedance calculations it is necessary to use a field solver.

• Since relative dielectric constant of a laminate or prepreg is frequency dependent, it is necessary to know the frequency of interest (not clock frequency, rather the frequency content of the switching edges).

• Since relative dielectric constant of a laminate or prepreg is dependent on glass to resin ratio, it is necessary to know this for each laminate and prepreg.

• Using field solvers with accurate information about the relative dielectric constant of the laminate, impedance calculations are more accurate than ±1%.

• Well run fabricators with good process control can achieve impedance accuracy of ±10%.
MEASURING IMPEDANCE

• Impedance of a transmission line is an “AC” property. Therefore, using an ohmmeter will not work.

• The instrument of choice for measuring impedance is a Time Domain Reflectometer (TDR).

• A TDR functions like a radar sending a very fast pulse down a signal path and looking for reflections.

• The size and polarity of these reflections can be used to calculate the impedance of the transmission line.

• In order for these measurements to be accurate, the TDR must be properly calibrated and the impedance measurement location carefully chosen. (Notice on slide 30 that the impedance appears to increase along the length of the transmission line.)
• TDR TEST SETUP USED FOR MEASURING TRANSMISSION LINE PROPERTIES

1. Set up TDR to show entire trace and reflection at open end.
2. Attach trim pot to open end of trace and adjust until reflection is gone.
3. Use ohmmeter setting on DVM to measure resistance of trim pot.
4. This value is Zo

STEPS IN BUILDING A STACKUP

- Determine how many signal layers are needed.
- Determine how many power planes are needed to distribute power and ground.
- Arrange signals and planes to accomplish
  - Partners for signal layers
  - Parallel plate capacitance between power and ground
- Set signal height above planes to meet cross talk requirements.
- Set trace widths to meet impedance requirements.
- Set spacing between planes to meet capacitance requirements.
- Set spacing between signal layers to meet overall thickness.
TYPES OF SIGNAL LAYERS

<table>
<thead>
<tr>
<th>Layer</th>
<th>Type</th>
<th>Trace Width (mils)</th>
<th>Impedance (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>OUTER &quot;CAP&quot; LAYER</td>
<td>7.0</td>
<td>50.0</td>
</tr>
<tr>
<td>L2</td>
<td>SIGNAL 1</td>
<td>7.0</td>
<td>5.0  50.0</td>
</tr>
<tr>
<td>L3</td>
<td>GROUND 1</td>
<td>5.0</td>
<td>3.0  50.0</td>
</tr>
<tr>
<td>L4</td>
<td>Vdd 1</td>
<td>3.0</td>
<td>3.0  LAMINATE</td>
</tr>
<tr>
<td>L5</td>
<td>SIGNAL 2</td>
<td>5.0</td>
<td>5.0  50.0</td>
</tr>
<tr>
<td>L6</td>
<td>SIGNAL 3</td>
<td>7.0</td>
<td>5.0  50.0</td>
</tr>
<tr>
<td>L7</td>
<td>Vdd 2</td>
<td>5.0</td>
<td>3.0  PREPREG</td>
</tr>
<tr>
<td>L8</td>
<td>GROUND 2</td>
<td>3.0</td>
<td>3.0  PREPREG</td>
</tr>
<tr>
<td>L9</td>
<td>SIGNAL 4</td>
<td>5.0</td>
<td>5.0  50.0</td>
</tr>
<tr>
<td>L10</td>
<td>OUTER &quot;CAP&quot; LAYER</td>
<td>7.0</td>
<td>50.0</td>
</tr>
</tbody>
</table>

Signal layers on the outside of a PCB are called surface microstrip (L1 and L10 above). Signal layers embedded in the dielectric with a plane on only one side are buried microstrip (L2 and L9 above). Signal layers between two planes are stripline layers (L5 and L6). These can be centered between the planes or offset as shown above.
### FIRST PASS IMPEDANCE USING SOLVER AND GOOD LAMINATE DATA

**FIRST TRY IMPEDANCE TEST RESULTS**

<table>
<thead>
<tr>
<th>Layer#</th>
<th>Material Name</th>
<th>Material Type</th>
<th>Material Constv</th>
<th>$\varepsilon_r \mu_r$ (Gn)</th>
<th>Metalized Unpvn Thickness (mil)</th>
<th>Picture</th>
<th>Copper/Total Thickness (mil)</th>
<th>Single Sided Trace Width (mil)</th>
<th>Single Sided Impedance (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SML</td>
<td>Copper</td>
<td>Copper</td>
<td>0.7</td>
<td>105</td>
<td>0</td>
<td>0.7</td>
<td>0.1</td>
<td>48.6</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Lamin M692 H</td>
<td>Plating</td>
<td>0.25 ± 0.06</td>
<td>0.07</td>
<td>4.6</td>
<td>2.1</td>
<td>0.1</td>
<td>105</td>
<td>0.7</td>
</tr>
<tr>
<td>2</td>
<td>Lamin M692 H</td>
<td>Comers</td>
<td>0.25 ± 0.06</td>
<td>0.12</td>
<td>2.0</td>
<td>2.0</td>
<td>0.1</td>
<td>105</td>
<td>0.7</td>
</tr>
<tr>
<td>3</td>
<td>Lamin M692 H</td>
<td>Plating</td>
<td>0.25 ± 0.06</td>
<td>0.14</td>
<td>4.5</td>
<td>2.1</td>
<td>0.1</td>
<td>105</td>
<td>0.7</td>
</tr>
<tr>
<td>4</td>
<td>Lamin M692 H</td>
<td>Comers</td>
<td>0.25 ± 0.06</td>
<td>0.16</td>
<td>2.0</td>
<td>2.0</td>
<td>0.1</td>
<td>105</td>
<td>0.7</td>
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<td>5</td>
<td>Lamin M692 H</td>
<td>Plating</td>
<td>0.25 ± 0.06</td>
<td>0.18</td>
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<td>0.1</td>
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<td>0.7</td>
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<td>Comers</td>
<td>0.25 ± 0.06</td>
<td>0.20</td>
<td>4.5</td>
<td>2.1</td>
<td>0.1</td>
<td>105</td>
<td>0.7</td>
</tr>
<tr>
<td>7</td>
<td>Lamin M692 H</td>
<td>Plating</td>
<td>0.25 ± 0.06</td>
<td>0.22</td>
<td>4.5</td>
<td>2.1</td>
<td>0.1</td>
<td>105</td>
<td>0.7</td>
</tr>
<tr>
<td>8</td>
<td>Lamin M692 H</td>
<td>Comers</td>
<td>0.25 ± 0.06</td>
<td>0.24</td>
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<td>2.1</td>
<td>0.1</td>
<td>105</td>
<td>0.7</td>
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<td>9</td>
<td>Lamin M692 H</td>
<td>Plating</td>
<td>0.25 ± 0.06</td>
<td>0.26</td>
<td>4.5</td>
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<tr>
<td>10</td>
<td>Lamin M692 H</td>
<td>Comers</td>
<td>0.25 ± 0.06</td>
<td>0.28</td>
<td>4.5</td>
<td>2.1</td>
<td>0.1</td>
<td>105</td>
<td>0.7</td>
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</tbody>
</table>

All well within ±10% limits.

**TARGET IMPEDANCE:**

50Ω ±10%
COMMENTS ON STACKUP DRAWING

• Notice that there is far more information on this drawing than is typically provided to a fabricator.

• Exact callouts are done for each laminate and prepreg location.

• The reason for this is to insure that all SI goals are met and that manufacturing is repeatable from fabricator to fabricator.

• When stackup drawing is supplied to fabricator, the impedance column is removed. Specifying both impedance and exact cross section creates a conflict.

• Fabricators will usually recalculate impedance and get different results unless their skills are extremely good.

• Prepreg layers shrink during lamination due to resin flow into adjacent copper layers.
### A 26 Layer Stackup with Single Stripline Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Natural Name</th>
<th>Natural Type</th>
<th>Natural Orientation</th>
<th>Material Unpumped (oz/ft^2)</th>
<th>Material Packed SI (oz/ft^2)</th>
<th>Material Prepreg Thickness (mil)</th>
<th>Prepreg</th>
<th>Copper Thickness (mil)</th>
<th>Single Edge Trace Width (mil)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FR-4 Glass</td>
<td>1.031 RC C 0.015%</td>
<td>0.7</td>
<td>0.05</td>
<td>0.06</td>
<td>0.06</td>
<td>22</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>FR-4 Glass</td>
<td>1.031 RC C 0.015%</td>
<td>0.7</td>
<td>0.05</td>
<td>0.06</td>
<td>0.06</td>
<td>22</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>FR-4 Glass</td>
<td>1.031 RC C 0.015%</td>
<td>0.7</td>
<td>0.05</td>
<td>0.06</td>
<td>0.06</td>
<td>22</td>
<td>1.5</td>
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<td>FR-4 Glass</td>
<td>1.031 RC C 0.015%</td>
<td>0.7</td>
<td>0.05</td>
<td>0.06</td>
<td>0.06</td>
<td>22</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>FR-4 Glass</td>
<td>1.031 RC C 0.015%</td>
<td>0.7</td>
<td>0.05</td>
<td>0.06</td>
<td>0.06</td>
<td>22</td>
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<td>1.031 RC C 0.015%</td>
<td>0.7</td>
<td>0.05</td>
<td>0.06</td>
<td>0.06</td>
<td>22</td>
<td>1.5</td>
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<td>7</td>
<td>FR-4 Glass</td>
<td>1.031 RC C 0.015%</td>
<td>0.7</td>
<td>0.05</td>
<td>0.06</td>
<td>0.06</td>
<td>22</td>
<td>1.5</td>
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<td>8</td>
<td>FR-4 Glass</td>
<td>1.031 RC C 0.015%</td>
<td>0.7</td>
<td>0.05</td>
<td>0.06</td>
<td>0.06</td>
<td>22</td>
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<td>0.05</td>
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<td>0.06</td>
<td>22</td>
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<td>0.05</td>
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<td>11</td>
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<td>0.7</td>
<td>0.05</td>
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<td>22</td>
<td>1.5</td>
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<tr>
<td>13</td>
<td>FR-4 Glass</td>
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<td>0.05</td>
<td>0.06</td>
<td>0.06</td>
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<td>15</td>
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<td>0.05</td>
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<td>16</td>
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<tr>
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<td>FR-4 Glass</td>
<td>1.031 RC C 0.015%</td>
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<td>0.05</td>
<td>0.06</td>
<td>0.06</td>
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<tr>
<td>23</td>
<td>FR-4 Glass</td>
<td>1.031 RC C 0.015%</td>
<td>0.7</td>
<td>0.05</td>
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<td>24</td>
<td>FR-4 Glass</td>
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</tr>
</tbody>
</table>

*Note: Copper thickness is determined by removing prepreg in layers.*
# A 14 LAYER STACKUP

## 14 LAYER PCB 11/02/06

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>Top</td>
<td>FR-408</td>
<td>Prepreg</td>
<td>1 x 3313 RC = 53.8%</td>
<td>3.7</td>
<td>4</td>
<td>3.4</td>
<td>Prepreg</td>
<td>0.7</td>
<td>Spider Mask</td>
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<td>1.5</td>
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</tr>
<tr>
<td>S1</td>
<td>FR-408</td>
<td>Core</td>
<td>1 x 3313 RC = 53.8%</td>
<td>3.7</td>
<td>4</td>
<td>Core</td>
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<td>0.5</td>
<td>6</td>
<td>52.0</td>
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<td>2</td>
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</tr>
<tr>
<td>Ground</td>
<td>FR-408</td>
<td>Prepreg</td>
<td>2 x 106 RC = 63.3%</td>
<td>4</td>
<td>4</td>
<td>3</td>
<td>Prepreg</td>
<td>0.6</td>
<td>0.5</td>
<td>5</td>
<td>50.0</td>
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</tr>
<tr>
<td>3</td>
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<tr>
<td>V1</td>
<td>FR-408</td>
<td>Core</td>
<td>1 x 3313 RC = 53.8%</td>
<td>3.7</td>
<td>4</td>
<td>Core</td>
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<td>0.5</td>
<td>5</td>
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<td>4</td>
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<tr>
<td>S2</td>
<td>FR-408</td>
<td>Prepreg</td>
<td>1 X 3315 RC = 53.8%</td>
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<td>4</td>
<td>3</td>
<td>Prepreg</td>
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<tr>
<td>5</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>S3</td>
<td>FR-408</td>
<td>Core</td>
<td>1 x 3313 RC = 53.8%</td>
<td>3.7</td>
<td>4</td>
<td>Core</td>
<td>0.6</td>
<td>0.5</td>
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<td>50.0</td>
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**Note:** Place only information to left of dark line on fabrication drawing. Do not place impedance information on fabrication drawing.

Prepared by Speeding Edge, 11/02/06

Layers 1 and 14 are to be used for component mounting and traces that are not controlled impedance. 10GIGE/T net signals to be routed only on layer 2 and be connected using blind vias to layer 1.
ACCOUNTING FOR RESIN FLOW INTO COPPER

• During lamination, heat is applied and the resin in prepreg layers melts and flows into voids in the adjacent power and signal layers.

• As a result, the overall thickness of the PCB and the prepreg layers will be less than expected.

• Allowance must be made for this decrease in thickness.

• The best way to do this is to obtain from the fabricator these shrinkage factors. (plane against plane, plane against signal, signal against signal)

• The amount of shrinkage depends on copper thickness and area of copper remaining in each layer after etching.

• For ½ ounce copper I use: plane against plane- .2 mils, plane against signal- .4 mils, signal against signal- .5 mils (for ½ ounce copper)
CHECKING FINAL STACKUP

• After PCBs are fabricated, it is essential to have a method for verifying that they comply with all of the requirements.

• Among the requirements that must be verified are:
  – Layers are in correct order
  – Copper is the correct thickness
  – Laminates are the correct thickness
  – Impedance goals have been met.

• A common method for doing some of the above is a test coupon designed by the fabricator.

• Some problems with test coupons:
  – No guarantee that impedance test traces match main PCB
  – No way to check layer order
  – Often unavailable when investigation into problems occur.

• Alternative to test coupons- build test structures into PCB
STACING STRIPE SET WITH TEST TRACES

Note: Impedance test trace vias need to be 30 mils diameter with 0.1" separation. Velocity test trace should be 12" long.

STACKING STRIPE AND IMPEDANCE TEST TRACE DESCRIPTION

Note: Locate stacking strips on a side of the PCB that allows viewing without cutting away part of the PCB.
COMMENTS ON STACKING STRIPES

• Occasionally there is an objection to copper protruding at the edge of a PCB.

• This can be a problem if this copper is connected to internal circuits. Properly designed stacking stripes are not connected to internal circuits, so this problem is avoided.

• Some fabricators claim that this copper dulls router bits. Those same fabricators route and drill through copper everywhere else in their operations without complaint.

• In satellite applications, this “floating” copper is not allowed for static reasons. Connect the stripes to the ground planes to solve this problem.

• There isn’t any downside to adding stacking stripes other than a little extra CAD time.
SAMPLE STACKING STRIPES

6 LAYER STACKUP DONE CORRECTLY

24 LAYER STACKUP DONE INCORRECTLY
Note: When designing differential pairs using the “not closer than” spacing rule, it is not necessary to measure differential impedance. Single ended test traces are all that are necessary.
SUMMARY

• PCB Stackup design is an integral part of the signal integrity engineering process.

• PCB stackup design is far too complex to be left in the hands of the fabricator. It is not that fabricators are not capable of designing stackups, their skill set does not cover all the areas that are important.

• PCB stackup design is a joint effort between SI engineers and fabricators. Neither can do it alone.

• PCB stackup design requires detailed knowledge of the materials used to fabricate PCBs as well as the fabrication process itself.

• PCB Stackup design is not a difficult process given good materials data and design tools.
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