Designing a Multilayer PCB Stackup to Balance Signal Integrity Against Manufacturability and Reliability

PRESENTED TO IEEE EMC GROUP

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THE CHANGING WORLD OF PCB FABRICATION

- **At the outset of PCB fabrication PCBs were:**
  - **Single sided**
  - **Single layer**
  - **Had no vias**
  - **Dealt with clock speeds of 100 KHz**
  - **Had components with no more than four leads**
- **As technology has advanced speeds have increased to the present where PCBs:**
  - **Can have as many as 50 layers**
  - **Can have components on both sides**
  - **Have data paths as high as 28 Gb/S**
  - **Have components with as many as 2400 leads**
  - **May have both buried and blind vias as well as through hole**

PCB PARAMETERS OF CONCERN

- **At the outset of PCB fabrication, the concerns were:**
  - Accurate etching of 20 mil (.51 mm) wide traces
  - Drilling unplated holes 40 mils in diameter
  - Insuring traces and pads adhered to PCB during soldering
- **PCB fabrication concerns of today are:**
  - Accurate etching of traces as narrow as 3 mils (76 microns)
  - Drilling holes as small as 8 mils (.254 mm) and plating them
  - Aligning as many as 50 layers to each other
  - Maintaining impedance accuracy
  - Minimizing path loss
  - Creating interplane capacitance
  - Minimizing signal degradation from irregular glass weaves
  - Minimizing cross talk

OBJECTIVES

- Review how stackups are usually done.
- Discuss deficiencies in this method.
- Outline the increased demands on PCB stackups created by faster, denser electronics.
- Examine possible ways to construct a multilayer PCB.
- Examine materials choices.
- Discuss impedance and how to calculate it.
- Examine methods for determining that the final PCB has the correct cross section and impedance.
- Look at some typical stackups and the documentation needed to insure they are correctly fabricated.

WHAT IS STACKUP DESIGN?

Stackup design is the arranging of the signal and power layers of a PCB to meet the electrical and mechanical performance needs of a specific design.

Historically, the primary electrical requirements have been a controlled impedance in the signal layers and enough copper in the plane layers to deliver DC power to the circuits mounted on the PCB.

The primary mechanical requirements have been mechanical stability and ability to withstand soldering and rework.

TRADITIONAL DESIGN APPROACH

- In most cases, PCB stackup design has traditionally been done by each PCB fabricator to exploit the materials and processes it has in place.
- Because of this, a given design may have as many stackups as there are fabricators manufacturing it.
- Initially, the primary concerns were manufacturability and reliability, followed closely by cost.
- As IC speeds increased, the need for controlled impedance was added.
- Most design engineers did not know how to design for a specific impedance.
- As a result, PCB fabricators had to acquire the ability to calculate impedance in order to achieve correct impedance.

DEFICIENCIES WITH TRADITIONAL DESIGN APPROACH

- Impedance calculation is an electrical engineering problem.
- The strengths of PCB fabricators are:
  - Plating
  - Lamination
  - Etching
  - Drilling
- Electrical engineering is not part of that skill set.
- Even so, many fabricators have learned to calculate impedance. (The skill level at each fabricator varies widely.)
- Times have changed and impedance is only one of the electrical requirements that are important in a stackup.
- Crosstalk and interplane capacitance are two other parameters that have been added to the stackup requirements.

REQUIREMENTS FOR A HIGH PERFORMANCE PCB

- Provide enough signal layers to allow successful routing of all signals to signal integrity rules.
- Provide enough power and ground layers to meet needs of the PDS (Power Delivery System).
- Trace widths, spacing and dielectric thickness that meet both impedance and cross talk goals.
- Spacing between power and ground planes that results in adequate plane capacitance while complying with breakdown voltage rules.
- Use of materials that are readily available and comply with assembly requirements.

MULTILAYER PCB MATERIALS

- The three main components that make up a multilayer PCB are:
  - Copper foils
  - Cured laminate with copper foil on both sides
  - Uncured glass/resin sheets called prepreg that will serve as the "glue" during lamination.
- Copper foils are available in many thicknesses. The three main thicknesses are ½ ounce, 1 ounce and 2 ounce with ½ ounce being the dominant thickness. (1 ounce copper is 1.4 mils thick or 36 microns.)
- Laminates and prepreg come as sets from each material supplier. Both are known by their thicknesses and the styles of glass weave used in their makeup. For a given material type such as FR408 there is a wide selection of laminates coupled with a much smaller selection of prepreg styles. Laminates can have any combination of foil thicknesses on each side, but the most commonly have the same thickness copper on both sides.

A TYPICAL LAMINATE DATA SHEET

Core Thickness	Standard Constructions	Resin Content	Dk at 100 MHz	Dk at 500 MHz	Dk at 1 GHz	Dk at 2.0 GHz	Dk at 5.0 GHz	Dk at 10.0 GHz
0.0020	1-106	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0027	1-1080	60	3.52	3.51	3.51	3.51	3.47	3.47
0.0030	1-1080	63	3.45	3.45	3.44	3.44	3.40	3.40
0.0035	2-106	66	3.39	3.38	3.38	3.37	3.33	3.33
0.0035	1-2113	51	3.74	3.74	3.73	3.73	3.70	3.70
0.0040	2-106	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0040	1-3070	49	3.80	3.79	3.79	3.78	3.75	3.75
0.0040	1 - 3313	55	3.64	3.64	3.63	3.63	3.59	3.59
0.0043	106/1080	62	3.48	3.47	3.47	3.46	3.42	3.42
0.0045	106/1080	63	3.45	3.45	3.44	3.44	3.40	3.40
0.0050	2-1080	57	3.59	3.59	3.58	3.58	3.54	3.54
0.0050	106/2113	55	3.64	3.64	3.63	3.63	3.59	3.59
0.0050	1-1652	43	3.96	3.95	3.93	3.94	3.92	3.92
0.0055	1-1652	47	3.85	3.84	3.84	3.84	3.81	3.81
0.0060	1080/2113	54	3.67	3.66	3.66	3.65	3.62	3.62
0.0060	106/ 1080	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0065	1080/2113	57	3.59	3.59	3.58	3.58	3.54	3.54
0.0070	1080/2116	58	3.57	3.56	3.56	3.55	3.52	3.52
0.0070	2-2113	52	3.72	3.72	3.71	3.70	3.67	3.67
0.0075	2 - 3313	52	3.72	3.72	3.71	3.70	3.67	3.67
0.0080	2-3070	49	3.80	3.79	3.79	3.78	3.75	3.75
0.0100	2-1652	43	3.96	3.95	3.93	3.94	3.92	3.92
0.0100	3-1080	66	3.39	3.38	3.38	3.37	3.33	3.33
0.0100	2-2116	54	3.67	3.66	3.66	3.65	3.62	3.62
0.0120	2-2113/ 1652	48	3.82	3.82	3.81	3.81	3.78	3.78
0.0140	2-2116/1652	47	3.85	3.84	3.84	3.84	3.81	3.81
0.0160	3-1652	46	3.88	3.87	3.87	3.86	3.83	3.83
0.0180	2-3070/2-1652	46	3.88	3.87	3.87	3.86	3.83	3.83
0.0210	2-2116/2-1652	50	3.77	3.76	3.76	3.76	3.72	3.72

Courtesy of Isola Corporation. This table is for Isola IS620i low loss laminate.

A TYPICAL PREPREG DATA SHEET

Prepreg	Resin Content	Thickness (in)	Dk at 100 MHz	Dk at 500 MHz	Dk at 1 GHz	Dk at 2.0 GHz	Dk at 5.0 GHz	Dk at 10.0 GHz
106	75	0.0025	3.20	3.19	3.19	3.18	3.14	3.14
1080	65	0.0033	3.41	3.40	3.40	3.39	3.35	3.35
2113	58	0.0042	3.57	3.56	3.56	3.55	3.52	3.52
3313	54	0.0036	3.67	3.66	3.66	3.65	3.62	3.62
3070	55	0.0046	3.64	3.64	3.63	3.63	3.59	3.59
2116	55	0.0052	3.64	3.64	3.63	3.63	3.59	3.59
1652	51	0.0061	3.74	3.74	3.73	3.73	3.70	3.70

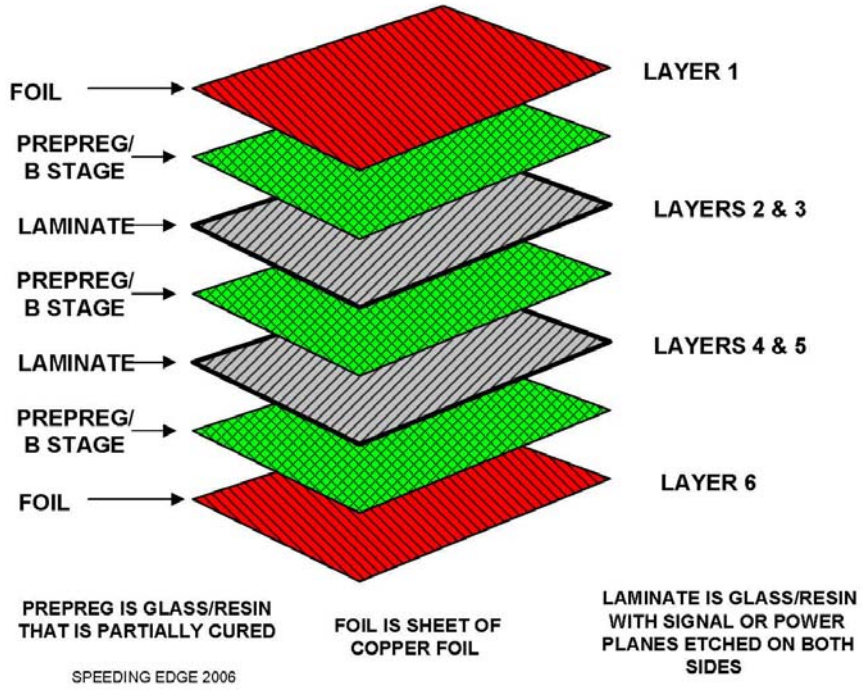
Prepreg	Resin Content	Thickness (in)	Df at 100 MHz	Df at 500 MHz	Df at 1 GHz	Df at 2.0 GHz	Df at 5.0 GHz	Df at 10.0 GHz
106	75	0.0025	0.0046	0.0050	0.0056	0.0058	0.0066	0.0073
1080	65	0.0033	0.0049	0.0052	0.0057	0.0059	0.0066	0.0072
2113	58	0.0042	0.0051	0.0054	0.0058	0.0060	0.0066	0.0071
3313	54	0.0036	0.0052	0.0055	0.0059	0.0060	0.0066	0.0071
3070	55	0.0046	0.0051	0.0055	0.0059	0.0060	0.0066	0.0071
2116	55	0.0052	0.0051	0.0055	0.0059	0.0060	0.0066	0.0071
1652	51	0.0061	0.0053	0.0055	0.0059	0.0060	0.0066	0.0070

Courtesy of Isola Corporation. This table is for Isola IS620i low loss prepreg.

MULTILAYER FABRICATION PROCESS

1. Create inner layers details by etching signal and plane layers on adjacent pairs of copper foils on a piece of laminate.
2. Stack inner layers with alternating layers of prepreg.
3. Add foil to outside of stack.
4. Press/laminate stack.
5. Process laminated stack through the outer layer processing steps (drilling, plating, etching and masking).
6. Route PCB from process panel.
7. Test finished PCB to net list.

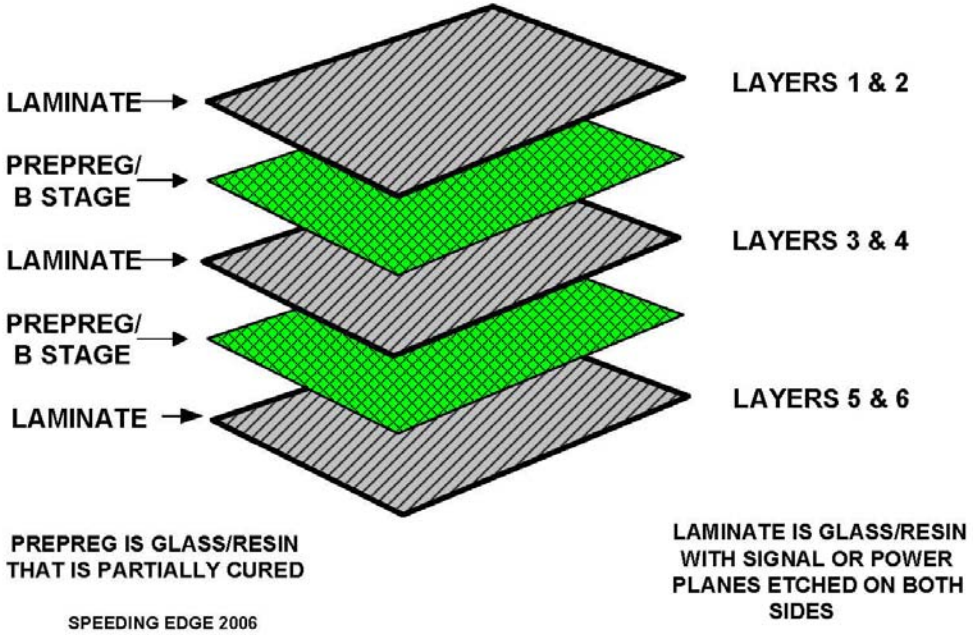
HOW MOST MULTILAYER PCBS ARE BUILD



STACK UP FOR 6 LAYER PCB AS IT ENTERS LAMINATION (FOIL LAMINATION)

Foil lamination is the most common method for creating a multilayer PCB.

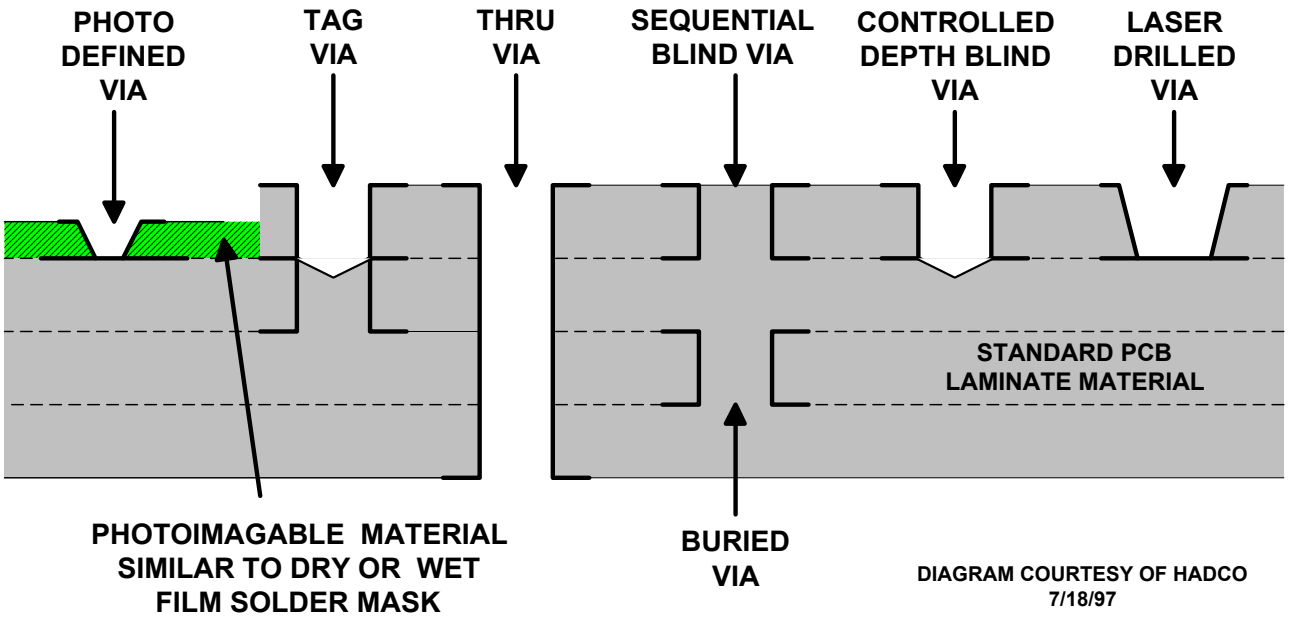
ALTERNATE PCB FABRICATION METHOD



STACK UP FOR 6 LAYER PCB AS IT ENTERS LAMINATION (CAP LAMINATION)

Cap lamination is the original method for creating a multilayer PCB. It is more expensive that foil lamination. When materials such as Rogers RO4350 are used between L1 and L2 this method is required.

BURIED AND BLIND VIA FABRICATION



The use of blind and buried vias is often called buildup or HDI construction. It is clearly more expensive than either foil or cap lamination when the same number of layers are involved and is used only when through hole technology is not possible.

CHOOSING A FABRICATOR AS A DESIGN PARTNER

- As can be seen from previous slides, PCB stackup design is a combination of manufacturing engineering and electrical engineering.
- Successful stackup design required close cooperation between electrical engineers and fabrication engineers.
- Therefore, it is advisable for the design engineer to seek out a fabricator whose capabilities are in line with the complexity of the PCB being designed. (This means that the traditional method of allowing purchasing to select fabricators on a price basis will no longer work.)
- Once this alliance is established, the design engineer needs to propose a stackup that meets the electrical requirements and have it reviewed by the fabricator for feasibility.

TYPES OF SIGNAL LAYERS

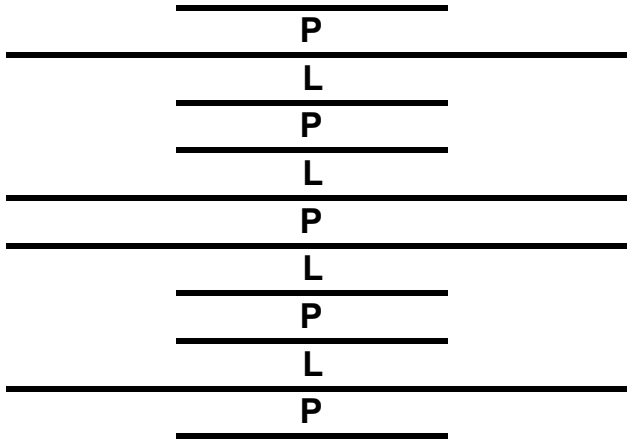
			TRACE WIDTH (mils)	IMPEDANCE (ohms)
L1	OUTER "CAP" LAYER			
L2	SIGNAL 1	7.0	5.0	50.0
L3	GROUND 1	5.0		
L4	Vdd 1	3.0		
L5	SIGNAL 2	5.0	5.0	50.0
L6	SIGNAL 3	7.0	5.0	50.0
L7	Vdd 2	5.0		
L8	GROUND 2	3.0		
L9	SIGNAL 4	5.0	5.0	50.0
L10	OUTER "CAP" LAYER	7.0		

LAMINATE

PREPREG

Signal layers on the outside of a PCB are called surface microstrip (L1 and L10 above). Signal layers embedded in the dielectric with a plane on only one side are buried microstrip (l2 and L9 above). Signal layers between two planes are stripline layers (L5 and L6). These can be centered between the planes or offset as shown above.

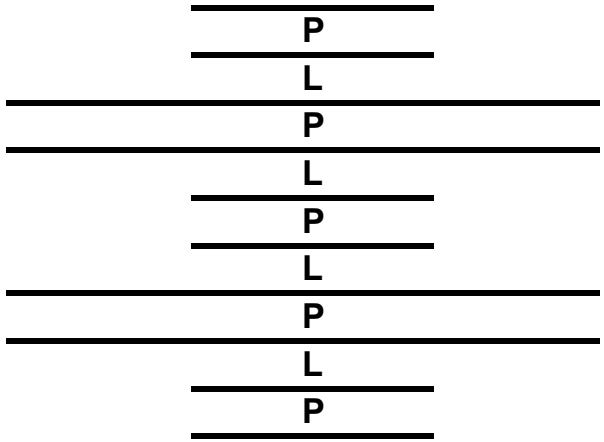
ALTERNATE WAYS TO STACK LAYERS



OPTION 1

6 SIGNAL LAYERS, ONLY ONE PLANE PAIR

GOOD FOR ROUTING SIGNALS
POOR FOR POWER DISTRIBUTION



OPTION 2

4 SIGNAL LAYERS, TWO PLANE PAIRS (L1 AND L10 ARE NOT USEFUL SIGNAL LAYERS.)

FAIR FOR ROUTING SIGNALS,
GOOD FOR POWER DISTRIBUTION.

P = Prepreg L = Laminate
Long bars are plane layers and short bars are signal layers.

SELECTING AN IMPEDANCE

- Common transmission line impedances for PCBs are:
- 28-33 ohms as specified for Rambus®
- 50 ohms as used with ECL and other fast logic
- 62-65 ohms as used with the PCI bus
- 72-75 ohms as used with video signals.
- 100 ohm differential- just two 50 ohm lines in a PCB

MULTIPLE IMPEDANCES IN A SINGLE PCB

- It is very difficult to design a PCB stackup for more than one impedance.
- One example is a PCB with a PCI bus and ECL or GTL.
- ECL and GTL require 50 ohms. PCI is usually specified at 62 or 65 ohms.
- Trying to put two different trace widths in the same layer is difficult and sometimes, impossible.
- Designing a stackup with signal layers of different impedances is possible.
- Getting the wiring space correct for each impedance is difficult resulting in some signal layers that are poorly used, others crowded.

IS IT POSSIBLE TO MAKE ALL IMPEDANCES THE SAME?

- Making all of the transmission line impedances the same greatly reduces stackup complexity.
- Making all the transmission line impedances the same greatly reduces design complexity.
- Is it possible to make all impedances the same?
- If so, what impedance?
- 50 ohms is the most common impedance for cables, testers and PCBs.
- Let’s see if it is possible to make all signals 50 ohms.

CAN ALL TECHNOLOGIES WORK WITH 50 OHM TRANSMISSION LINES?

- All currently available logic technologies are capable of operating with 50 ohm transmission lines.
- What about the PCI bus? This bus works fine with 50 ohm impedance transmission lines. (See reference 1.)
- What about 100 ohm differential pairs? Diff pairs are really just two 50 ohm lines. (See reference 2.)
- What about 72 ohm video interfaces? These normally connect to cables that exit the PCB. Placing the driver or receiver close to the connector, so the length of mismatched 50 ohm trace is very short solves this problem without requiring a 72 ohm trace on the PCB. (Simulation will verify this.)
- Yes, one impedance will work and the best values is 50 ohms.

SELECTING LAMINATES

- Laminate systems are commonly made using “E” glass for the woven reinforcement.
- Laminate systems are know by their resin systems.
- There are a wide range of resin systems to choose from.
- Some of these resin systems are listed on the next slide.
- Each resin system was formulated to meet a particular application.
- The merits of many of them are discussed in Chapter 5 of reference 21.

POTENTIAL LAMINATE SYSTEMS

- Epoxy based systems (sometimes called FR4)
- Polyimide
- PPO- Polyphenylene Oxide
- PPE- Polyphenylene Ester
- BT- Bismalamine Triazine.
- CE- Cyanate Ester
- Phenolic cured epoxy
- Cyanate Ester modified epoxy
- Filled Phenolic cured epoxy

PROPERTIES OF SOME COMMON PCB LAMINATES

Material	T_g	e_r*	Tan(f)**	DBV(V/Mil)	WA %
Standard Epoxy Glass (FR-4)	125C	4.1	0.02	1100	0.04
Multifunctional EG (FR-4)	145C	4.1	0.022	1050	0.14
Tetrafunctional EG (FR_4)	150C	4.1	0.022	1050	0.13
Nelco N4000-6 Hi Tg FR-4	170C	4.0	0.012	1300	0.10
Getek (Megtron 4)	180C	4.1	0.011	1100	0.12
BT Epoxy Glass	185C	4.1	0.023	1350	0.20
Nelco 4000-13SI	210	3.3	0.009	1400	0.09
Cyanate Ester	245C	4.0	0.01	800	0.70
Rogers RO4350	280C	3.5	0.004	780	0.04
Polyamide Glass	285C	4.1	0.015	1200	0.43
Teflon Glass	N/A	2.2	0.002	450	0.01

* Measured at 2 GHz with a resin content of 55%.

** This is loss tangent, an expression of how much signal is lost in the dielectric.

Tg = Glass Transition Temperature

DBV= Dielectric breakdown voltage.

WA = Water Absorption, more than 0.25% results in PCBs that fail leakage tests.

All materials reinforced with woven glass.

Notice that a 5 mil thickness of any glass reinforced material has a dielectric breakdown voltage approaching or exceeding 5000 volts.

CONSIDERATIONS WHEN SELECTING A LAMINATE SYSTEM

- Lead free assembly
- Halogen free materials
- Ability to withstand high temperatures
- Need for low dielectric loss
- Sensitivity to single source materials
- Need to prototype one place and produce another
- Cost and price

OBTAINING LAMINATE INFORMATION

- First choice for laminate information is the laminate manufacturer.
- Second choice is fabricators.
- The amount of information held by fabricators varies from virtually none to very complete data sets.
- Type of information needed is:
  - dielectric constant vs. frequency for each laminate and prepreg
  - Dielectric loss vs. frequency for each laminate and prepreg
  - Types of glass cloth used in each laminate and prepreg
  - Copper foil roughness needed for good adhesion.

Some laminate supplier web sites:

www.isola-group.com

www.parknelco.com

www.rogerscorp.com

HOW THIN SHOULD LAMINATE AND PREPREG BE?

- As can be seen on slides 8 and 9, laminate and prepreg is available in thicknesses as thin as 2 mils (51 microns).
- Some specialty materials are available as thin as 1 mil (25 microns) and 0.5 mil (13 microns).
- The principal consideration when selecting thin laminates and prepregs is the breakdown voltage requirement of the design.
- For most products intended for the Telco market this is 1500 volts.
- Most commercially available laminates have breakdown voltages around 1000 volts per mil of thickness (25 microns). This would make it unwise to use materials thinner than 2 mils.

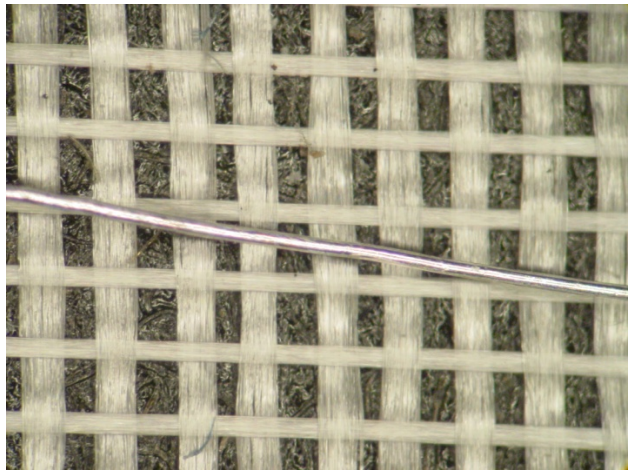
EFFECTS OF GLASS WEAVE ON FAST DIFFERENTIAL SIGNALS

- If the distribution of glass in the dielectric is not uniform it can result in variations in impedance and velocity along the length of a trace.
- When differential signals travel over loose weave glass, one member of the pair may be faster than the other resulting in skew and data errors.
- Variations in impedance along a trace can result in unwanted reflections that degrade the signal amplitude.
- This effect can be pronounced on signals of 2.4 Gb/S an higher.

GLASS STYLES OR WEAVES

- The glass used as reinforcement in PCB materials is available as random glass and woven glass.
- Random glass has not proved to be sufficiently stable for use in precision PCBs.
- Woven glass is the reinforcement of choice for nearly all PCBs. (There are woven non-glass cloths available at high price premiums.)
- Woven glass is available in a wide variety of styles. The next slide shows some of them. The "standard construction" columns on slides 8 and 9 show many of them. Page 109 of reference 4 shows more examples.)
- Certain glass weaves can have undesirable effects on very high speed signals. (References 5, 7, 9 & 10)

SOME REPRESENTATIVE GLASS STYLES



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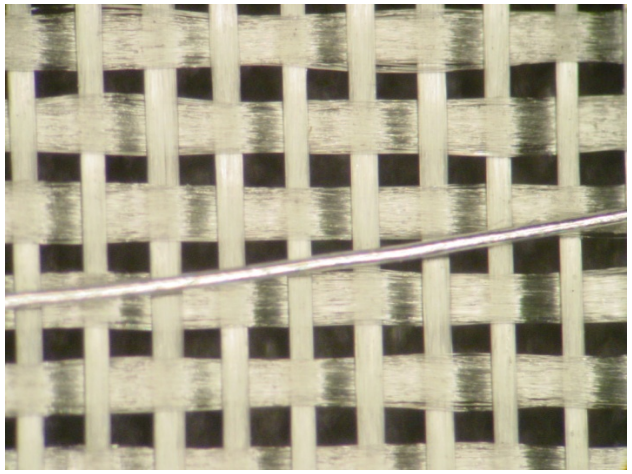
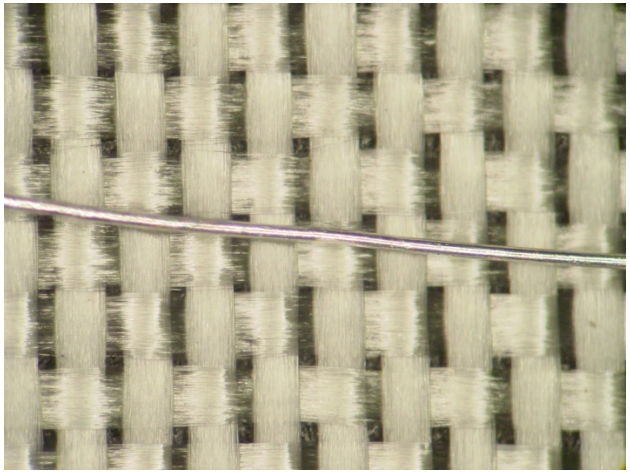
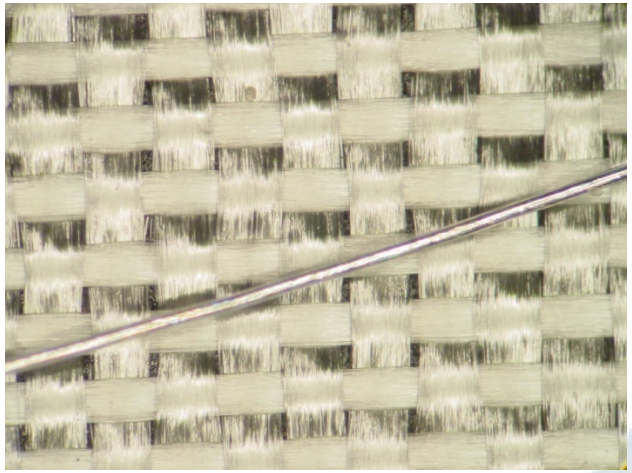


1080

WIRE IS 3.5 MILS IN DIAMETER



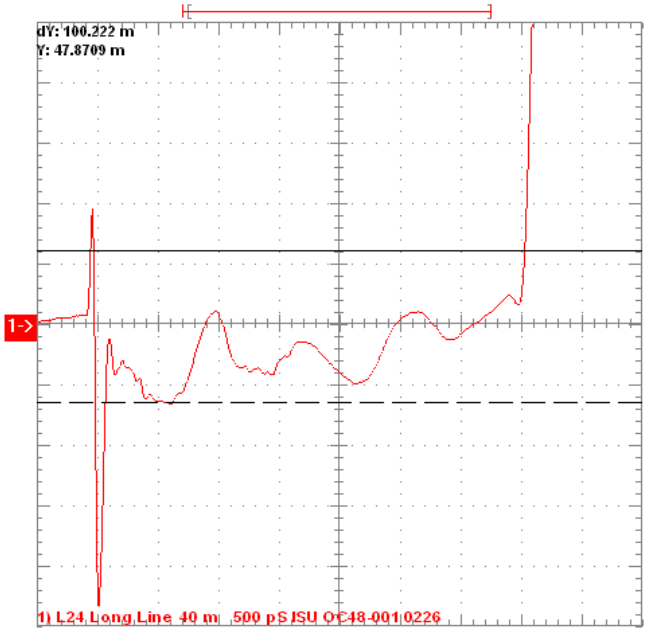
2113



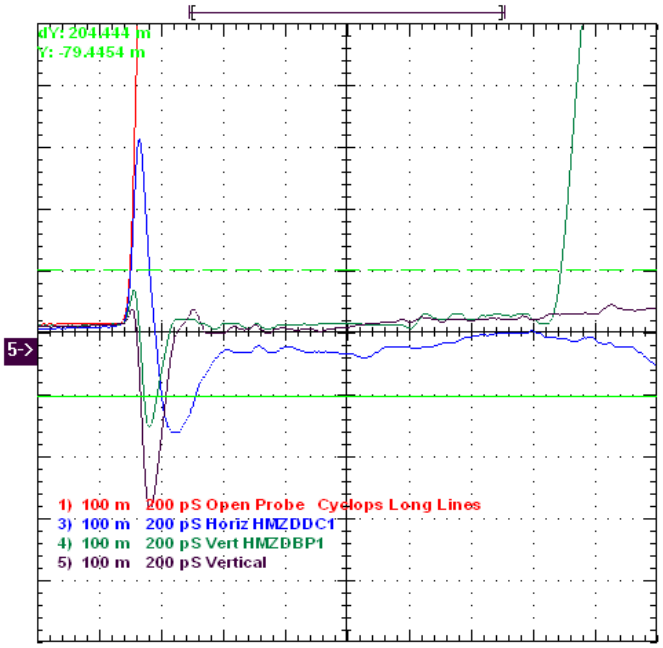
3313

GLASS STYLE CAN ADVERSELY AFFECT IMPEDANCE UNIFORMITY

IMPEDANCE VARIATION OVER 1080 GLASS



IMPEDANCE VARATION OVER 3313 GLASS



Impedance variation is due to variation of dielectric constant. This also causes velocity to vary, resulting in differential skew in differential pairs.

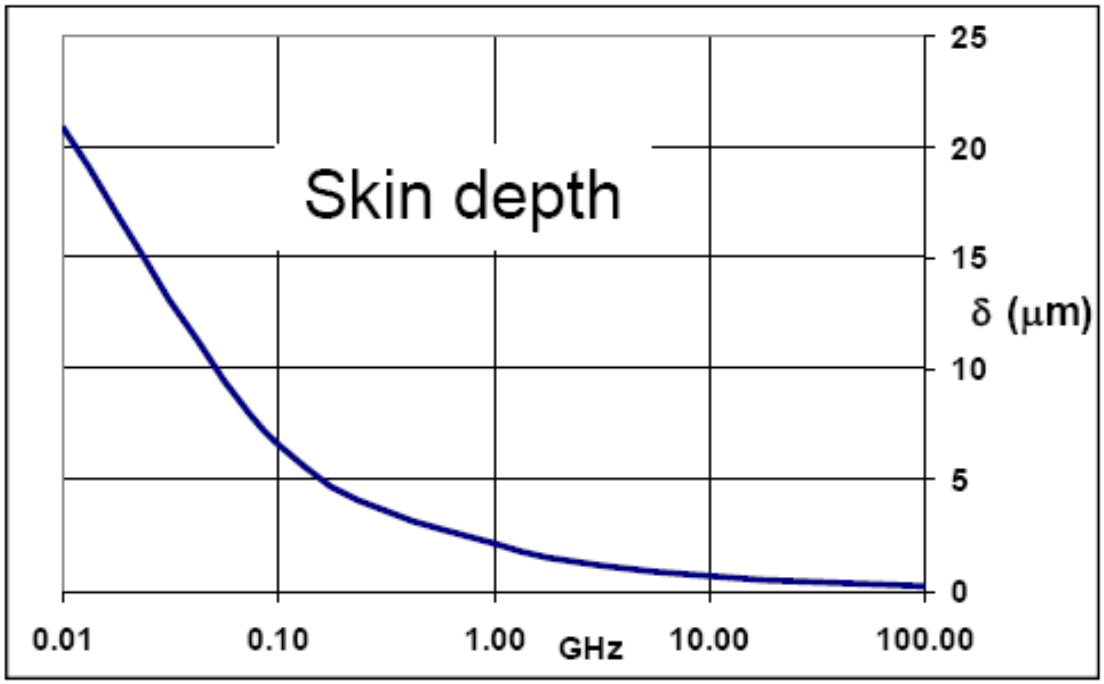
SELECTING THE PROPER COPPER FOIL THICKNESS

- Copper foils are available in a variety of thicknesses. They are rated in ounces. One ounce copper is 1.4 mils (36 microns) thick. ½ ounce 0.7 mils (18 microns) etc.
- Thicker copper is more difficult to etch and process. Thinner copper has less conductivity.
- Thickness may differ between signal and power layers.
- For etching reasons, it is desirable to use the same thickness copper on both sides of a piece of laminate.
- If one side of a piece of laminate is a signal layer and the other a power plane, which should dominate?

SIGNAL LAYER THICKNESS

- Nearly all signal layers in modern designs have signals fast enough that skin effect loss and skin depth determine how thick the signal traces need to be.
- " Skin effect " is the behavior of current flow in conductors at high frequencies where the current flows near the surface of a conductor rather than all the way through it. (See reference 12.)
- When frequencies are high enough that the current is penetrating less than half the thickness of the conductor, making that conductor any thicker is of no value.
- For etching uniformity it is useful to make signal layers as thin as possible. (1/2 ounce being a good compromise).

SKIN DEPTH VS. FREQUENCY

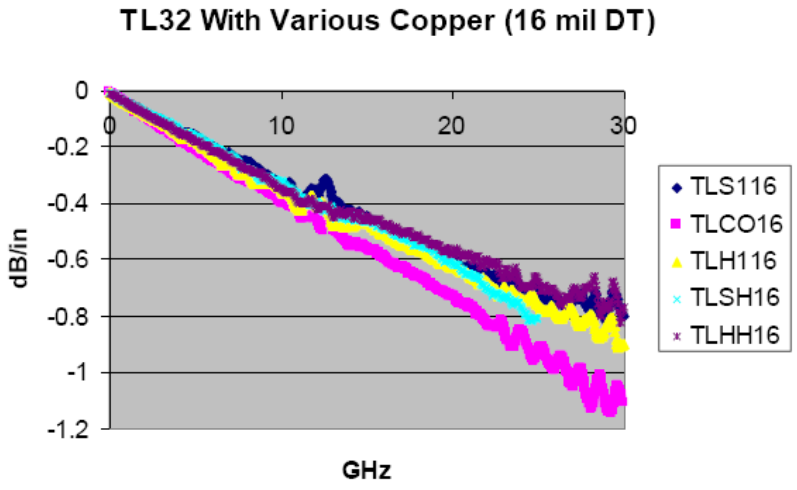


Notice that at 1 GHz, skin depth is 2 microns or 80 micro inches. Trace layers thicker than ½ ounce copper do not help above this frequency.

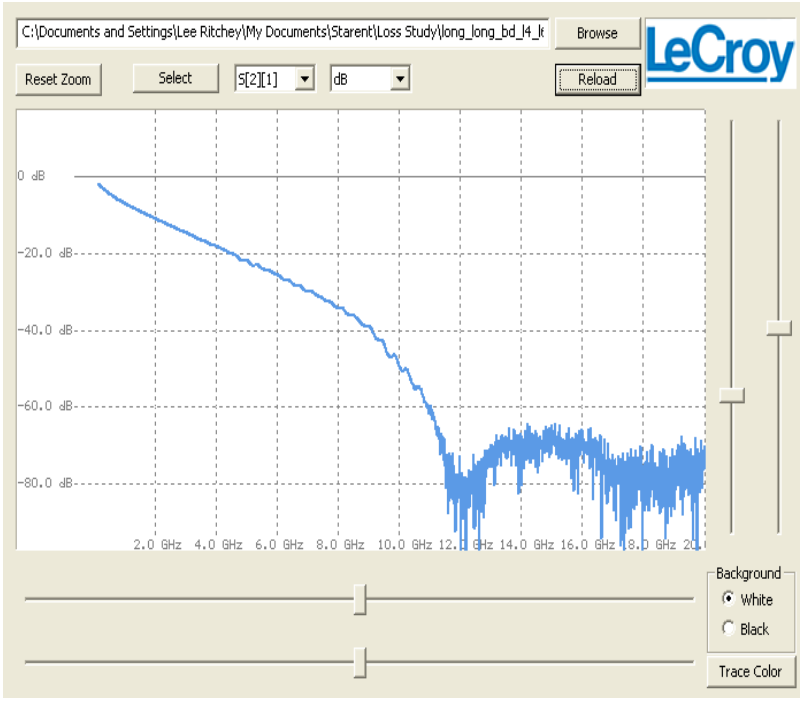
Therefore, ½ ounce signal layers are ” good enough ” for high speed signals.

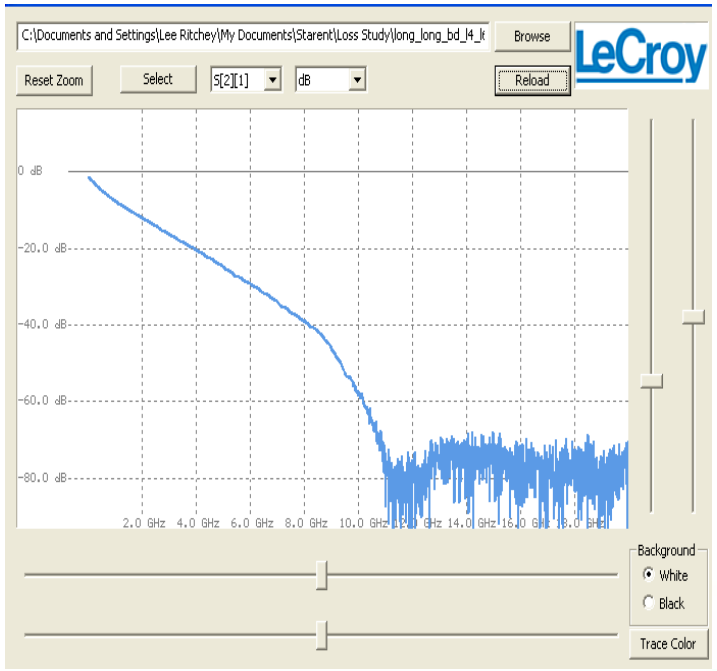
COPPER SURFACE ROUGHNESS

- There has been much concern over the roughness of the copper surface and its effect on loss at high frequencies.
- The graph below depicts loss due to roughness from smooth copper to the roughest used in lamination.
- At 5 GHz (10Gb/S) loss varies 0.1 db per inch from roughest to smoothest. It is desirable to use smooth copper finish.



LOSS VARIATION DUE TO SURFACE ROUGHNESS DIFFERENCE BETWEEN FABRICATORS





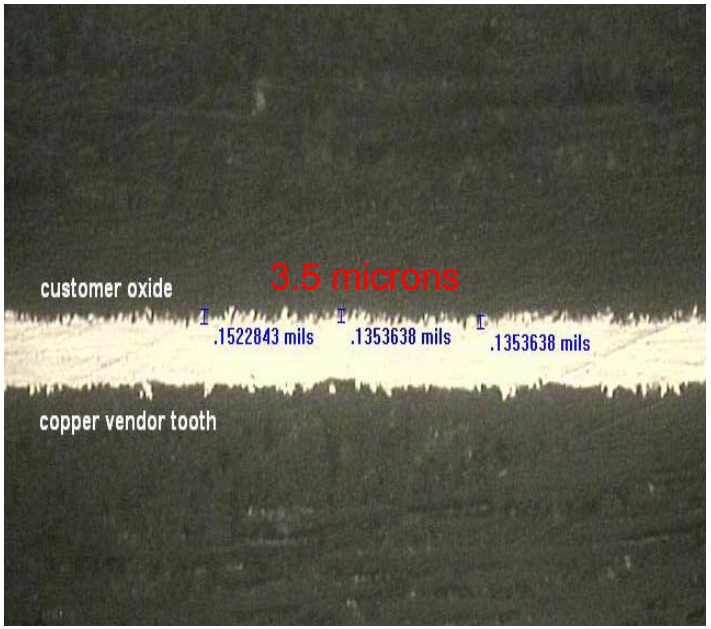
Two PCBs built at two different fabricators using the same materials and the same stackup yield different losses due to differing surface roughness done during processing. Copper roughness has been left to each fabricator. With the advent of 10 Gb/S and higher signal paths, this is no longer allowable. Test structure is 7 ” Daughterboard made from FR408HR, 13 ” backplane made from Megtron 6 and 7” daughter board made from FR408HR. Only daughter boards were changed.

INSURING UNIFORM LOSS FROM LOT TO LOT

- The two PCBs in the previous slide were build from the same artwork and material by two different fabricators.
- They differ only in the roughness of the copper as finished by each fabricator.
- Copper roughness, by fabricator, varies substantially. Why?
- Until recently, the only driving force for copper roughness has been to insure delamination does not occur.
- Fabricators with prior experience with delamination tend to be aggressive with their roughening step.
- In order to insure uniform loss from this operation it is necessary to call out copper roughness maximums on fabrication drawings.

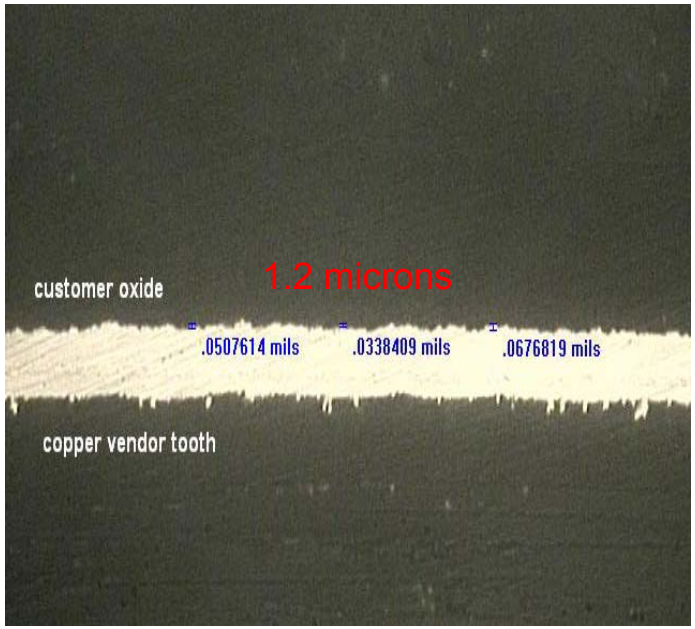
CROSS SECTION OF TWO PCBS ON PREVIOUS SLIDE

Supplier # 1 Oxide



Poor Loss

Supplier # 2 Oxide



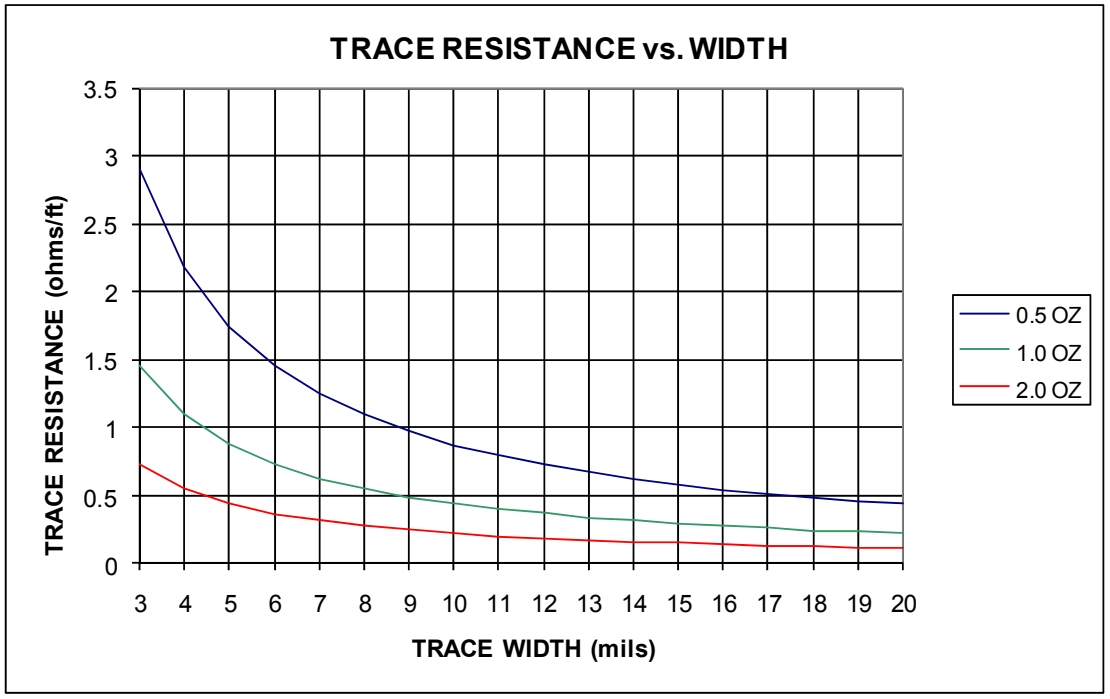
Good Loss

PROBLEMS WITH ROUGHNESS SPECIFICATIONS

- At the present time, there are no standards for specifying copper roughness.
- There are several designators such as low profile, but each copper supplier uses the term differently.
- It appears there is no activity underway to develop a reliable roughness standard.
- At present, the only reliable way to control copper roughness is to determine the minimum copper roughness required to assure delamination does not occur and put this requirement on the fabrication drawing.
- The proper place to obtain the copper roughness spec. is the laminate manufacturer.

BASIC COPPER CONDUCTIVITY

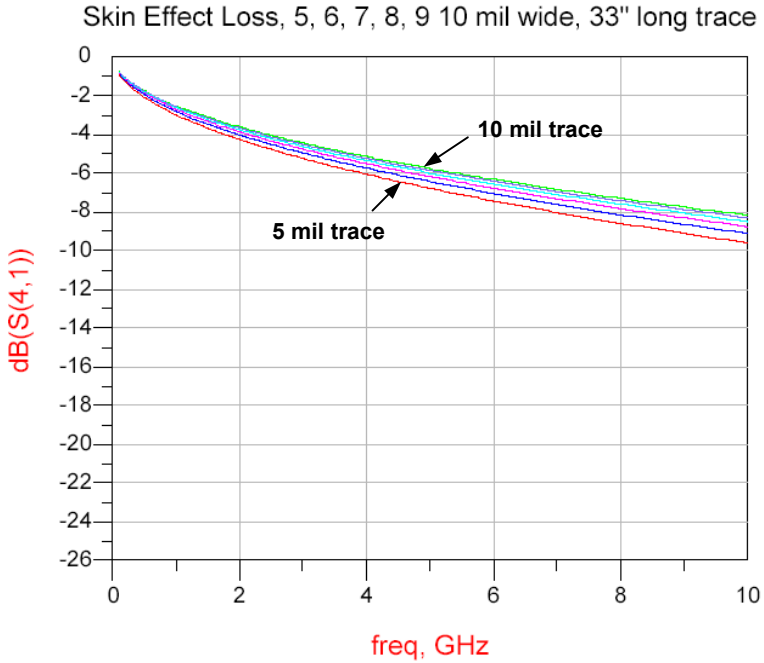
- **The chart below illustrates DC resistivity of copper traces by foil thickness and trace width.**
- **This data is useful for calculating trace width for DC signals.**

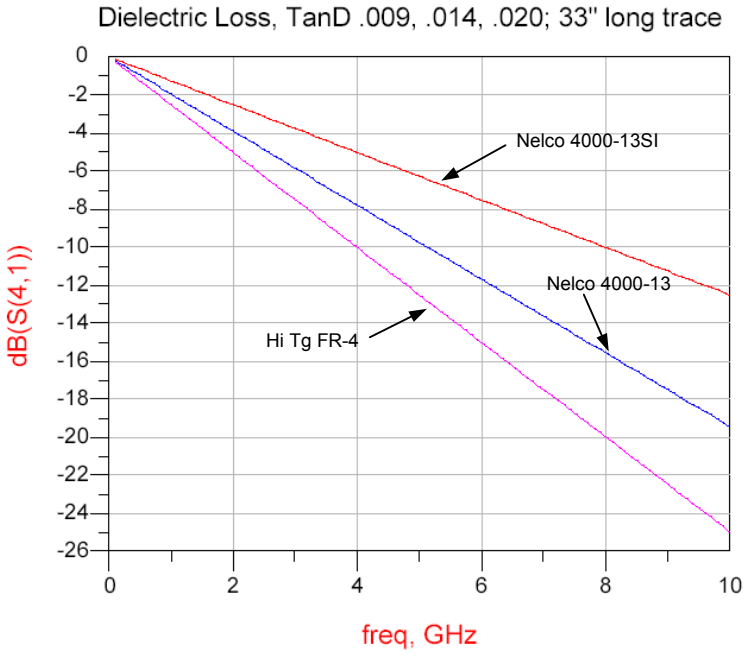


TRADING OFF TRACE WIDTH VS. OVERALL PCB THICKNESS

- Skin effect loss in traces is primarily a function of frequency and outer surface layer area of the trace.
- To minimize skin effect loss it is tempting to select the widest trace that will fit between pins of components.
- In order to maintain a 50 ohm impedance the height above the nearest plane must be increased, making the overall PCB thick. This also increases overall cost.
- Traces farther away from planes also have higher crosstalk.
- Making traces wide reduce skin effect loss, but has undesirable side effects. (higher crosstalk, thicker PCBs, more cost)

AN EXAMPLE OF SKIN EFFECT AND DIELECTRIC LOSS IN A SIGNAL PATH





Dielectric loss dominates the loss problem for current technologies. Changing dielectric is much better than using wider traces.

TRACE WIDTH CONCLUSIONS

- From the previous slide, varying trace width from 5 mils (127 microns) to 10 mils (254 microns) reduces skin effect loss at 2.5 GHz (5 Gb/S) approximately 1 db for 33” (84 cm) long trace.
- Changing trace width from 5 mils to 10 mils results in a PCB that is often twice as thick. (This makes cost go up and plating more difficult.)
- Changing from a lossy dielectric to a less lossy dielectric has a much bigger impact on overall loss.
- To minimize overall loss and maximize manufactur-ability, it is wise to use lower loss laminate and minimize trace width. (My standard trace width is 5 mils (127 microns, even at 10 Gb/S).

DECIDING WHETHER TO A USE “LOW LOSS” LAMINATE SYSTEM

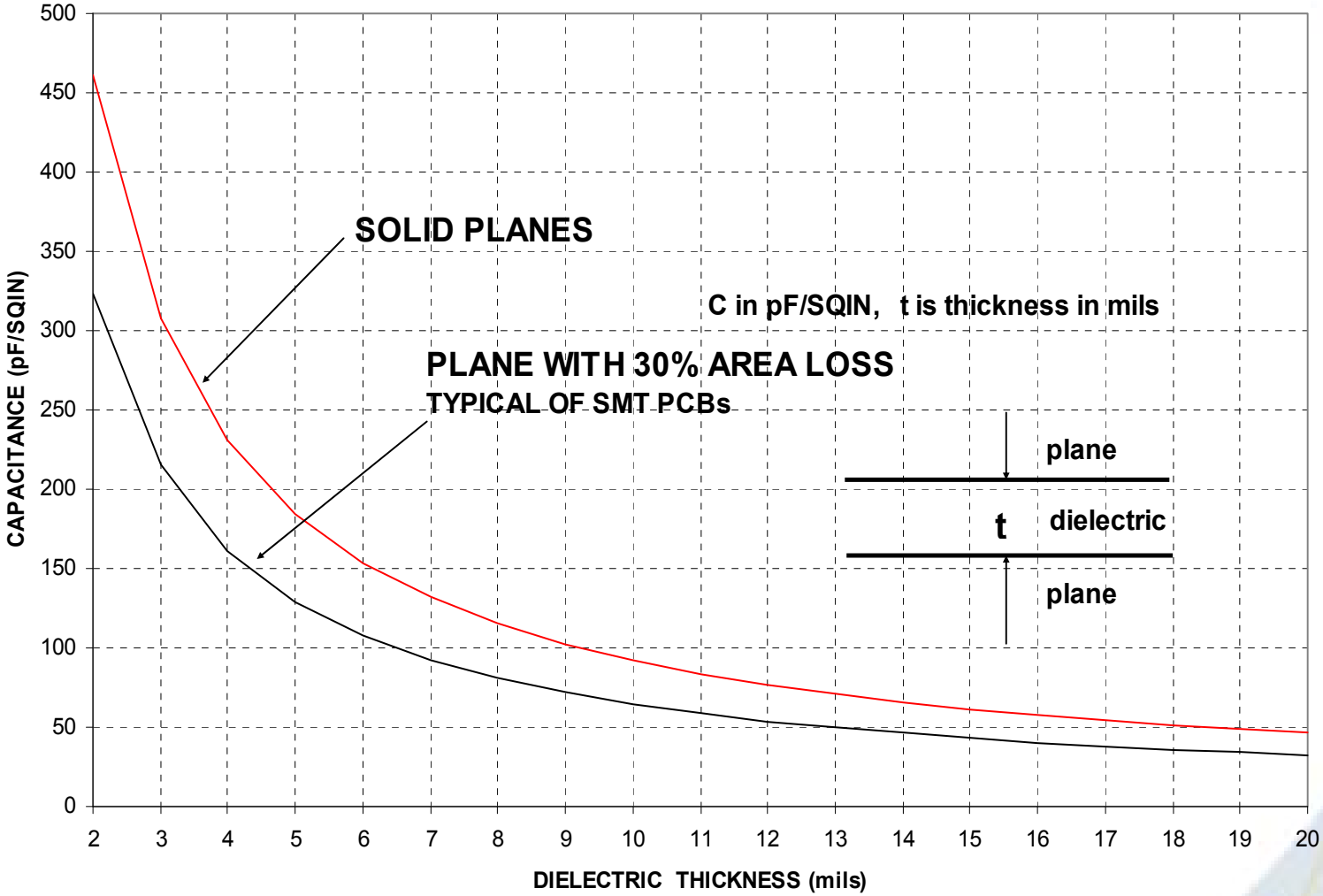
- In this context low loss means low dielectric loss.
- Dielectric loss in a path is a function of path length and operating frequency.
- In order to determine whether a low loss laminate is needed for a particular application it is necessary to employ an analytical tool to model the proposed path.
- As always, the results of any analysis should be verified by constructing a test circuit to validate them.
- From experience designing many “ high speed ” PCBs, I have found that most products do not need low loss laminates.

SELECTING PLANE COPPER THICKNESS

- When pairing plane layers with signal layers across a piece of laminate, it is wise to use the same copper thickness on both sides to insure etching is uniform on both sides.
- For impedance control reasons, it is desirable to mate every signal layer with a plane.
- From previous slides it was shown that ½ ounce in signal layers is the best choice.
- Is ½ ounce copper good enough for plane layers? Depends on the current flow and allowable voltage drop in the planes. (Chapter 33 in reference 3 discusses how to perform this analysis.)
- In most cases, ½ ounce planes are satisfactory.

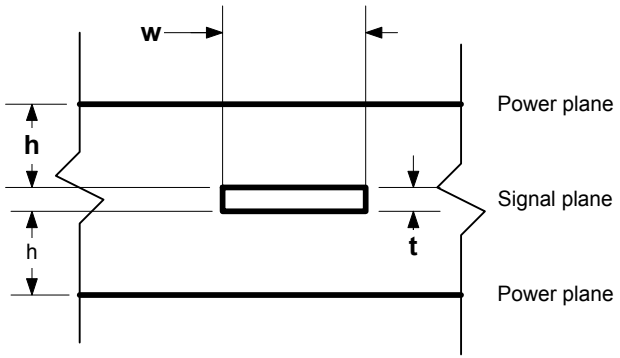
POWER PLANE CAPACITANCE

- A key component of any high performance PCB is the capacitance formed by adjacent power and ground layers.
- This high quality (low inductance) capacitance is necessary to support the very fast switching transients associated with driving single ended transmission lines and the rapidly changing IC core supply currents.
- The amount of plane capacitance needed is calculated as part of the PDS design.
- Once the amount of plane capacitance is known, the plane area and separation needed to achieve that capacitance can be designed into the stackup.
- In some cases it may be necessary to have more than one plane pair to support a given power supply voltage.

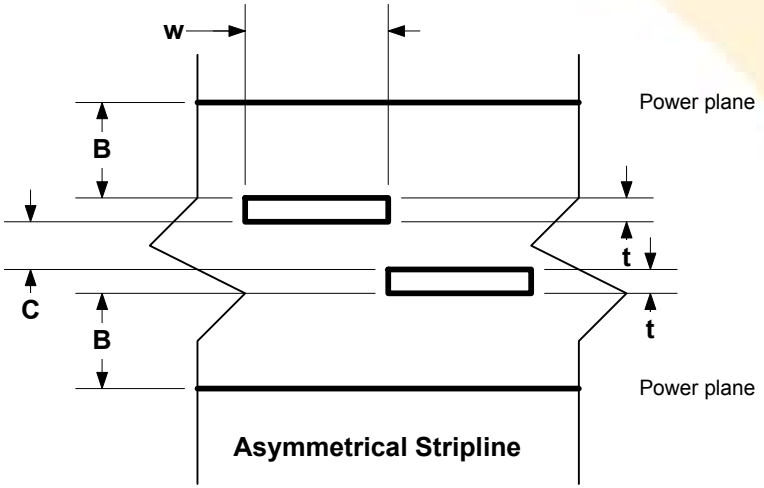

POWER PLANE CAPACITANCE vs. DIELECTRIC THICKNESS
DIELECTRIC CONSTANT = 4.1 (FR-4)
CAPACITANCE (pF/SQIN)
500
450
400
350
300
250
200
150
100
50
0
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
DIELECTRIC THICKNESS (mils)
SOLID PLANES
C in pF/SQIN, t is thickness in mils
PLANE WITH 30% AREA LOSS
TYPICAL OF SMT PCBs
plane
t
dielectric
plane

IMPEDANCE CALCULATING METHODS

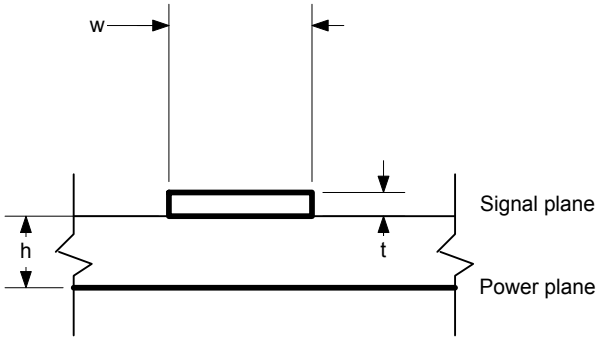
- There are two basic methods for calculating impedance. They are:
  - Equations
  - Field solvers
- All equations are partial solutions that are accurate over a narrow range of variables.
- Field solvers employ Maxwell's equations to precisely calculate impedance for any geometry and are more accurate than any of the equations.



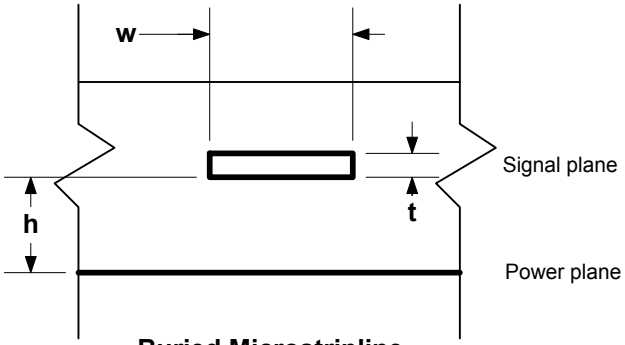
Symmetrical or Balanced Stripline



Asymmetrical Stripline



Surface Microstripline



Buried Microstripline

FOUR BASIC TYPES OF PCB TRANSMISSION LINES

NOTE: VARIABLES ABOVE CORRESPOND TO THOSE USED IN THE IMPEDANCE EQUATIONS IN THIS COURSE.

AN IMPEDANCE EQUATION FOR SURFACE MICROSTRIP

e_r = RELATIVE DIELECTRIC CONSTANT

H = HEIGHT OF TRACE ABOVE PLANE

W = TRACE WIDTH

T = TRACE THICKNESS

Z_O = TRACE IMPEDANCE IN OHMS

ANY DIMENSION SYSTEM IS APPLICABLE

NOTE: VALID FOR 5<w<15 MILS

A more precise calculation can be obtained using a 2D field solver which the author recommends.

$$Z_0 = \frac{79}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98\,H}{0.8W + T}\right)$$

e_r value is that obtained from velocity measurements made with a TDR.

BURIED MICROSTRIP IMPEDANCE EQUATION

Z_O = TRANSMISSION LINE IMPEDANCE (OHMS)

H = HEIGHT OF LINE ABOVE POWER PLANE

W = TRACE WIDTH

T = TRACE THICKNESS

e_r = RELATIVE DIELECTRIC CONSTANT

A more precise calculation can be obtained using a 2D field solver which the author recommends.

Valid for 5 < W < 15 mils, valid for any dimension system

Assumes at least 5 mils of dielectric lying on top of trace.

$$Z_0 = \left(43.037 \ln \frac{H}{W}\right) + 5.048\left(\frac{T}{W}\right) + \frac{106.76}{1.09\sqrt{e_r}}$$

ASYMMETRIC STRIPLINE IMPEDANCE EQUATION

- Z_0 = TRANSMISSION LINE IMPEDANCE
- B = TRACE TO PLANE SPACING
- C = TRACE PLANE TO TRACE PLANE SPACING
- T = TRACE THICKNESS
- W = TRACE WIDTH
- e_r = relative dielectric constant of insulator
- FOR C = 0, equation applies to centered stripline
- Valid for 5 < W < 15 mils

A more precise calculation can be obtained using a 2D field solver which the author recommends.

$$Z_0 = 80\left[\frac{1-\frac{B}{4(B+C+T)}}{\sqrt{e_r}}\right]\ln\left[\frac{1.9(2B+T)}{(0.8W+T)}\right]$$

SOME 2D FIELD SOLVERS FOR IMPEDANCE CALCULATIONS

- Hyperlynx Linsym- Does whole cross section at once,
- Polar Instruments Si9000b- Can do whole cross section at once. Most used by fabrication shops.
- Cadence PCB SI- Does whole cross section at once.
- Applied Simulation Technologies RLGC.
- ADS by Agilent (also 3D)
- HFSS by Ansoft (Also 3D)

R, L, C TRANSMISSION LINE MODEL

O - R - L - R - L - R - L - R - L - O

I I I I

C C C C

I I I I

P P P P

O = END OF LINE

P = PLANE

C = CAPACITANCE PER UNIT LENGTH

R = RESISTANCE PER UNIT LENGTH

L = INDUCTANCE PER UNIT LENGTH

Model assumes a plane of negligible inductance and resistance.

The following equations permit one to calculate the reactance of capacitors and inductors as a function of frequency.

$$Xc = \frac{1}{2\Pi fC}$$

Xc = Capacitive Reactance

$$X_L = 2\Pi fL$$

X_L = Inductive Reactance

THE IMPEDANCE EQUATION

Z_O = CHARACTERISTIC IMPEDANCE OF LINE

L_O = INDUCTANCE PER UNIT LENGTH

C_O = CAPACITANCE PER UNIT LENGTH

R_0 = RESISANCE PER UNIT LENGTH

Go= TRANSCONDUCTANCE PER UNIT LENGTH

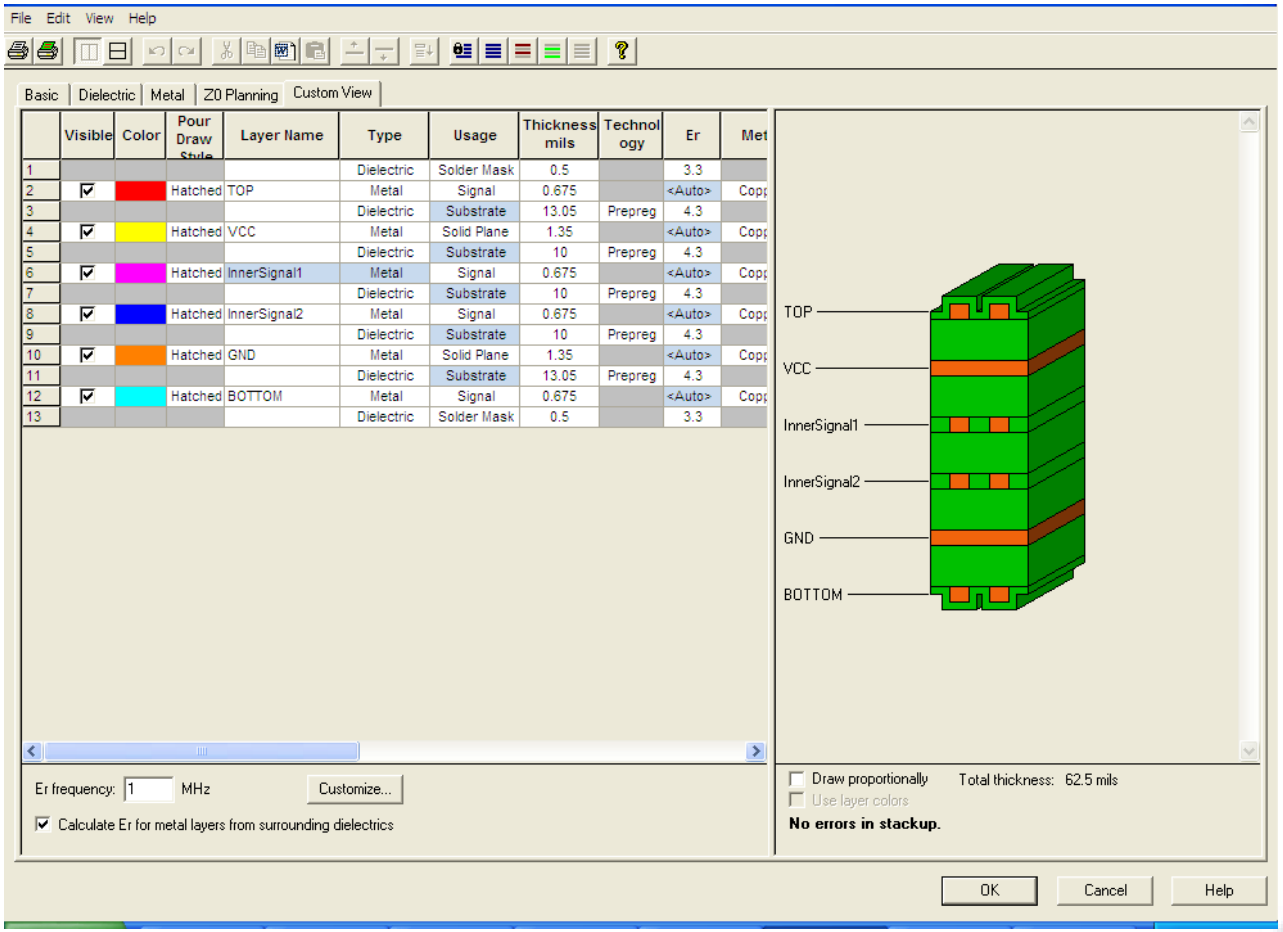
$$Z_O = \sqrt{\frac{R_O + j\omega L_O}{G_O + j\omega C_O}} \qquad Z_o = \sqrt{\frac{L_o}{C_o}}$$

Exact Equation Simplified Equation

As capacitance is added to a transmission line (example: periodic loads) the impedance goes down. Note that impedance is independent of length and frequency.

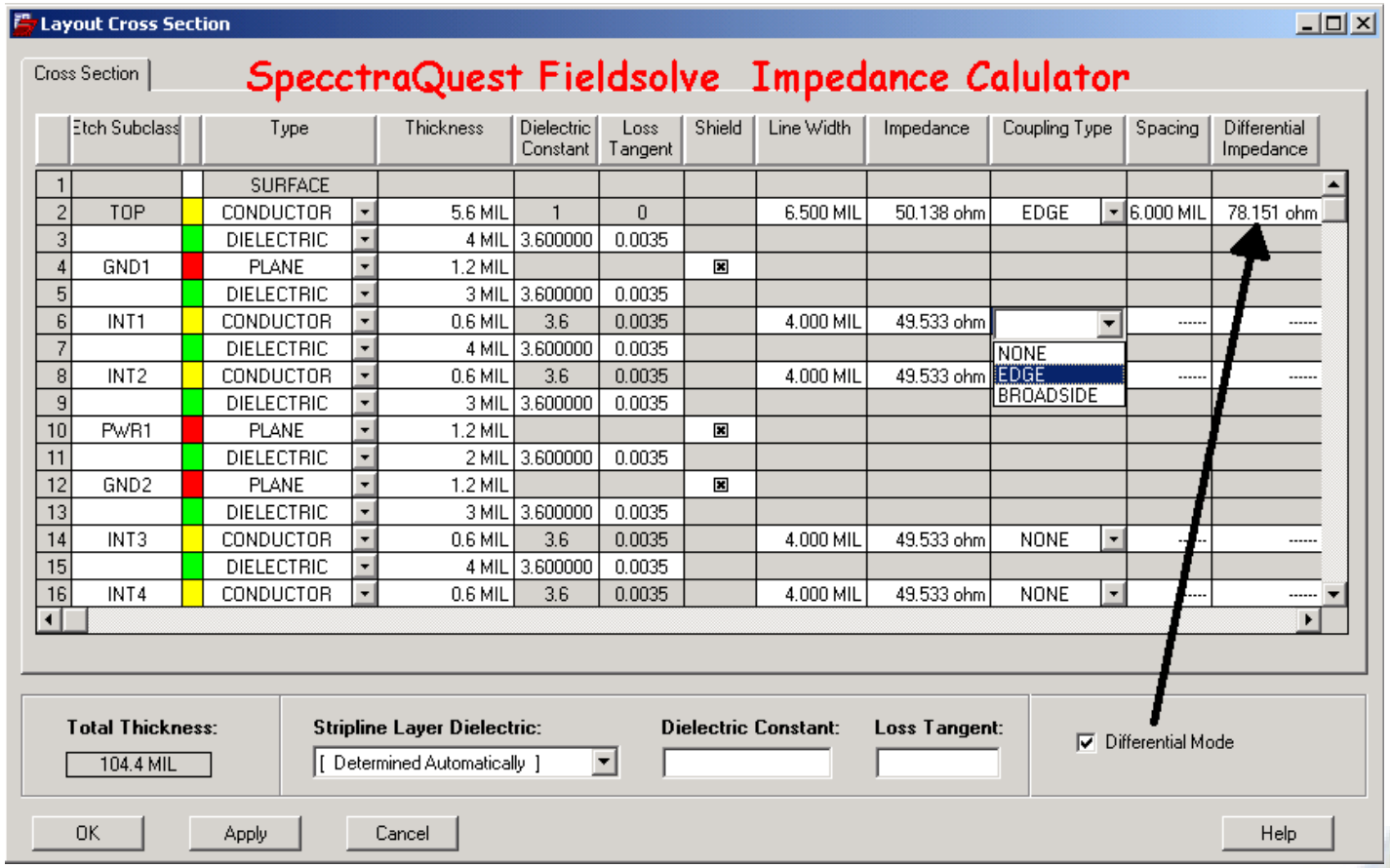
These equations are useful only when there is a ready means for determining values per unit length.

THE CONTROL SCREEN FOR THE HYPERLYNX 7.0 FIELD SOLVER

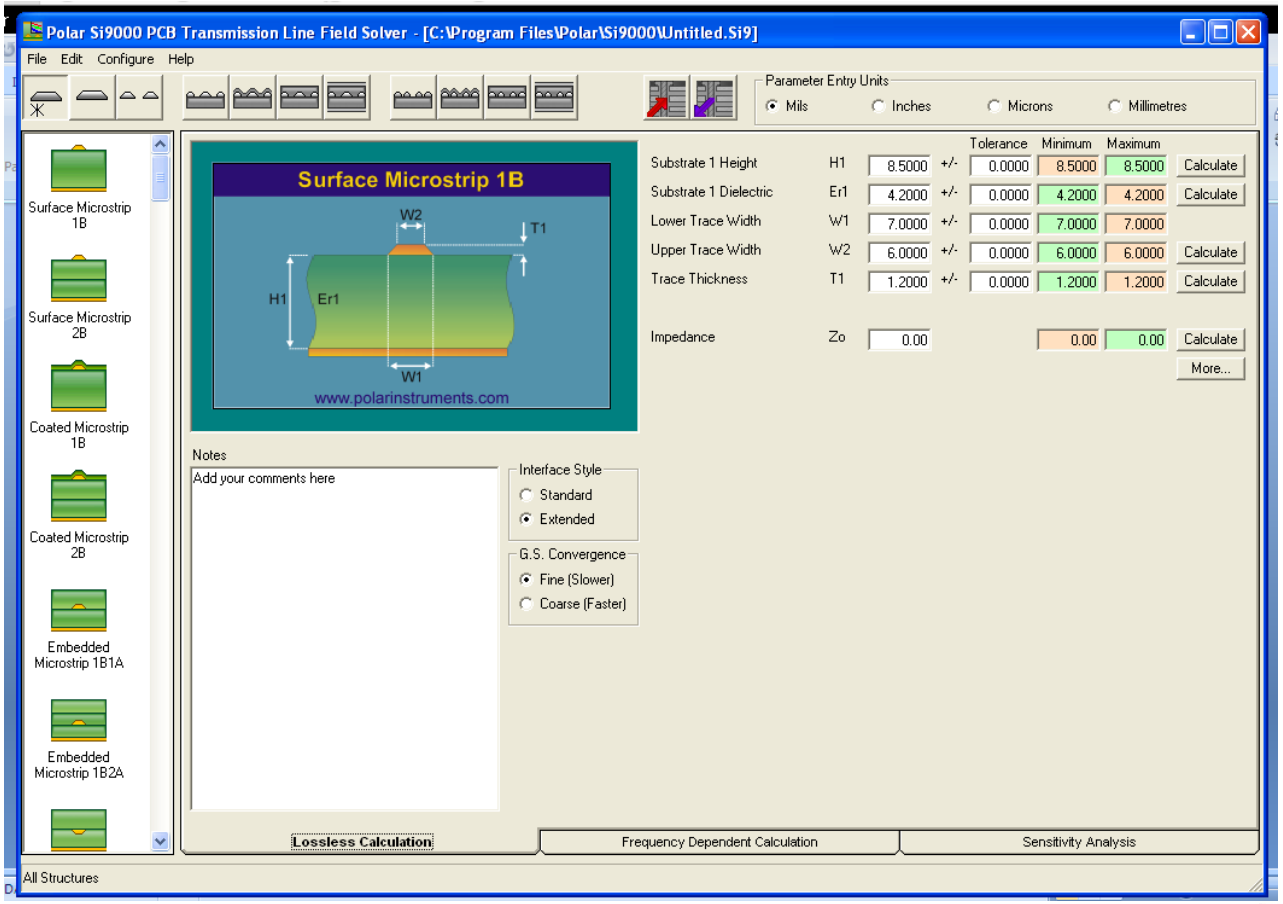


COURTESY OF HYPERLYNX

CADENCE PCB SI FIELD SOLVER



THE CONTROL SCREEN FOR THE POLAR INSTRUMENTS Si8000/SB200

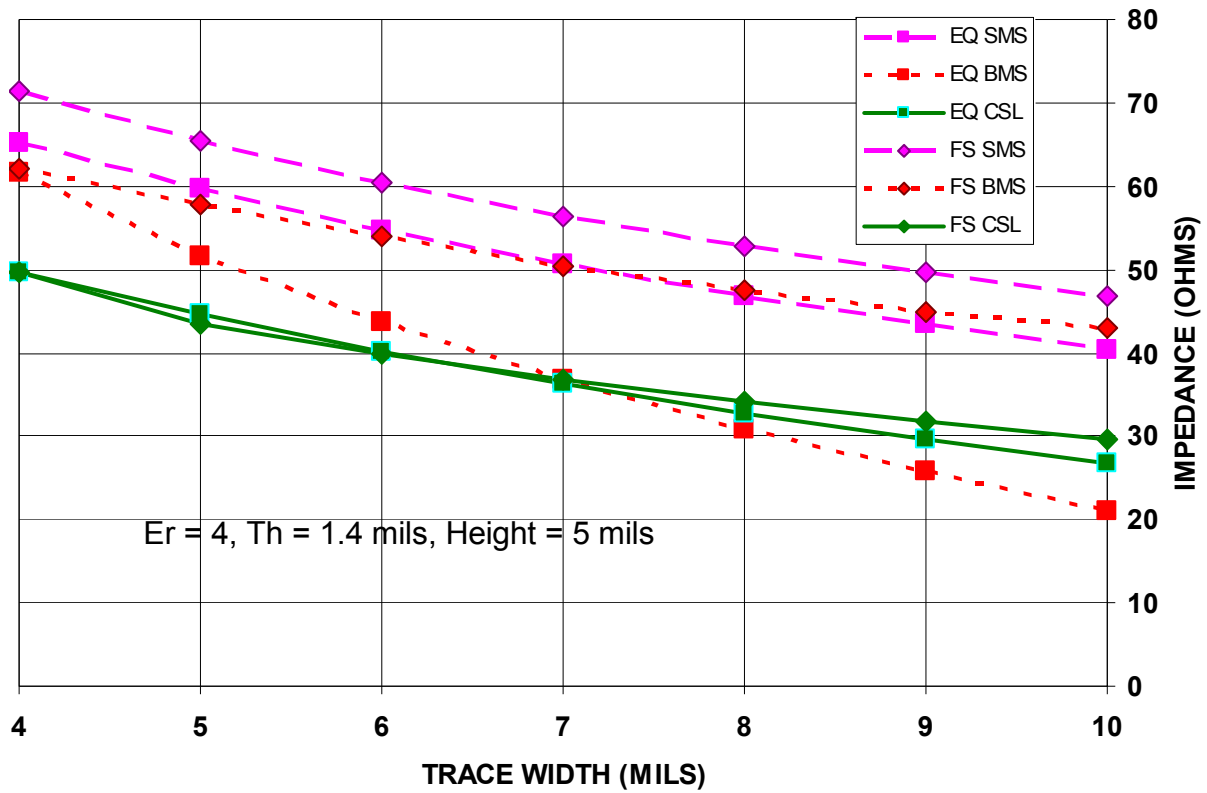


http://www.polarinstruments.com/help/sb200/lang/en/index.htm

POTENTIAL ERRORS IN IMPEDANCE CALCULATIONS

- There are several places errors can creep into impedance calculations. Among these are:
- Equation inaccuracy
- Incorrect dielectric constant for laminate
- Tool precision
- Bad assumptions by fabrication houses
- From experience, it has been demonstrated that field solvers are capable of calculating impedance to an accuracy of less than 1%.

COMPARING FIELD SOLVER RESULTS TO EQUATION RESULTS



SMS = Surface microstrip, EMS = embedded microstrip, CSL = centered stripline

WHAT IS RELATIVE DIELECTRIC CONSTANT, e_r?

- **Relative dielectric constant, e_r, is a measure of the affect an insulator has on the capacitance of a pair of conductors as compared to the same conductor pair in a vacuum.**

- **The dielectric constant of a vacuum is 1. All materials have dielectric constants higher than 1.**

- **A common method for measuring e_r is the parallel plate method at 1 MHz. *A more useful method for transmission line design is signal velocity in the dielectric.***

AN EQUATION FOR CALCULATING e_r USING VELOCITY MEASURED WITH A TDR

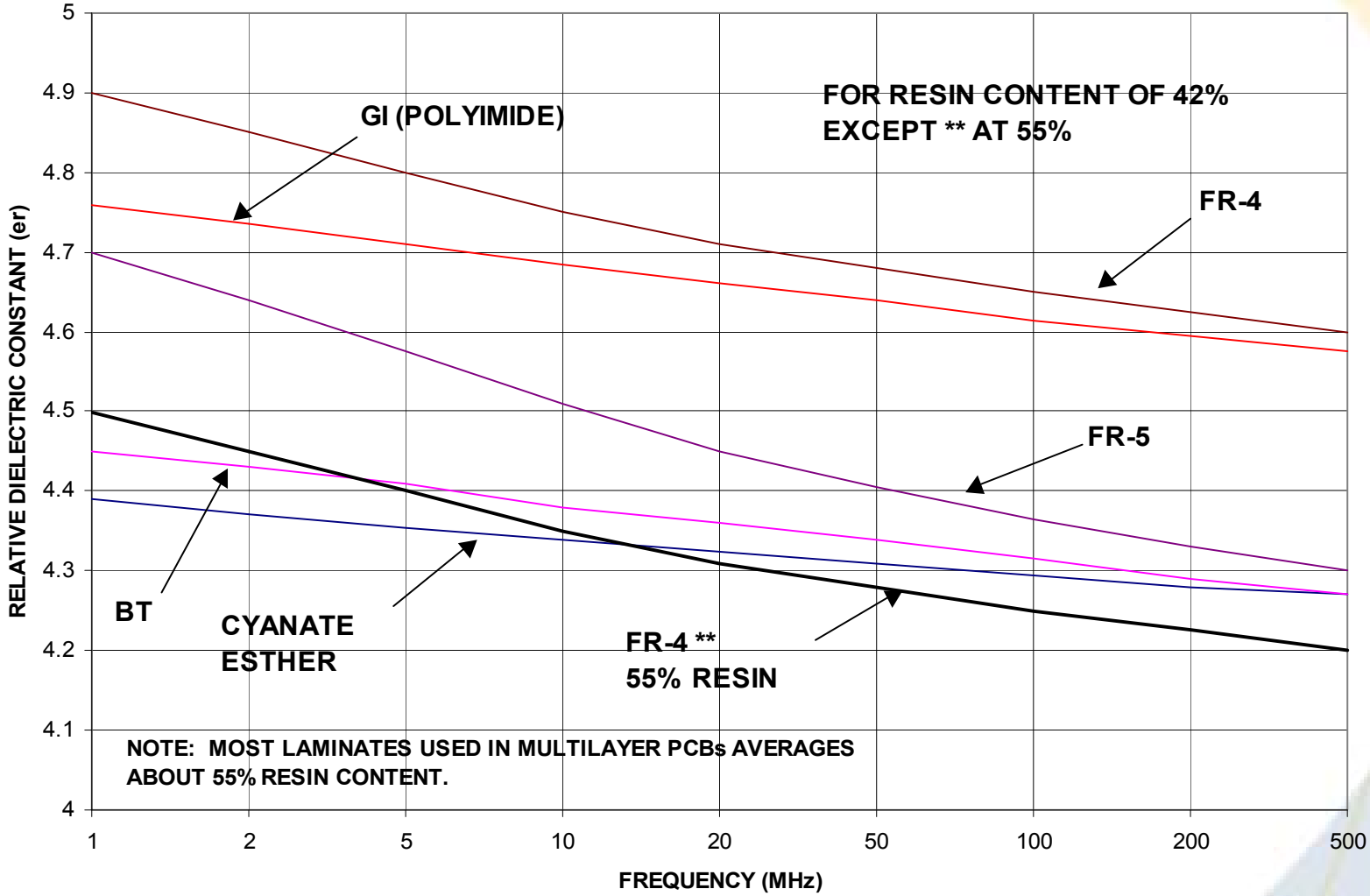
- C = SPEED OF LIGHT, .0118 INCH/pSEC
- V = MEASURED PROPAGATION VELOCITY

$$\sqrt{e_r} = \frac{C}{V}$$

NOTE: All dielectrics slow electromagnetic waves down according to the above formula.

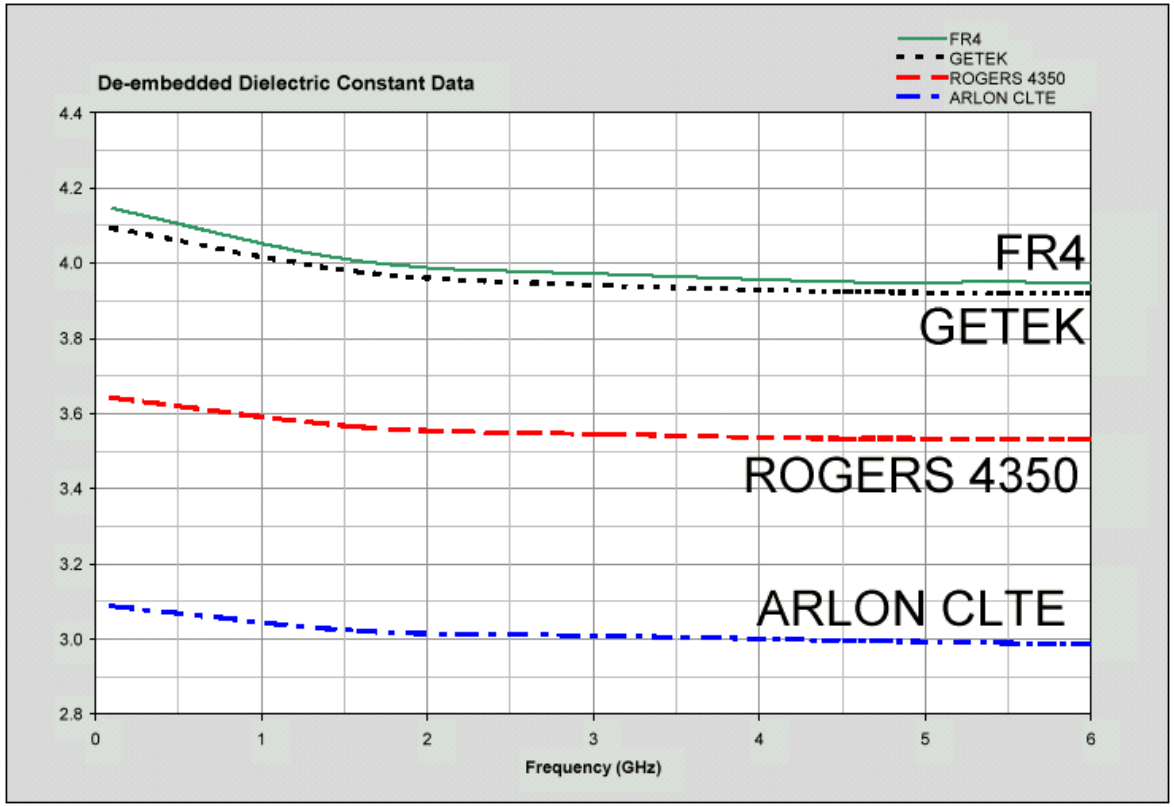
Note: As will be seen later, e_r varies with frequency in most PCB materials.

RELATIVE DIELECTRIC CONSTANT vs. FREQUENCY
FOR VARIOUS LAMINATES



Materials Comparison

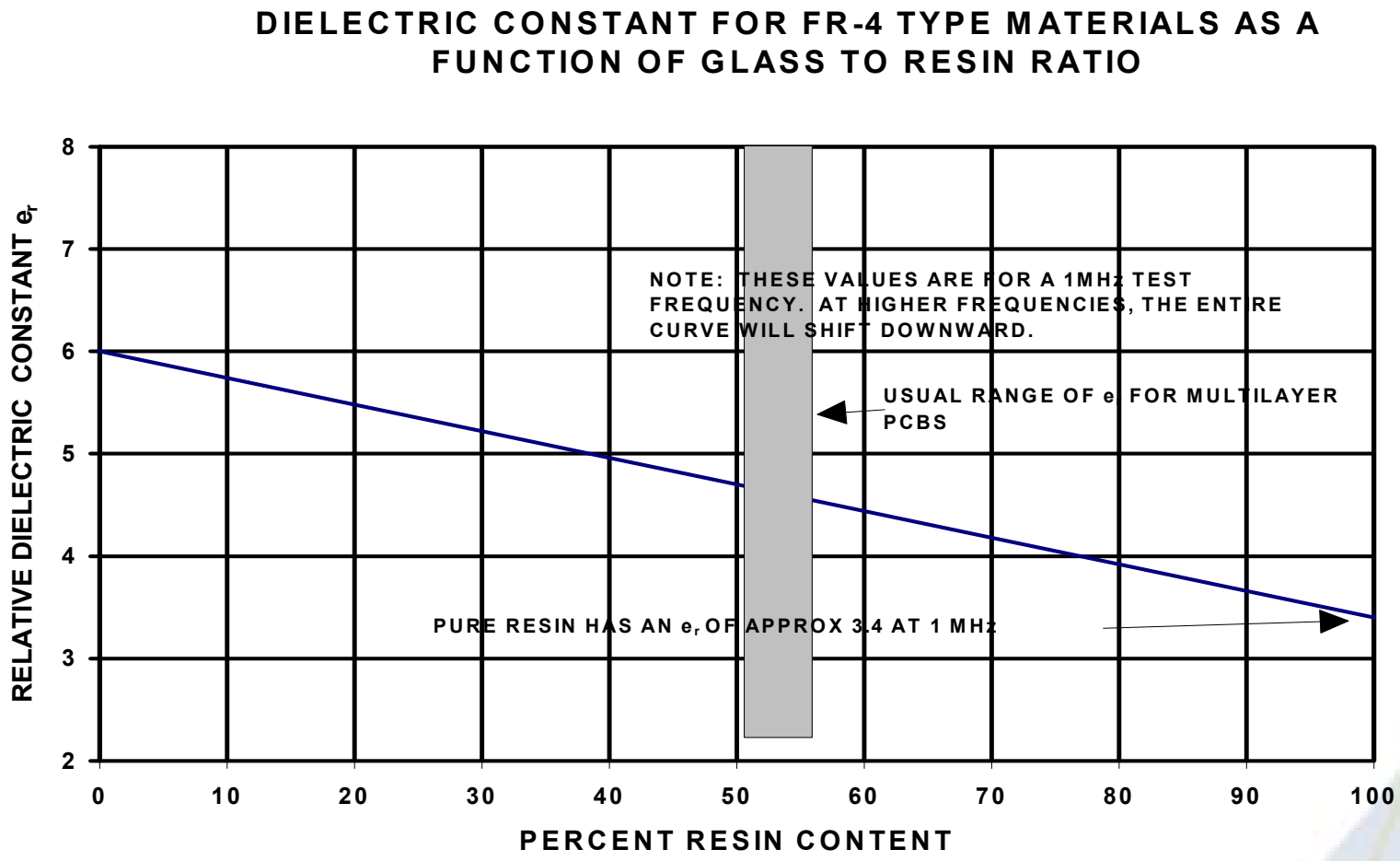
- Dielectric constant (ε_r) vs. frequency



Morgan, Chad & Helster, Dave, "The Impact of PWB Construction on High-Speed Signals"DesignCon99.

Courtesy AMP Circuits and Design 3/99

DIELECTRIC CONSTANT AS A FUNCTION OF GLASS TO RESIN RATIO



SOME PROPERTIES OF HI Tg "FR-4" LAMINATE

Data courtesy of NELCO

Thickness	Construction	Resin Content	er @ 1 MHz	er @ 1 GHz
.002	1 x 106	69.0%	3.84	3.63
.003	1 x 1080	62.0%	4.00	3.80
.004	1 x 2113	54.4%	4.19	4.00
.004	1 x 106 + 1 x 1080	57.7%	4.11	3.91
.004	1 x 2116	43.0%	4.54	4.37
.005	1 x 106 + 1 x 2113	52.8%	4.24	4.05
005	1 x 2116	51.8%	4.26	4.08
.006	1 x 1080 + 1 x 2113	52.2%	4.25	4.06
.006	1 x 106 + 1 x 2116	50.8%	4.29	4.11
.006	2 x 2113	43.5%	4.52	4.35
.007	2 x 2113	49.6%	4.33	4.14
.008	1 x 7628	44.4%	4.49	4.32
.010	2 x 2116	51.8%	4.26	4.08
.014	2 x 7628	38.8%	4.69	4.53

Under construction, the three or four digit number refers to the glass weave type.

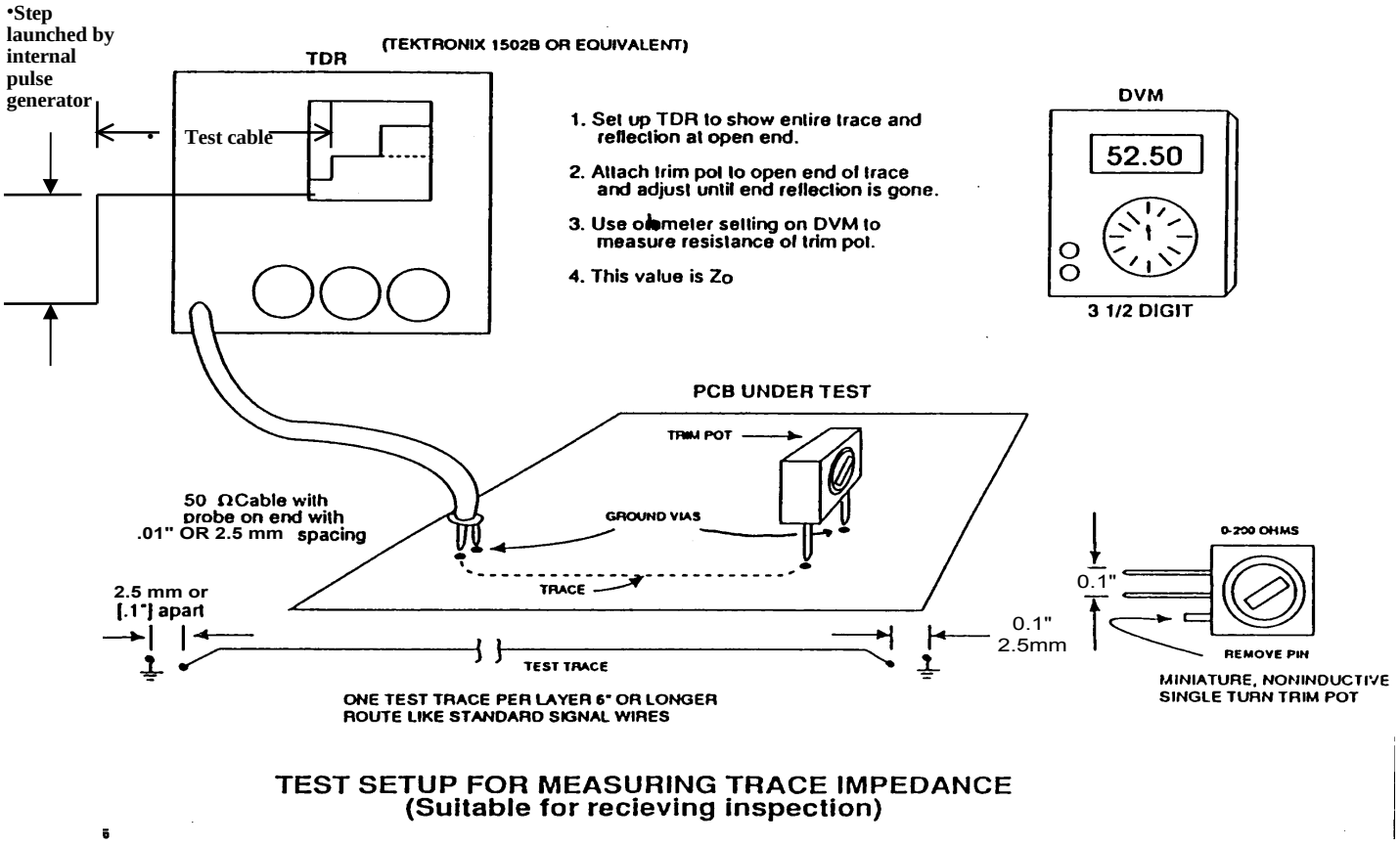
IMPEDANCE ACCURACY

- In order to achieve accurate impedance calculations it is necessary to use a field solver.
- Since relative dielectric constant of a laminate or prepreg is frequency dependent, it is necessary to know the frequency of interest (not clock frequency, rather the frequency content of the switching edges).
- Since relative dielectric constant of a laminate or prepreg is dependent on glass to resin ratio, it is necessary to know this for each laminate and prepreg.
- Using field solvers with accurate information about the relative dielectric constant of the laminate, impedance calculations are more accurate than ±1%.
- Well run fabricators with good process control can achieve impedance accuracy of ±10%.

MEASURING IMPEDANCE

- Impedance of a transmission line is an "AC" property. Therefore, using an ohmmeter will not work.
- The instrument of choice for measuring impedance is a Time Domain Reflectometer (TDR).
- A TDR functions like a radar sending a very fast pulse down a signal path and looking for reflections.
- The size and polarity of these reflections can be used to calculate the impedance of the transmission line.
- In order for these measurements to be accurate, the TDR must be properly calibrated and the impedance measurement location carefully chosen. (Notice on slide 30 that the impedance appears to increase along the length of the transmission line.)

•TDR TEST SETUP USED FOR MEASURING TRANSMISSION LINE PROPERTIES



TEST SETUP FOR MEASURING TRACE IMPEDANCE
(Suitable for recieving inspection)

Smolyansky, Dima & Corey, Steven, "PCB Interconnect Characterization From TDR Measurements." Printed Circuit Design, May 1999.

STEPS IN BUILDING A STACKUP

- Determine how many signal layers are needed.
- Determine how many power planes are needed to distribute power and ground.
- Arrange signals and planes to accomplish
  - Partners for signal layers
  - Parallel plate capacitance between power and ground
- Set signal height above planes to meet cross talk requirements.
- Set trace widths to meet impedance requirements.
- Set spacing between planes to meet capacitance requirements.
- Set spacing between signal layers to meet overall thickness.

TYPES OF SIGNAL LAYERS

			TRACE WIDTH (mils)	IMPEDANCE (ohms)
L1	OUTER "CAP" LAYER			
L2	SIGNAL 1	7.0	5.0	50.0
L3	GROUND 1	5.0		
L4	Vdd 1	3.0		
L5	SIGNAL 2	5.0	5.0	50.0
L6	SIGNAL 3	7.0	5.0	50.0
L7	Vdd 2	5.0		
L8	GROUND 2	3.0		
L9	SIGNAL 4	5.0	5.0	50.0
L10	OUTER "CAP" LAYER	7.0		

LAMINATE

PREPREG

Signal layers on the outside of a PCB are called surface microstrip (L1 and L10 above). Signal layers embedded in the dielectric with a plane on only one side are buried microstrip (l2 and L9 above). Signal layers between two planes are stripline layers (L5 and L6). These can be centered between the planes or offset as shown above.

FIRST PASS IMPEDANCE USING SOLVER AND GOOD LAMINATE DATA

	26 LAYER PCB		FAB=MEI									
	Layer #	Material Name	Material Type	Material Construction	Er (at ~2 GHz)	Material Unpressed Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness* (mils)	Copper Thickness (oz)	Single Ended Trace Width (mils)	Single Ended Imped. (ohms)
			Soldermask				0.7	Solder Mask				
Top	1							1	2.025	1.5	14	49.9
		Isola FR408HR	Prepreg	1 x 3313 RC = 59%	3.57	4.6	4.3	Prepreg				
S1	2							2	0.675	0.5	5	49.3
		Isola FR408HR	Core	1 x 1086 RC = 58%	3.59		3	Core				
GND1	3							3	0.675	0.5		
		Isola FR408HR	Prepreg	1 x 1086 RC = 62%	3.5	3.5	3	Prepreg				
V1	4							4	0.675	0.5		
		Isola FR408HR	Core	1 x 3313 RC = 53.8%	3.68		4	Core				
S2	5							5	0.675	0.5	5	49.9
		Isola FR408HR	Prepreg	1 x 3313 RC = 59%	3.57	4.6	4.1	Prepreg				
S3	6							6	0.675	0.5	5	49.9
		Isola FR408HR	Core	1 x 3313 RC = 53.8%	3.68		4	Core				
V2	7							7	0.675	0.5		
		Isola FR408HR	Prepreg	1 x 1086 RC = 62%	3.5	3.5	3	Prepreg				
GND2	8							8	0.675	0.5		
		Isola FR408HR	Core	1 x 3313 RC = 53.8%	3.68		4	Core				
S4	9							9	0.675	0.5	5	49.9
		Isola FR408HR	Prepreg	1 x 3313 RC = 59%	3.57	4.6	4.1	Prepreg				
S5	10							10	0.675	0.5	5	49.9
		Isola FR408HR	Core	1 x 3313 RC = 53.8%	3.68		4	Core				
V3	11							11	0.675	0.5		
		Isola FR408HR	Prepreg	1 x 1086 RC = 62%	3.5	3.5	3	Prepreg				
GND3	12							12	0.675	0.5		
		Isola FR408HR	Core	1 x 3313 RC = 53.8%	3.68		4	Core				
S6	13							13	0.675	0.5	5	49.9
		Isola FR408HR	Prepreg	1 x 3313 RC = 59%	3.57	4.6	4.1	Prepreg				
S7	14							14	0.675	0.5	5	49.9
		Isola FR408HR	Core	1 x 3313 RC = 53.8%	3.68		4	Core				
GND4	15							15	0.675	0.5		
		Isola FR408HR	Prepreg	1 x 1086 RC = 62%	3.5	3.5	3	Prepreg				
V4	16							16	0.675	0.5		
		Isola FR408HR	Core	1 x 3313 RC = 53.8%	3.68		4	Core				
S8	17							17	0.675	0.5	5	49.9
		Isola FR408HR	Prepreg	1 x 3313 RC = 59%	3.57	4.6	4.1	Prepreg				
S9	18							18	0.675	0.5	5	49.9
		Isola FR408HR	Core	1 x 3313 RC = 53.8%	3.68		4	Core				
GND5	19							19	0.675	0.5		
		Isola FR408HR	Prepreg	1 x 1086 RC = 62%	3.5	3.5	3	Prepreg				
V5	20							20	0.675	0.5		
		Isola FR408HR	Core	1 x 3313 RC = 53.8%	3.68		4	Core				
S10	21							21	0.675	0.5	5	49.9
		Isola FR408HR	Prepreg	1 x 3313 RC = 59%	3.57	4.6	4.1	Prepreg				
S11	22							22	0.675	0.5	5	49.9
		Isola FR408HR	Core	1 x 3313 RC = 53.8%	3.68		4	Core				
V6	23							23	0.675	0.5		
		Isola FR408HR	Prepreg	1 x 1086 RC = 62%	3.5	3.5	3	Prepreg				
GND6	24							24	0.675	0.5		
		Isola FR408HR	Core	1 x 1086 RC = 58%	3.59		3	Core				
S12	25							25	0.7	0.5	5	49.3
		Isola FR408HR	Prepreg	1 x 3313 RC = 59%	3.57	4.6	4.3	Prepreg				
Bottom	26							26	2.025	1.5	14	49.9
			Soldermask				0.7	Solder Mask				
							------		------			
							94.5	114.8	20.3			
							Material Thickness	Total Thickness	Copper Thickness			

*Copper is nominal finished thickness

= Power/Ground
= High Speed
= Low Speed

FIRST TRY IMPEDANE TEST RESULTS

L2- 47.4 OHMS
L5- 50.7 OHMS
L6- 51.2 OHMS
L9- 50.1 OHMS
L10- 51.5 OHMS
L13- 51.9 OHMS
L14- 50.5 OHMS
L17- 48.9 OHMS
L18- 49.6 OHMS
L21- 50.3 OHMS
L22 49.6 OHMS
L25- 54.7 OHMS

All well within ±10% limits.

TARGET IMPEDANCE:

50Ω ±10%

COMMENTS ON STACKUP DRAWING

- Notice that there is far more information on this drawing than is typically provided to a fabricator.
- Exact callouts are done for each laminate and prepreg location.
- The reason for this is to insure that all SI goals are met and that manufacturing is repeatable from fabricator to fabricator.
- When stackup drawing is supplied to fabricator, the impedance column is removed. Specifying both impedance and exact cross section creates a conflict.
- Fabricators will usually recalculate impedance and get different results unless their skills are extremely good.
- Prepreg layers shrink during lamination due to resin flow into adjacent copper layers.

A 26 LAYER STACKUP WITH SINGLE STRIPLINE LAYERS

	26 Layer Stackup, 130 mils thick, modified to remove 1080 prepreg, 03/28/08												
	Layer #	Material Name	Material Type	Material Construction	Material Unpressed Er (at ~2 GHz)	Material Pressed Er (at ~2 GHz)	Material Unpressed Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness (mils)	Copper Thickness (oz)		Single Ended Trace Width (mils)
								0.7	Solder				
Top	1								1	2.2	1.5		
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.5	Prepreg				
S1	2								2	0.6	0.5		4
		FR-408	Core	1 x 2113 RC = 44%	4			3	Core				
Ground	3								3	0.6	0.5		
		FR-408	Prepreg	1 x 2113 RC = 44%	4		3	2.4	Prepreg				
V1	4								4	0.6	0.5		
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
S2	5								5	0.6	0.5		4
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.5	Prepreg				
Ground	6								6	0.6	0.5		
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
S3	7								7	0.6	0.5		4
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.5	Prepreg				
Ground	8								8	0.6	0.5		
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
S4	9								9	0.6	0.5		4
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.5	Prepreg				
Ground	10								10	0.6	0.5		
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
S5	11								11	0.6	0.5		4
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.5	Prepreg				
Ground	12								12	1.2	1.0		
		FR-408	Core	1 x 106 RC = 63%	3.5			2	Core				
V2	13								13	1.2	1.0		
		FR-408	Prepreg	3 x 7628 RC = 39%	4		21	20.5	Prepreg				
Ground	14								14	1.2	1.0		
		FR-408	Core	1 x 106 RC = 63%	3.5			2	Core				
V3	15								15	1.2	1.0		
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.5	Prepreg				
S6	16								16	0.6	0.5		4
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
Ground	17								17	0.6	0.5		
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.5	Prepreg				
S7	18								18	0.6	0.5		4
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
Ground	19								19	0.6	0.5		
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.5	Prepreg				
S8	20								20	0.6	0.5		4
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
Ground	21								21	0.6	0.5		
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.5	Prepreg	<-			
S9	22								22	0.6	0.5		4
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core				
V6	23								23	0.6	0.5		
		FR-408	Prepreg	1 x 2113 RC = 44%	4		3	2.4	Prepreg				
Ground	24								24	0.6	0.5		
		FR-408	Core	1 x 2113 RC = 44%	4			3	Core				
S10	25								25	0.6	0.5		4
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.5	Prepreg				
Bottom	26								26	2.2	1.5		
								0.7	Solder				
								-------		-------			
								103.7	124.9	21.2			
								Material Thickness	Total Thickness	Copper Thickness			

Layers 1 and 26 are to be used for component mounting and traces that are not controlled impedance.
Capture pads for laser drilled holes on L1, L2, L25 and L26 must be 18 mils in diameter.

A 14 LAYER STACKUP

	14 LAYER PCB 11/02/06													
	Layer #	Material Name	Material Type	Material Construction	Material Unpressed Er (at ~2 GHz)	Material Pressed Er (at ~2 GHz)	Material Unpressed Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness (mils)	Copper Thickness (oz)		Single Ended Trace Width (mils)	Single Ended Imped. (ohms)
								0.7	Solder Mask					
Top	1								1	2.2	1.5			
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.4	Prepreg					
S1	2								2	0.6	0.5		6	52.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core					
Ground	3								3	0.6	0.5			
		FR-408	Prepreg	2 x 106 RC = 63.3%	4		4	3	Prepreg					
V1	4								4	0.6	0.5			
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core					
S2	5								5	0.6	0.5		5	50.0
		FR-408	Prepreg	1 X 3313 RC = 53.8%	3.7		4	3.4	Prepreg					
S3	6								6	0.6	0.5		5	50.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core					
Ground	7								7	0.6	0.5			
		FR-408	Prepreg	2 x 106 RC = 63.3%	4		4	3	Prepreg					
V2	8								8	0.6	0.5			
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core					
S4	9								9	0.6	0.5		5	50.0
		FR-408	Prepreg	1 X 3313 RC = 53.8%	3.7		4	3.4	Prepreg					
S5	10								10	0.6	0.5		5	50.0
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core					
V4	11								11	0.6	0.5			
		FR-408	Prepreg	2 x 106 RC = 63.3%	4		4	3	Prepreg					
Ground	12								12	0.6	0.5			
		FR-408	Core	1 x 3313 RC = 53.8%	3.7			4	Core					
S8	13								13	0.6	0.5		6	52.0
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7		4	3.4	Prepreg					
Bottom	14								14	2.2	1.5			
								0.7	Solder Mask					
								--------		--------				
								48.0	59.6	11.6				
								Material Thickness	Total Thickness	Copper Thickness				

Note: Place only information to left of dark line on fabrication drawing. Do not place impedance information on fabrication drawing.

Prepared by Speeding Edge, 11/02/06

Layers 1 and 14 are to be used for component mounting and traces that are not controlled impedance.

10GENET signals to be routed only on layer 2 and be connected using blind vias to layer 1.

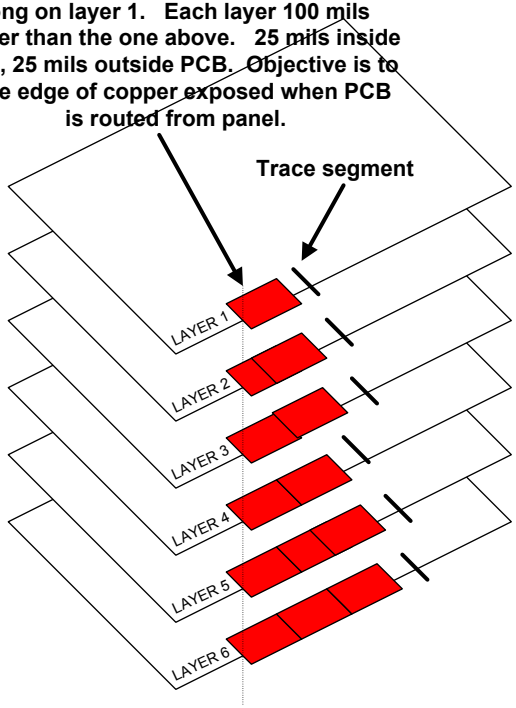
ACCOUNTING FOR RESIN FLOW INTO COPPER

- During lamination, heat is applied and the resin in prepreg layers melts and flows into voids in the adjacent power and signal layers.
- As a result, the overall thickness of the PCB and the prepreg layers will be less than expected.
- Allowance must be made for this decrease in thickness.
- The best way to do this is to obtain from the fabricator these shrinkage factors. (plane against plane, plane against signal, signal against signal)
- The amount of shrinkage depends on copper thickness and area of copper remaining in each layer after etching .
- For ½ ounce copper I use: plane against plane- .2 mils, plane against signal- .4 mils, signal against signal- .5 mils (for ½ ounce copper)

CHECKING FINAL STACKUP

- After PCBs are fabricated, it is essential to have a method for verifying that they comply with all of the requirements.
- Among the requirements that must be verified are:
  - Layers are in correct order
  - Copper is the correct thickness
  - Laminates are the correct thickness
  - Impedance goals have been met.
- A common method for doing some of the above is a test coupon designed by the fabricator.
- Some problems with test coupons:
  - No guarantee that impedance test traces match main PCB
  - No way to check layer order
  - Often unavailable when investigation into problems occur.
- Alternative to test coupons- build test structures into PCB

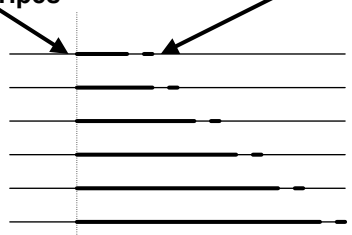
Stacking Stripe- 50 mils wide by 200 mils long on layer 1. Each layer 100 mils longer than the one above. 25 mils inside PCB, 25 mils outside PCB. Objective is to have edge of copper exposed when PCB is routed from panel.



STACKING STRIPE SET WITH TEST TRACES

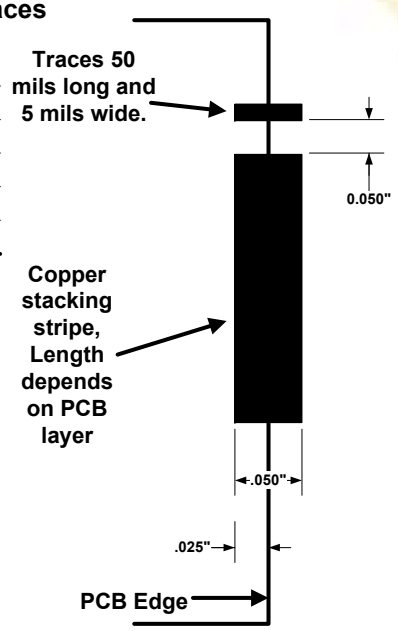
Side view of stacking stripes

End on view of traces



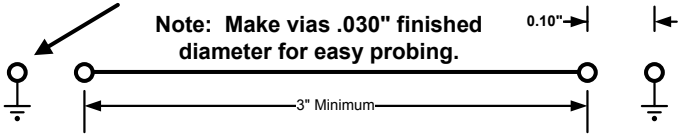
Edge on view of stacking stripes and test traces.

NOTE: Stacking stripes must not contact copper features such as power planes on any layer. If necessary, powerplane must be indented where stacking stripes are plotted to increase space to at least .010" between plane or feature and stripe.



Stacking stripe dimensions as plotted on film layers

Connect ground via to plane nearest test trace. One test trace per signal layer. Test trace same width as signal traces.



IMPEDANCE TEST TRACE

Note: Impedance test trace vias need to be 30 mils diameter with 0.1" separation. Velocity test trace should be 12" long.

6/24/97
Lee Ritchey

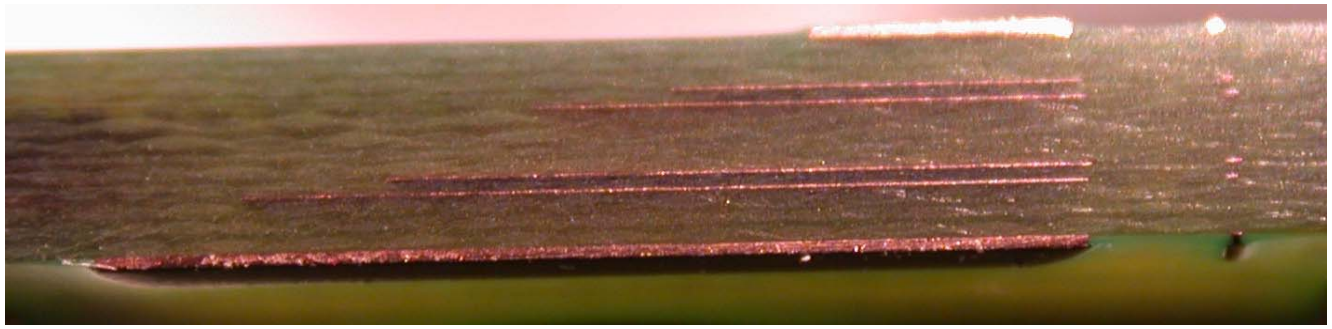
STACKING STRIPE AND IMPEDANCE TEST TRACE DESCRIPTION

Note: Locate stacking strips on a side of the PCB that allows viewing without cutting away part of the PCB.

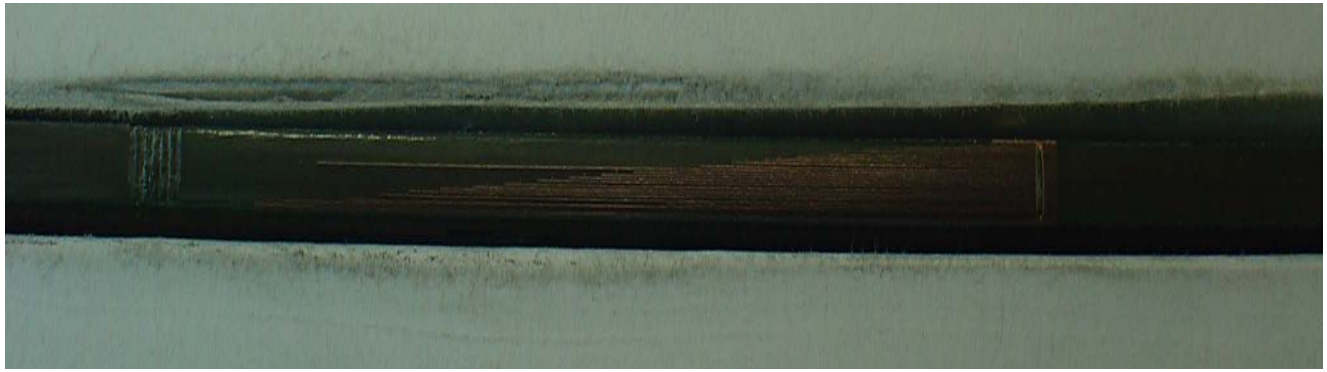
COMMENTS ON STACKING STRIPES

- Occasionally there is an objection to copper protruding at the edge of a PCB.
- This can be a problem if this copper is connected to internal circuits. Properly designed stacking stripes are not connected to internal circuits, so this problem is avoided.
- Some fabricators claim that this copper dulls router bits. Those same fabricators route and drill through copper everywhere else in their operations without complaint.
- In satellite applications, this "floating" copper is not allowed for static reasons. Connect the stripes to the ground planes to solve this problem .
- There isn't any downside to adding stacking stripes other than a little extra CAD time.

SAMPLE STACKING STRIPES

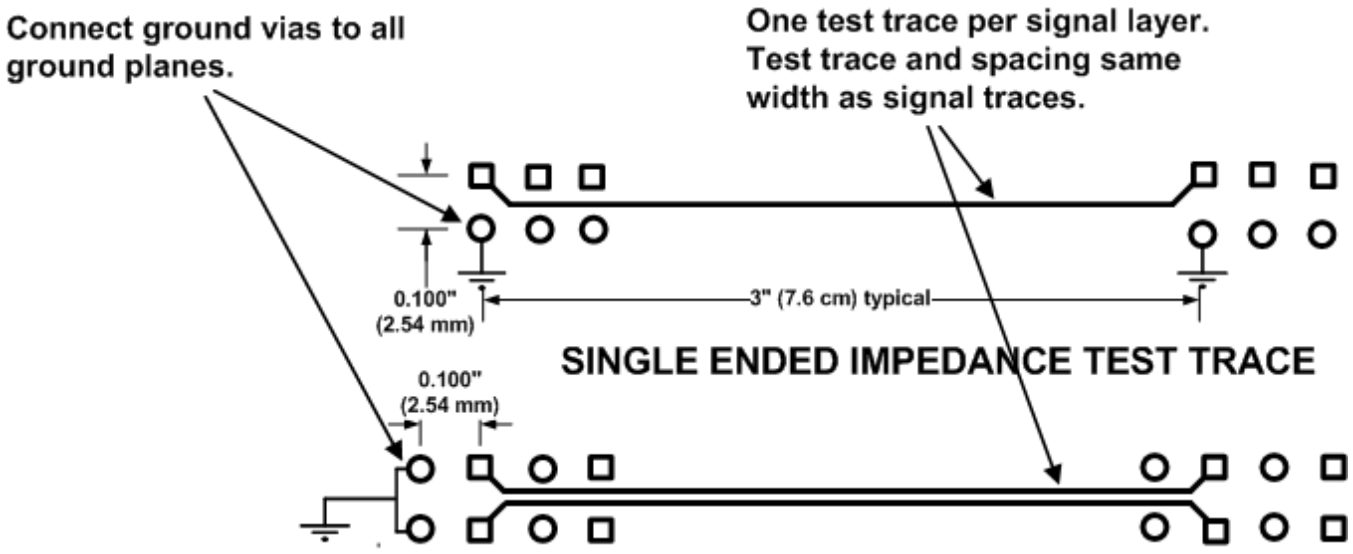


6 LAYER STACKUP DONE CORRECTLY



24 LAYER STACKUP DONE INCORRECTLY

IMPEDANCE TEST TRACE CONFIGURATIONS



IMPEDANCE TEST COUPON DESCRIPTION

Note: When designing differential pairs using the "not closer than" spacing rule, it is not necessary to measure differential impedance. Single ended test traces are all that are necessary.

SUMMARY

- PCB Stackup design is an integral part of the signal integrity engineering process.
- PCB stackup design is far too complex to be left in the hands of the fabricator. It is not that fabricators are not capable of designing stackups, their skill set does not cover all the areas that are important.
- PCB stackup design is a joint effort between SI engineers and fabricators. Neither can do it alone.
- PCB stackup design requires detailed knowledge of the materials used to fabricate PCBs as well as the fabrication process itself.
- PCB Stackup design is not a difficult process given good materials data and design tools.

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2. A Treatment of Differential Signaling and Its Design Requirements, Ritchey, Lee W. Speeding Edge, "Current Sources News Letter, April 2008.

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