

Trends and Challenges in VLSI Technology Scaling Towards 100nm

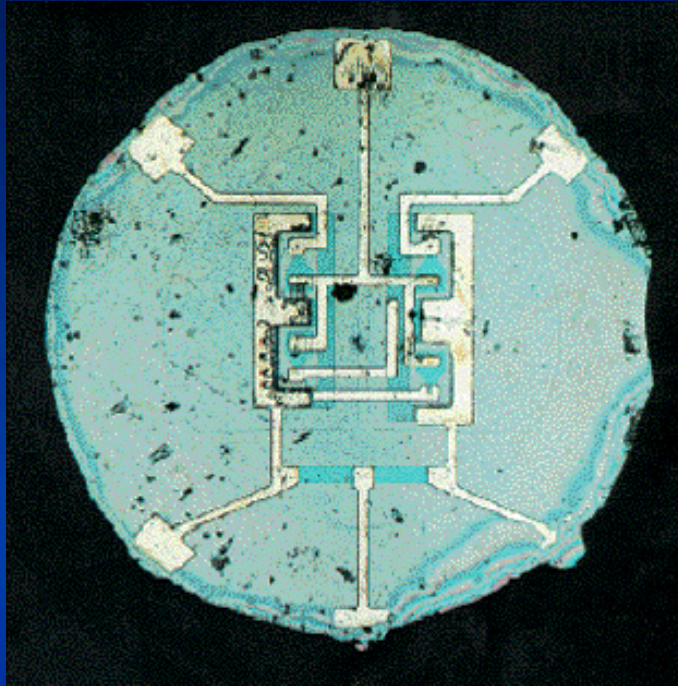
Stefan Rusu
Intel Corporation
stefan.rusu@intel.com

September 2001

Agenda

- **VLSI Technology Trends**
 - Frequency and power trends
- **Scaling Challenges**
 - Transistor scaling
 - Interconnect scaling
 - Capacitive and inductive coupling
 - Leakage
- **Summary**

Process Technology Evolution



1961

First Planar Integrated Circuit
Two transistors



2001

Pentium® 4 Processor
42 million transistors

Moore's Law - 1965

The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor Division of Fairchild Camera and Instrument Corp.

The future of integrated electronics in the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to central computers—automatic controls for automobiles, and personal portable communication equipment. The electronic watch will mean only a display, as it has today.

For the highest potential lies in the production of large computers. In telephone communications, integrated circuits in digital filters will replace channels in multiple equipment. Integrated circuits will also replace telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, numerous banks of integrated electronics may be distributed throughout the

machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turnaround.

Present and future

In integrated electronics, I mean all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as available units. These microtechniques were first investigated in the late 1950's. The object was to miniaturize electronic equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including micro-miniaturized techniques for individual components, thin film structures and semiconductor integrated circuits.

Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the way of the future to be a combination of the various approaches.

The advances of semiconductor integrated circuitry are already using the improved characteristics of thin film resistors by applying each film directly to an active semiconductor substrate. Those advancing a technology based upon thin films are developing sophisticated techniques for the attachment of active semiconductor devices to the passive film system.

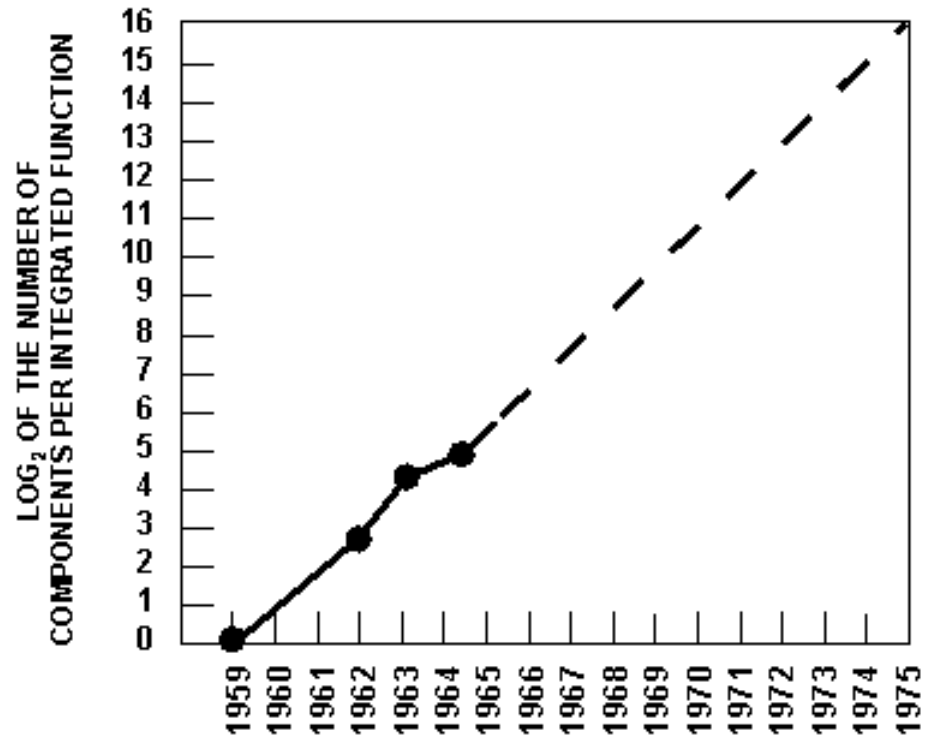
Both approaches have worked well and are being used in equipment today.

The author



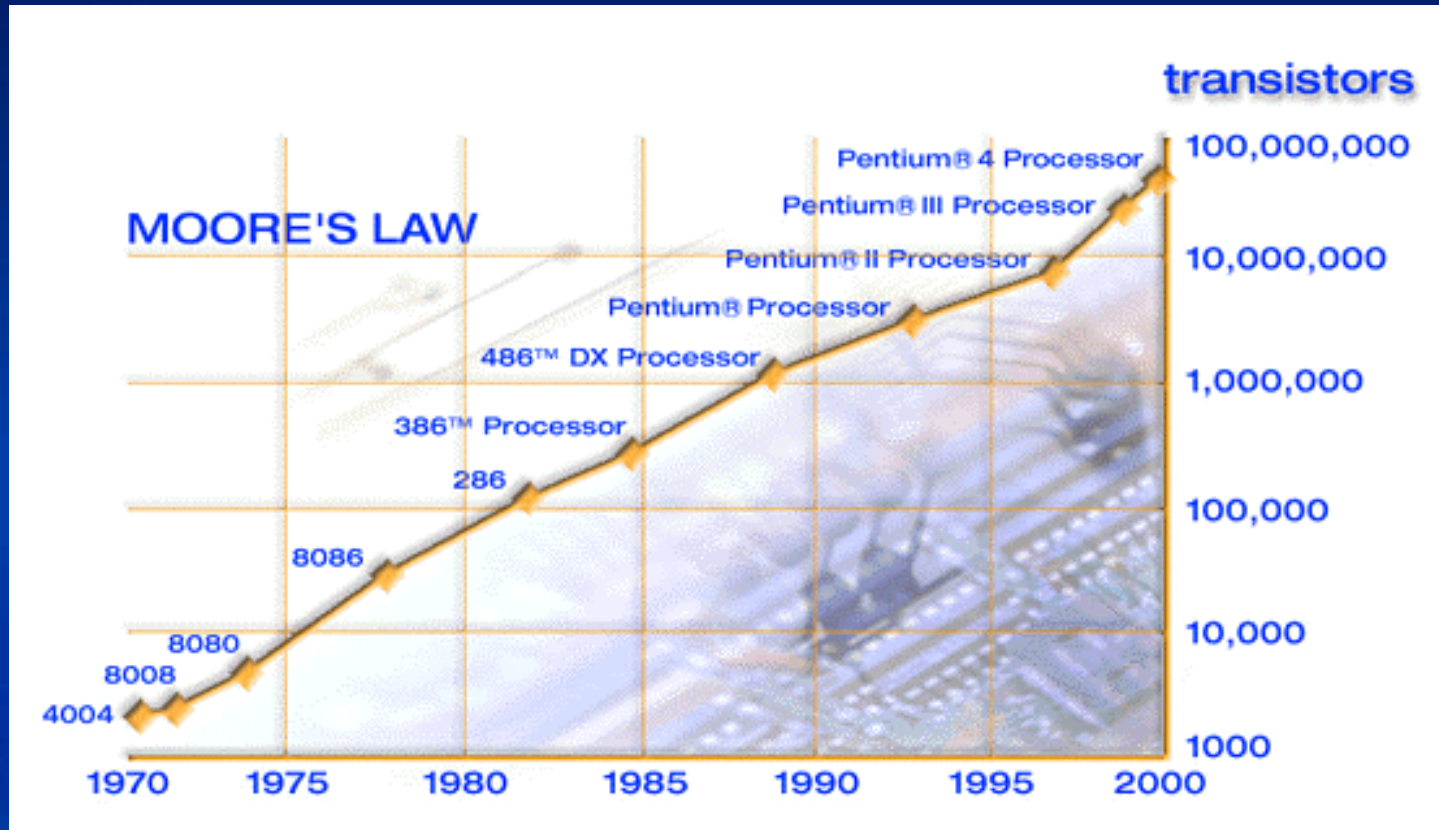
Dr. Gordon E. Moore is one of the new breed of electronic engineers, interested in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1955.

Electronics, Volume 22, Number 4, April 15, 1965



Electronics, April 1965

Moore's Law - Today

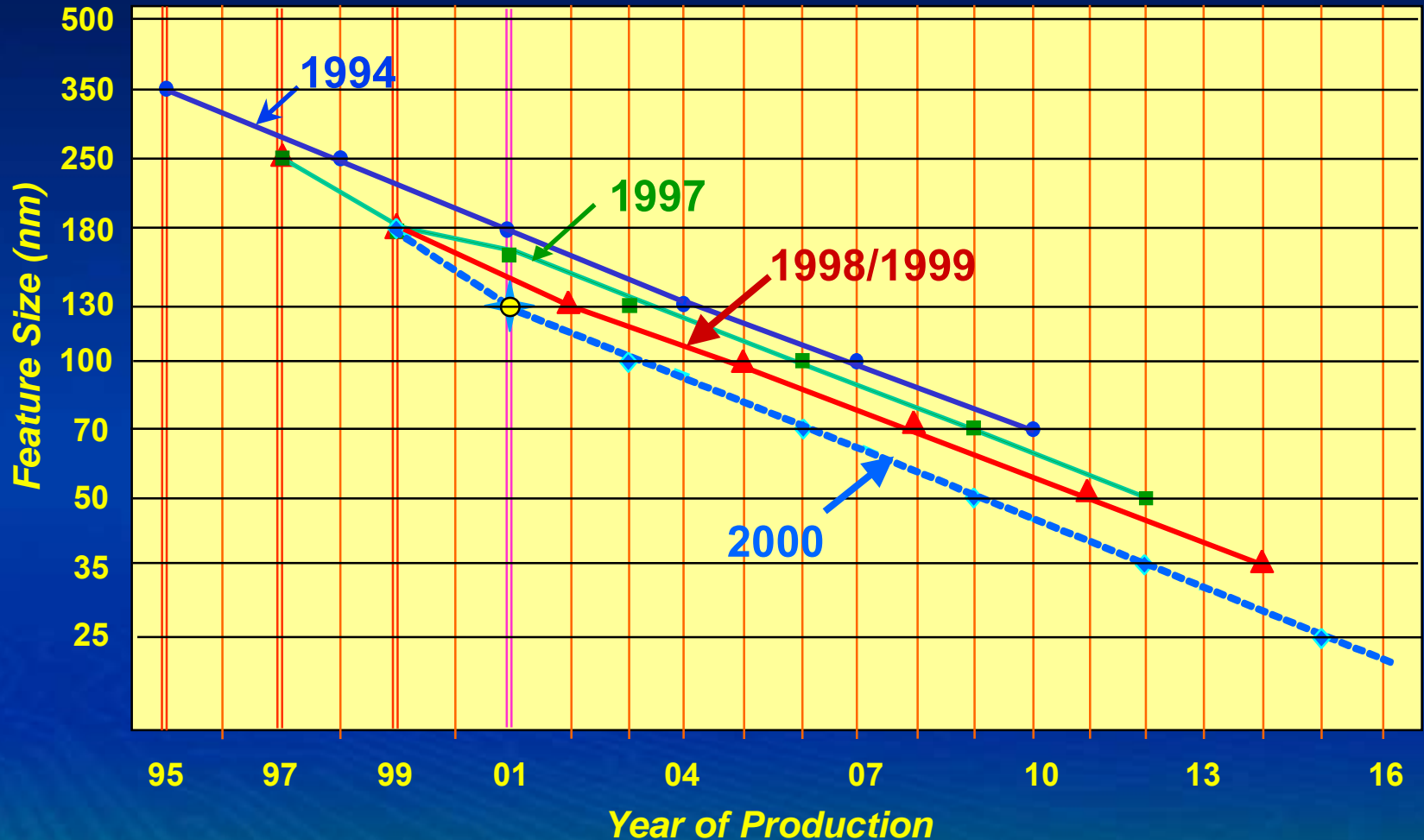


- Number of transistors per integrated circuit doubles every two years

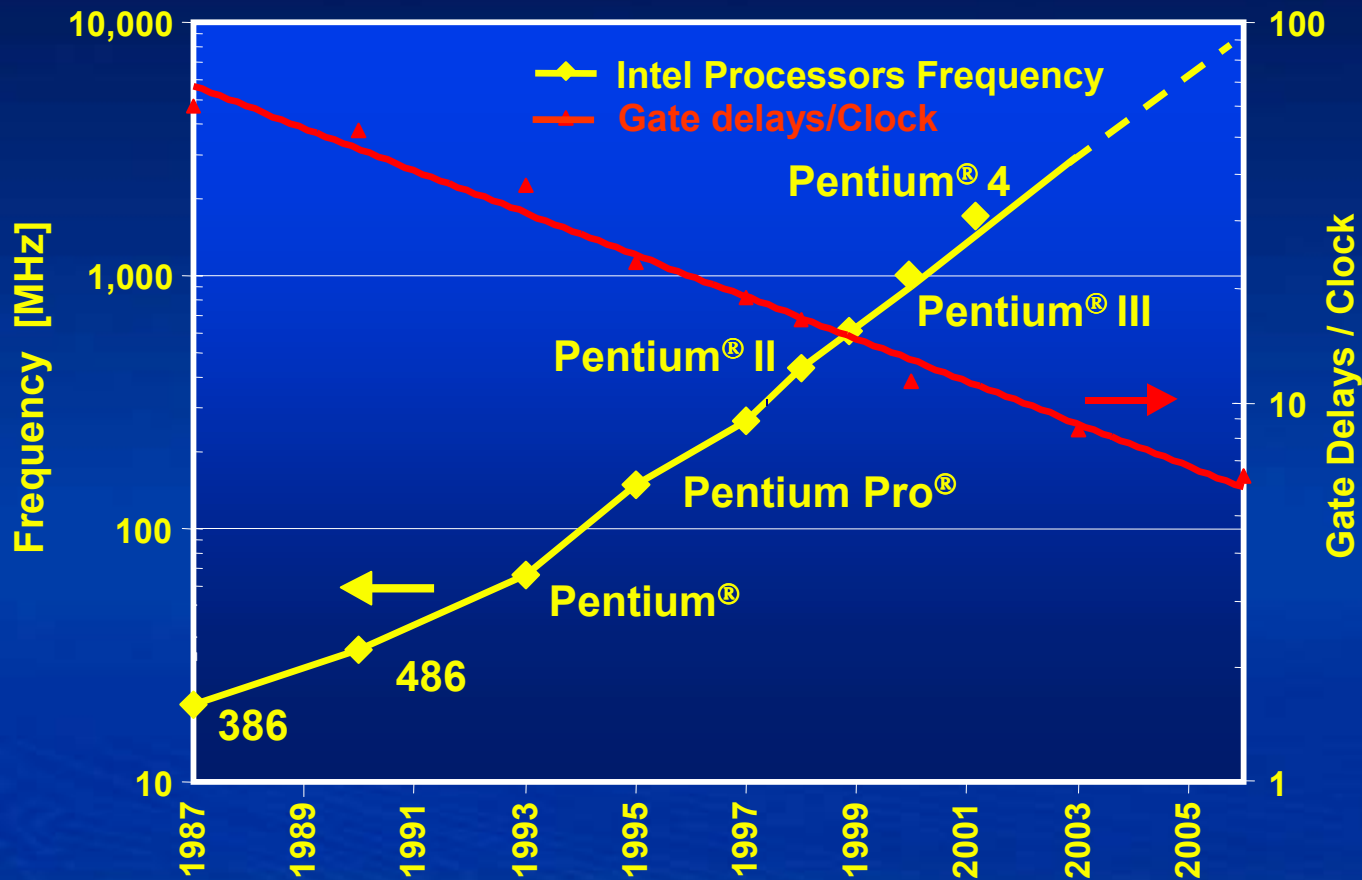
SIA Technology Roadmap

Characteristic	1999	2001	2004	2008
Process Technology [nm]	180	130	90	60
Logic Transistors [mil]	23.8	47.6	135	539
Across-chip Clock Speed [MHz]	1200	1600	2000	2655
Die area [sq. mm]	340	340	390	468
Wiring Levels	6	7	8	9

ITRS Roadmap Acceleration Continues

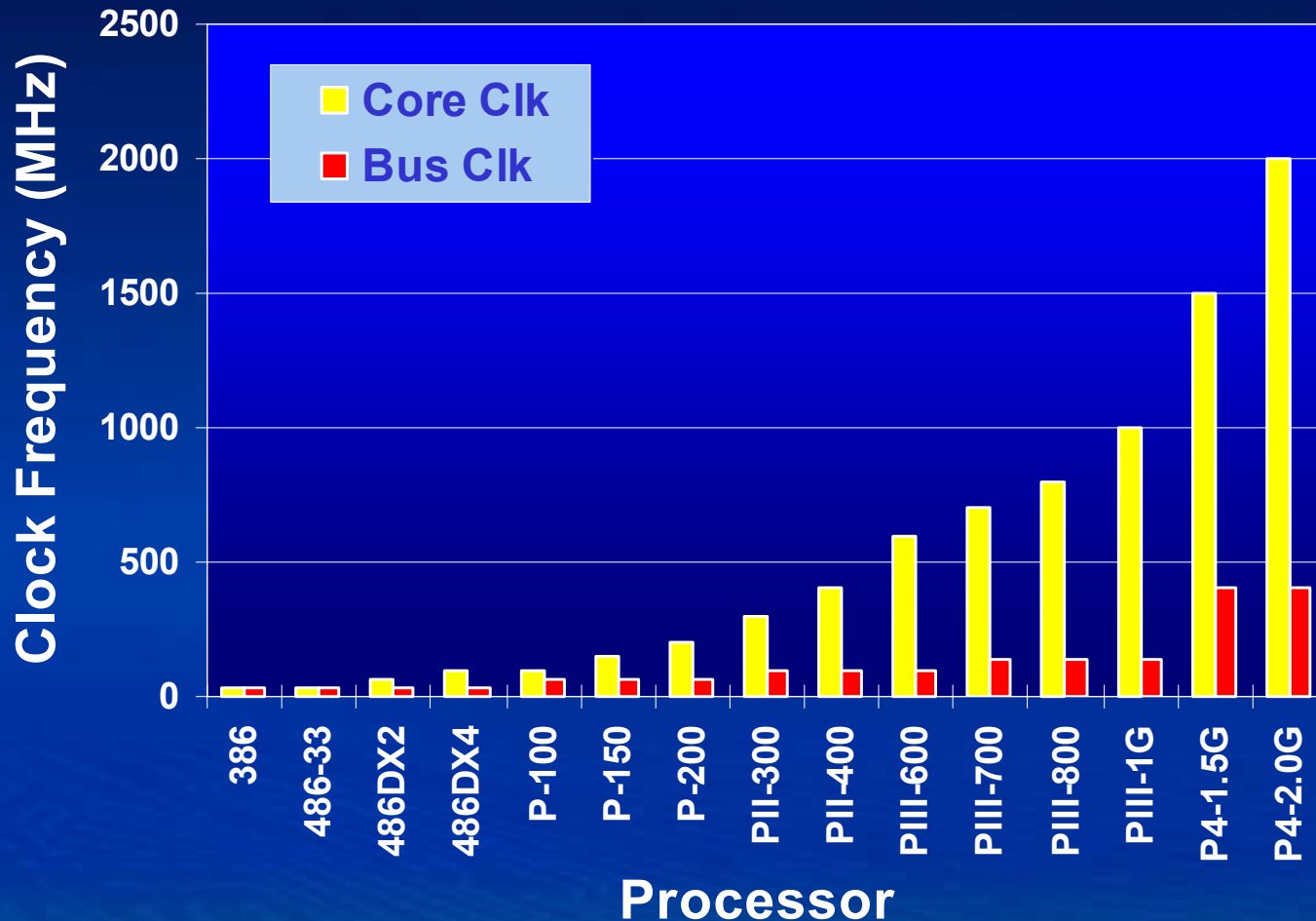


Processor Frequency Trend



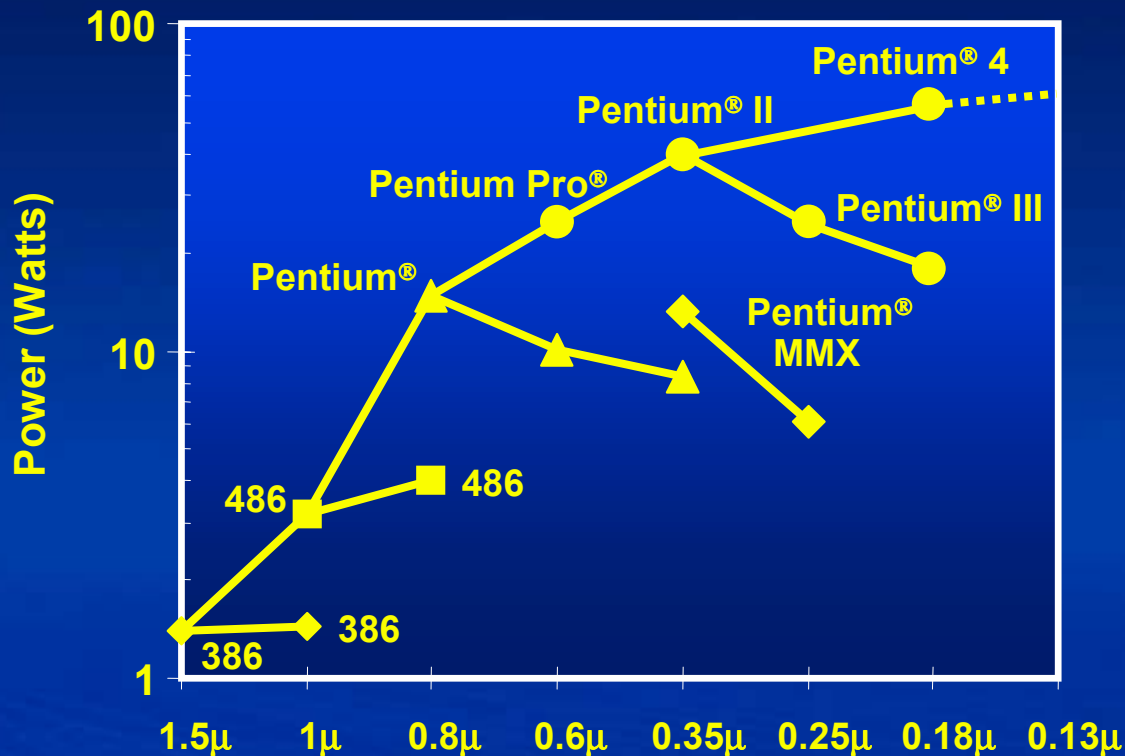
- Frequency doubles each generation
- Number of gates per clock reduces by 25%

Processor Core Vs. Bus Clock



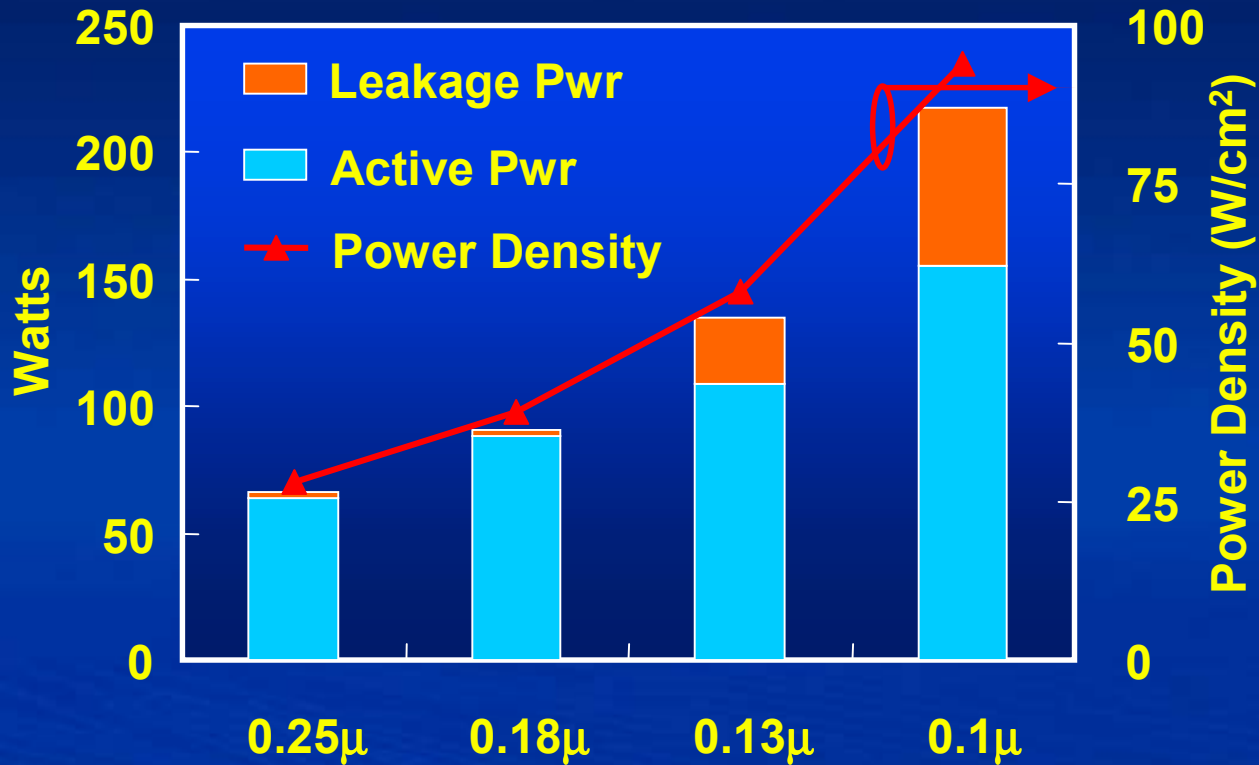
Bus frequency is not keeping up with the processor core

Processor Power Trend



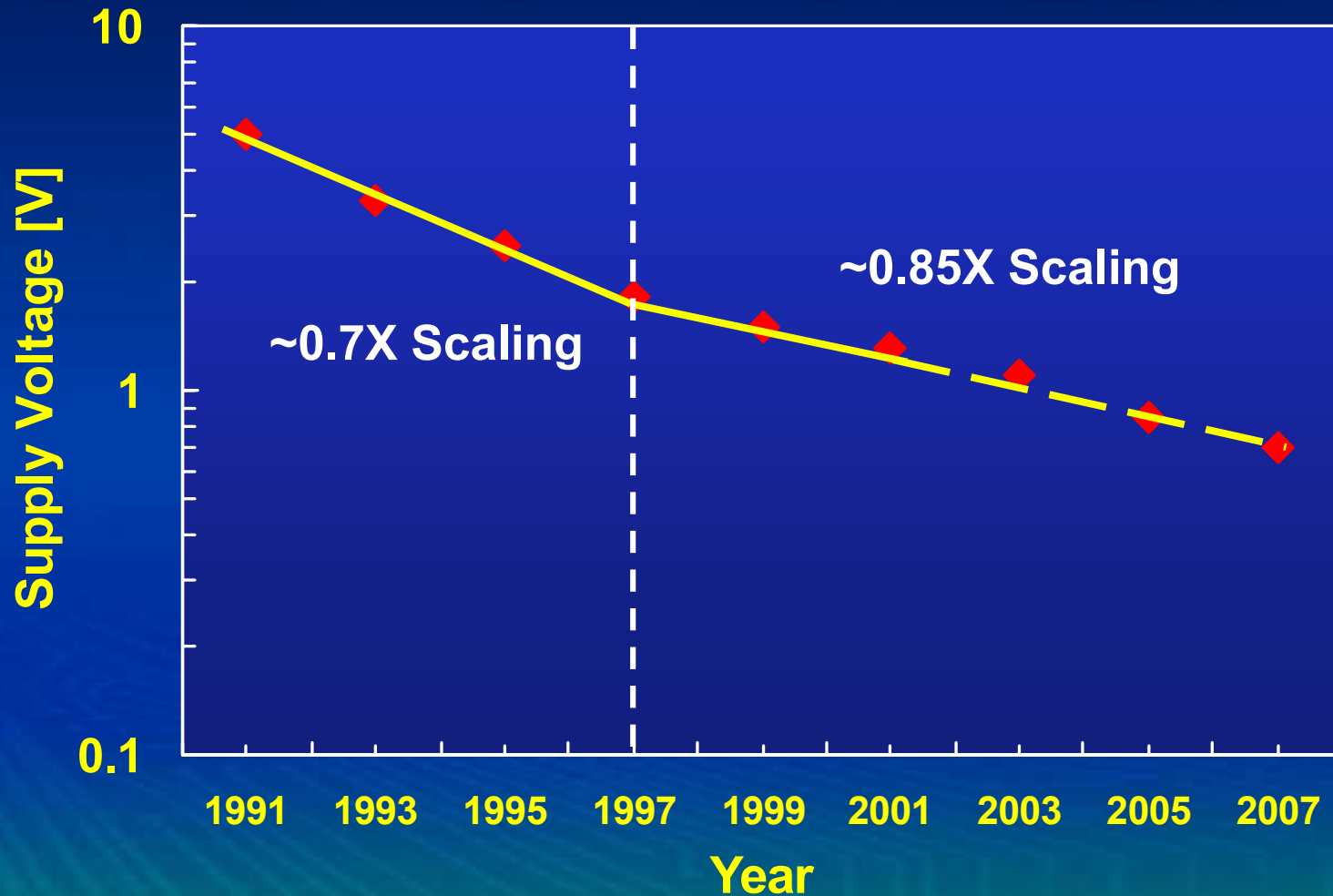
- Lead processor power increases every generation
- Compactions provide higher performance at lower power

Power Density Trend

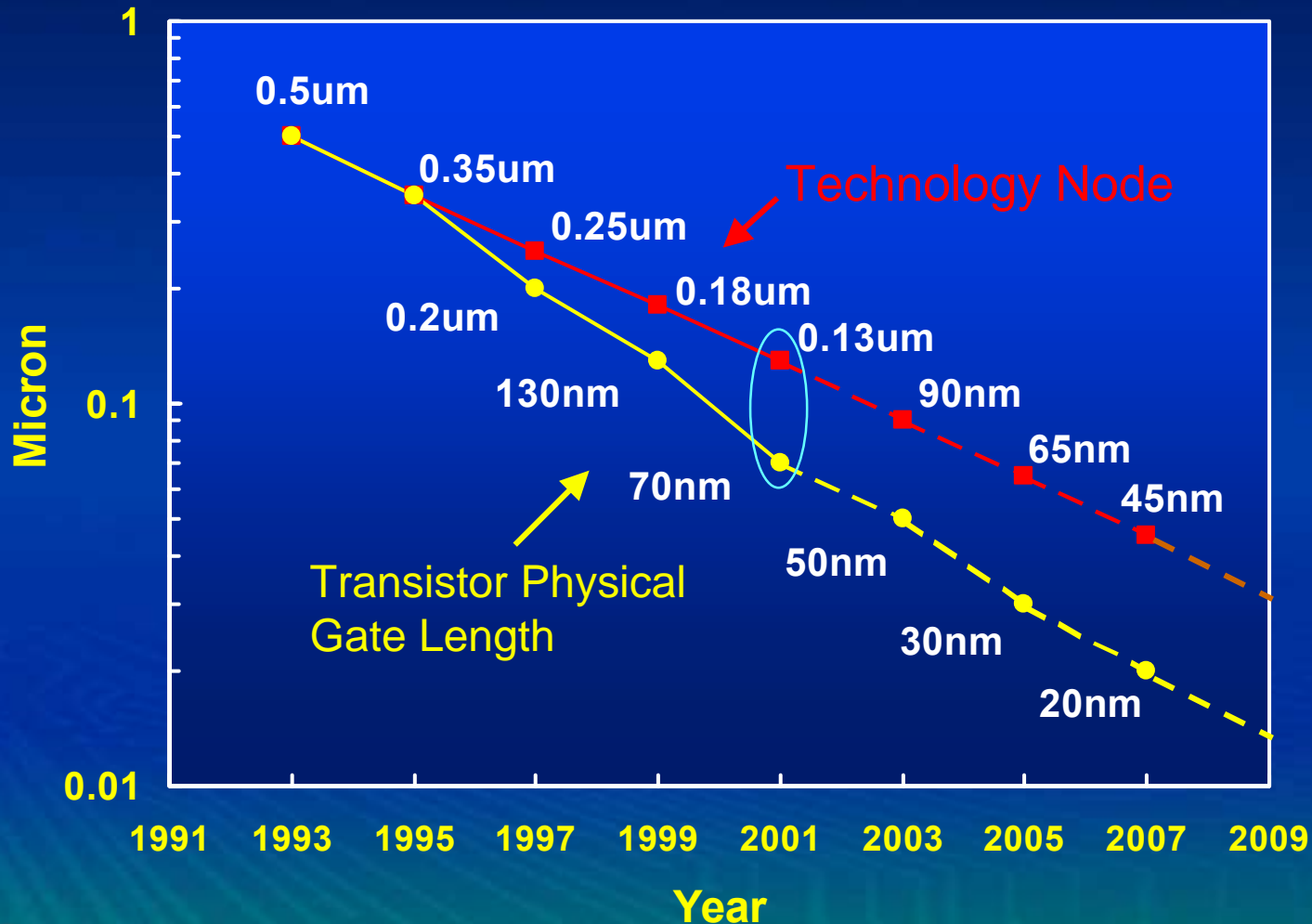


- Assumptions: 15mm die, 1.5x frequency increase per generation

Voltage Scaling



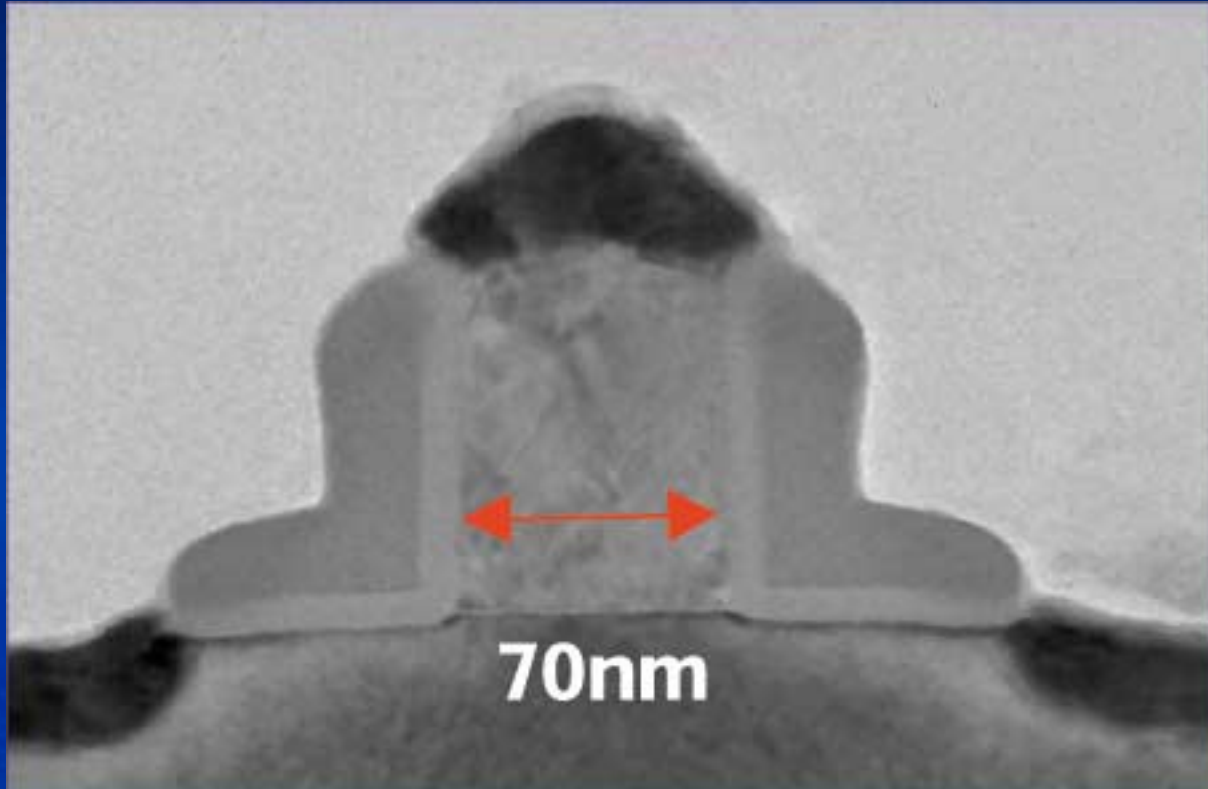
Transistor Physical Gate Length



Source: Robert Chau, 6/2001

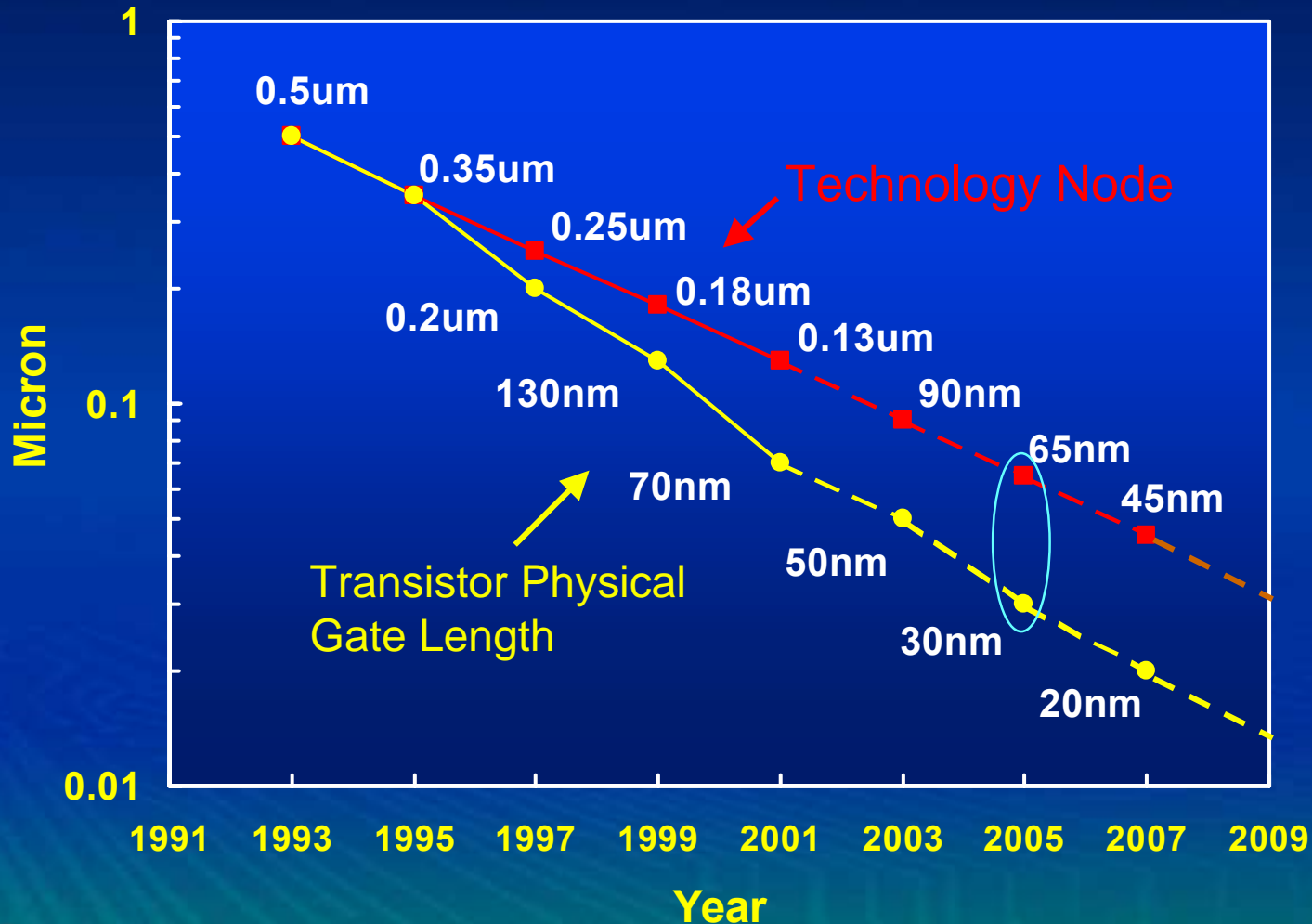


0.13 μm Process Technology



70nm Lgate NMOS transistor – in production today

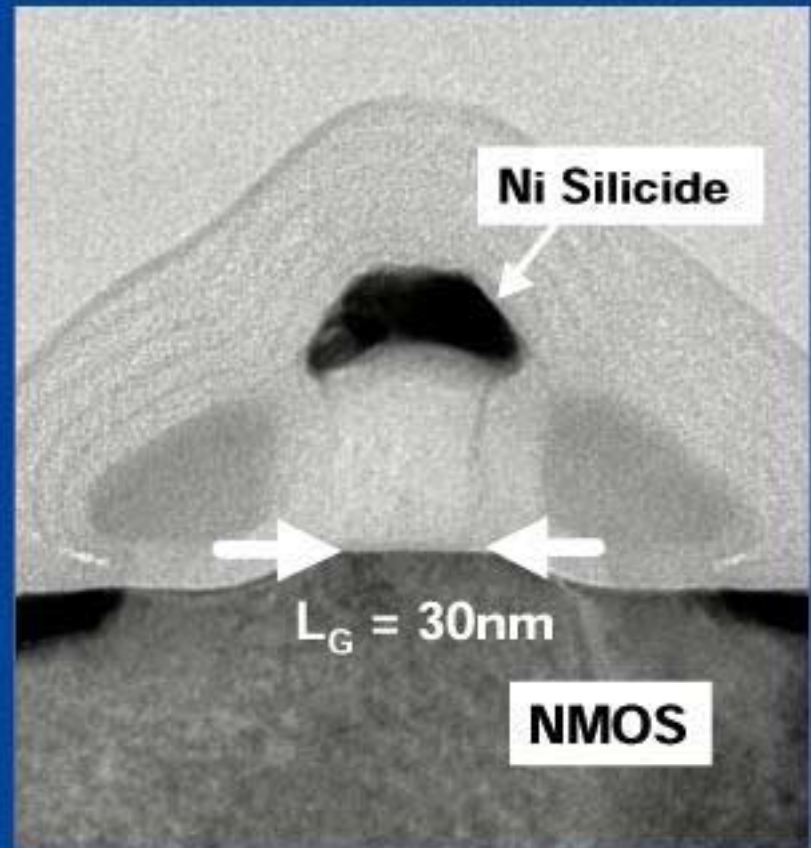
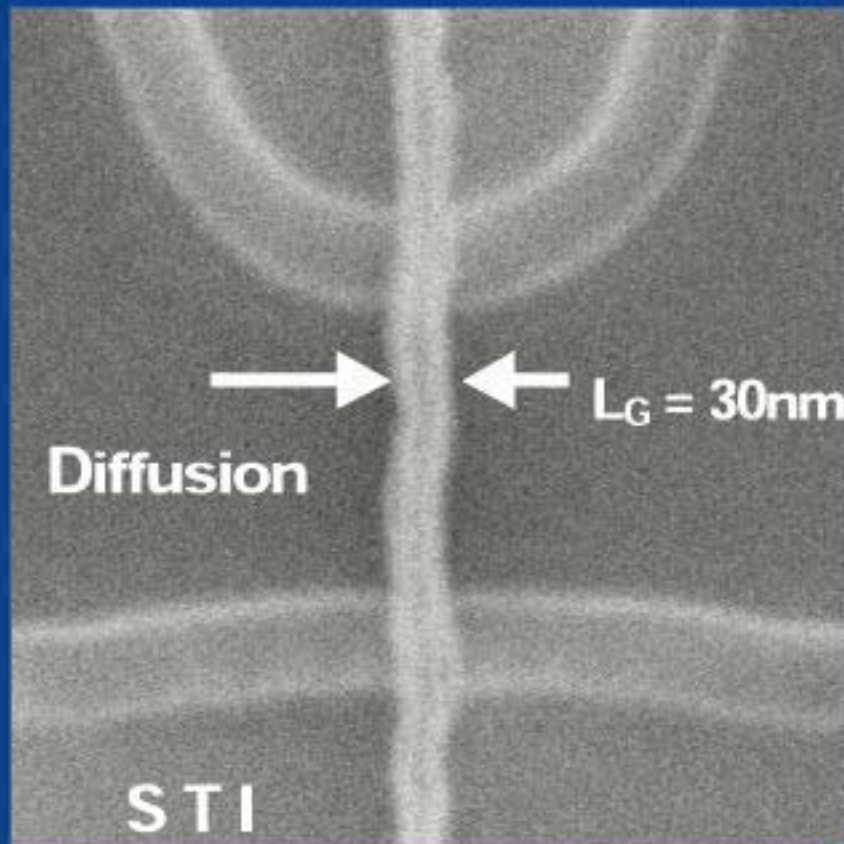
Transistor Physical Gate Length



Source: Robert Chau, 6/2001

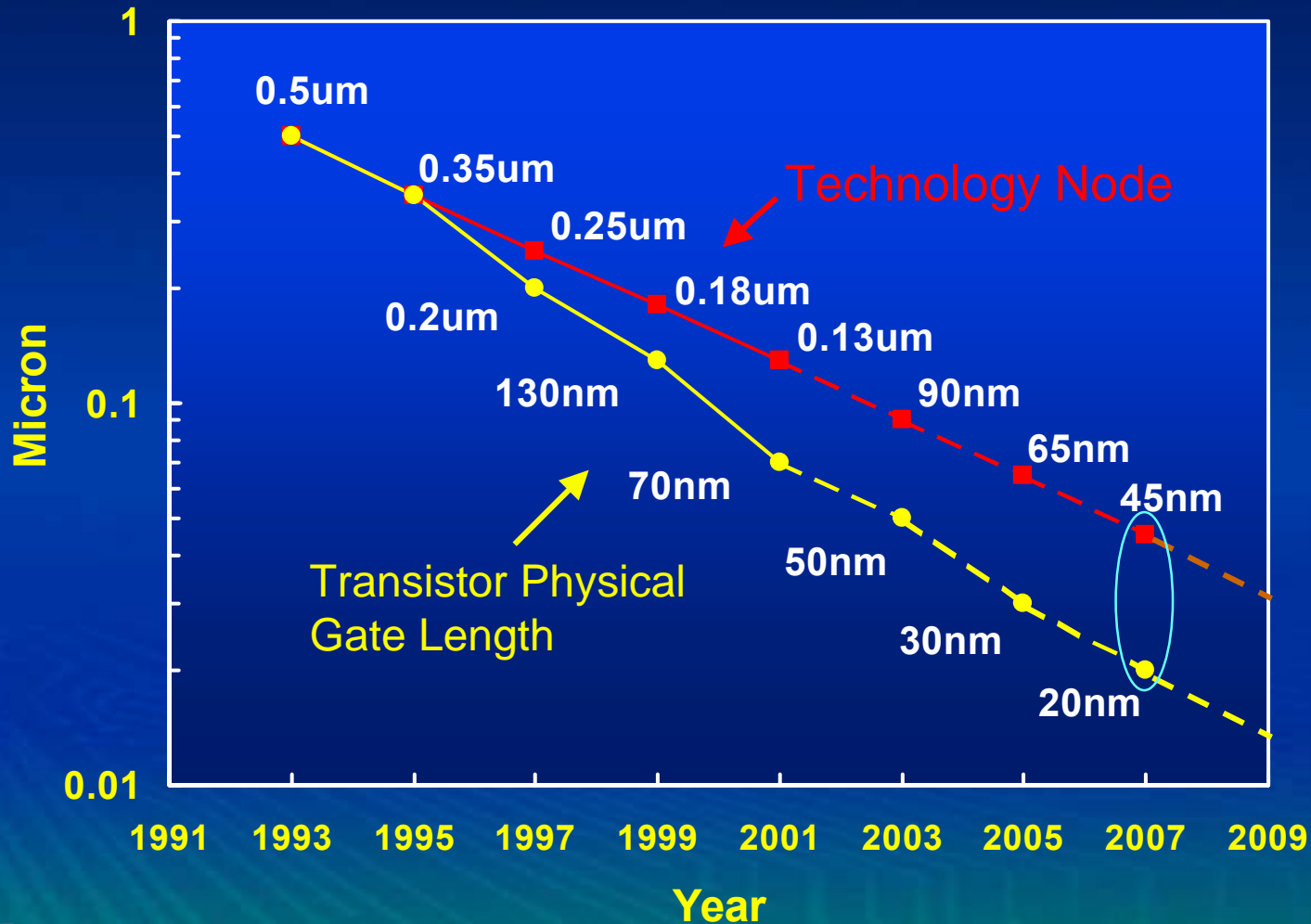


30nm Physical Gate Length Transistor



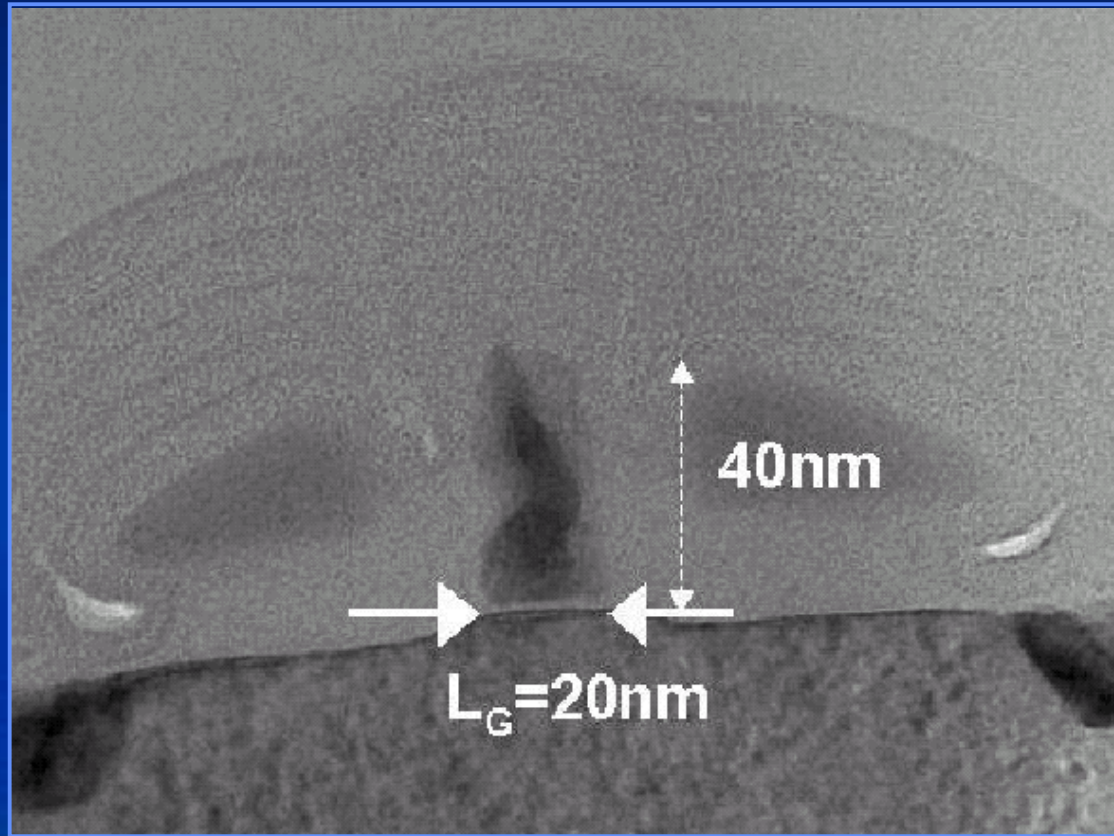
For the 65nm technology node – production 2005

Transistor Physical Gate Length



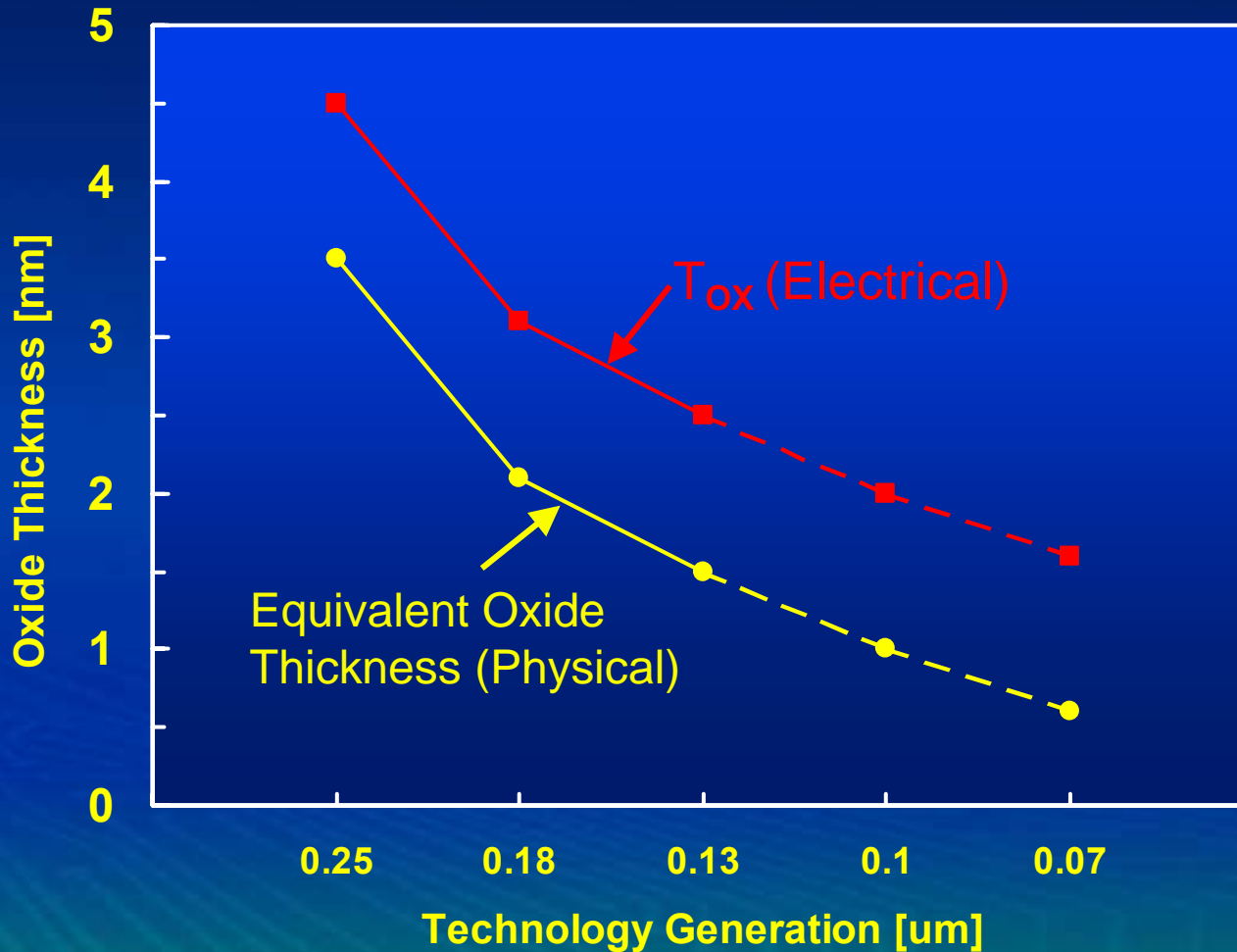
Source: R. Chau, 6/2001

Research Transistor with 20nm Physical Gate Length

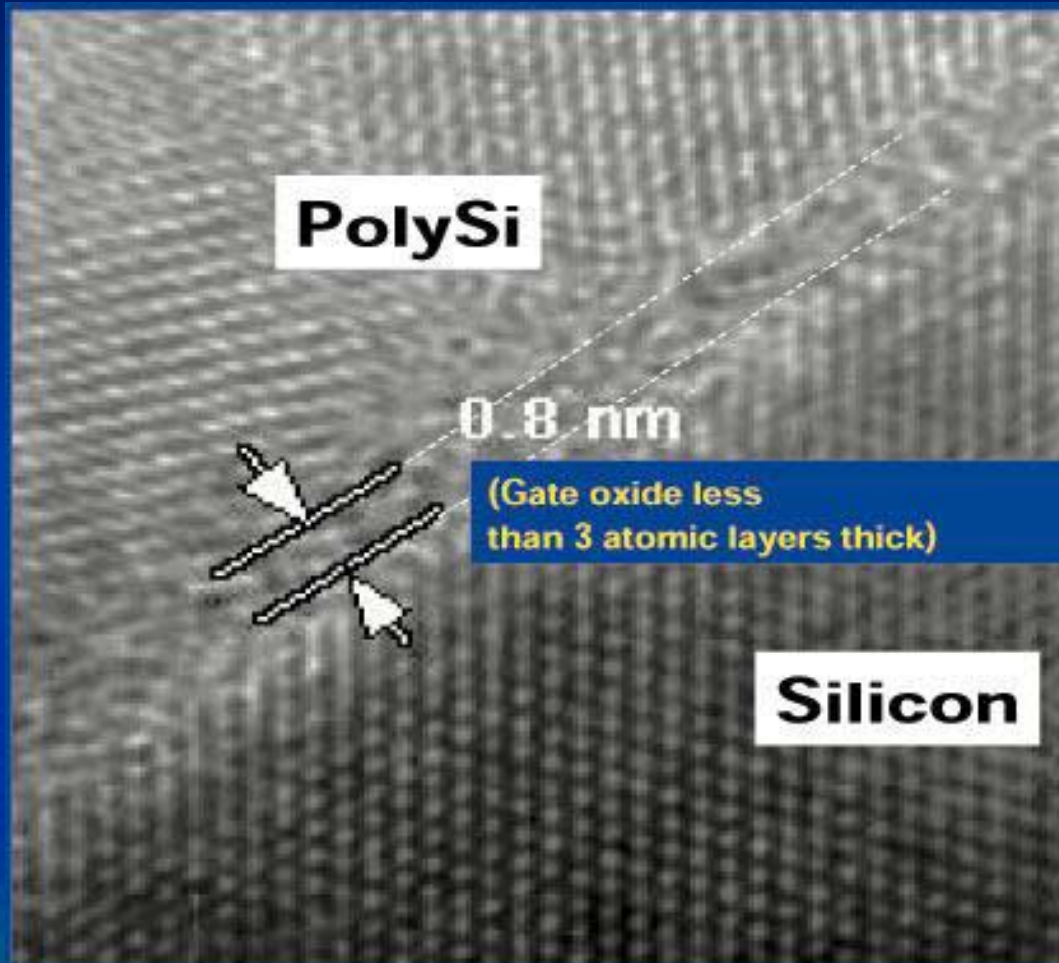


For the 45nm technology node – research phase

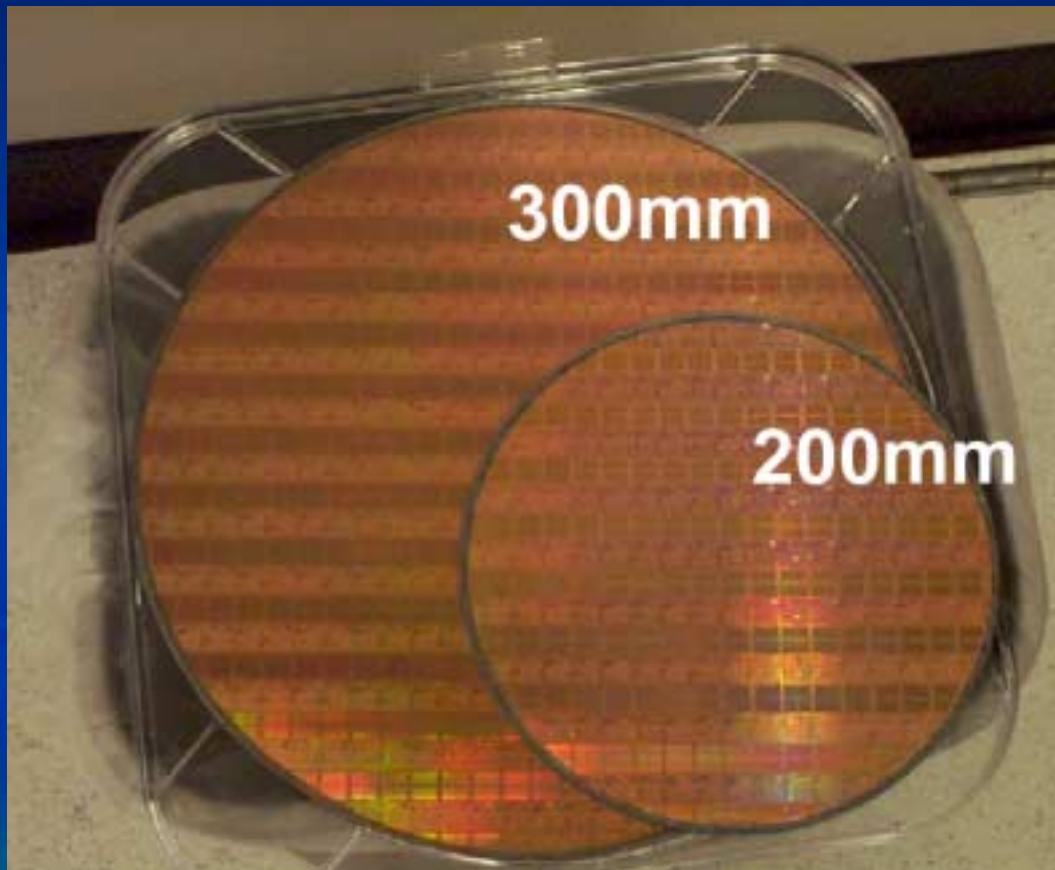
Oxide Thickness Scaling



Atoms-Thin Gate Oxide

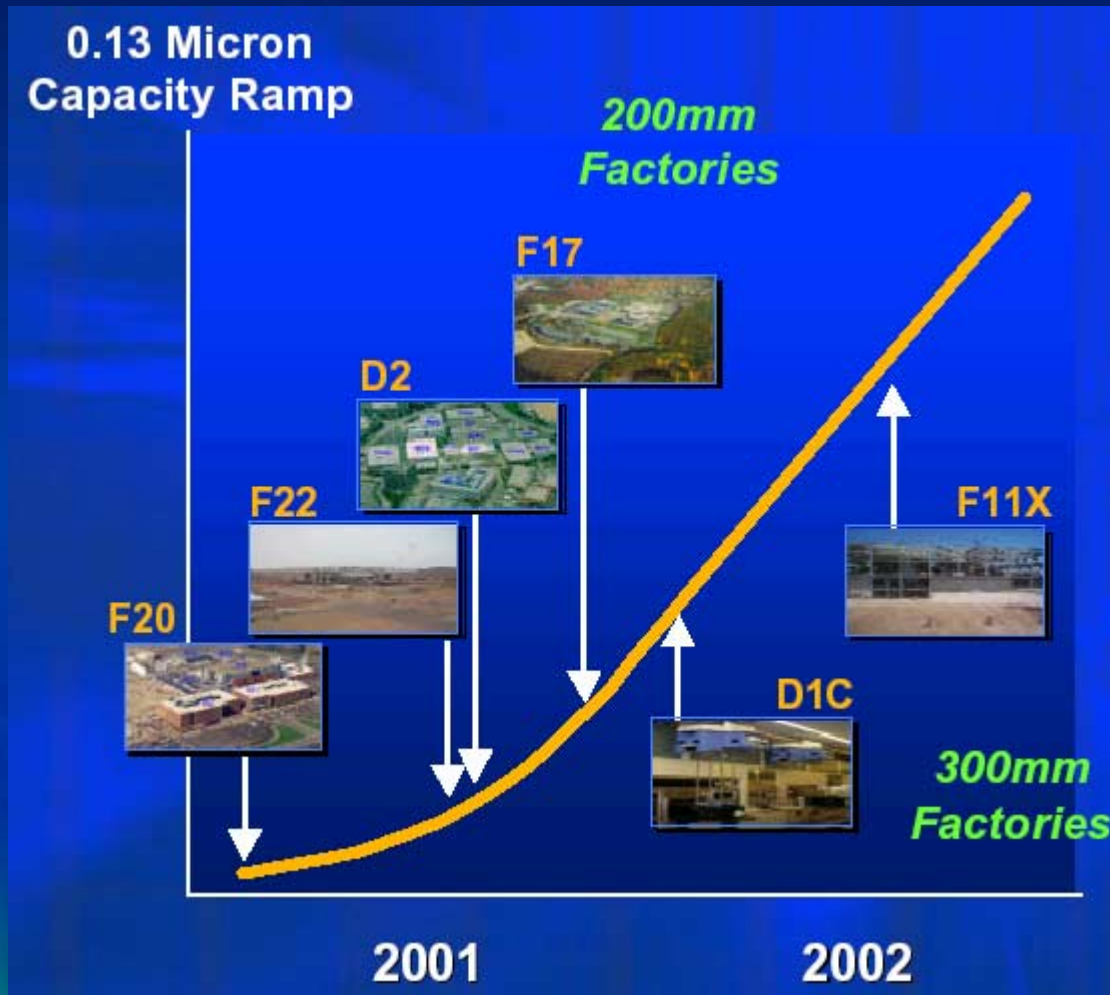


Moore's Law + 300mm Wafers = 4x advantage



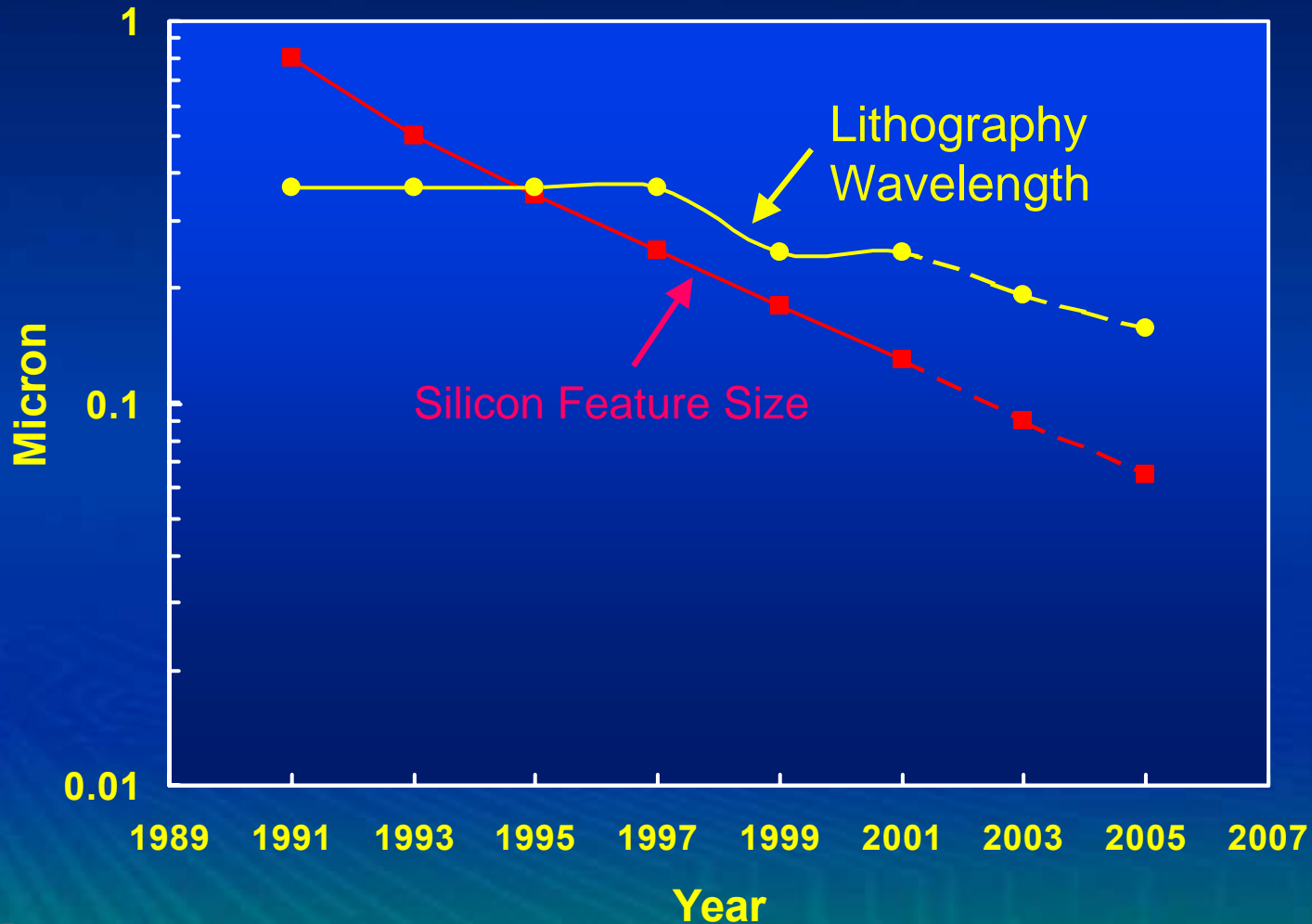
- Moore's Law:
 - From $0.18\mu\text{m}$ to $0.13\mu\text{m}$ = 2x output
- 300mm Wafers:
 - From 200mm to 300mm = 2x output
- Combined output advantage:
 - 4x output

0.13μm Production Ramp



- **Six factories readying 0.13μm production**
 - Plan to spend \$7.5B on capital in 2001
- **Yields and volume exceeding expectations**
 - 0.13μm products have been shipping since May

Lithography Challenges



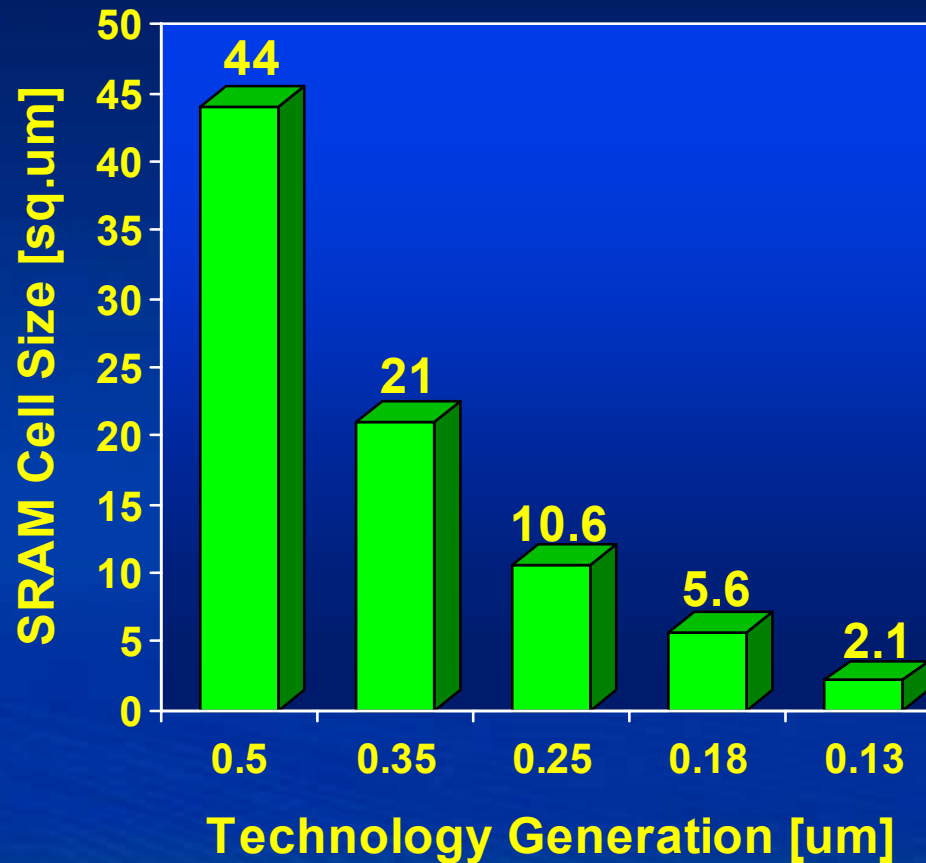
Extreme Ultraviolet Lithography

- EUV lithography uses extremely short wavelength light (20x shorter than today's lithography processes)
 - *Visible light* – 400 to 700 nm
 - *DUV lithography* – 193 and 248 nm
 - *EUV lithography* – 13 nm
- Will be used first in 2005 for critical lithography steps to produce 70 nm patterns

World's First 6-inch EUV ETS Mask

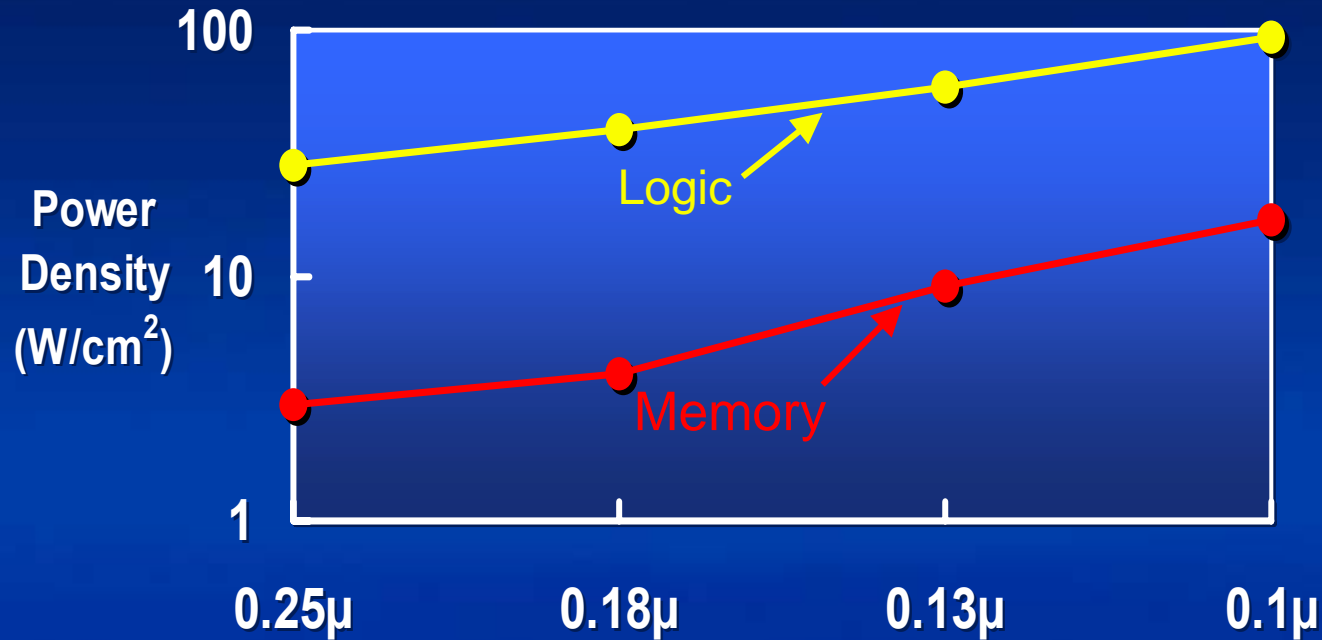


SRAM Cell Size Scaling



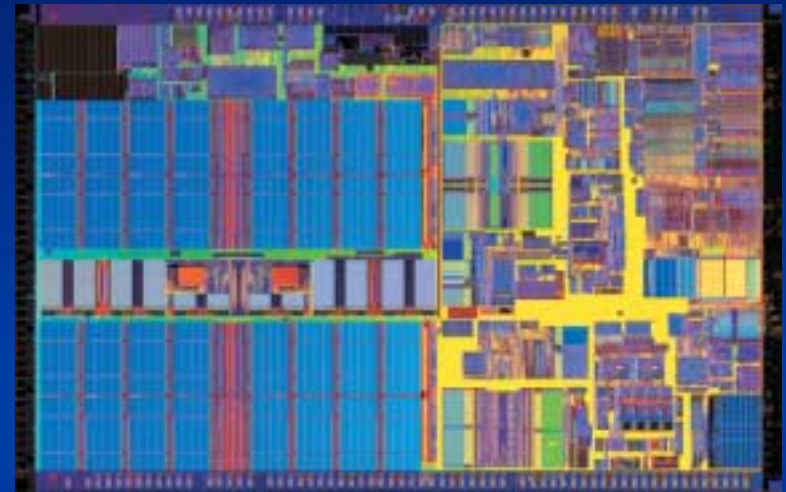
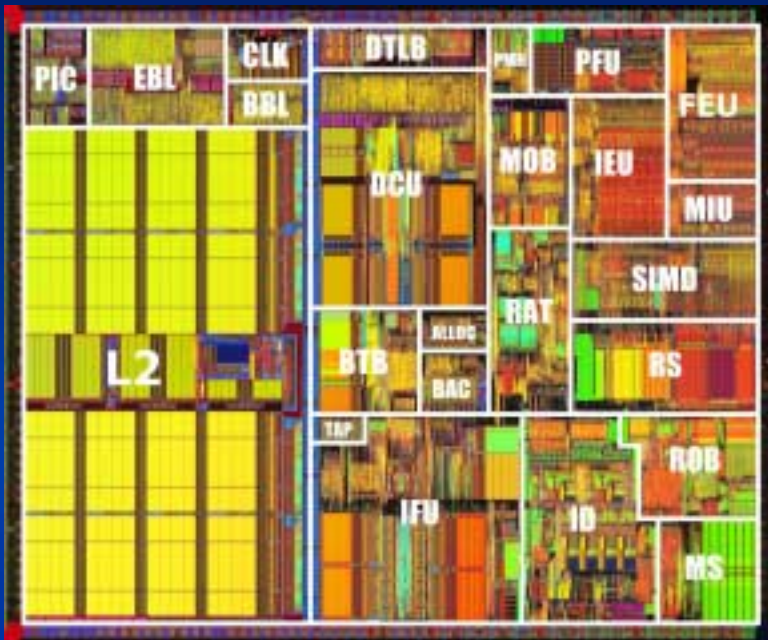
- SRAM cell size will continue to scale ~0.5x per generation

Exploit Memory Power Efficiency



- Static memory has 10X lower active power density
- Lower leakage than logic
- Integrated L2 provides higher bandwidth and lower latency

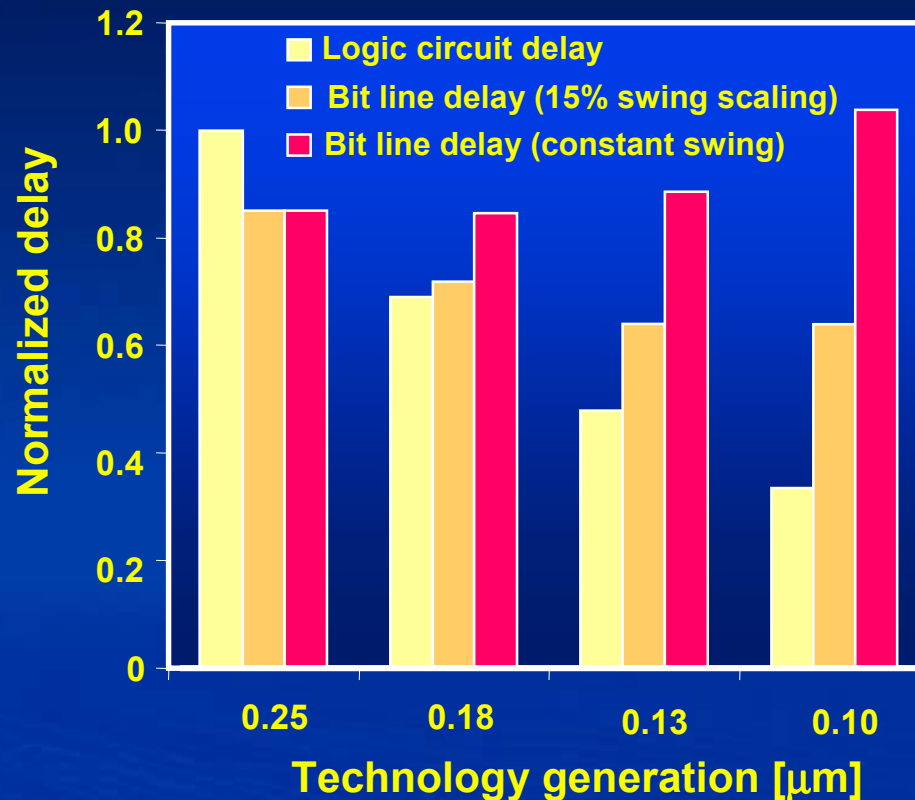
Example: Pentium® III Processor Evolution



- 0.18µm technology
- 256KB L2
- 28 million transistors
- 106 mm² die size

- 0.13µm technology
- 512KB L2
- 44 million transistors
- 80 mm² die size

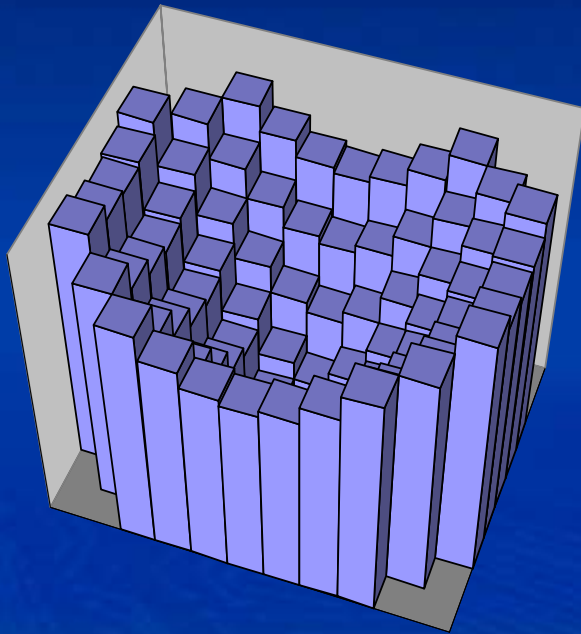
Bit Line Delay Scaling



- Bit line swing limited by parameter mismatch & differential noise
- Cell stability degrades with V_t lowering
- Reducing number of rows per bitline approaching limit

Process Fluctuations

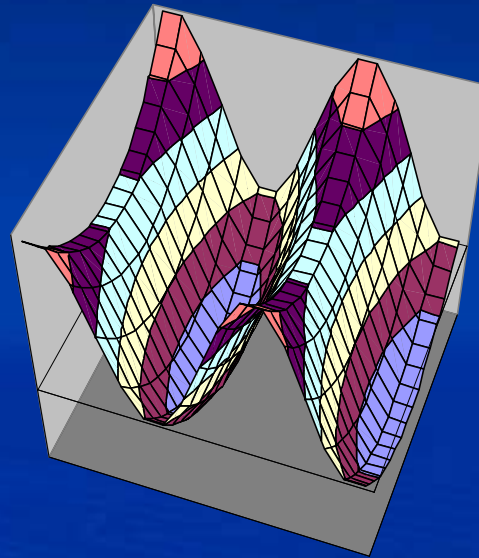
Die-to-Die Fluctuations



Resist Thickness

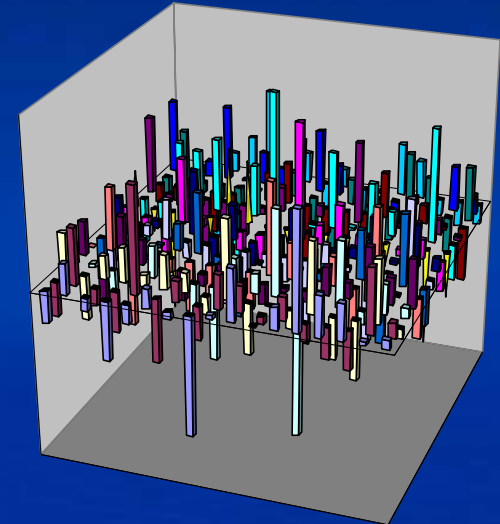
Within-Die Fluctuations

Systematic



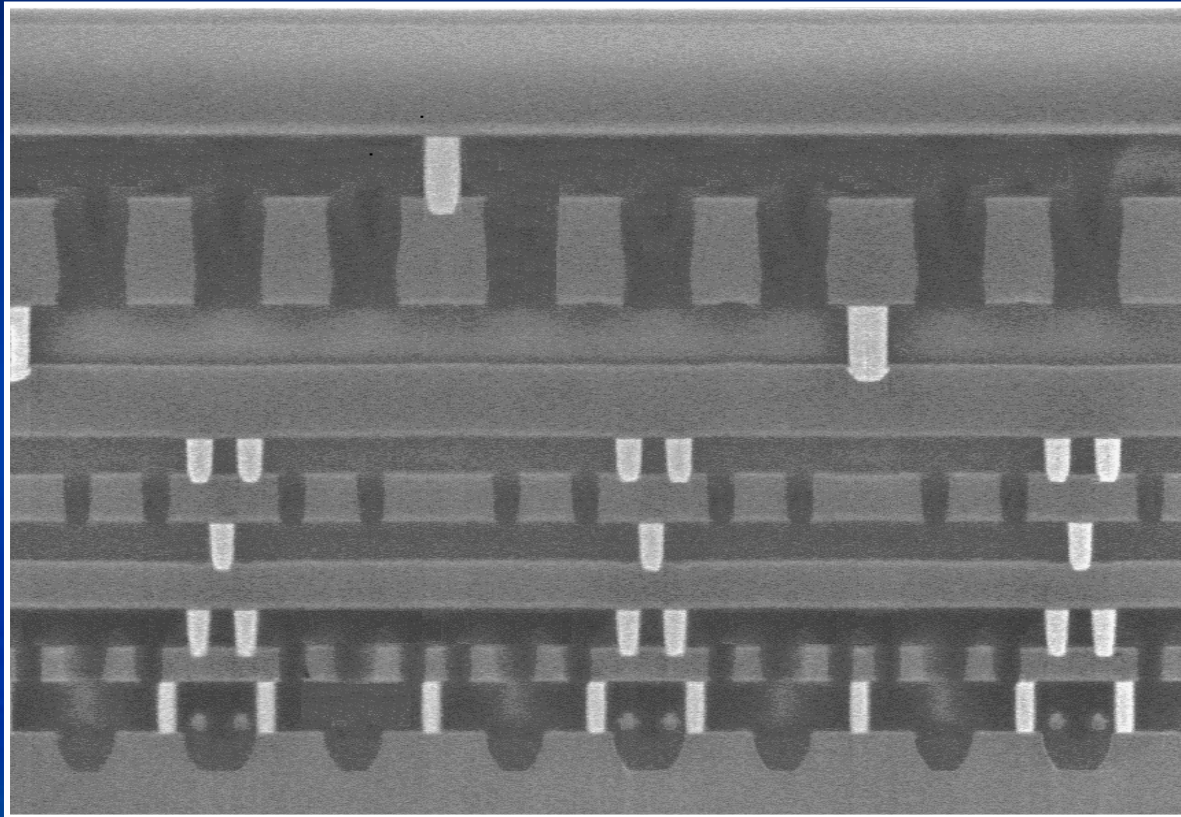
Lens Aberrations

Random



Random Placement of Dopant Atoms

0.18 μm Al Interconnect



Metal 6

Metal 5

Metal 4

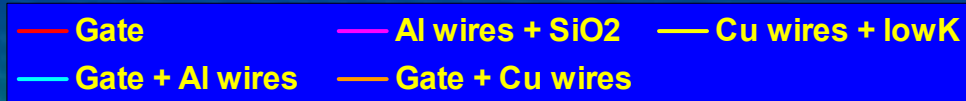
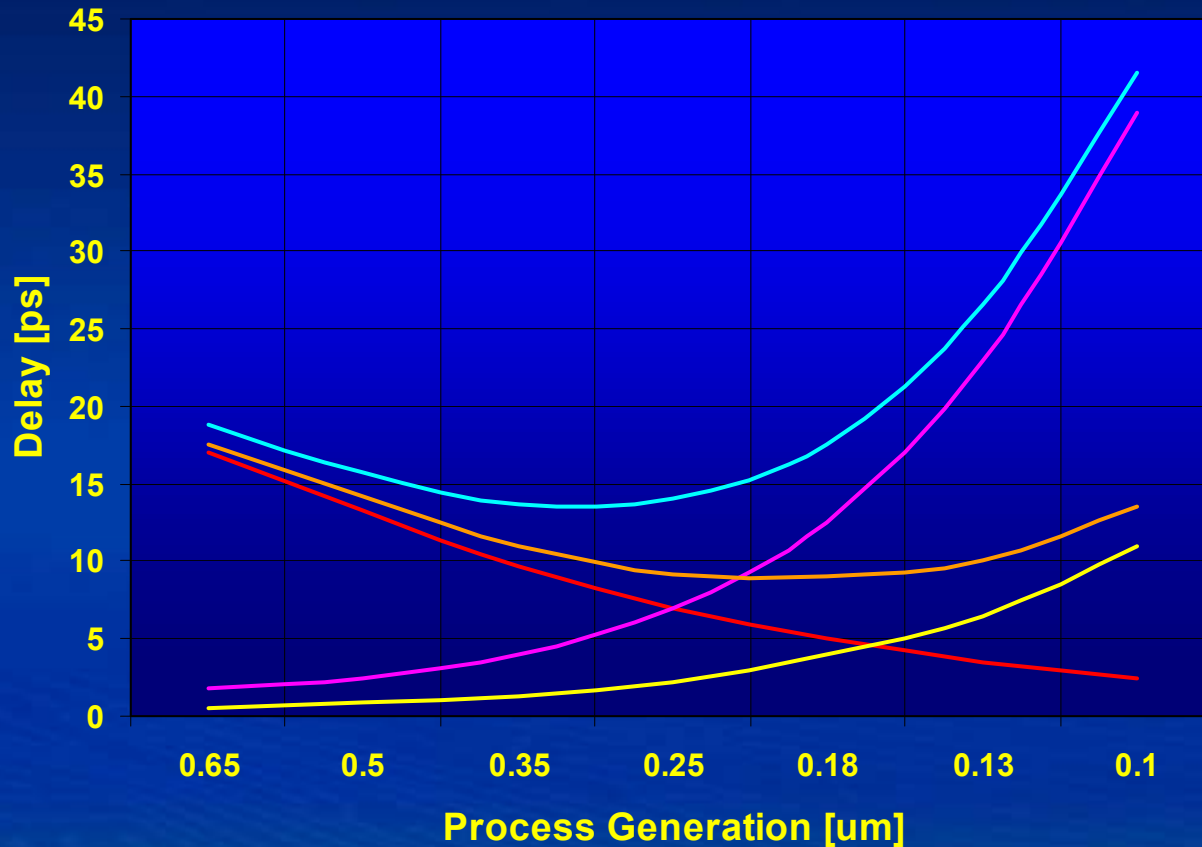
Metal 3

Metal 2

Metal 1

Transistors

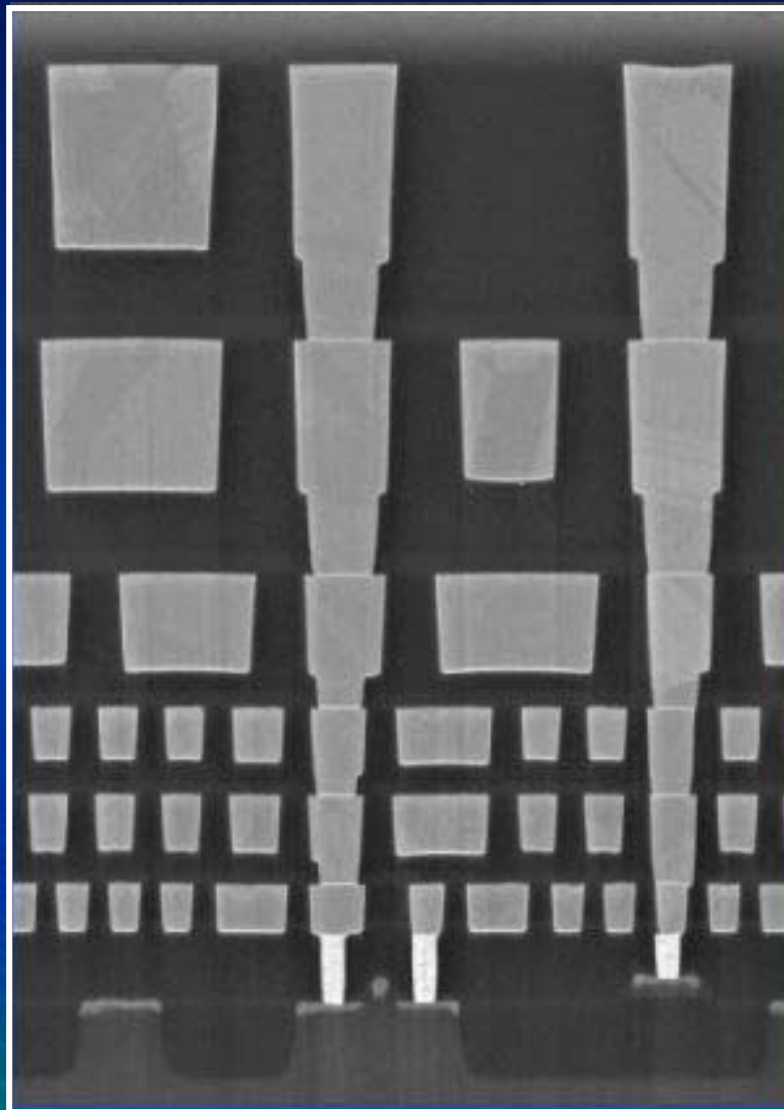
Wires Are Not Scaling Well



Source: SIA NTRS projection



0.13 μm Cu Interconnect



Metal 6

Metal 5

Metal 4

Metal 3

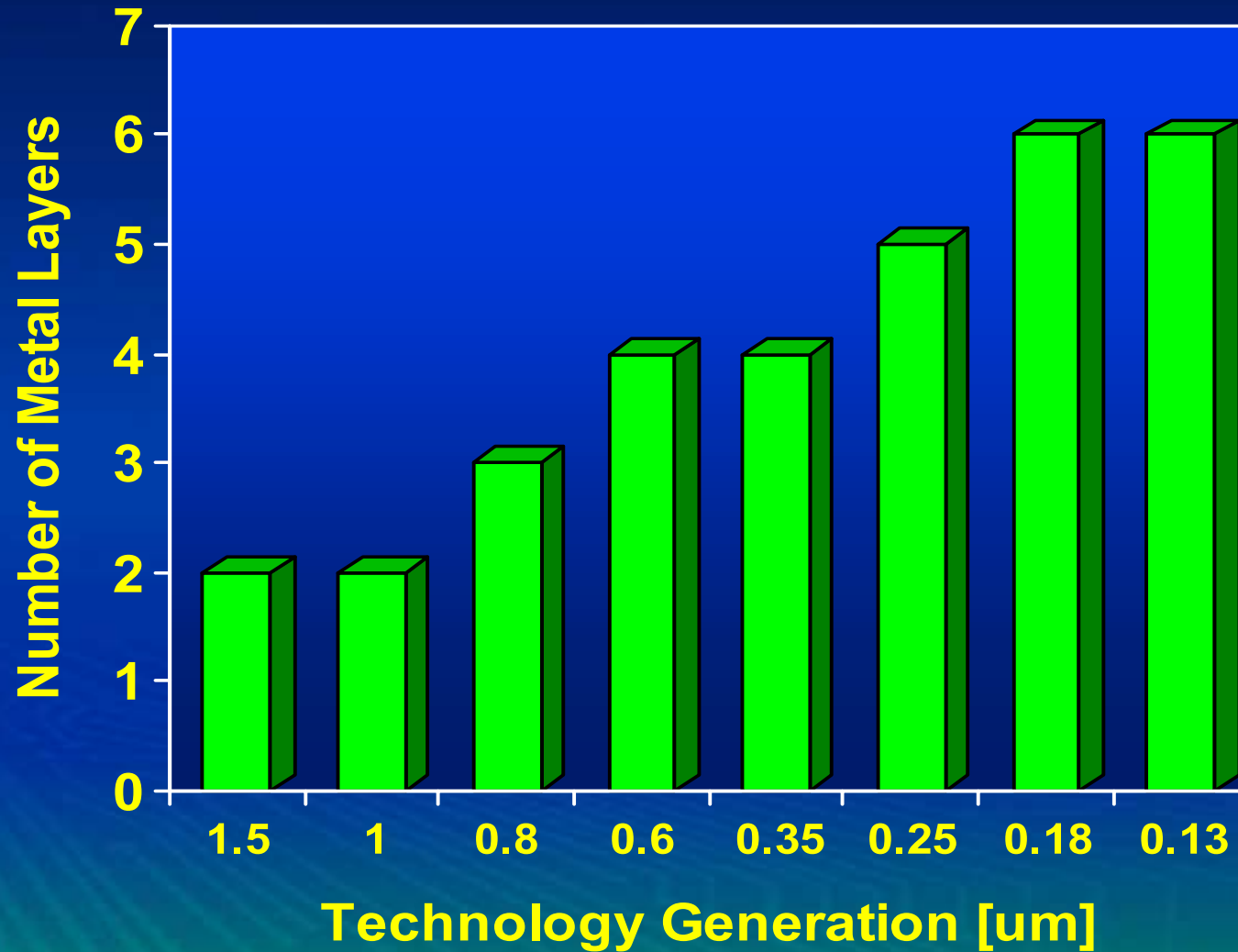
Metal 2

Metal 1

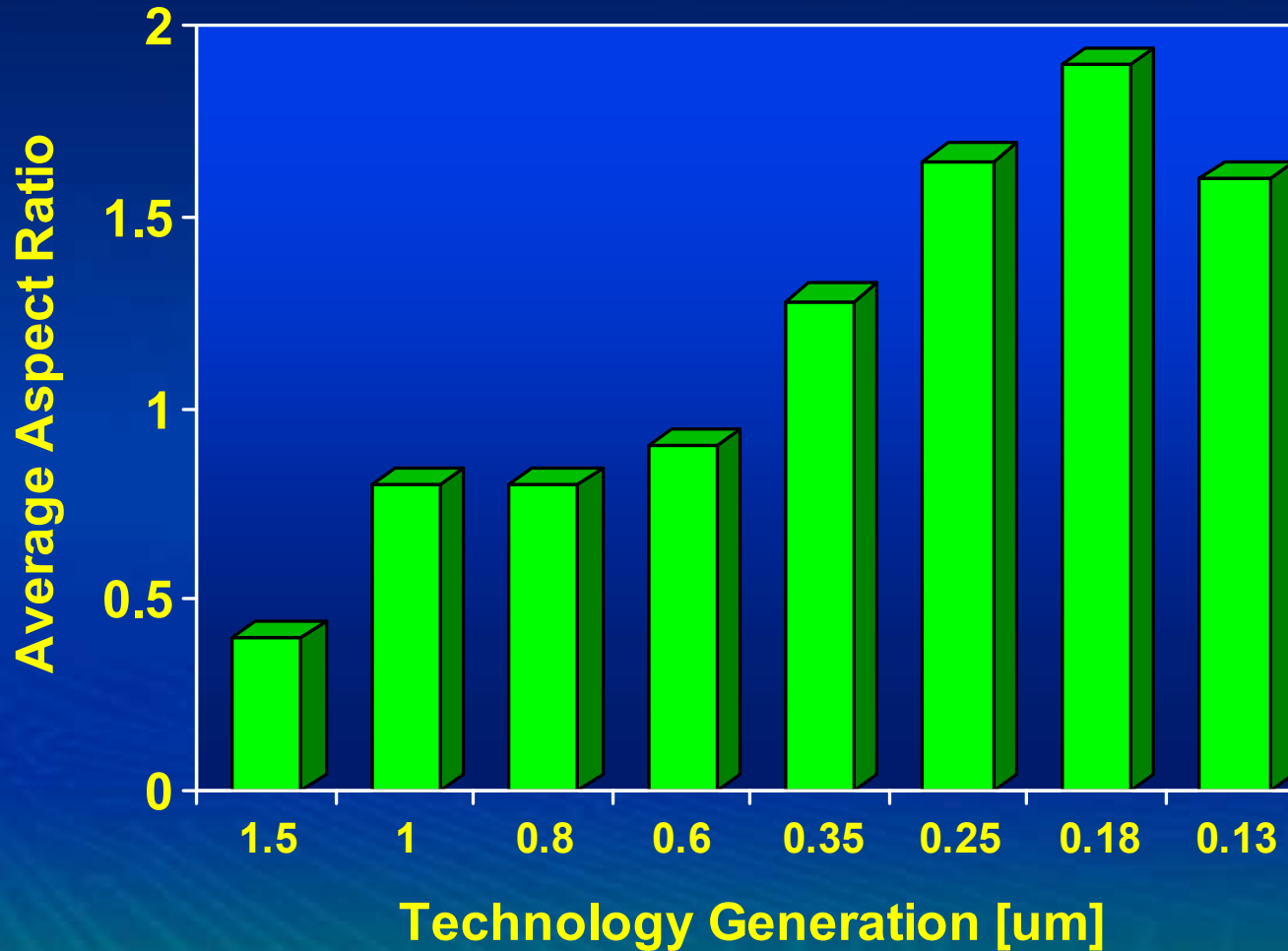
Transistors

Source: S. Tyagi, et.al., IEDM 2000

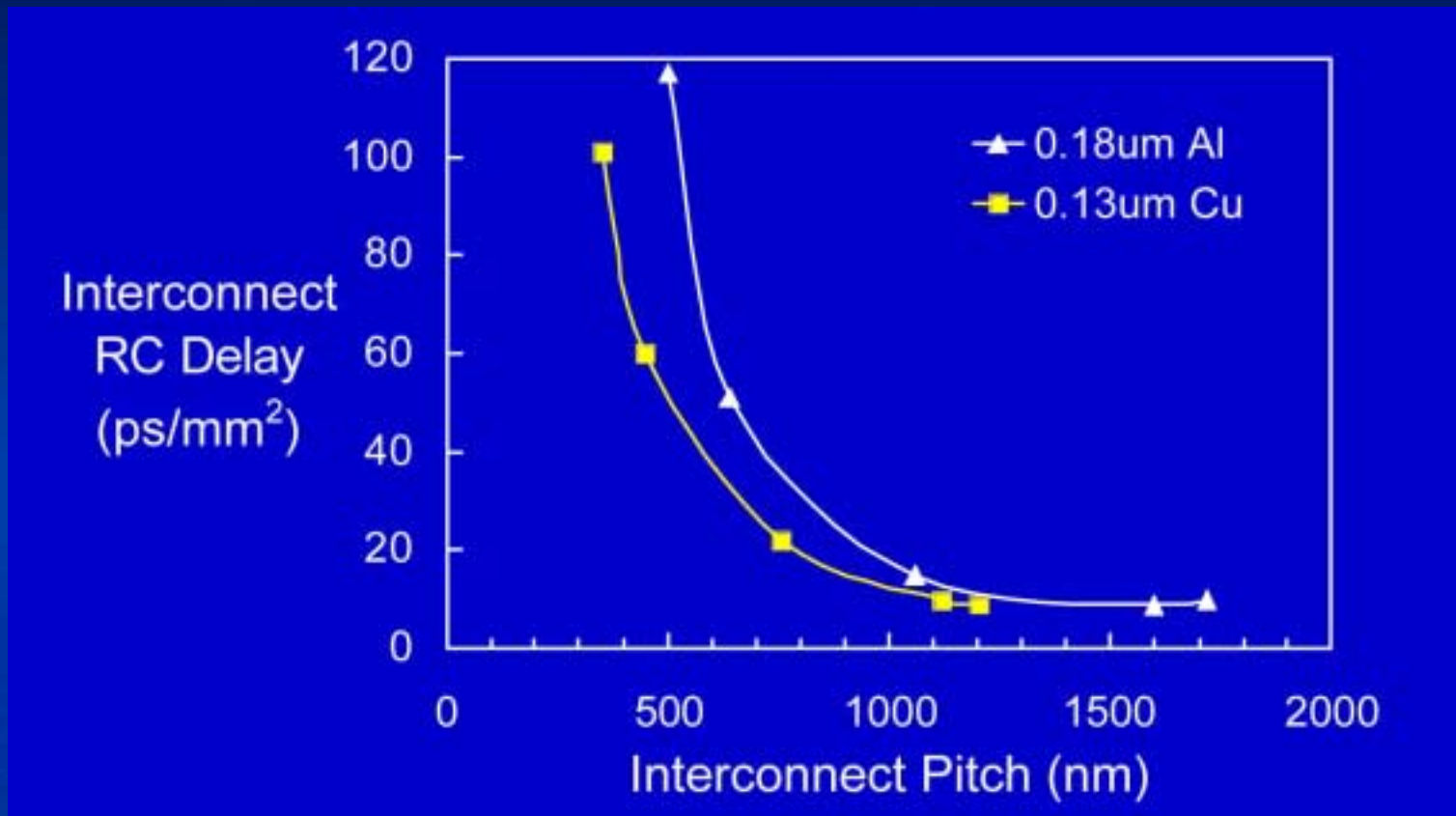
Metal Layers



Metal Aspect Ratios

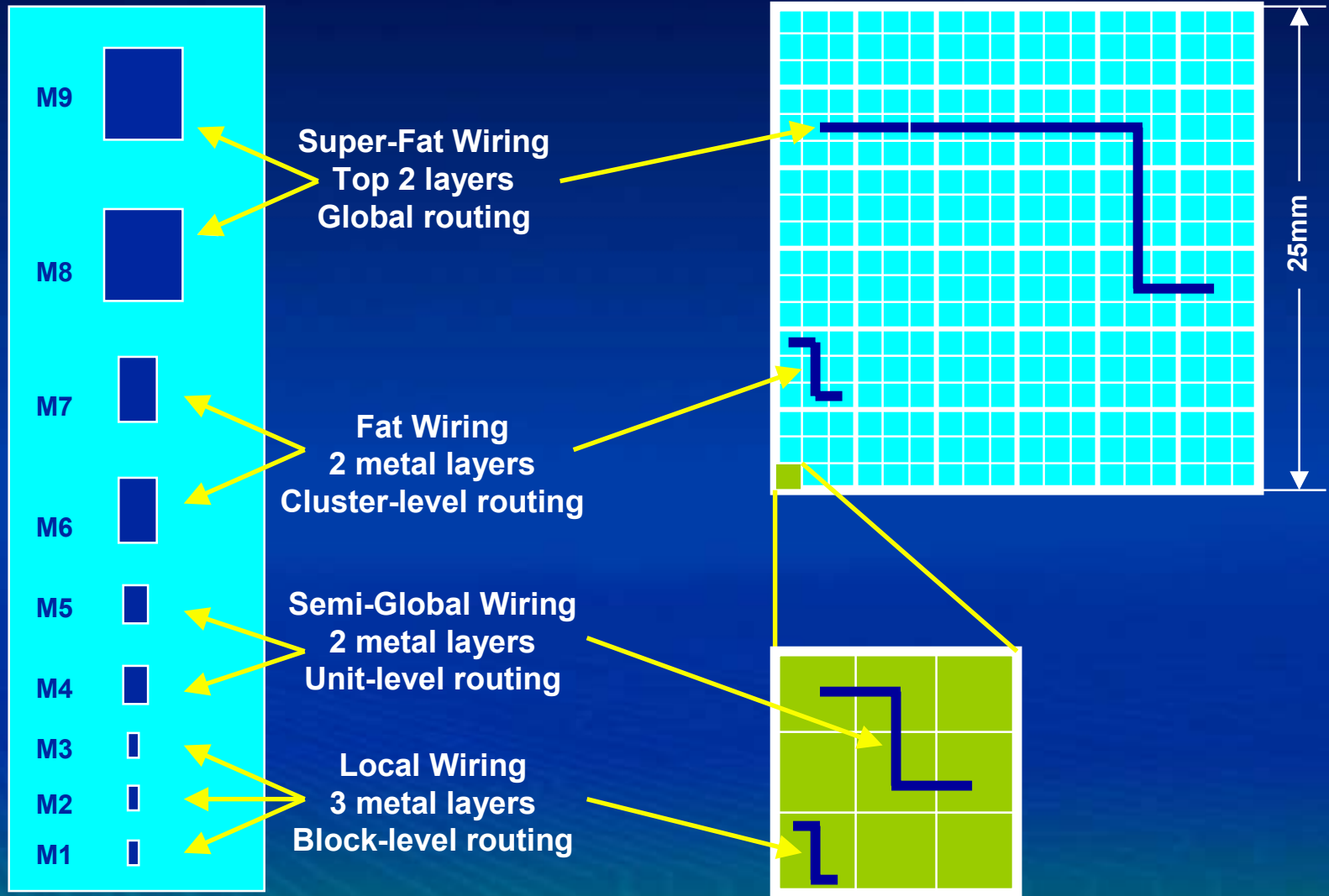


Interconnect RC Delay vs. Pitch

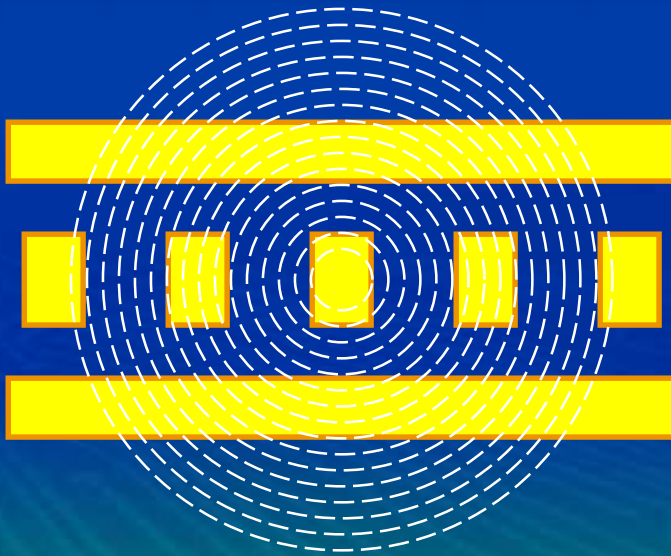
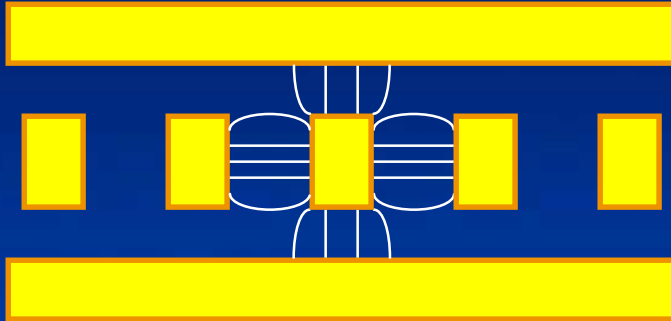


- **40% lower RC delay by using Cu + FSG ILD**

Routing a 70nm Processor

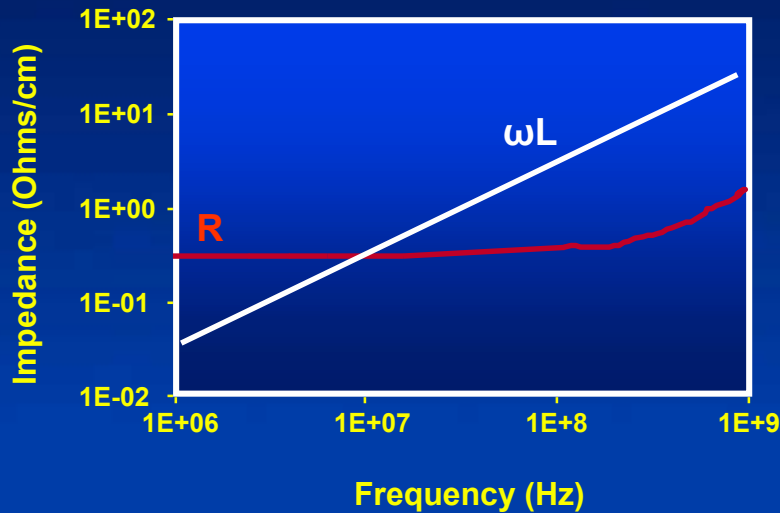


Noise Sources

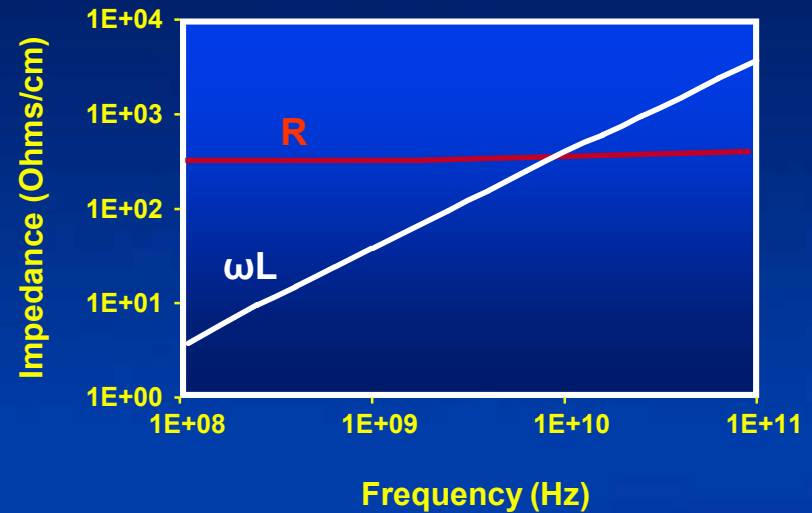


- Capacitive Coupling
 - Due to electric field
 - “Near” field effect
 - Measures resistance to a voltage change
- Inductive Coupling
 - Due to magnetic field
 - “Far” field effect
 - Measures resistance to a current change
 - Frequency dependent

Inductive Noise



PCB (FR4) Signal Trace

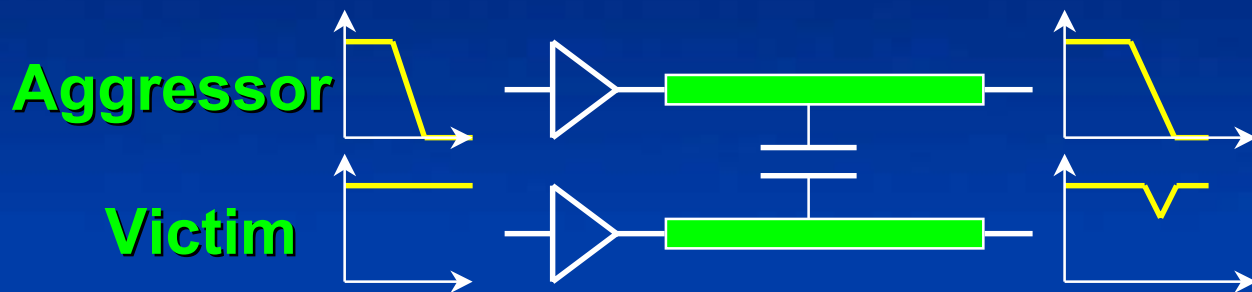


VLSI Metal Line

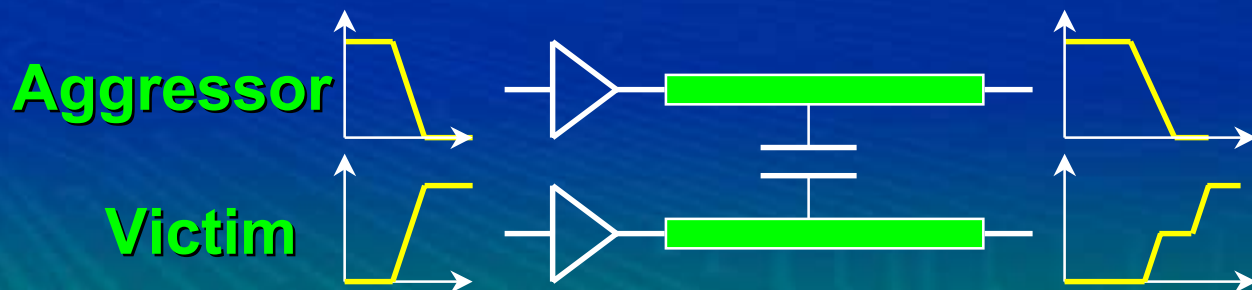
- Inductance of VLSI metal lines is becoming important at operating frequencies above 1GHz

Effects of Capacitive Coupling

- Capacitive coupling can translate into a noise problem



- or a delay problem

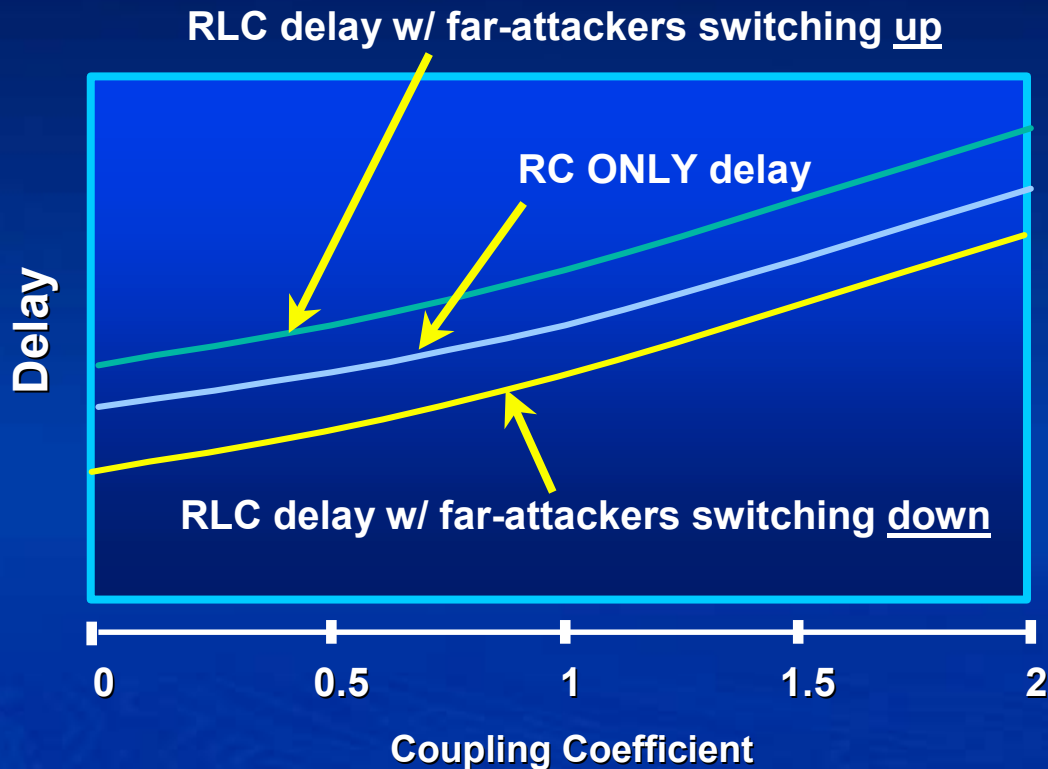


Worst Case Input Patterns



- Near attackers couple mostly by capacitance
- Far attackers couple mostly by inductance
- Lenz's law - a change in current will generate an opposing current which resists the change
- Worst-case switching pattern when near and far attackers switch anti-phase

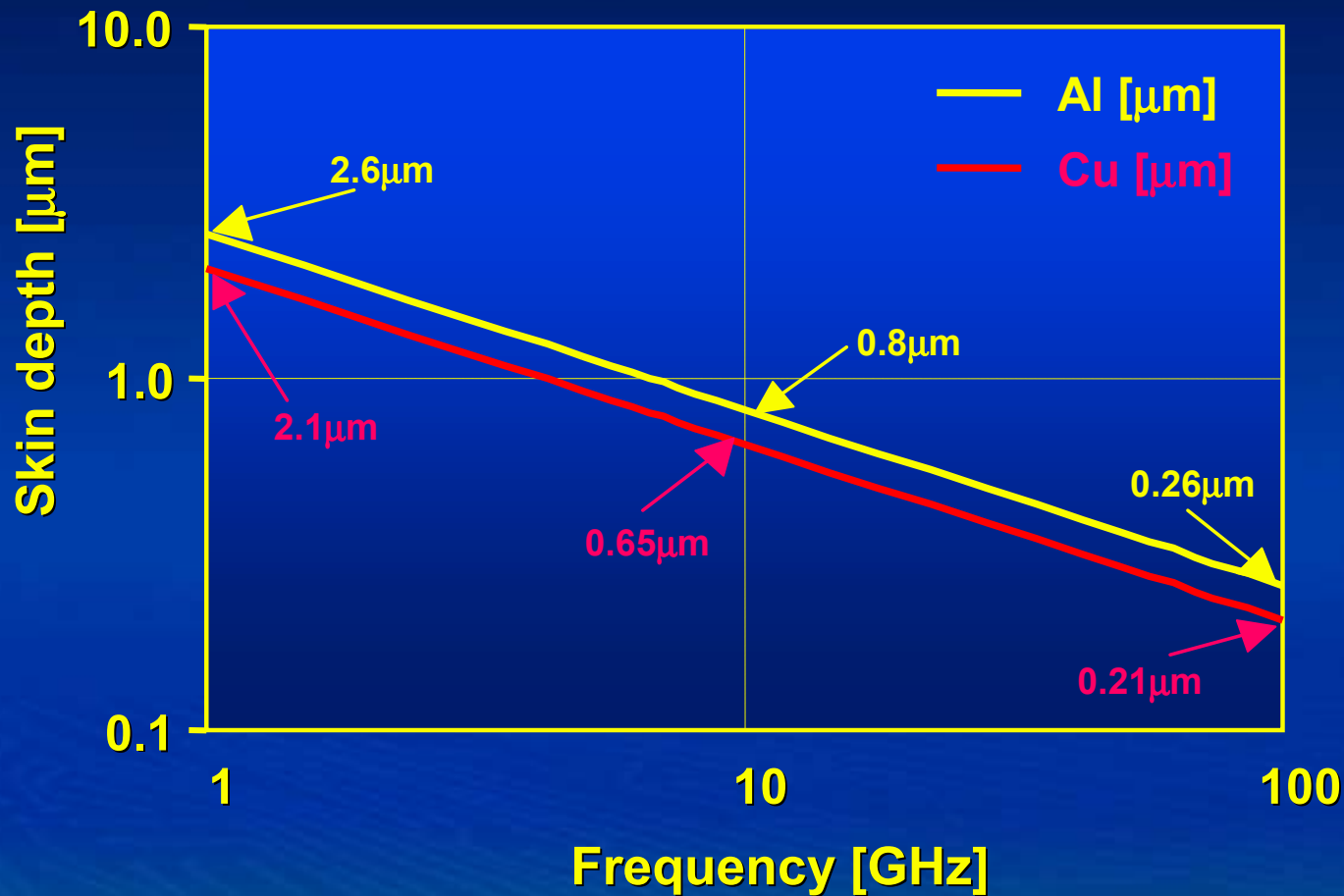
Inductive Noise Impact on Delay



- Capacitive noise effect on delay is modeled by coupling coefficient
- Inductive noise affects delay too
- Inductive noise can also decrease delay

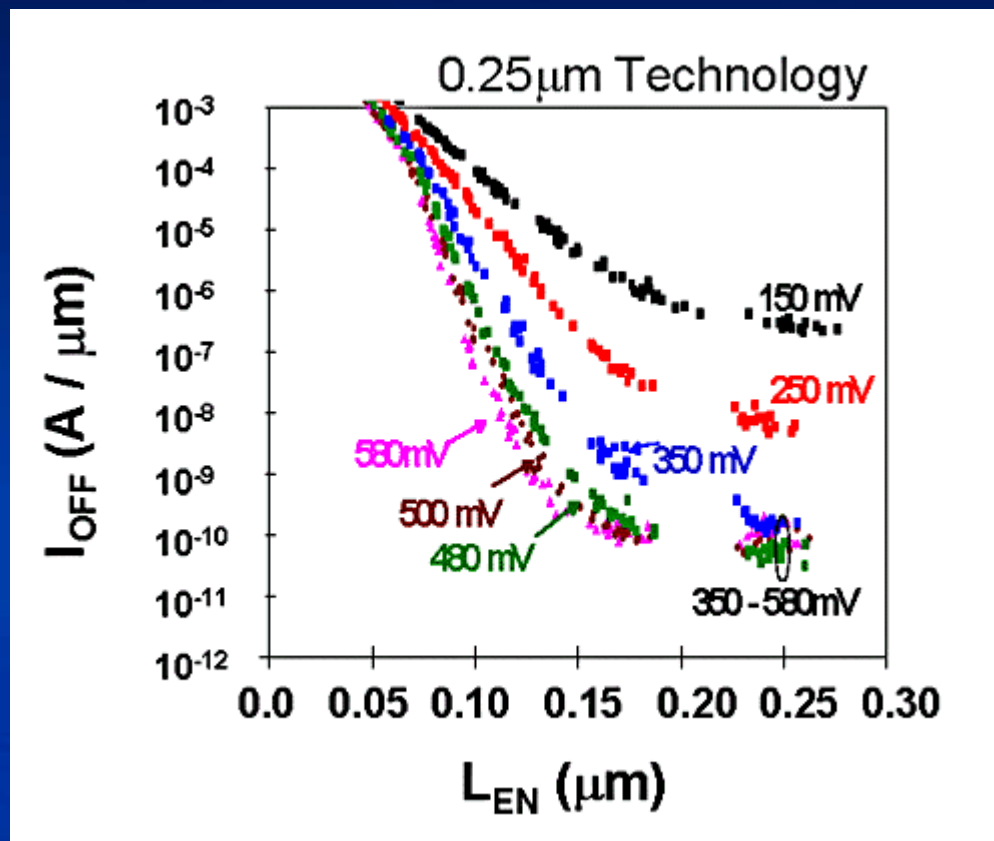


Skin Effect in VLSI Circuits



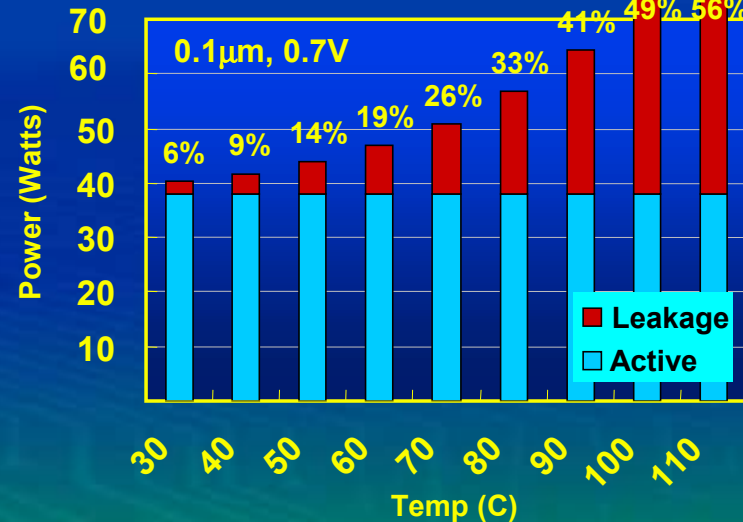
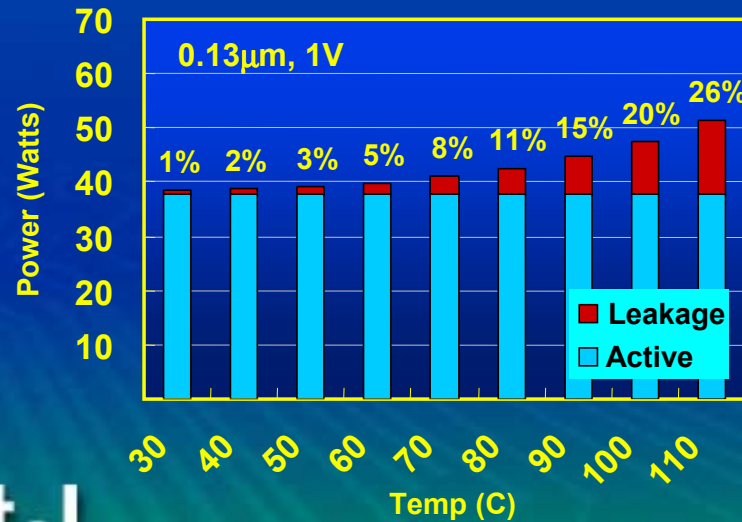
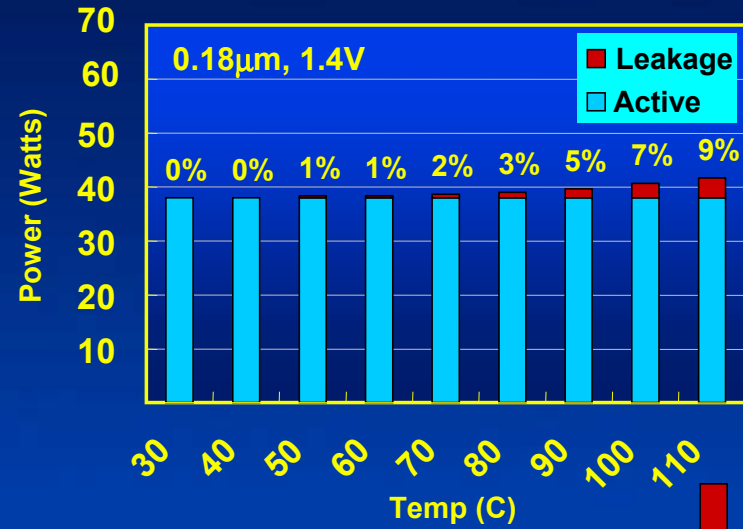
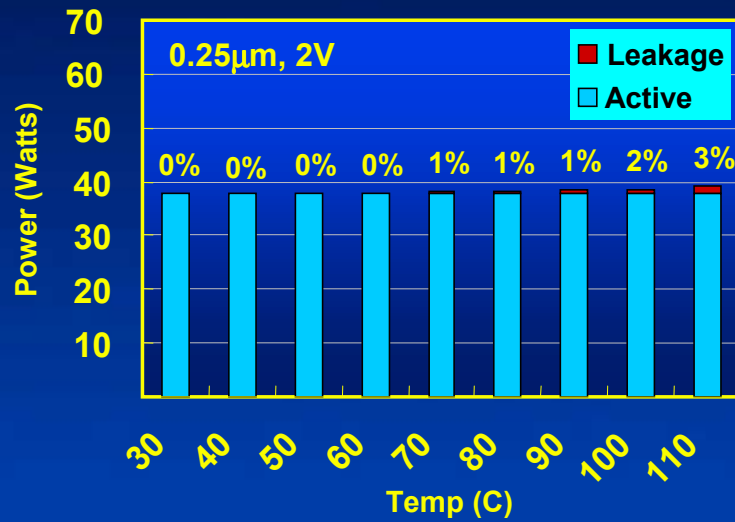
- Edge frequency is 5-9x the clock frequency

Sub-Threshold Leakage

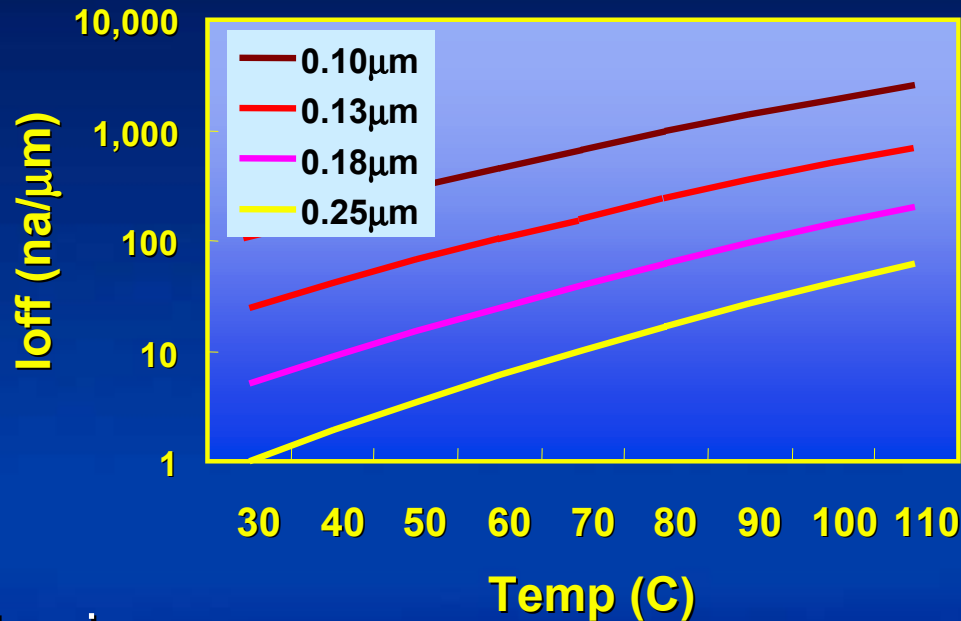


- Sub-threshold leakage increases for lower channel lengths and lower V_T 's

Estimated Power of a 15mm Processor



Leakage Impact



- Design issues:
 - Dynamic circuits may fail
 - Design workarounds needed to guarantee burn-in functionality
- Test issues:
 - IDDQ testing may become ineffective
 - Thermal-runaway problems, especially at burn-in

Conclusion

- We still have not found a fundamental barrier to extending Moore's law
- The challenges are Power and Efficiency
 - Focus on dissipation, delivery, density
- VLSI technology scaling is expected to continue for the next decade