Minimizing EMI & Noise Coupling Among Circuit Regions In Circuit Boards

Valuable concepts that PCB Designers can use immediately for “partitioning” in layout topologies

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The “Process” has a name:

P A R T I T I O N I N G

← OR →

“How to have ‘lively & opinionated’ discussions with ***everyone*** in the company about ***‘what goes where’*** on a circuit board!”

Examples: Purposes of Partitioning

→ Separation of High-Amplitude from Low-Amplitude (e.g. “sensitive” signals or circuit regions) for optimal functionality

→ Containment of specifically unique Spectral Regions

→ Protection of analogue circuits from digital spectra intrusion (S/N Ratios)

→ Exclusion of EMI Emission from interface – interconnecting cables

→ Rejection of extraneously applied fields or currents (susceptibility-immunity factors) from functional intrusion

Partitioning Initially Requires A Recognition Plan

→ Recognition plan is a subset part of the system-product "Common-mode Architecture"

→ "Common-mode Architecture" is a derivative of the system-product electrical / functional block architecture

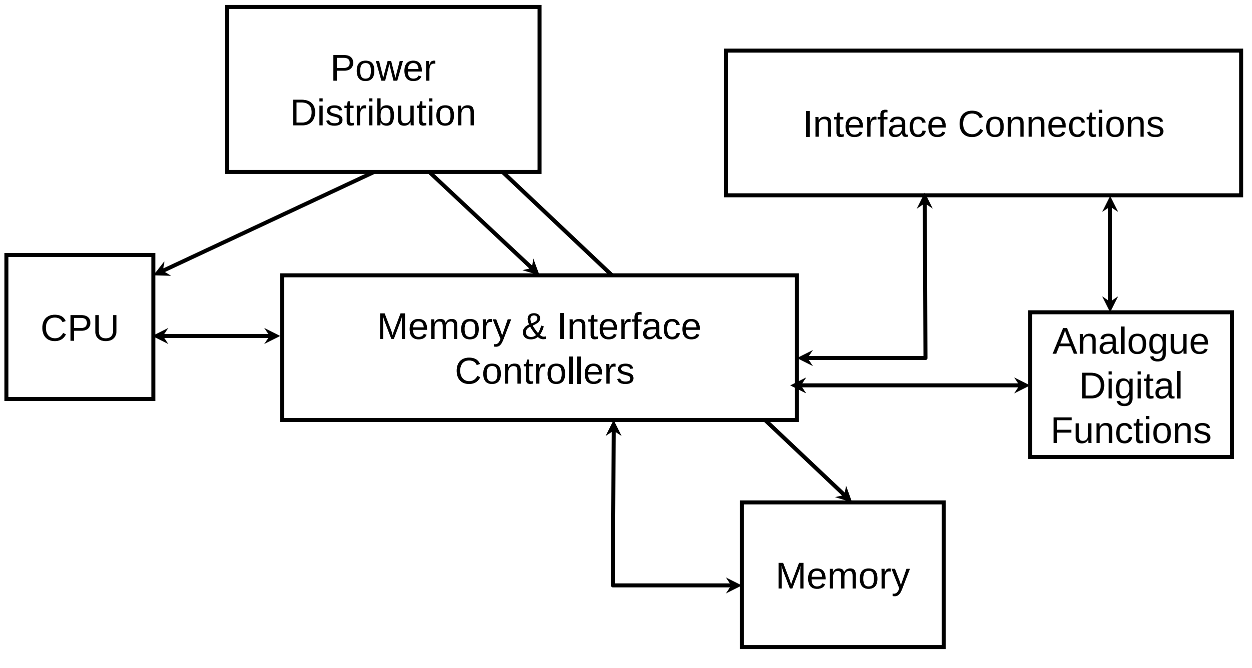
→ System-product functionality is identified initially in "block" structures

→ "Block" structures set the pattern approach initially for X-Y Axes topology, followed by Z-Axis implementations.

→ ***Inspection:*** *What are the "threat" SOURCES and HOW will they couple to VICTIM "receivers"?*

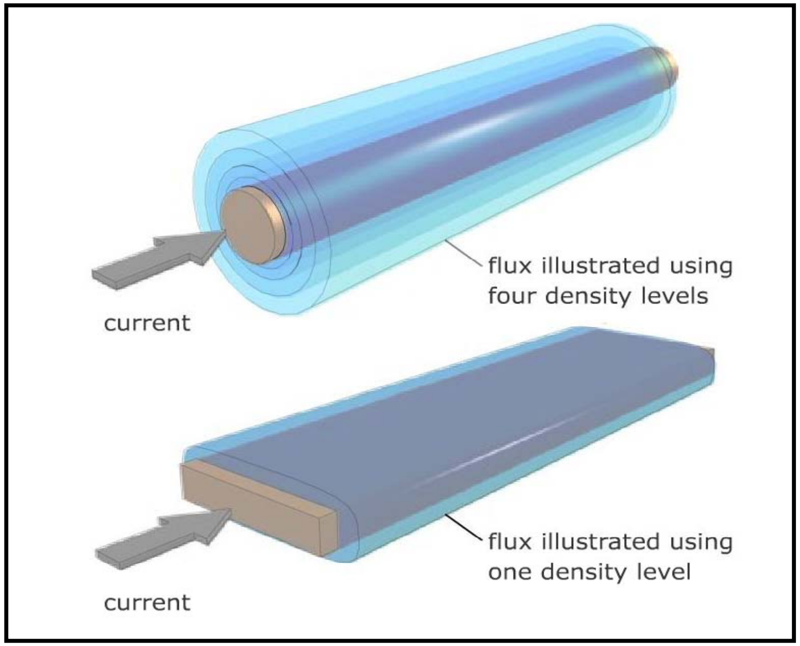
Electrical "Block" Architecture Initiates The "Evaluation" Process →

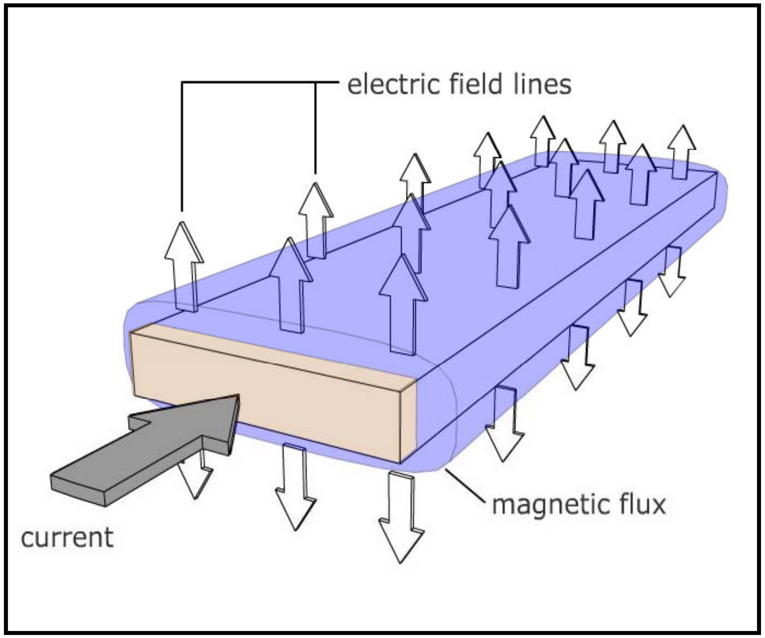
Is this enough?



Task: Identification of "Threat Sources" and "Victim Receivers"
GOAL: EMC (Self-compatibility)

Typical Prevalent Recognitions Might be Limited to Flux and Capacitance Coupling of Signals





What About Peak Transition Current Cross-Conduction *POWER* Surges?

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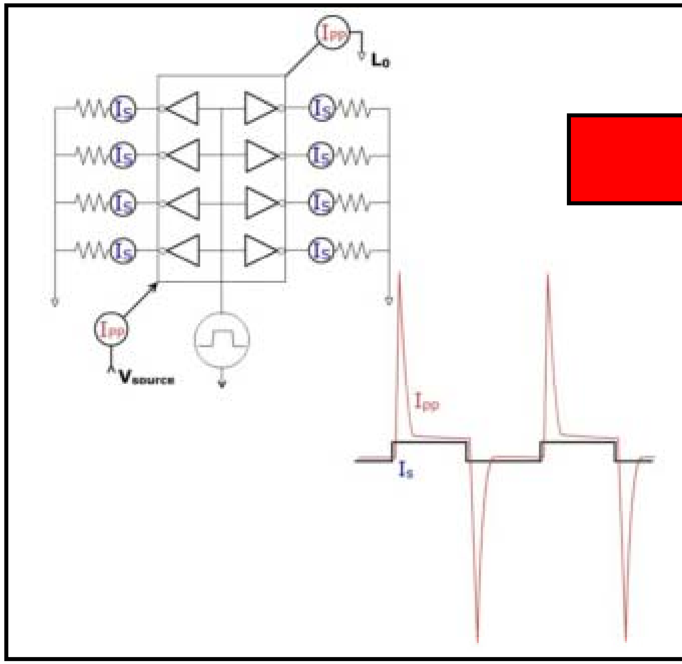
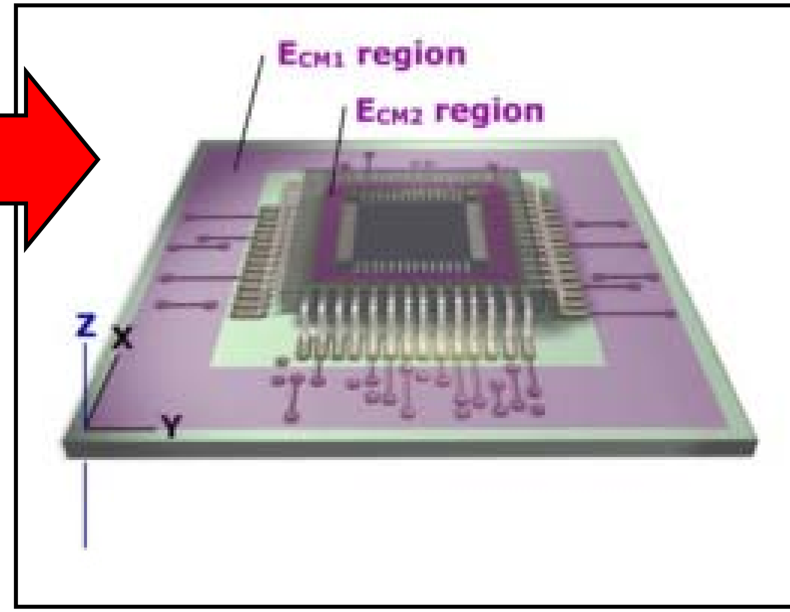
Inspection of “Threat” Sources: Recognition of Predominant Common-mode Losses & Potentials in the X & Y Axes





Peak-Current Cross-Conduction Surges With Circuit Devices……….

……Excites Common-mode Fields and Loss Potentials From Patterned Layout Inductance Surrounding Devices

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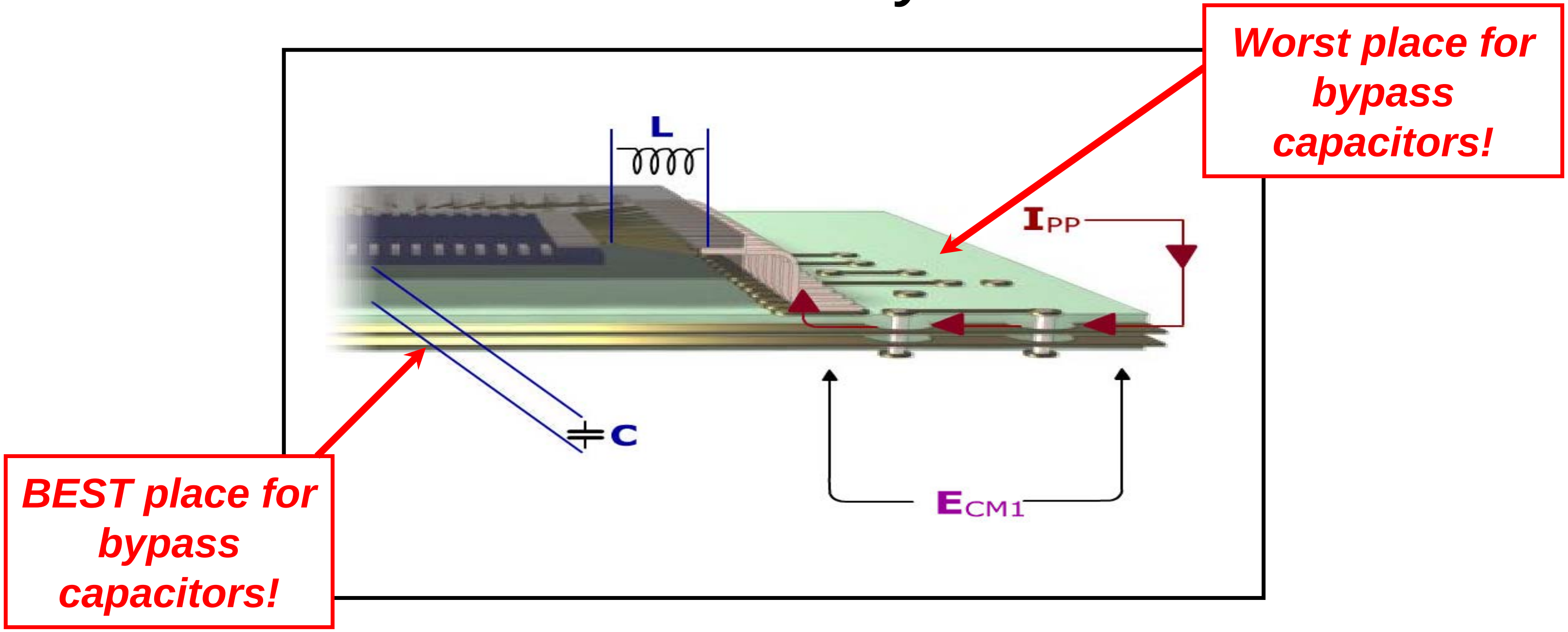
Patterned Layout Inductance: A "Phased Array" Effect



Peak-Current Cross-Conduction With Circuit Devices → *Surges* Across "Via" Apertures (at each rise and fall time).

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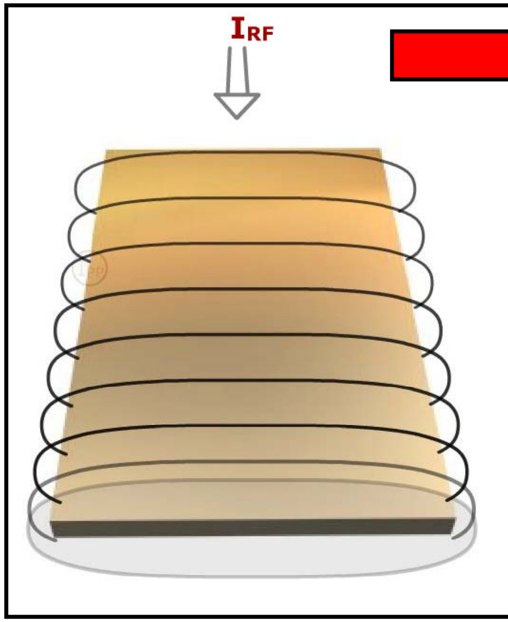
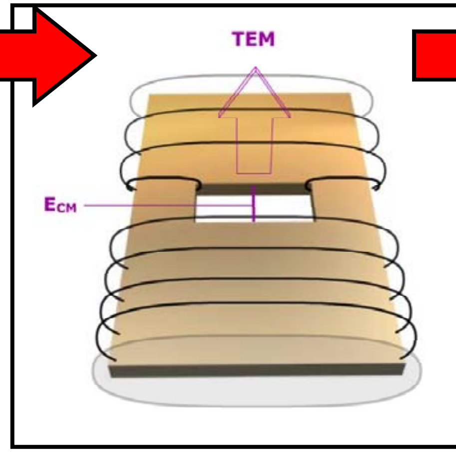
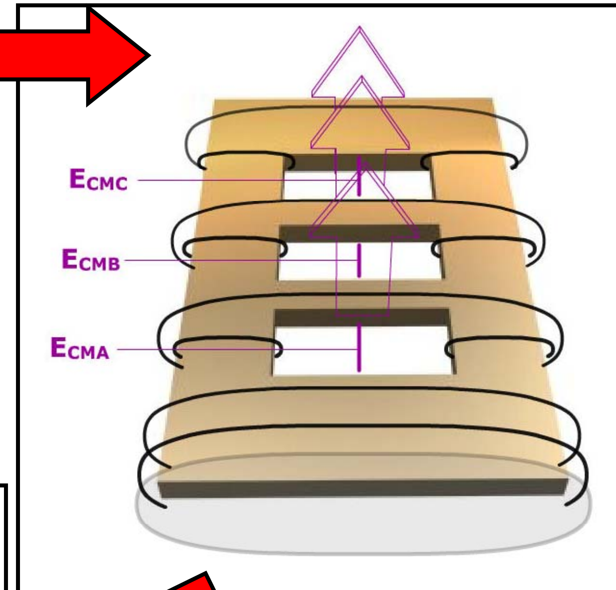
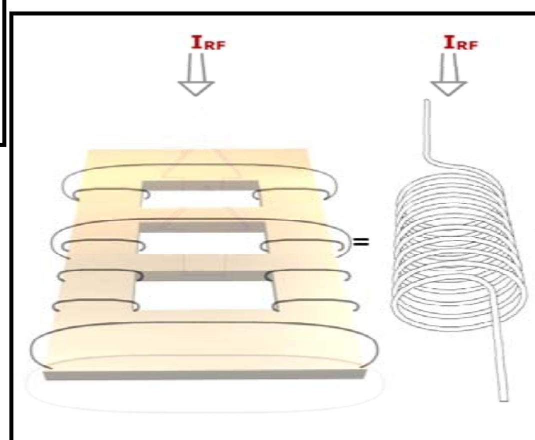
The “Patterned Layout Inductance” - Formation Sequence -







RF Common-mode Current in a contiguous plane has comparatively low loss……..



…….but as Apertures (escapes) are added, the cumulative losses progressively increase.

KEY DESIGN CONSIDERATION: WEB TO APERTURE SIZE RATIO – VIA HOLE DENSITY!

Blind Vias will dramatically reduce “patterned layout” inductance!

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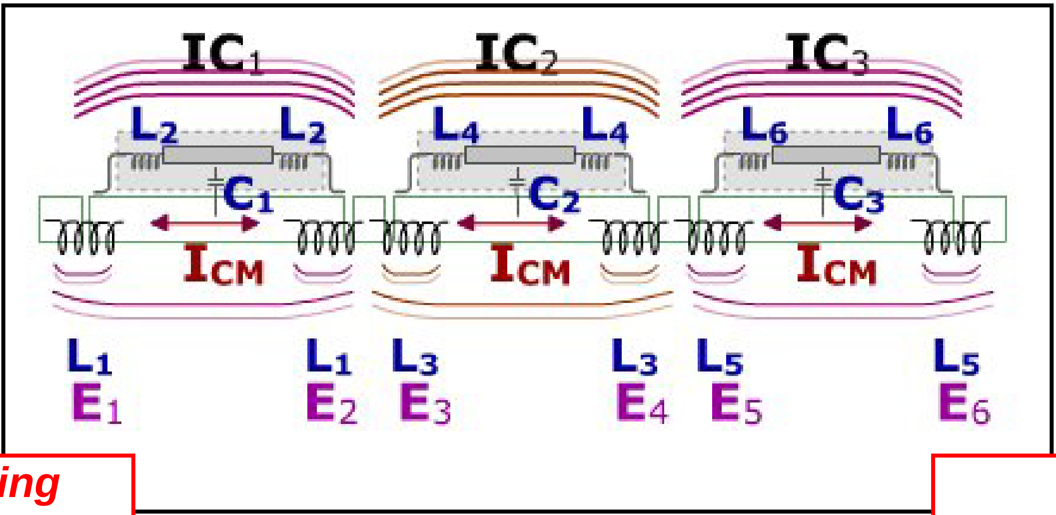
Distributed Common-mode Sequence

Examination of "Common-Mode Fields" From Excitation Of Patterned Layout Inductance Across 3 Axes



Can anything increase the harmful coupling distribution of these fields?

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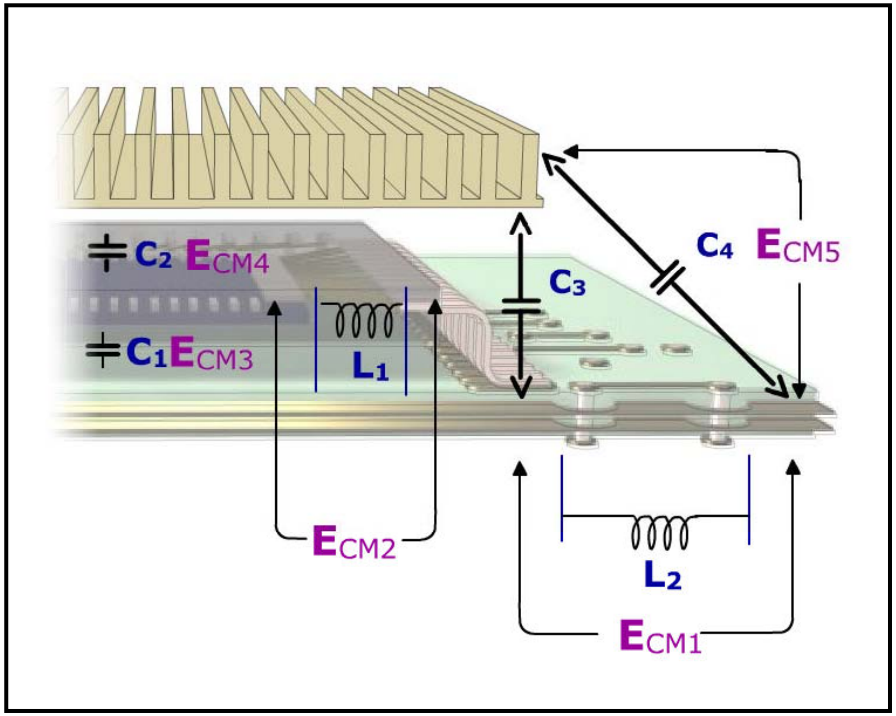
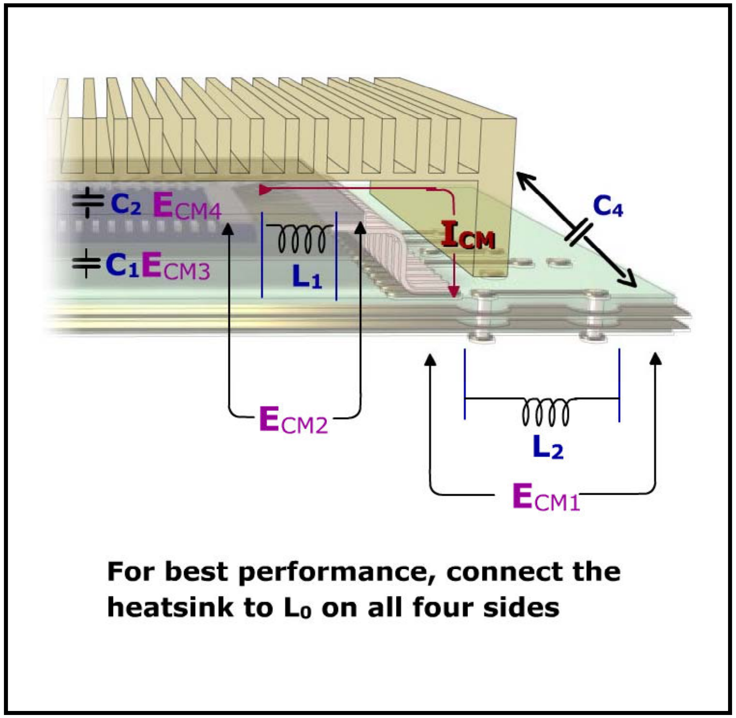
YES! Coupling of Fields → into MECHANICAL structures

What Happens When HEAT Sinks Are Added?!





Increased Fields and Coupling Probabilities Happen…………

………Unless the CURRENTS CAUSING the FIELDS are CAPTURED back to IMAGE Return Planes

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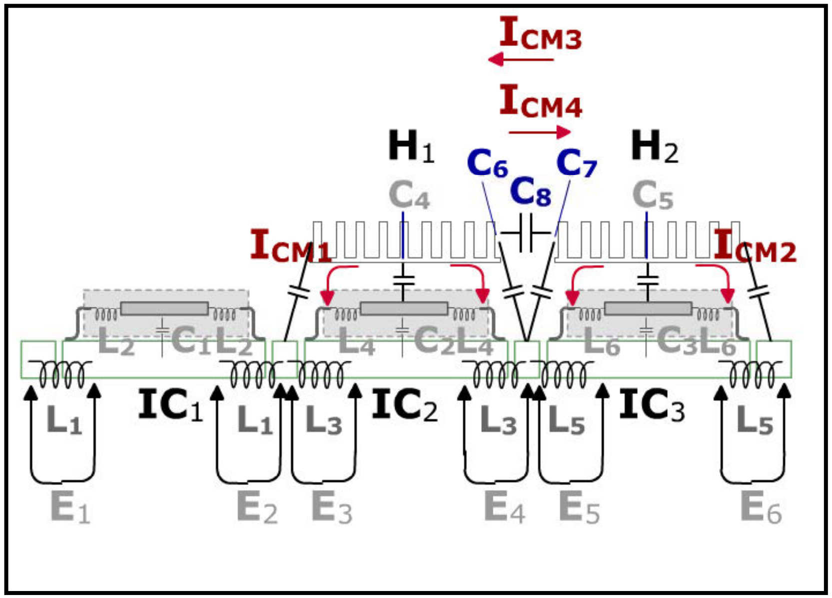
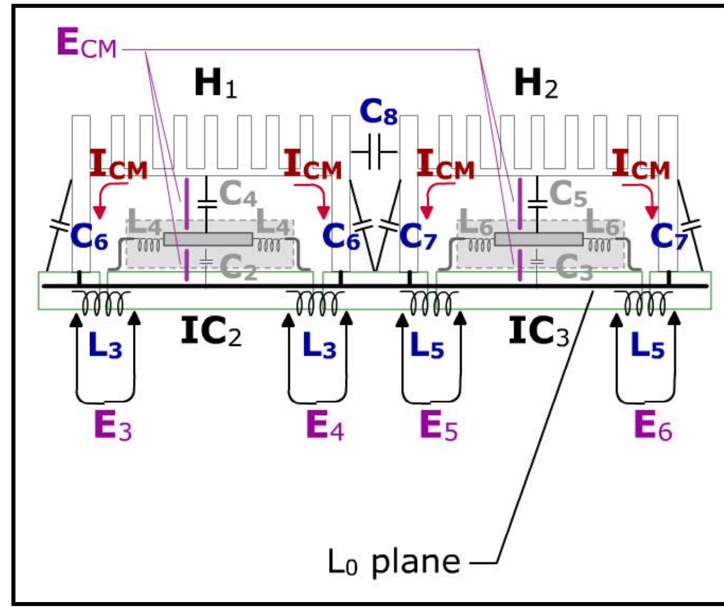
Common-Mode Coupling (Transfer Impedance) Across Partitions: HEAT SINKS!





RF Common-mode current results in EM fields that couple to, then across, heat sinks in LOW RF Transfer Impedances…..

……….for which the solution is to "terminate" both the "source" and "victim" heat sinks to the L0 Planes

Graphics from "EMCT: Electromagnetic Compatibility Tutorial"
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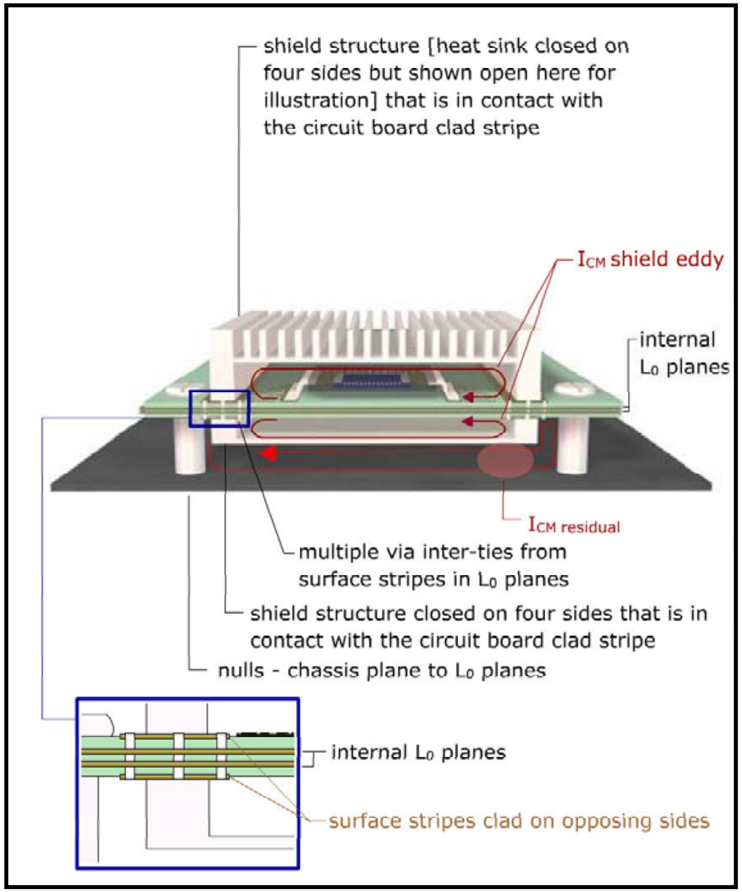
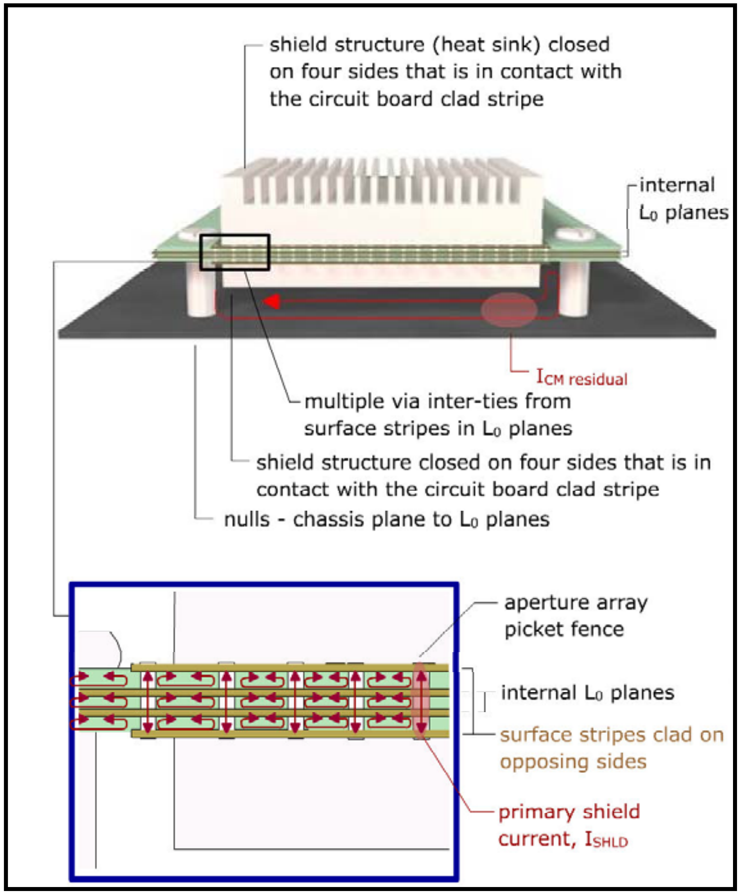
Termination of Heat Sinks Can Significantly Localize Even Multi-GHz Fields





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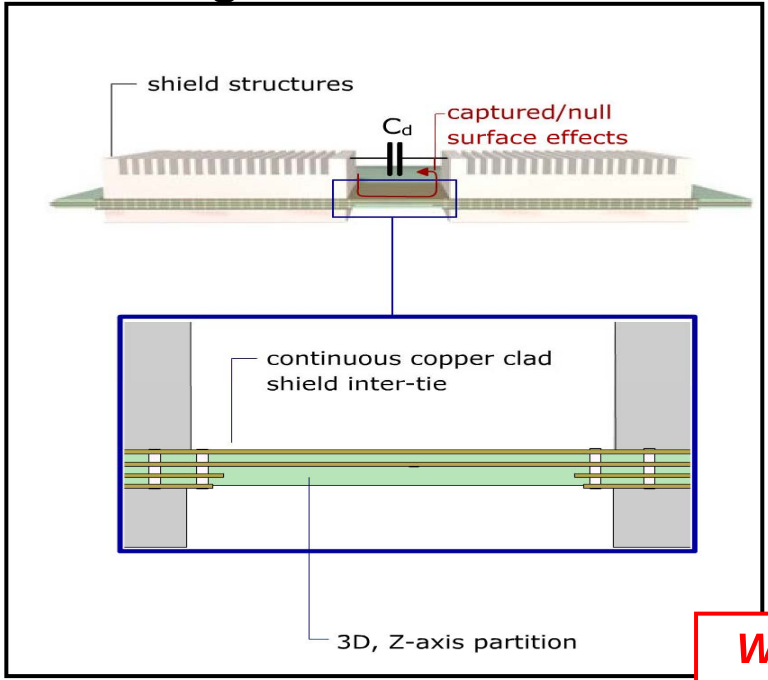
Termination of Heat Sinks Can Provide Significant Regional Partitioning Performance Values (>50dB)



What minimizes the development of the common-mode field structures before they spread?

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Process:
A Quick Litany Regarding Ohm's Law

Q: Where does current return?

A: To the source.

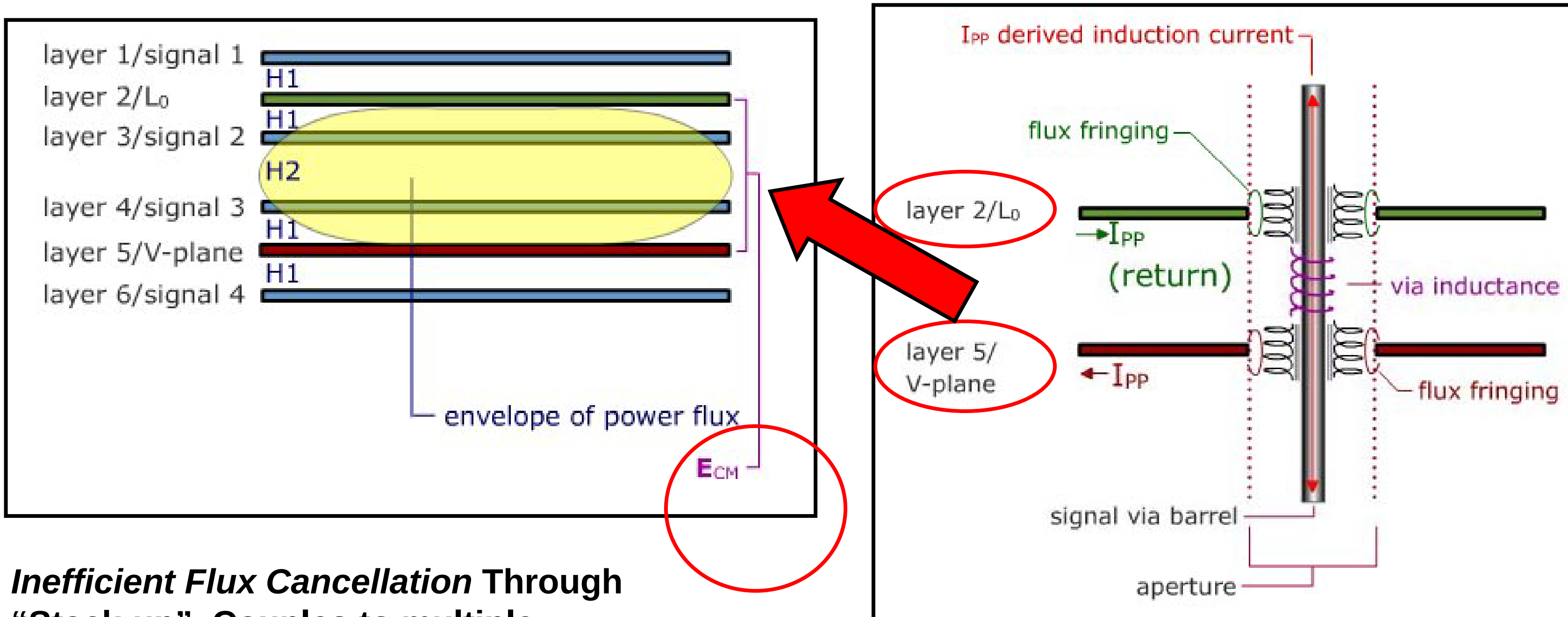
Q: Through what path?

A: The lowest impedance path.

Q: In an A.C. "dynamic system", where is the lowest impedance path?

A: Where the source flux phase and image counter-phase link to cancel inductance!

Inspection of “Threat” Sources: Recognition of Z-Axis → Within Circuit Board



Inefficient Flux Cancellation **Through “Stack-up”, Couples to multiple routing layers, Implies Increased Common-mode Potentials, and……….**

……May Degrade Signal Integrity (S/N Ratios) By POWER Flux (Current) Induction Into Z-Axis Signal Routing

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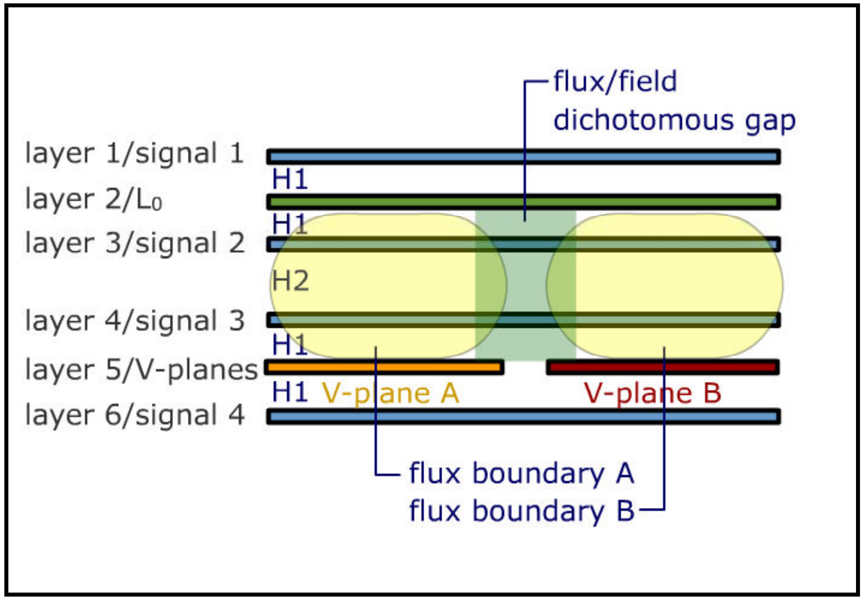
Inspection of "Threat" Sources: Recognition of Z-Axis Field Intrusions →Within Circuit Board



Split V-planes absent defined power images will intrude power coupling into 3 of 4 signal routing layers, and provide no uniform imaging. This will also highly distort signal quality in two routing layers.

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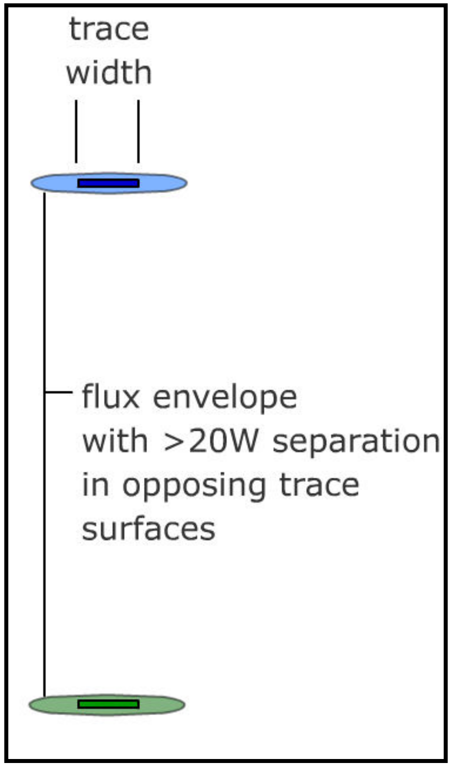
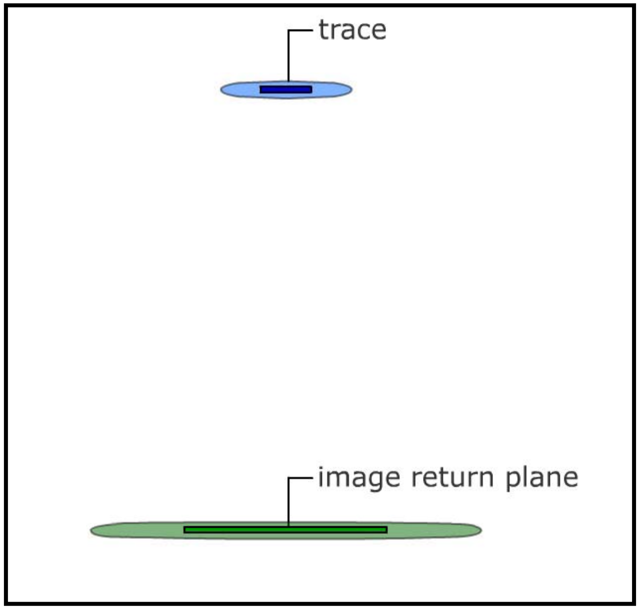
Inspection FLUX Formations as Z-Axis Fields Within Circuit Board





OBSERVATION: When Signal Trace and Image Plane (return) are far apart compared to trace width, there is NO efficient FLUX linkage.

Without LINKAGE there can be no CANCELLATION of inductance

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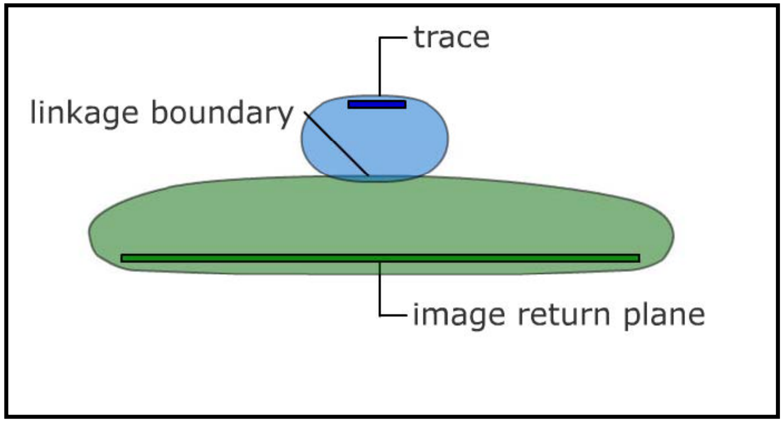
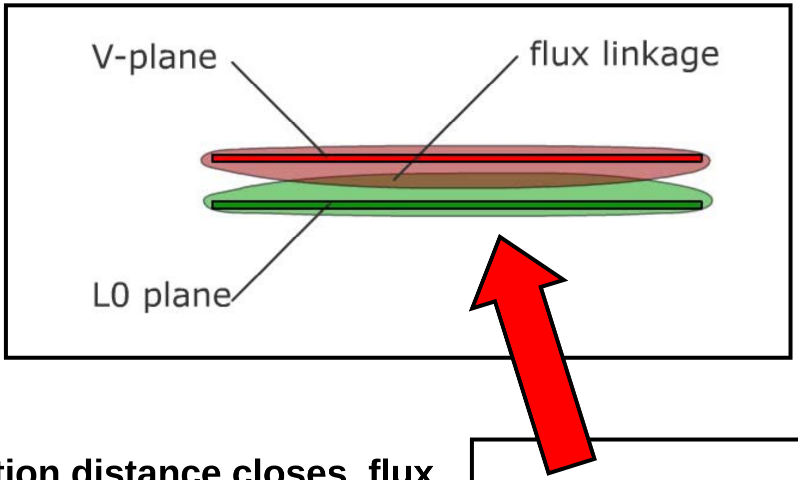
Inspection of FLUX Formations as Z-Axis Fields Within Circuit Board





OBSERVATION: As separation distance closes, flux will link and implode with increasing density on a log basis.

GOAL: Optimal LINKAGE = Optimal Cancellation
Optimal Cancellation = Optimal Containment

OBSERVATION: Imploding FLUX, constricts field boundaries.

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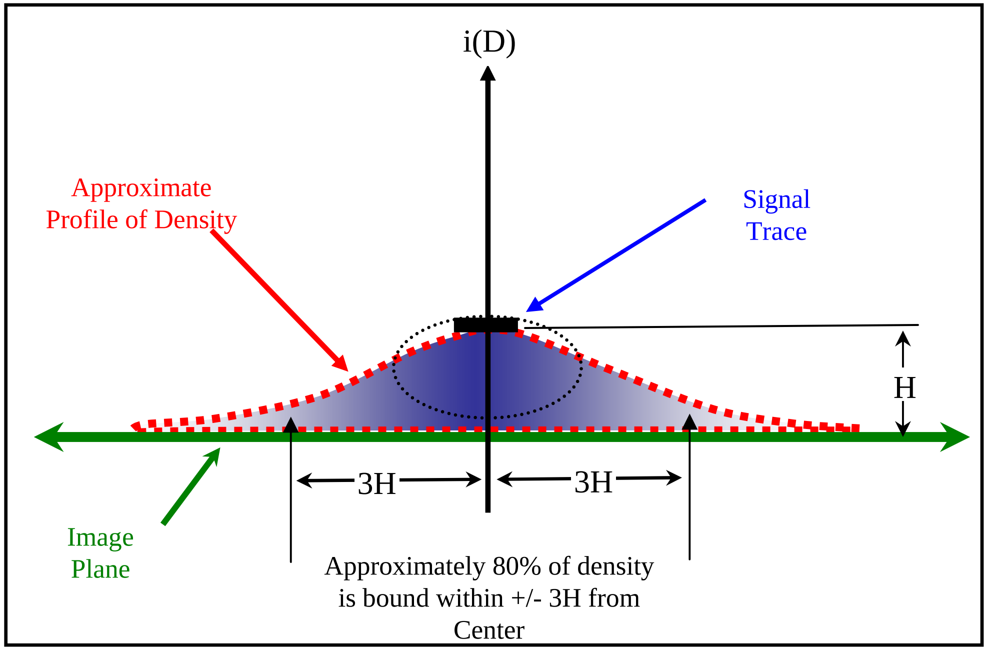
Inspection of FLUX LINKAGE Distribution as Z-Axis Fields Within Circuit Board



FLUX AND CURRENT DENSITY, as a profile, is more accurately characterized relative to the trace height above an image plane rather than the distance from the edge of the trace.

Hence, the "3W Rule" may be appropriately viewed as the "3H Rule" where "H" is the microstrip trace height above the image plane. REMEMBER: Optimally, all signal flux is intended to bind between the trace and the image plane.

$$i(D) \approx \frac{I_o}{\pi H}\frac{1}{1+(D/H)^2}$$

Where

i(D) = Current Density at distance "D" from center of trace

I_o = Trace Current

H = Height above image plane

NOTE:

Inductance results from a ratio of magnetic flux linked around a conductor and the current sourcing the flux.

$$L = \frac{\Phi}{I} = \frac{\int_s BdS}{I}$$

L = Inductance

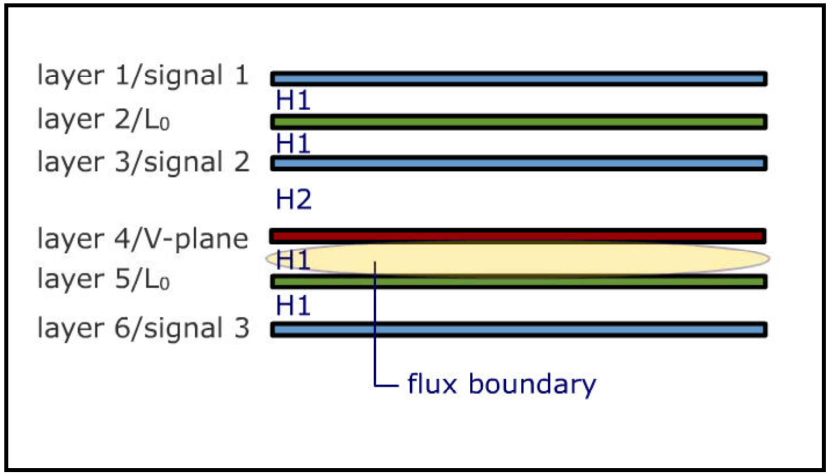
Φ = Magnetic flux

I = Current

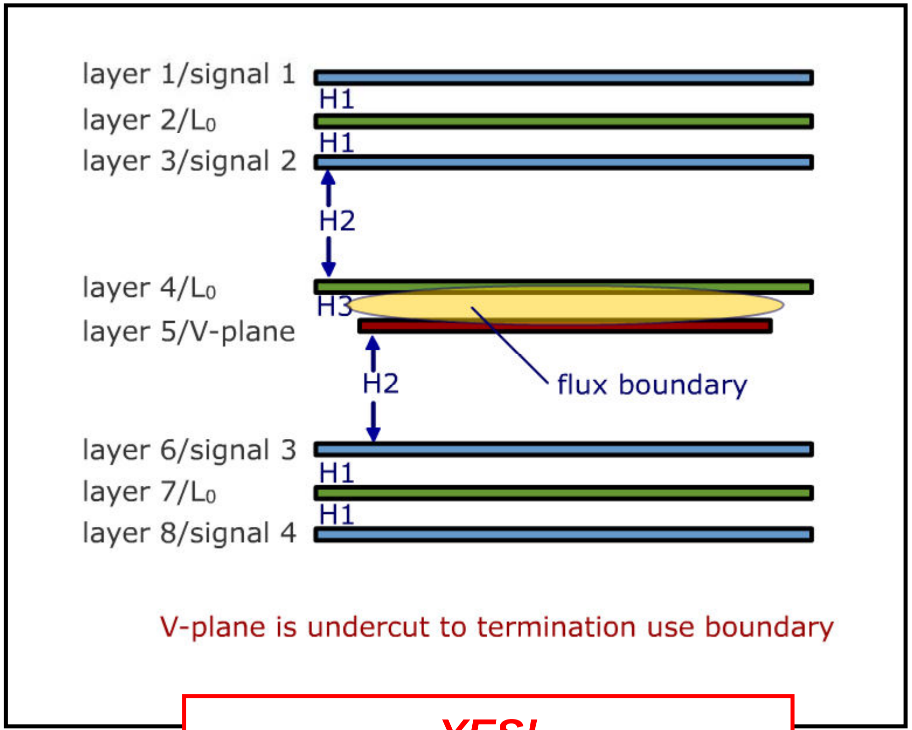
Bd = Magnetic flux density

S = Surface area of integration

Inspection of EFFICIENT FLUX CANCELLATION in the Z-Axis Fields Within Circuit Boards



EFFICIENT flux cancellation through "Stack-up" causes CONFINED common-mode potentials, and low impedance power distribution.



Inspection:
Are the flux- fields adequately confined?
Is there <u>more</u> to partitioning in the Z-Axis?

YES!
Concepts of Skin Depth due to Skin Effect!

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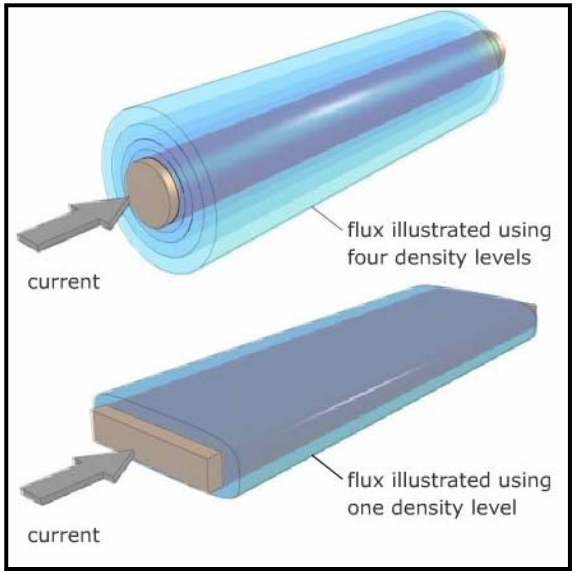
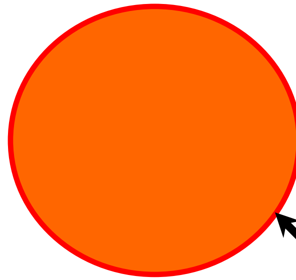
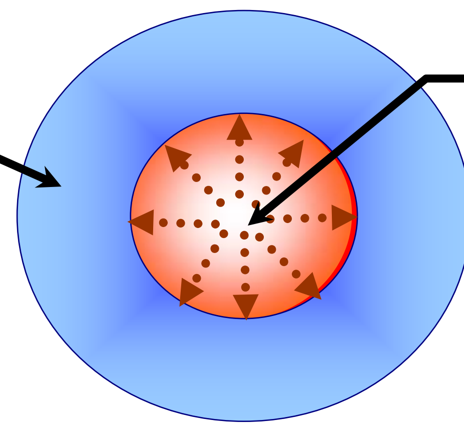
SKIN EFFECT – SKIN DEPTH
Within Conductors: Current Density Distribution





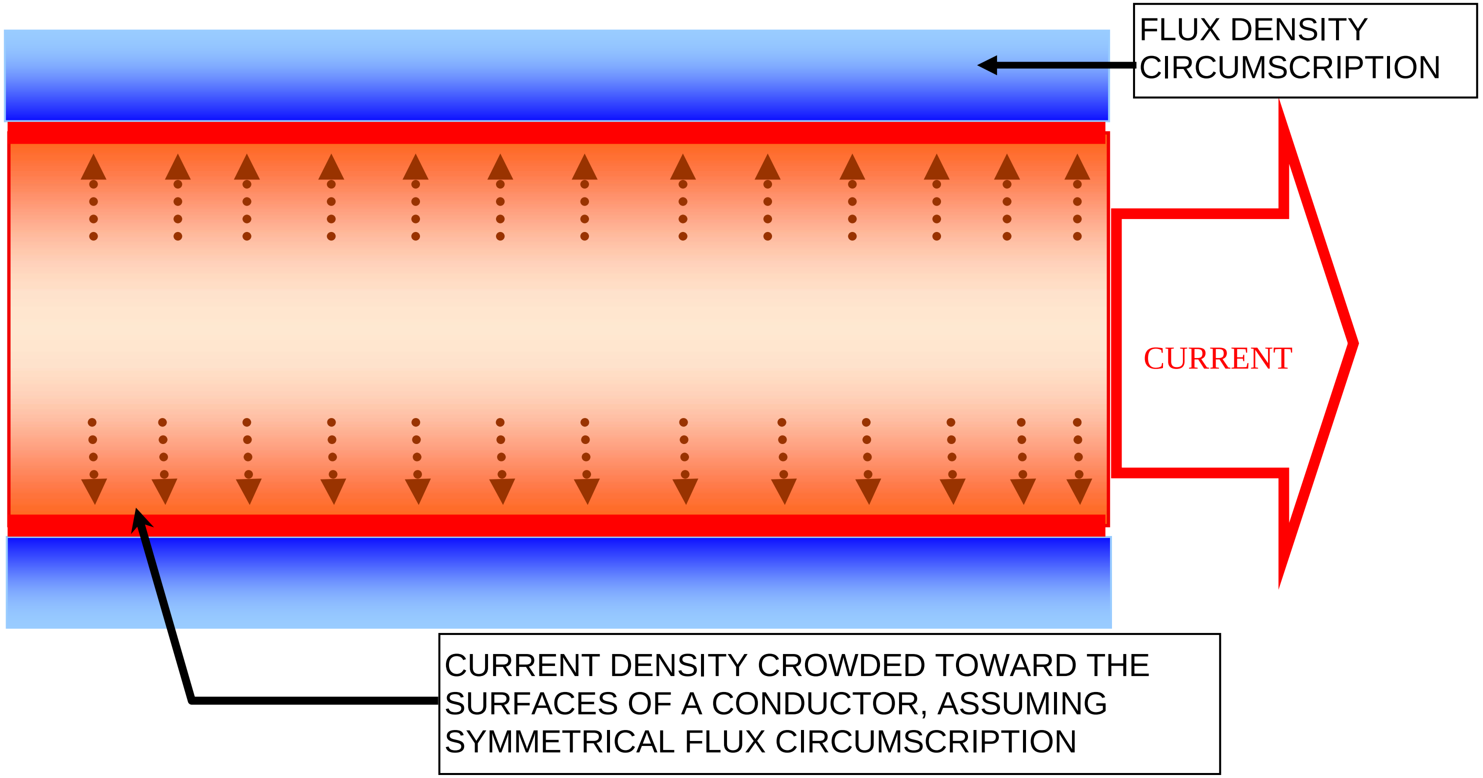
CURRENT DENSITY IS UNIFORMLY DISTRIBUTED THROUGHOUT CONDUCTOR CROSS SECTION → ***ONLY AT D.C. AND LOWER FREQUENCY A.C. APPLICATIONS.***

AT HIGHER FREQUENCIES THE CURRENT DENSITY ***DIMINISHES AT THE CENTER*** OF THE CONDUCTOR AND "CROWDS" TOWARD THE SURFACE



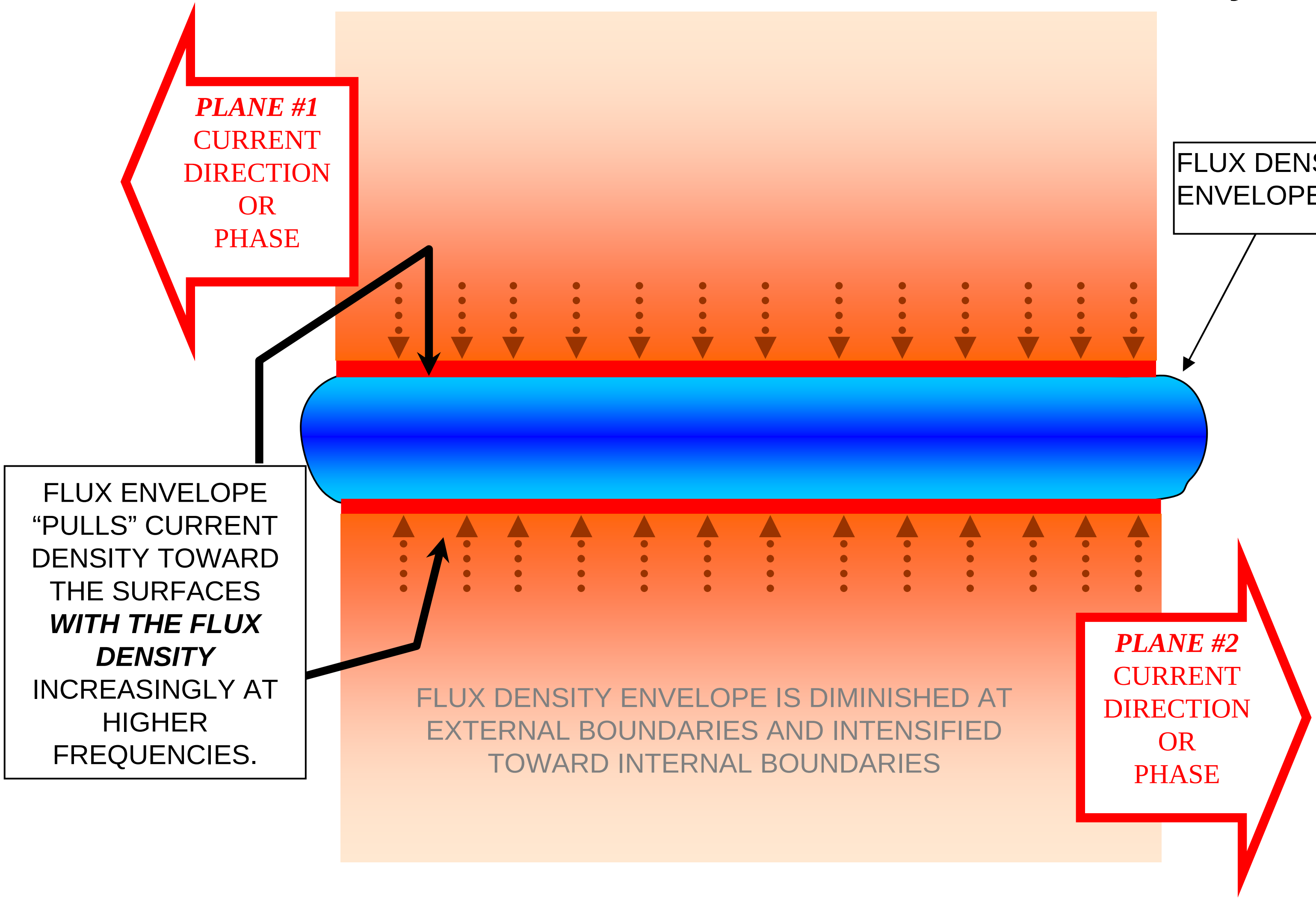
FLUX ENVELOPE "PULLS" CURRENT DENSITY TOWARD THE SURFACE INCREASINGLY AT HIGHER FREQUENCIES.

SKIN EFFECT – SKIN DEPTH In Planes Within Circuit Boards: Z-Axis Current Density

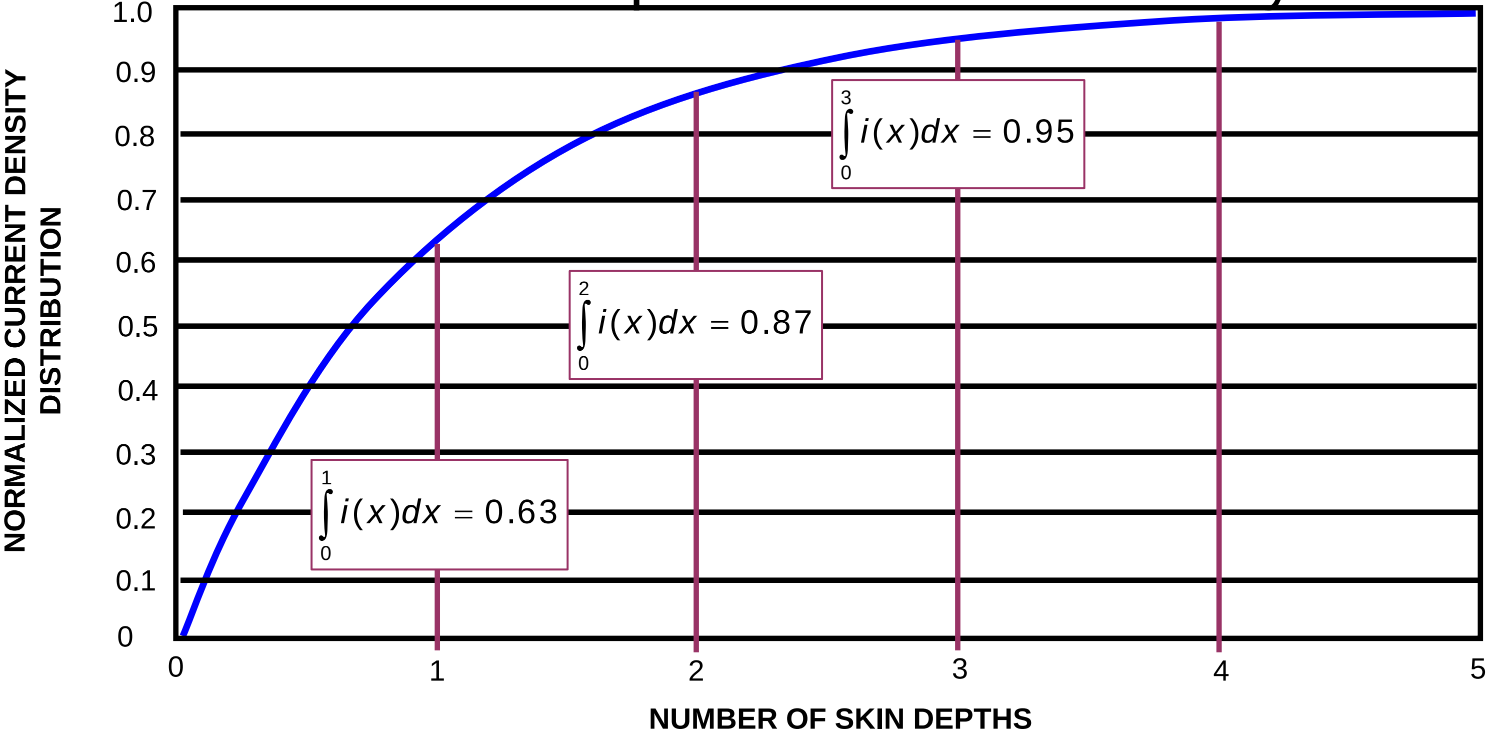


To emphasize the formation of skin effect, the *higher* the frequency, the *smaller* the skin depth – and - the *more conductive* and/or the *more permeable* the material (at higher frequency), the *smaller* the skin depth. Given that observation in terms of skin effect, the smallest skin depths occur with most conductive materials with higher permeability (assuming that the permeability is evident as a characteristic of the material at high frequency) and at the highest frequencies.

SKIN EFFECT – SKIN DEPTH In Planes Within Circuit Boards: Z-Axis Current Density



SKIN DEPTH In Planes Within Circuit Boards: Z-Axis “Captured” Current Density



EXPONENTIAL EFFECT DISPLAYED IN GRAPH:

$i(x) = I_0 e^{-x/1}$

$I_0 = 1$

Skin Depth = 1

APPROXIMATION OF CURRENT DENSITY CAPTURED TOWARD THE SURFACES OF A CONDUCTOR AT VARIOUS SKIN DEPTHS.

Frequency Relationship of SKIN DEPTH In Planes Within Circuit Boards: Z-Axis “Captured” Current Density

Frequency MHz	Skin Depth Mils (inch)	5 Depths Mils (inch)
1	3	15
10	0.8	4
100	0.26	1.3
1000	0.08	0.4

EXAMPLES OF SKIN DEPTHS FOR ANNEALED COPPER AT SPECIFIC FREQUENCIES.

Skin Depths	Percent Capture*
1	63
2	87
3	95
4	97
5	**99**

APPROXIMATION OF CURRENT DENSITY CAPTURED TOWARD THE SURFACES OF A CONDUCTOR AT VARIOUS SKIN DEPTHS.

Skin Depth VALUE Calculation

The value of skin depth is yielded by

$$\delta = \sqrt{\frac{2}{\mu_r \sigma_r \omega}}$$

(in meters since the values of μ_r and σ_r are expressed with relationship to meters)

where, $\omega = 2\pi f$ where f is in Hertz

For reference, the conductivity of annealed copper is given as the symbol σ, where

$\sigma = 5.82 \text{ x } 10^7$ mhos/meter for copper

with the relative values for other metals assigned the symbol σ_r .

σ_r is a numerical value that results by applying the factor indicated by that designated for σ_r to the value of the reference, .

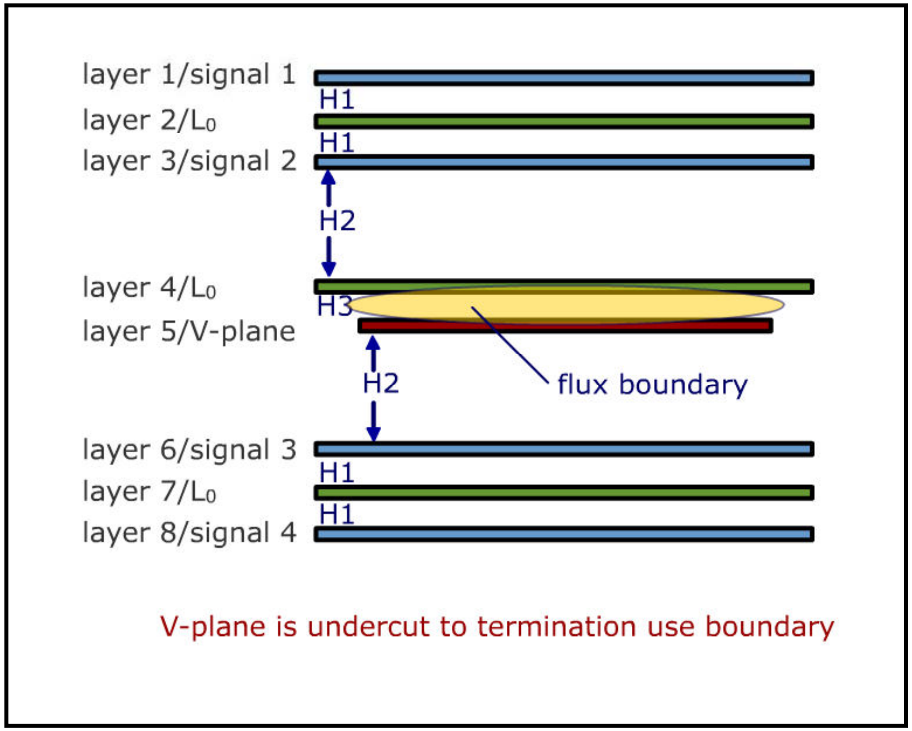
The permeability of free space is given the symbol μ, where

$\mu = 4\pi \text{ x } 10^{-7}$ Henrys/meter for free space

with the relative values of other materials assigned the symbol μ_r .

μ_r is a numerical value that results by applying the factor indicated by that designated for μ_r to the value of the reference.

REVIEW of Current Density and Flux Distribution as Z-Axis Fields Within Circuit Board



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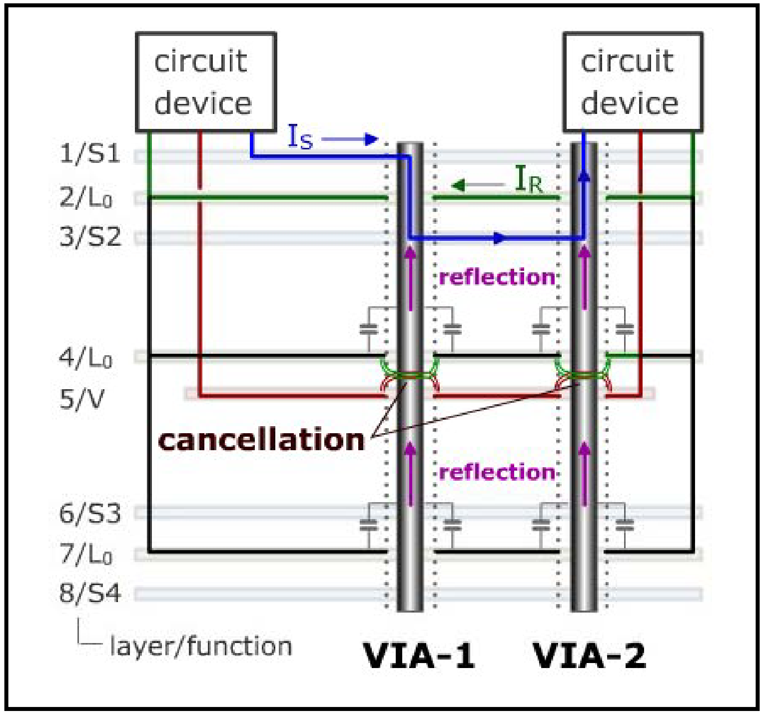
Efficient Flux Cancellation in Z-Axis – Within Circuit Board



- → **Power Impedance Is Dynamically Reduced.**
- → **Common-mode Potentials Reduced Proportionately**
- → **Power Flux Cancels in Small Loop Formations.**
- → **Signal Integrity is Defended.**

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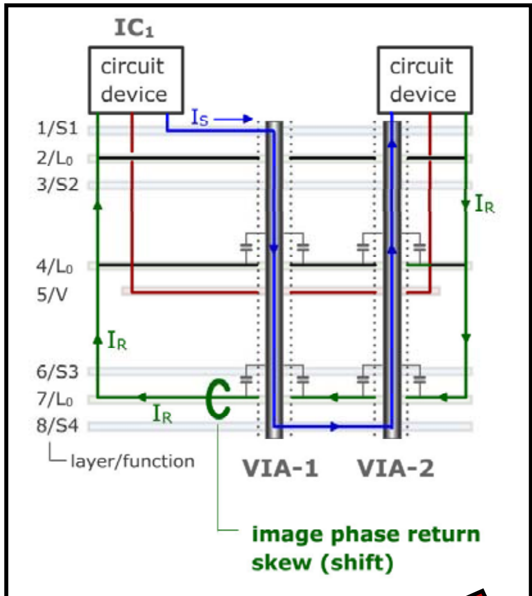
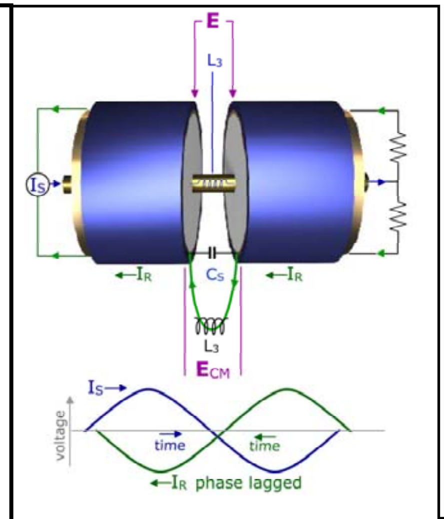
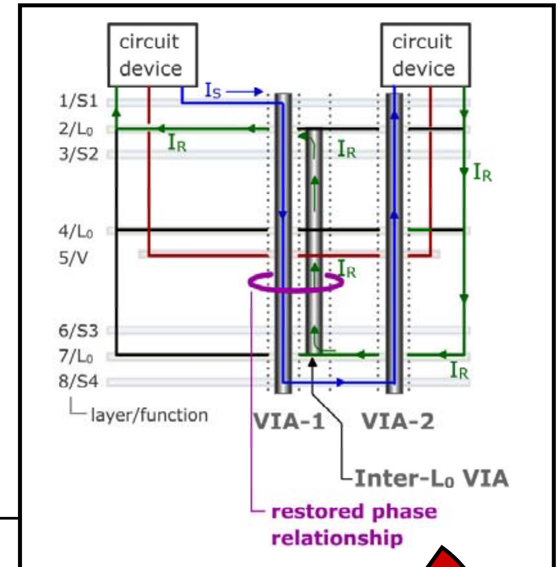
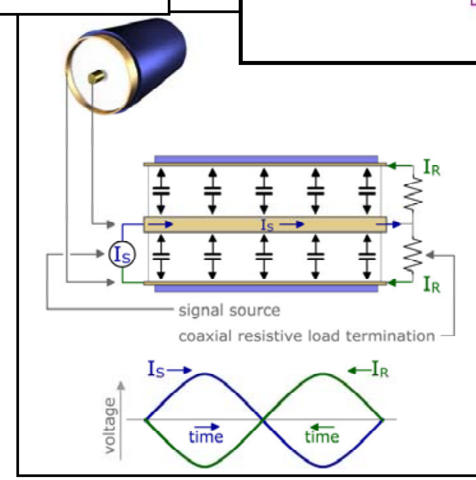
Inter-Stitched L0 Vias May be Needed To Cause Efficient Flux Cancellation Across the Z-Axis in Circuit Boards









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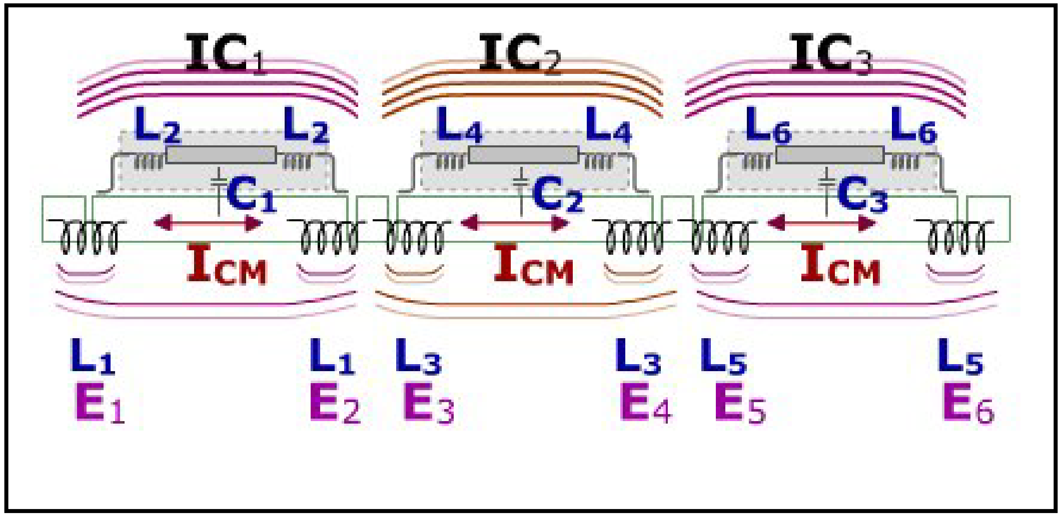
Review of "Common-Mode Fields" From Excitation Of Patterned Layout Inductance – 3 Axes



After Topology and "Patterned Layout Inductance", Coupling across regions through Heat Sinks, Stack-up and Skin Depth Boundaries,

Are there other considerations?

YES!

Coupling of Fields → into conductive CHASSIS

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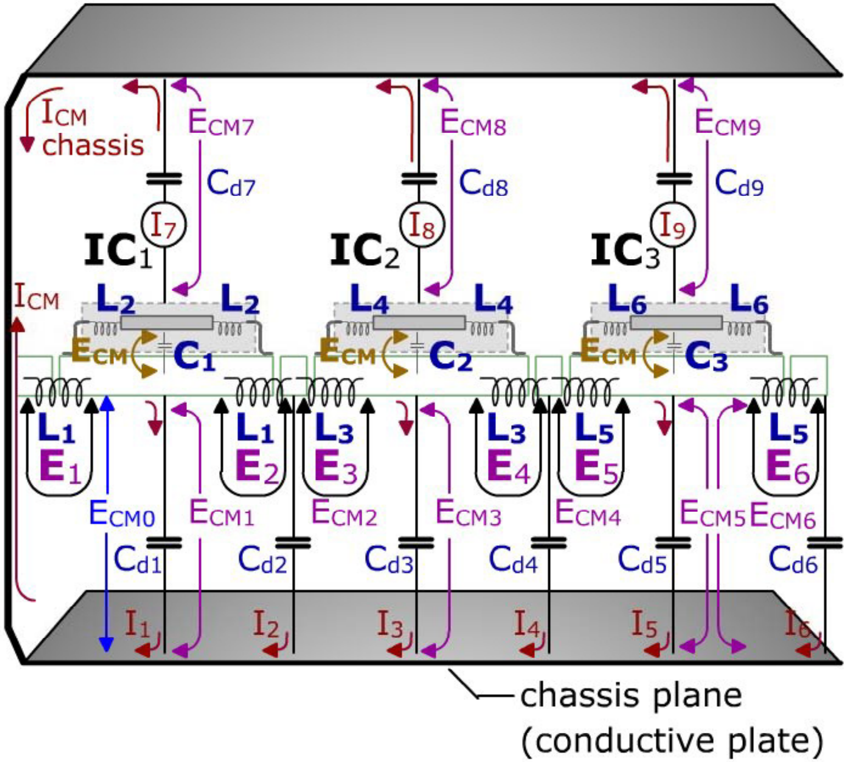
Coupling Through Field Transfers to Case & Chassis Structures!



What is the magnitude of coupling to and across the chassis structure?

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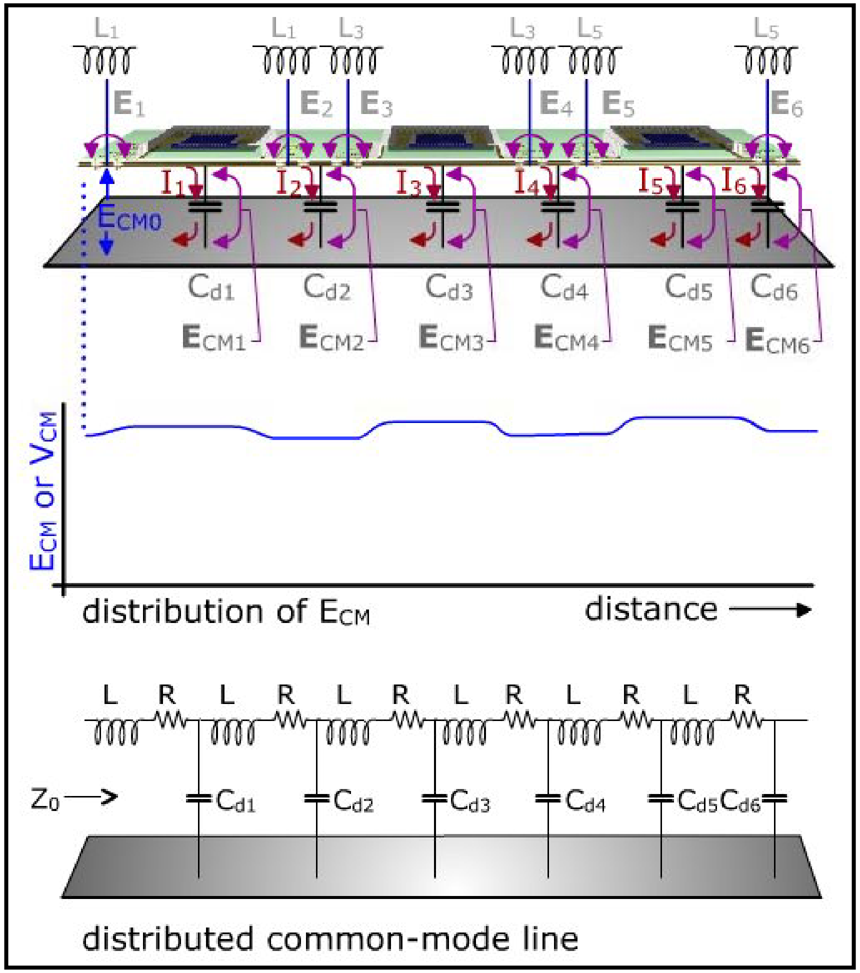
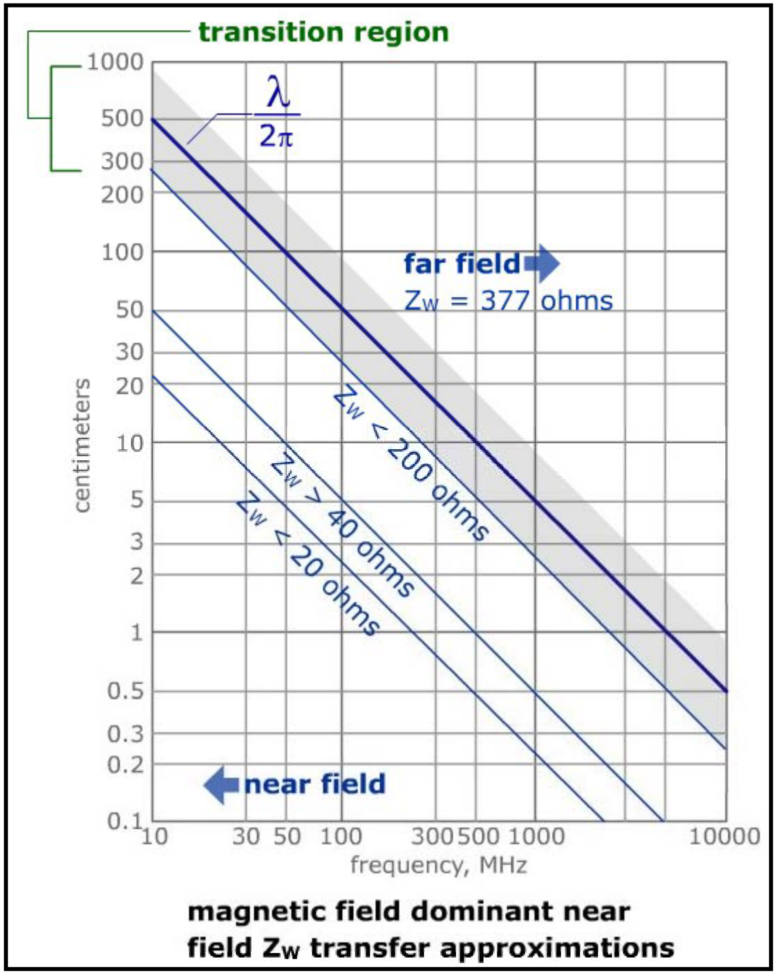
Examination of Common-Mode Field Transfer IMPEDANCES to Conductive Chassis Structures





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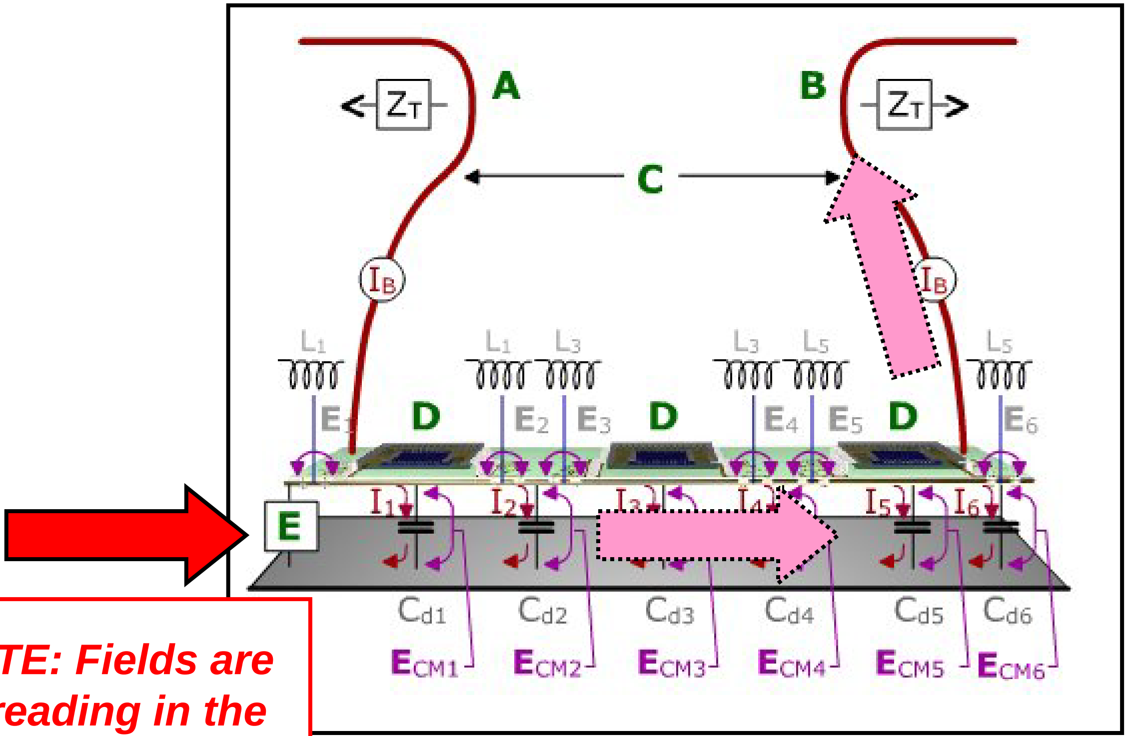
Implications of Common-Mode Transfers & Excitations in 3 Axes With Cables (Multiple Antenna Structures)



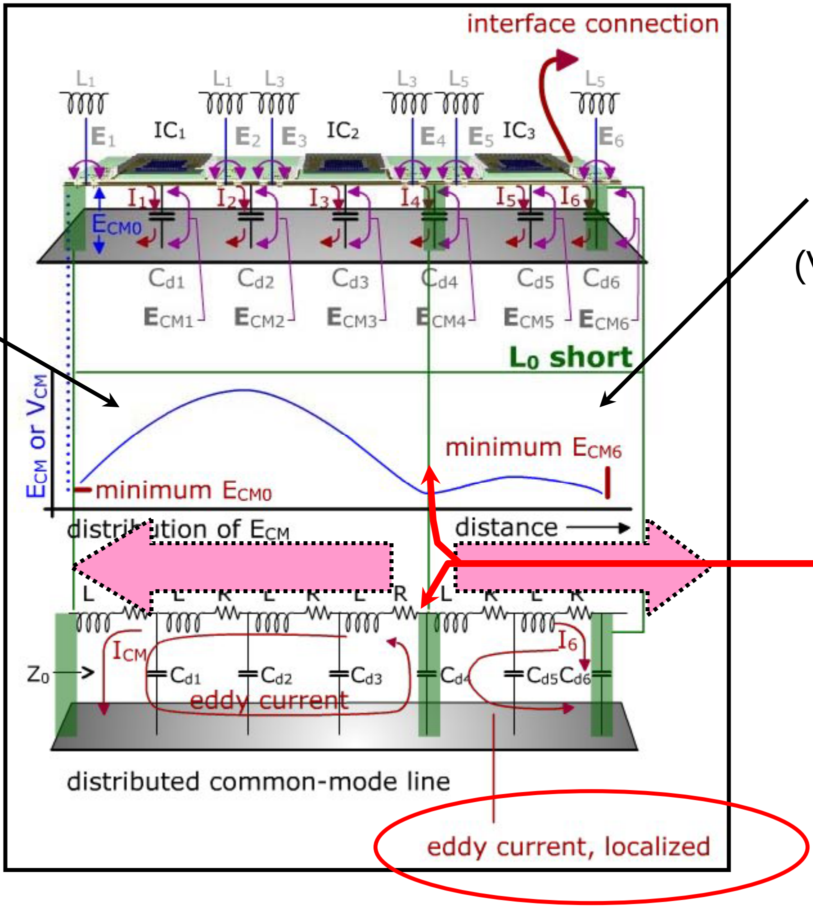
NOTE: Fields are spreading in the gap across regions of the circuit board!

Graphic from "EMCT: Electromagnetic Compatibility Tutorial"
Used with permission from W. Michael King, E. Pavlu, and Elliott Laboratories

Partitioning With NULLS In the Z-Axis Can Defend S/N Ratios and EMC

Digital Region
"noisy"

(Threat Sources)



Something
"sensitive"

(Victim Receiver)

NOTE: Field Partition!

Graphics from "EMCT: Electromagnetic Compatibility Tutorial"
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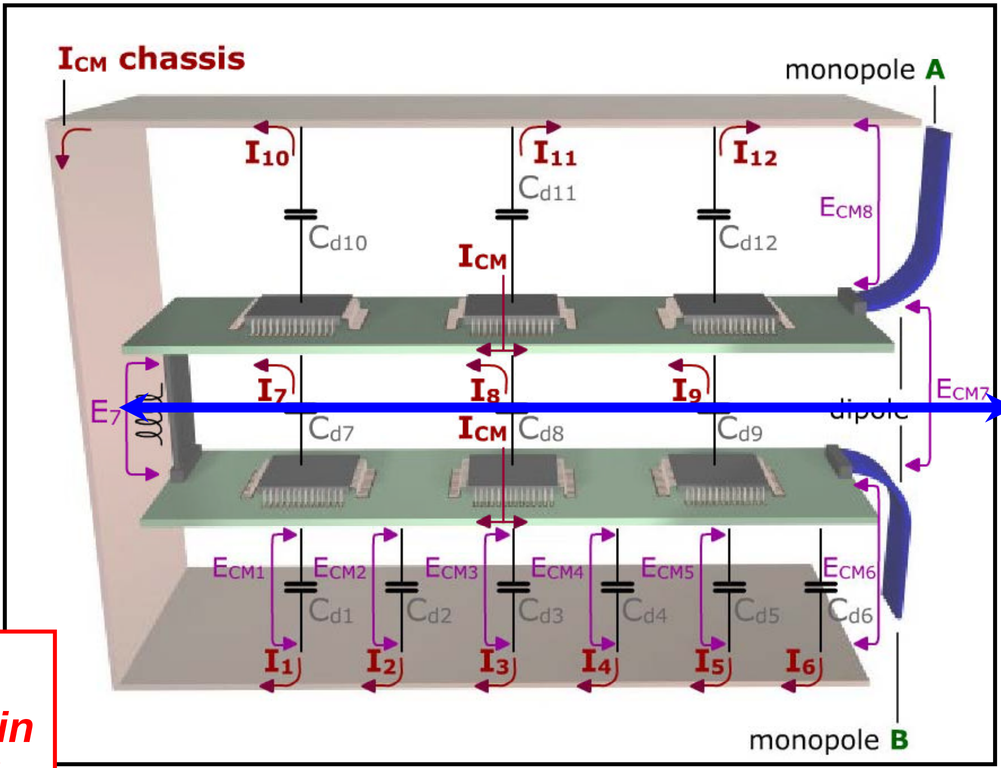
Close-Proximity Paralleled Boards Will Mutually Couple!



Demanding use of a shield partition between boards.

Mutual field coupling can be in the low tens of Ohms!

Graphic from “EMCT: Electromagnetic Compatibility Tutorial” Used with permission from W. Michael King, E. Pavlu, and Elliott Laboratories

What (Else) Can Influence EMI Partitioning in Planes?

HINTs

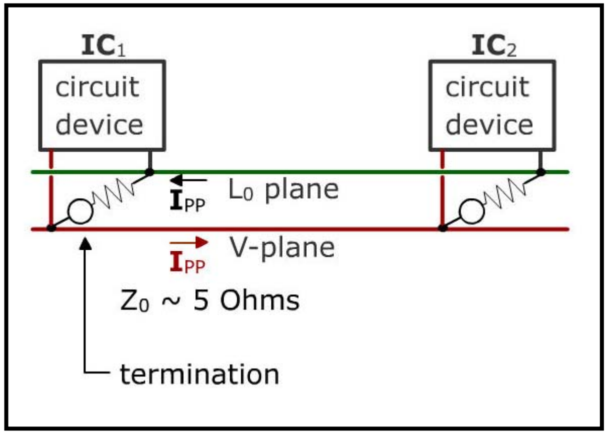
Remember: V-Planes with an image plane are Z-Axis Transmission Lines

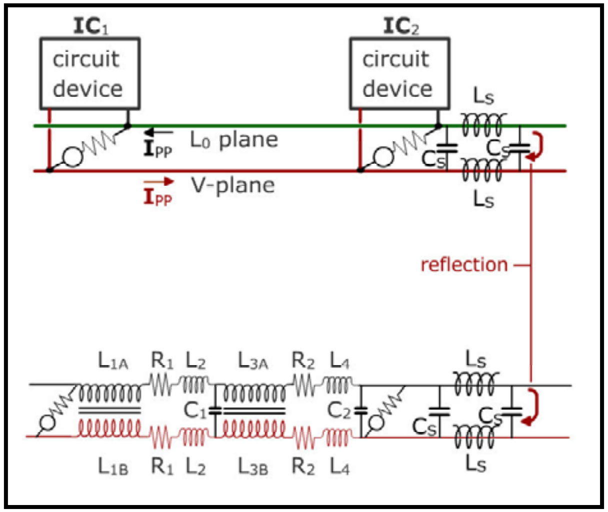
Are they appropriately "end-terminated?"

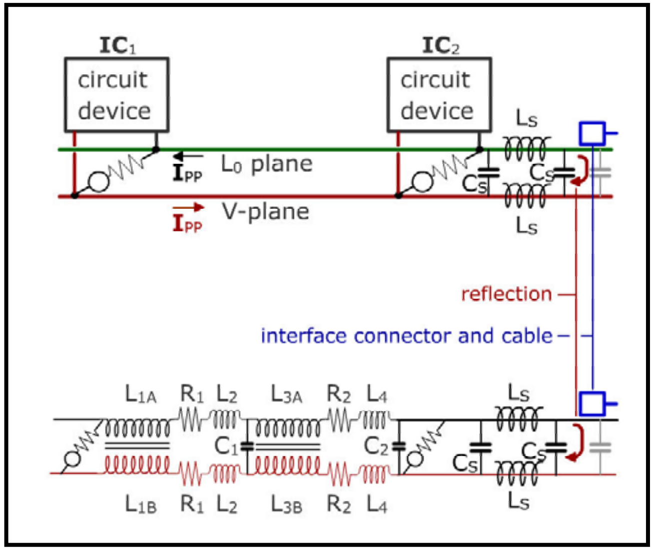
"End-terminated" in planes can mean *"edge-terminated!"*

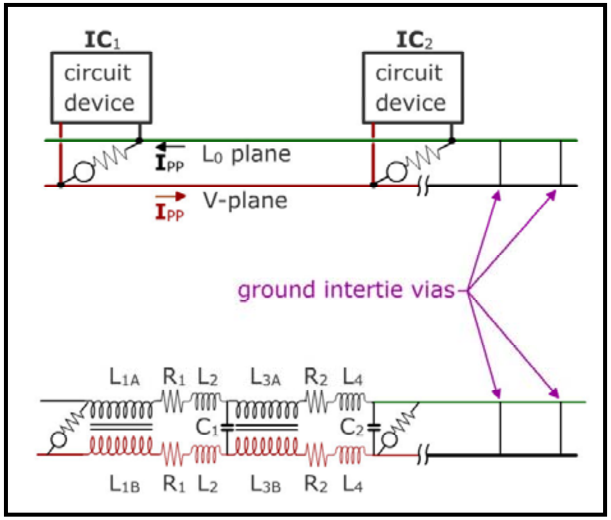
What optimally determines the use of "edge termination?"

Undercut V-planes can Defend S/N Ratios and EMI in Interface Cables









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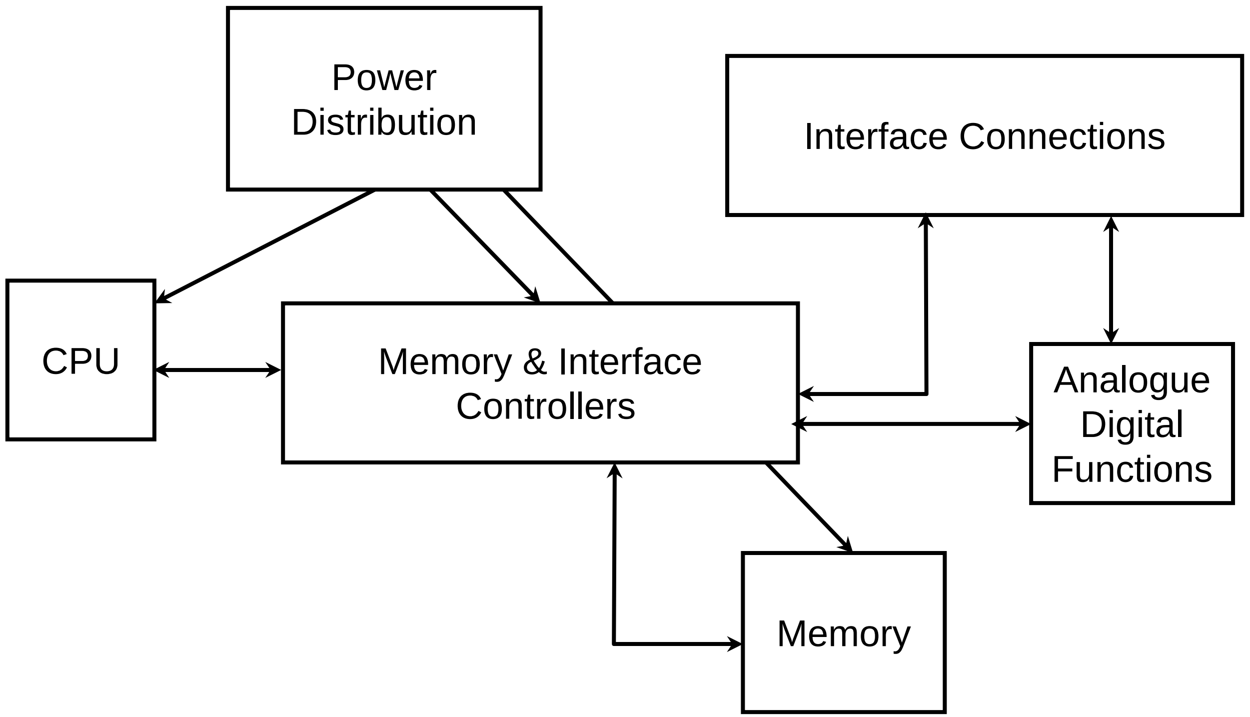
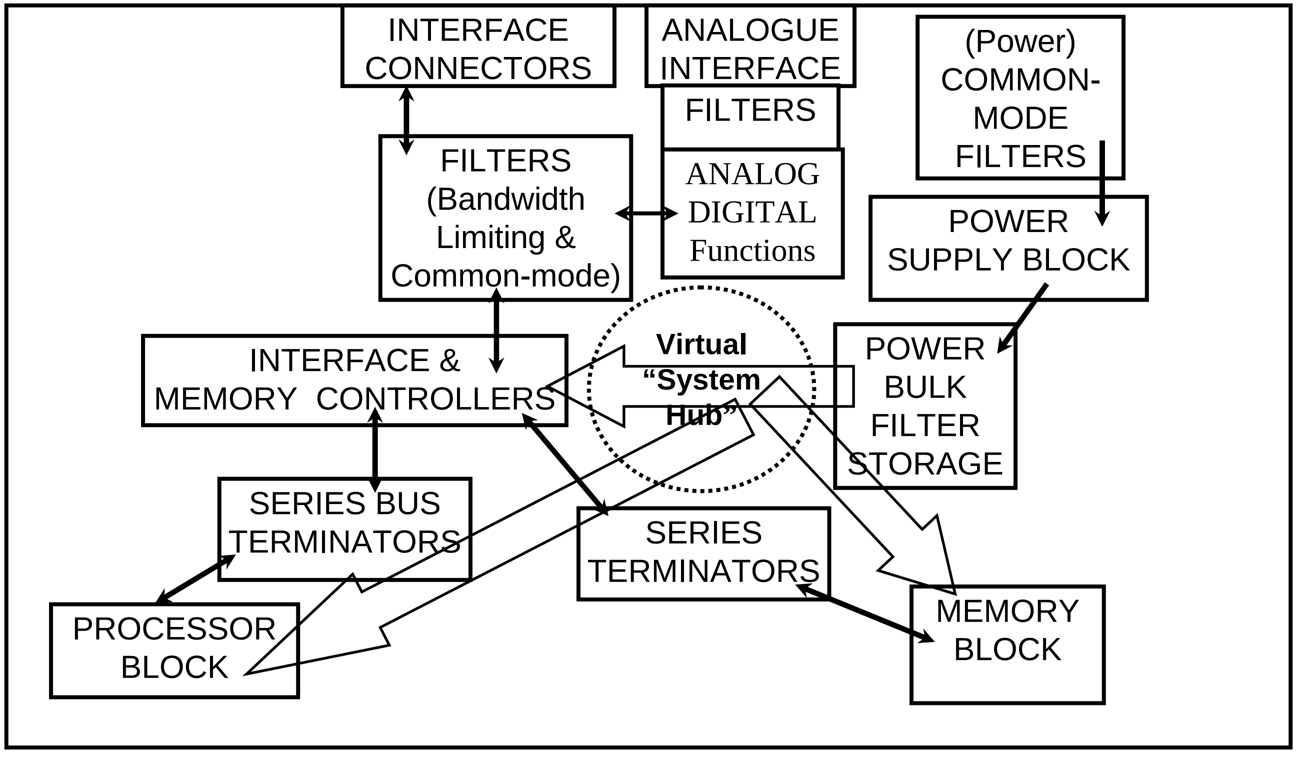
REVIEW of
Electrical "Block" Architecture



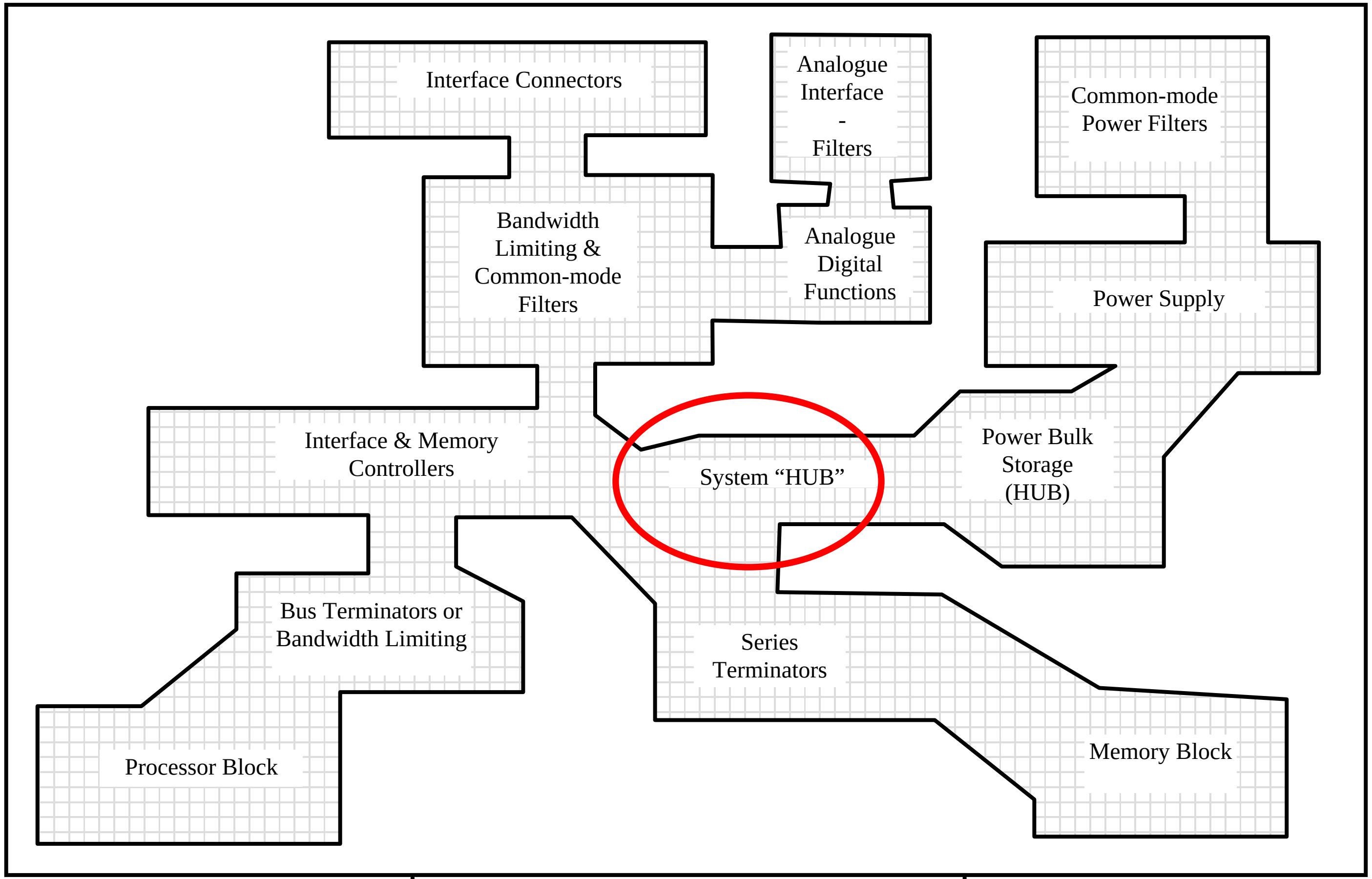
With the circuit board "recognition plan" in place to integrate fields in the X, Y, and Z axes, layout topology may be implemented.

Implied Common-mode Architecture Derivative of Electrical "Block" Diagram



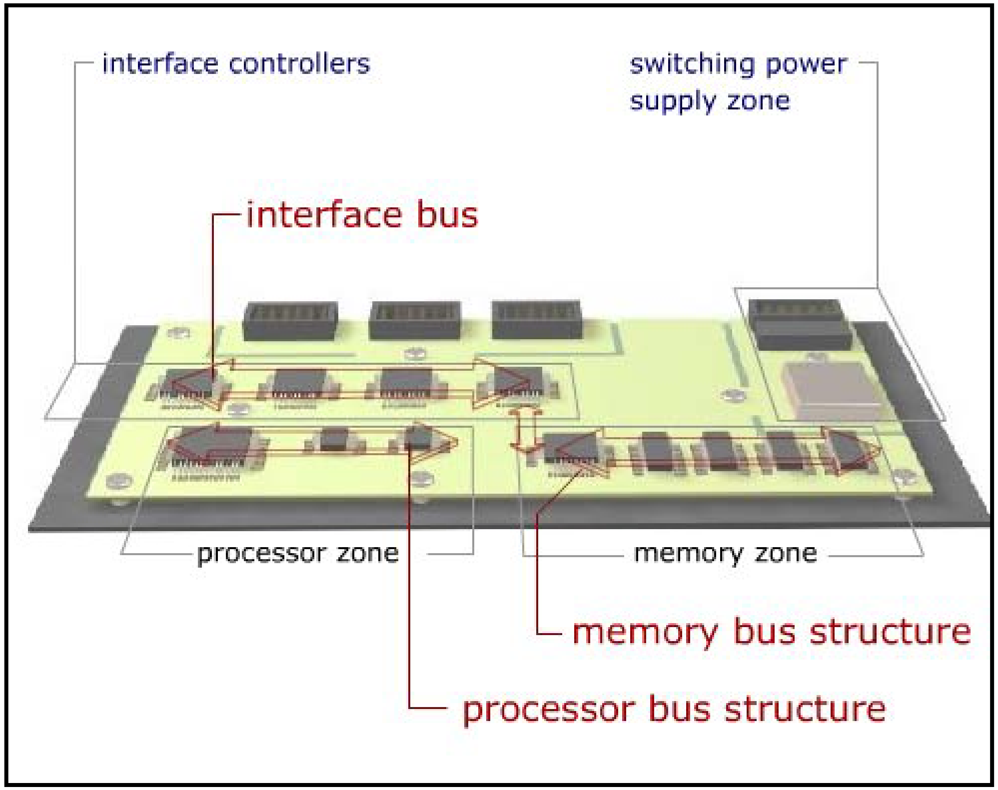
"MAP" of Architectural Topology With Function and HUB, Initially Limited to X-Y Axes

Resultant Architectural Routing Plan



Preliminary Routing "Plan" Formation

Implied Topology of Circuit Board With Chassis Plane



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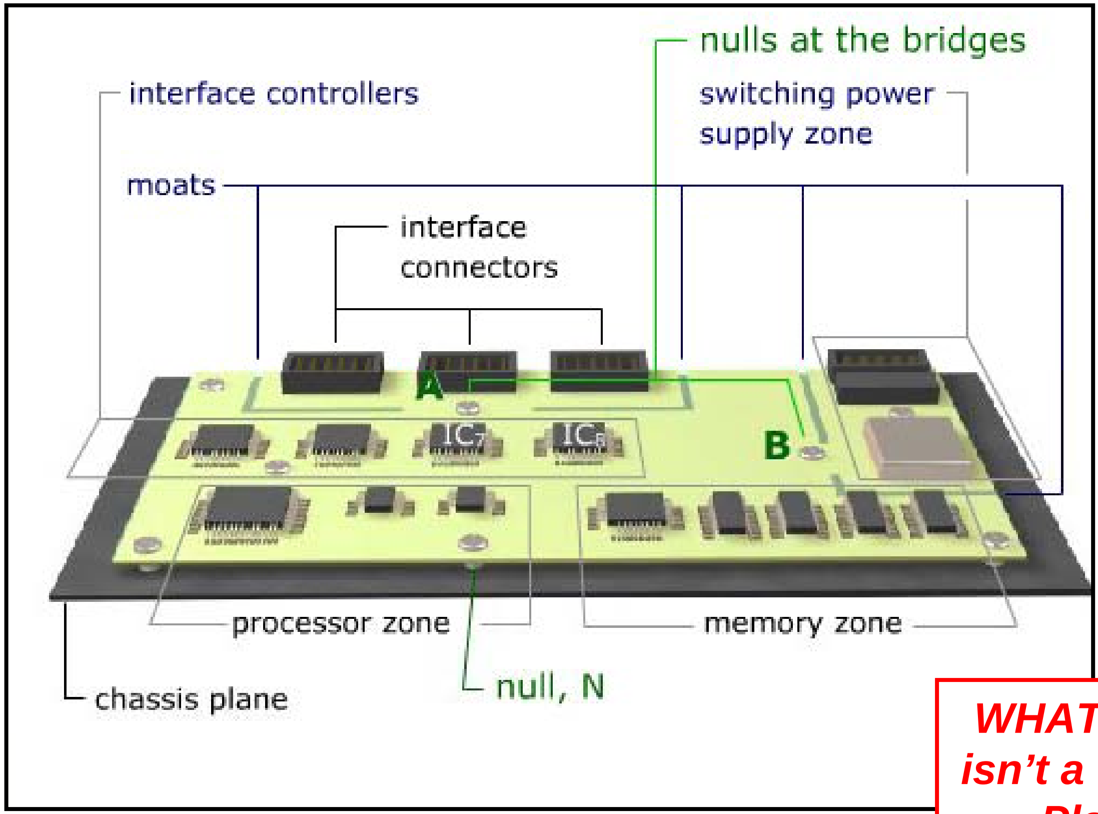
Implied Topology of Circuit Board With NULLS to Chassis Plane



WHAT IF there isn't a "Chassis Plane?"

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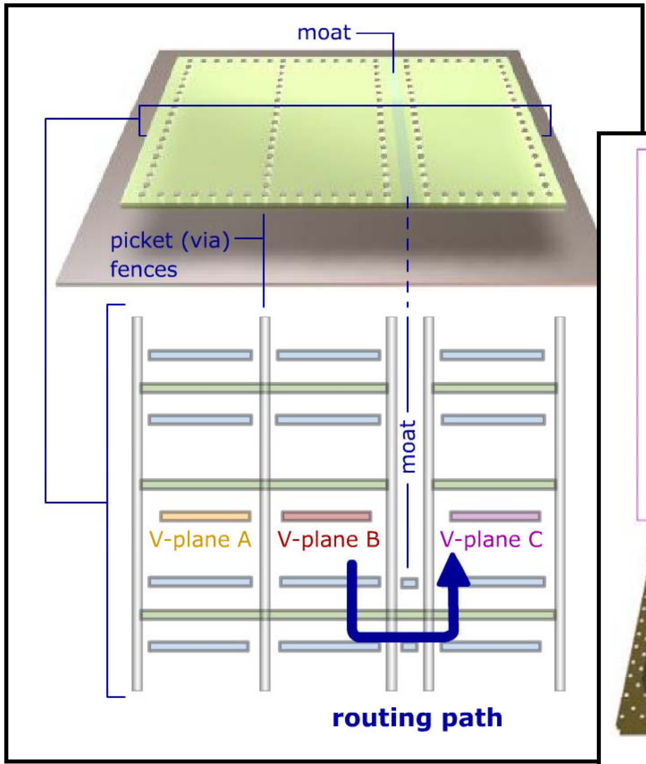
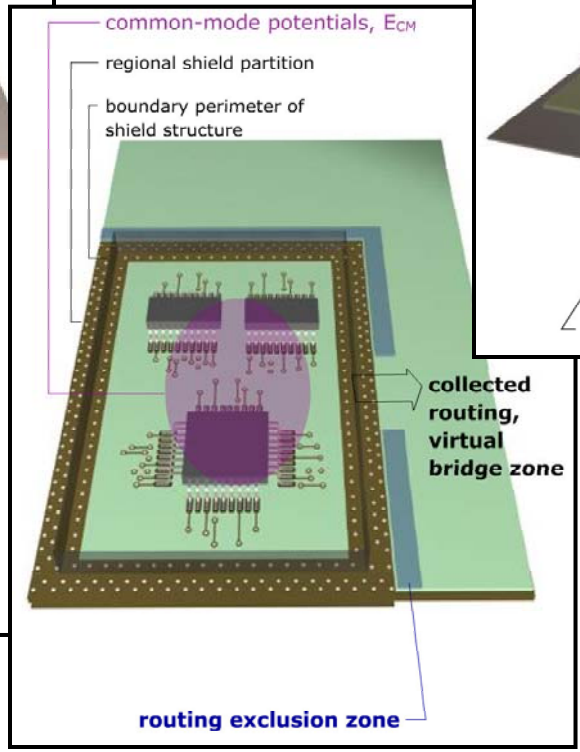
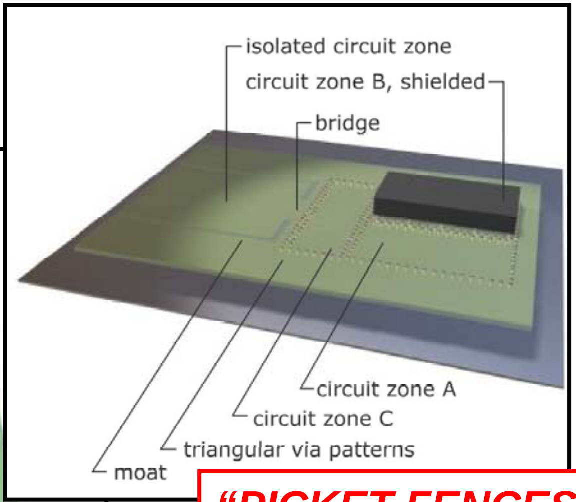
Implied Topology of Circuit Board With Inter-Stitched L0 Vias As Regional *NULL Partition Boundaries*







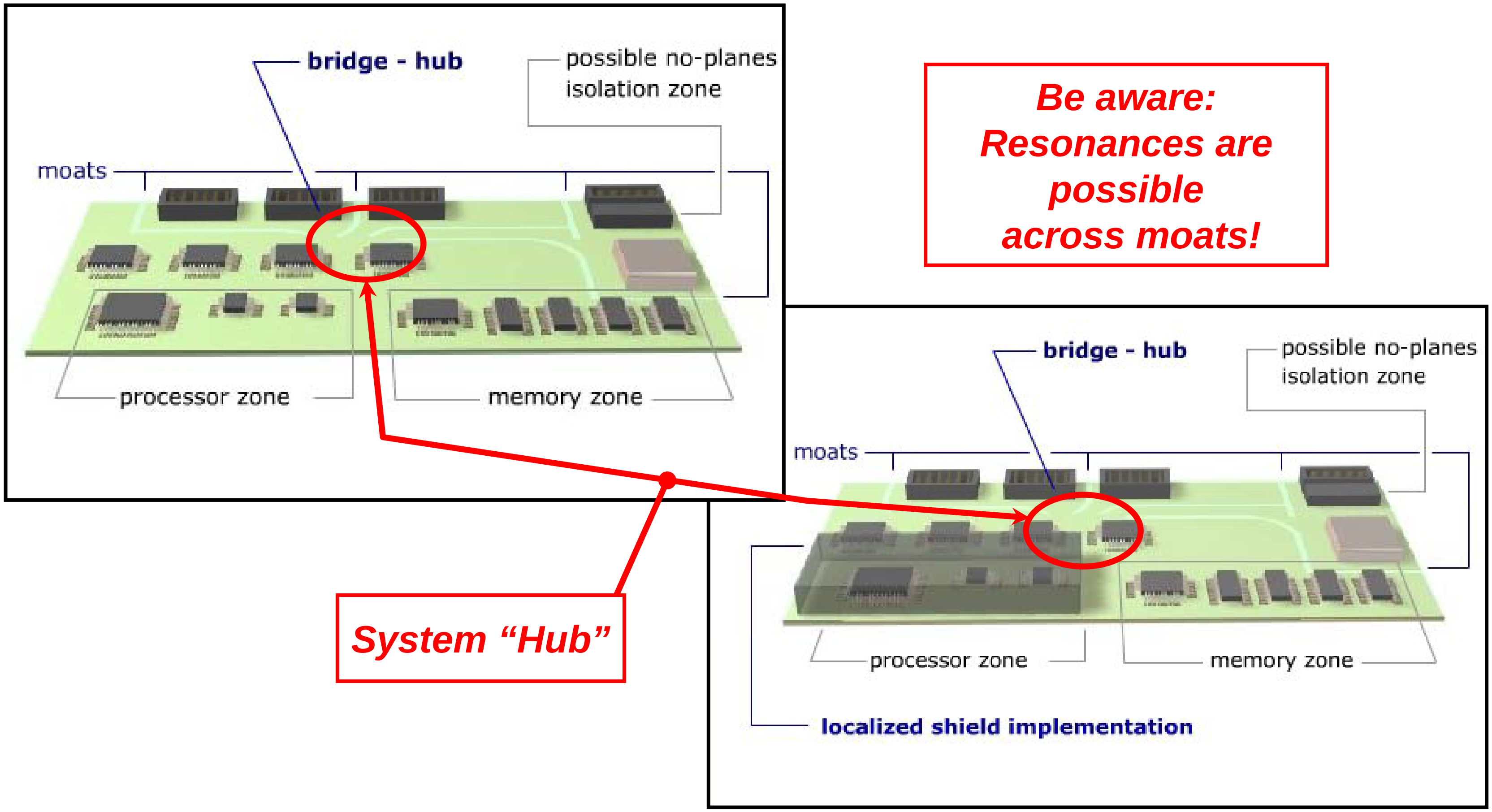
"PICKET FENCES" Can be implemented as regional partition boundaries.

Remember: Blind Vias dramatically reduce "patterned layout" inductance!

Inter-stitched nulls become boundaries to EM Fields.

Graphics from "EMCT: Electromagnetic Compatibility Tutorial" - Used with permission from W. Michael King, E. Pavlu, and Elliott Laboratories

Implied Partitioning Topology of Circuit Board Without Chassis Plane



Graphics from "EMCT: Electromagnetic Compatibility Tutorial"
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Original “Recognition Plan” – Modified → Becomes “Summary”

→ **PARTITIONING** recognition plan is a subset part of the system-product “Common-mode Architecture”

→ “Common-mode Architecture” is a derivative of the system-product electrical / functional block architecture

→ System-product functionality is identified initially in “block” structures

→ “Block” structures set the pattern approach initially for X-Y Axes topology, followed by Z-Axis implementations for **PARTITIONING CONCEPTS**

→ Separation of High-Amplitude from Low-Amplitude (e.g. “sensitive” signals or circuit regions) for optimal functionality is a criteria set for **PARTITIONING**

→ Containment of specifically unique Spectral Regions **requires 3-Axes Views**

→ Protection of analogue circuits from digital spectra intrusions (S/N Ratios) and Exclusion of EMI Emission from interface – interconnecting cables **must include examination of field transfer involvements “through” STRUCTURE & chassis coupling**

→ Rejection of extraneously applied fields or currents (susceptibility-immunity factors) from functional intrusion will follow the partitioning concept in proportion to the approach.

Author Information:

W. Michael King is a systems design advisor who has been active in the development of over 1,000 system-product designs in a 46 year career. He serves an international client base as an independent design advisor.
Many terms used for PC Board Layout, such as the “3-W Rule”, the “V-plane Undercut Rule”, and “ground stitching nulls”, were all originated by Mr. King.
His full biography may be seen through his web site: www.SystemsEMC.com.

Mr. King’s published original research changed the state the art on the subjects of the ESD dynamic waveform continuum and responses of cardiac pacemakers to electromagnetic fields. He has authored contributing feature articles to EDN Magazine, Design News Magazine, University of Oxford (England) CPD Newsletter, and Elliott Laboratories Compliance Advisory Service Newsletters as well as other publications.

Significantly, he is the author of *EMCT: High Speed Design Tutorial* (ISBN 0-7381-3340-X) which is the source of some of the graphics used in this presentation. EMCT is available through Elliott Laboratories, co-branded with the IEEE Standards Information Network.

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