We have an opening for a **Signal/Power Integrity Engineering Lead** at eASIC.

- Experience – Mid to Senior level
- Job function – Engineering
- Employment type – Full-time
- Industry – Semiconductors

DUTIES & ESSENTIAL JOB FUNCTIONS

Senior Staff Signal/Power Integrity Designer is to oversee both Signal and Power integrity for world-class highly flexible transceiver solutions for multiple eASIC platforms, supporting over 20 protocols with several customer applications.

You will be involved in working with next generation serial and parallel interfaces along with system level PDN, etc.

DUTIES & ESSENTIAL JOB FUNCTIONS

- The successful candidate should have an excellent track record in the following areas:
- Signal integrity and Power Integrity
- Power integrity analysis for each PWR/GND domain: package extraction, simulation & decoupling strategy
- PDN Methodology Development: Simultaneous switching noise/output (SSN or SSO) analysis for each I/O PWR/GND domain.
- High speed I/O package design for PCI-E I & II, XAUI, 10G SerDes, FSB, DDR I, II, and III:
- Flip-chip bump or wirebond pad re-arrangement for chip-package-board co-design
- Optimal layer stackup & PWR/GND plane/island assignment to minimize voltage drop/noise/coupling.
- Crosstalk analysis and reduction.
- Design and model characterization boards, load boards, and system level test boards
- EMI reduction and shielding techniques.
- Running and developing communication system simulators
- Writing specification for design teams.
- Presenting design trade-off analyses and implementation recommendations with custom circuit designers

REQUIRED

- BSEE or MSEE
- 10 or more years of architecture experience with signal and Power integrity analysis

- Experience with lab equipment for high-speed digital systems
- Experience with using and developing transceiver modeling, analysis, and characterization tools
- Excellent technical communication through presentations and documentation
- Familiarity with the following tools and flows: Hspice, Sigrity (Power SI/XcitePI), Apache (Redhawk/Sentinel-PI), ANSYS (Q3D, HFSS, SIwave). 5 or more years of hands on experience in design, characterization, debug of high Speed SERDES ranging from 1G to 32Gbps.

Please reply directly to Mustansir Fanaswalla @ mfanaswalla@easic.com

ABOUT eASIC

eASIC is a semiconductor company offering a differentiated solution that enables us to rapidly and cost-effectively deliver custom ICs, creating value for our customers' hardware and software systems. Our eASIC solution consists of our eASIC platform which incorporates a versatile, pre-defined and reusable base array and customizable single-mask layer, our ASICs, delivered using either our easicopy or standard ASIC methodologies, and our proprietary design tools.

We believe this innovative technology allows eASIC to offer the optimal combination of fast time-to-market, high performance, low power consumption, low development cost and low unit cost for our customers. eASIC Corporation is headquartered in Santa Clara, California.