IEEE Distinguished Lecturer

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Prof. Dr. Joao Antonio Martino
Distinguished Lecturer of the IEEE Electron Devices Society
Chair of the IEEE EDS South Brazil Section
University of Sao Paulo, Brazil
Department of Electronics Engineering
Micro and Nanoelectronics Laboratory
Email: martino@lsi.usp.br

"Field Effect Transistors: From MOSFET to Tunnel-FET"

The Field Effect Transistor (FET) is the main device structure for the integrated circuits era. The starting point was the Lilienfeld patent filled in 1926 that was not fabricated due to the technological difficult. Experimental Metal-Oxide-Semiconductor FET (MOSFET) was only fabricated in 1960. The classical structure was composed by Aluminum (Metal), silicon dioxide (Oxide) and Silicon (Semiconductor). The MOSFET has been upgraded with different gate electrode like polysilicon heavily doped, TiN and TaN. The gate oxide has also been changed to SiON, HfO2, HfSiON and others. Finally the bulk silicon has also been modified to strained silicon (uniaxial and biaxial), SiGe and Silicon-On-Insulator (SOI). The structure of MOSFET has changed from planar to vertical multiple-gate devices like FinFET, Triple Gate and Gate all around. New structures like Tunnel FET devices (TFETs) have been studied to replace the conventional drift-diffusion conduction mechanisms due to the possible benefits obtained by tunneling conduction. Nanowire TFET devices will be also analyzed.

BIOGRAPHICAL DATA - PROF. DR. JOÃO ANTONIO MARTINO - 2013

João Antonio Martino was born in Sao Paulo, Brazil in 1959. He has two nationalities: Brazilian and Italian. He received the Electrical Engineering degree from Faculdade de Engenharia Industrial (FEI) in 1981. He received the M.Sc (NMOS Technology) and the Ph.D (CMOS Technology) degrees in 1984 and 1988 respectively in Electrical Engineering (Microelectronics) from University of Sao Paulo (USP), Brazil. He worked as a post-doctoral researcher in joint collaboration between IMEC/KUL, Leuven, Belgium and University of Sao Paulo, Brazil from 1989 to 1994 in SOI Technology. He was full professor and head of the Electrical Engineering Department at FEI from 1996 to 2005. He creates and was a head of Post-Graduate Program in Electrical Engineering (Microelectronic) at FEI from 2005 to 2006.

Now he is full Professor at Electrical Engineering Department of University of Sao Paulo, Brazil (since 2005) and head of Electrical Engineering Department at University of Sao Paulo (since 2009).

He is author and co-author of more than 300 technical journal papers and conference proceedings and author/editor of 5 books. He concludes the advisor work of 33 students (12 Ph.D and 21 master students).

He introduced the study of SOI devices characterization and technology in Brazil in 1990. He was the advisor (or advisor of the advisor) of every Ph.D researcher working on SOI in Brazil. He was also the head of the first fabrication of triple gate devices in Brazil.

His expertise is in the area of the electrical characterization, simulation and modeling of SOI devices at low/high temperatures, strain and radiation environment.

He is also interested in SOI-CMOS fabrication process and Multiple Gate devices. He fabricated **the first 3D transistor** (triple gate FinFET) in South America.

Recently he is working in FB-DRAM memories fields (Floating Body Dynamic Memory Cell without capacitor) and Tunnel-FETs in collaboration between University of São Paulo and IMEC/Belgium.

He is Senior Member of IEEE, Member of Electrochemical Society and the Chapter Chair of South Brazil Session of IEEE – Electron Device Society (EDS) since 2007. He is a Distinguished Lecturer of EDS/IEEE since 2008. He is Vice-Chair of EDS/IEEE Region 9 since 2011.

He became researcher level 1A on microelectronics/nanoelectronics field in Brazil in 2012, given by the main Brazilian Federal Sponsor (CNPq/Brazil), which is the highest level in Brazil. There are only 6 people in Brazil in this position and he is the only one at University of Sao Paulo, which is the first University of the Latin America ranking.