Clock and Data Recovery in High-Speed Wireline Communications

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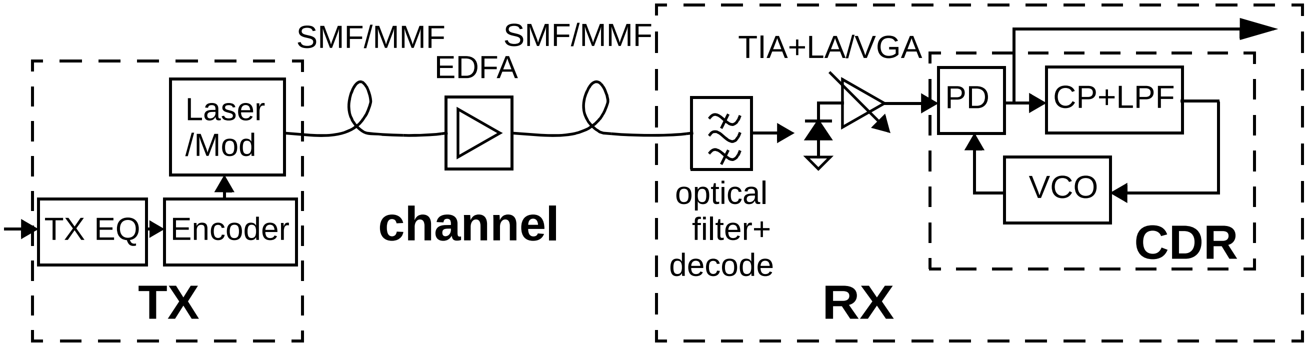
Outline

- **Introduction**
- **Conventional Design Strategy**
  - *System*
  - *Architecture*
  - *Circuits*
- **Hybrid Oversampling CDR**
- **Design Example**
- **Conclusion**

Introduction

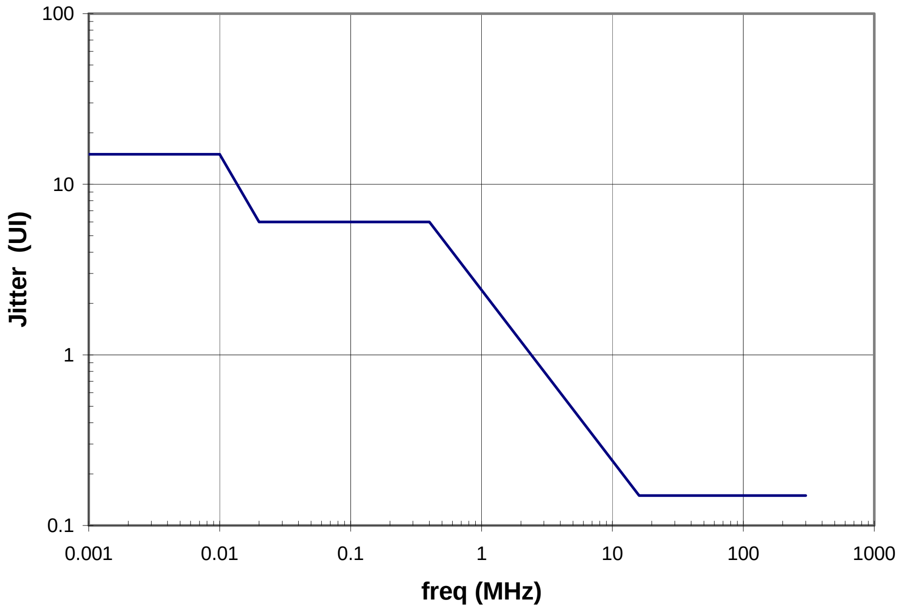


- **Input at the receiver:**
  - *Jitter - timing deviation from ideal phase*
  - *Wander - low frequency timing variations*
  - *Noise - voltage-domain fluctuations*
  - *Asynchronous to any clock in the system*
- **Clock and Data Recovery (CDR) widespread in communication systems**
- **Extracts clock from the incoming data stream and synchronizes the data with the clock**
- **Often performs demultiplexing to a lower data rate**

CDR Design Requirements

- **Specifications**
  - *Bit Error Rate (BER)*
  - *Electrical specifications*
  - *Jitter Tolerance*
  - *Jitter Transfer*
  - *Alarms specifications (Loss of Lock, Loss of Signal)*
  - *Power limit*
  - *Consecutive Identical Digits (CID)*

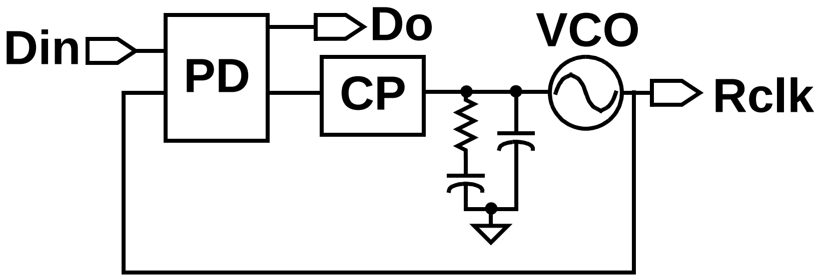
SONET OC-768 Jitter Tolerance Mask

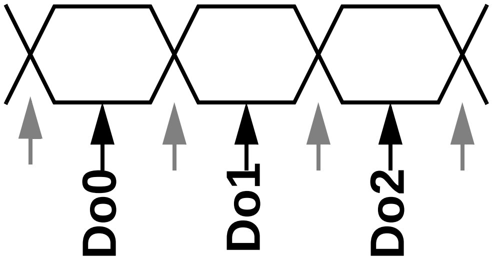


- **Specific requirement for particular system**
  - *Optical system may require phase adjust*
  - *Multi-bit-per-symbol signaling (e.g. PAM-4, duobinary) may require locking to specific edges*

CDR Architecture

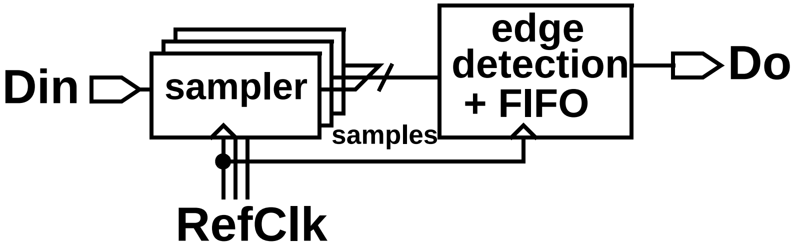
Phase-tracking

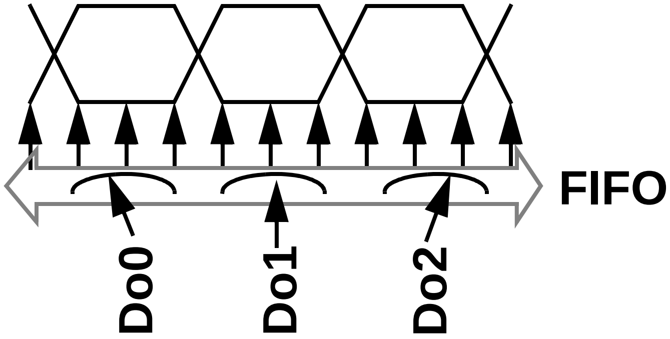




- Feedback architecture
- Center samples hard-wired to output
- CDR loop tracks low-frequency jitter
- Low-jitter VCO for high-freq. jitter tolerance

Blind oversampling



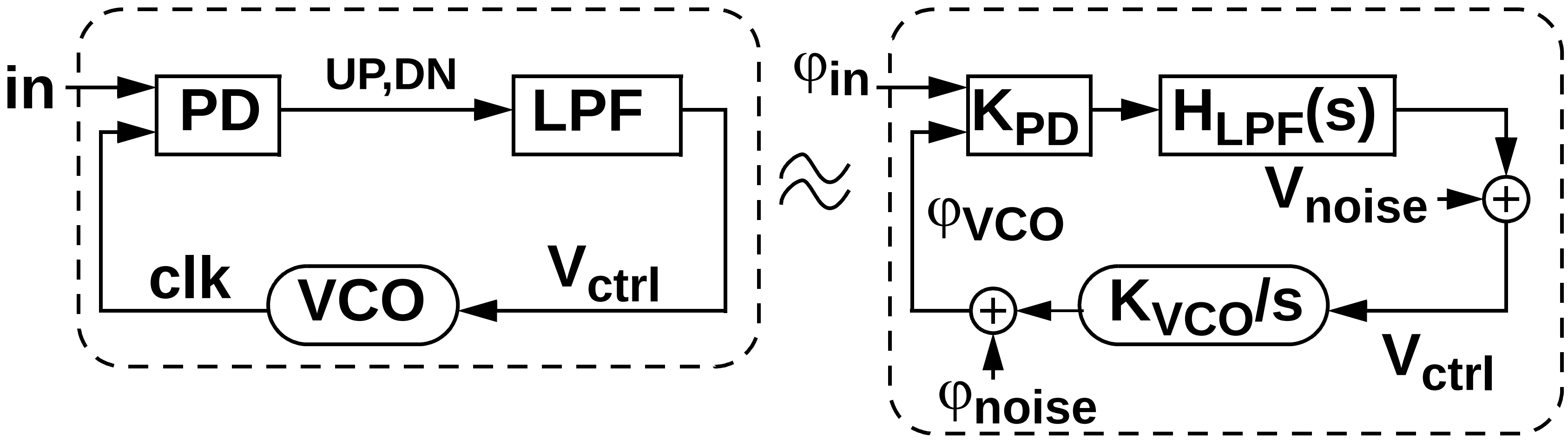


- Feedforward architecture
- Transitions detected from several samples per UI
- Inserting or removing bits from FIFO tracks low frequency jitter

CDR Implementations

- **Rate**
  - *Full rate:* $f_{VCO}/f_{DATA}=1$
    - Simplest architecture
    - Most challenging implementation
  - *1/n rate (1/2 rate, 1/4 rate etc)*
    - Requires multiple clock phases, multiple samplers
    - Tradeoff between simplicity of architecture and ease of implementation
    - Limited by phase deviation
- **Loop linearity**
  - *Linear CDR*
    - Phase detector output linear function of the phase error between input and VCO
    - Allows use of linear model, predictable modeling
    - Hard to implement at high data rates
  - *Bang-Bang CDR*
    - Phase detector reacts only to the sign of the error between input and VCO
    - Notoriously hard for modeling
    - Much easier to implement

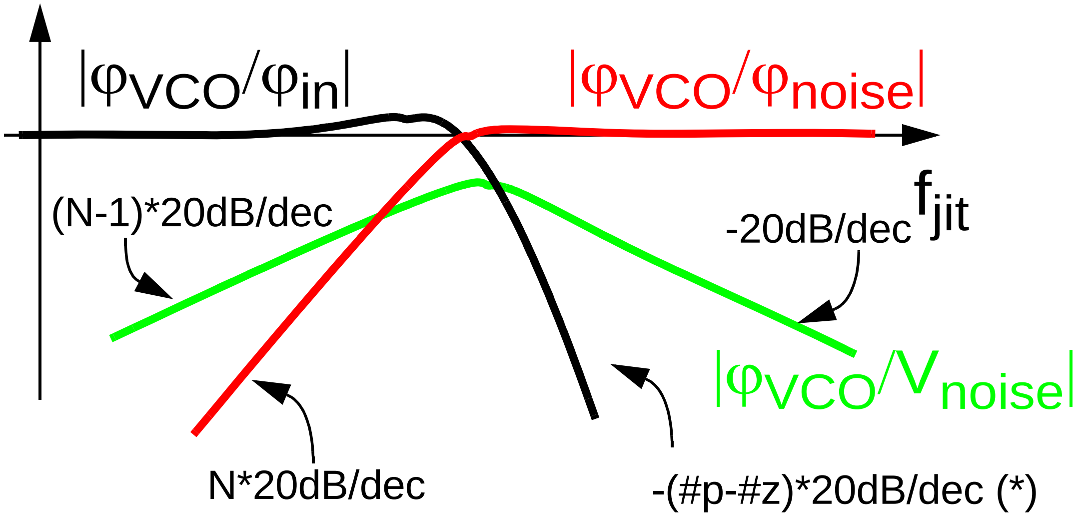
Linear Model



$$\beta A = K_{PD} \cdot K_{VCO} \cdot \frac{H_{LPF}(s)}{s}$$

- **Linear analysis from control systems possible and extremely useful**
  - *Stability, loop bandwidth, jitter transfer, steady-state error, noise transfer function...*
- **Linear model is only an approximation (sometimes crude)**
  - *Nonlinearities limit usability of the model, e.g. bang-bang PD*

Linear Model (cont'd)



$$\boxed{\beta A(s) = K\cdot\frac{P(s)}{s^N\cdot Q(s)}}$$

$$\varphi_{VCO}(s) = \underbrace{\left(K\cdot\frac{P(s)}{s^N\cdot Q(s)+K\cdot P(s)}\right)\cdot\varphi_{in}}_{\text{Jitter Transfer}} + \underbrace{\left(\frac{s^N\cdot Q(s)}{s^N\cdot Q(s)+K\cdot P(s)}\right)\cdot\varphi_{noise} + \left(\frac{s^{N-1}\cdot Q(s)\cdot K_{VCO}}{s^N\cdot Q(s)+K\cdot P(s)}\right)\cdot V_{noise}}_{\text{Jitter Generation}}$$

(*) #p-#z = difference between orders of denominator and numerator of βA

- **Output jitter has two components**
  - *Low-pass input jitter transfer*
  - *High-pass / band-pass jitter generation*

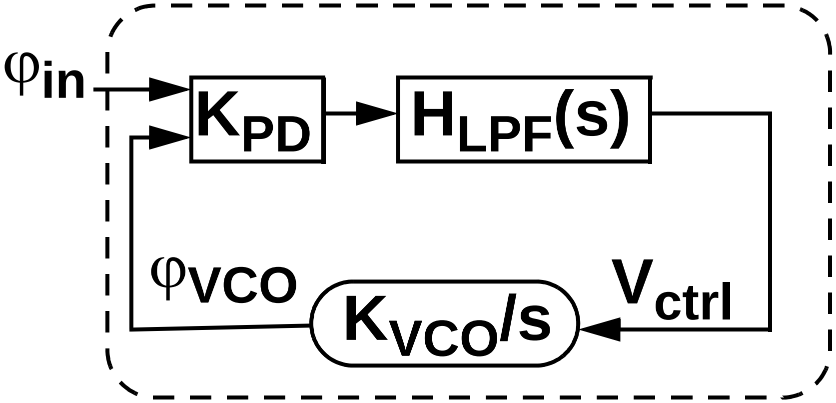
Design Strategy: System, Architecture, and Circuits

CDR Design Strategy: System

- **1) Choose technology if possible**
  - *CMOS slow but cheap, widely available, easy to integrate and low-power*
  - *III-V Compounds (GaAs, InP) - much faster but expensive and high-power*
  - *BiCMOS (e.g. SiGe)*
- **2) Decide architecture**
  - *Feedback phase tracking CDR dominant*
    - Simple, well understood, capable to support high data rates, relatively low power
  - *Blind oversampling only if wander is small*
  - *Special architecture for given application (e.g. burst, MIMO)*
- **3) Based on application, data rate, and available technology choose loop linearity type and rate**
  - *Bang-bang loop faster thus preferrable in high-speed applications*
  - *Linear loop easier to control and model thus preferrable at lower speeds*
  - *Choose highest rate that the technology can accommodate*
    - VCO frequency, sampler frequency and aperture usually critical

Design Strategy: Loop BW and Type

- **4) Choose loop bandwidth**
  - *Loop BW↑ ⇒ input noise transfer ↑, VCO noise generation ↓*
  - *BW lower bound: the knee of jitter tolerance characteristics*
  - *Upper bound: defined by bandwidth of jitter transfer if specified, ultimately by loop stability*
- **5) Choose loop type, gain, and numbers of poles and zeroes**
  - *Normally defined by loop filter*
  - *Desired type-II (two poles at f=0) for zero steady state error for a frequency step*
    - One 1/s term from phase integrating function of the VCO
    - Additional 1/s term from loop filter - typically done by an active circuit (e.g. charge pump)
  - *Simplest loop filter:*



$$H_{LPF}(s) = \frac{K_{CP}}{s}$$

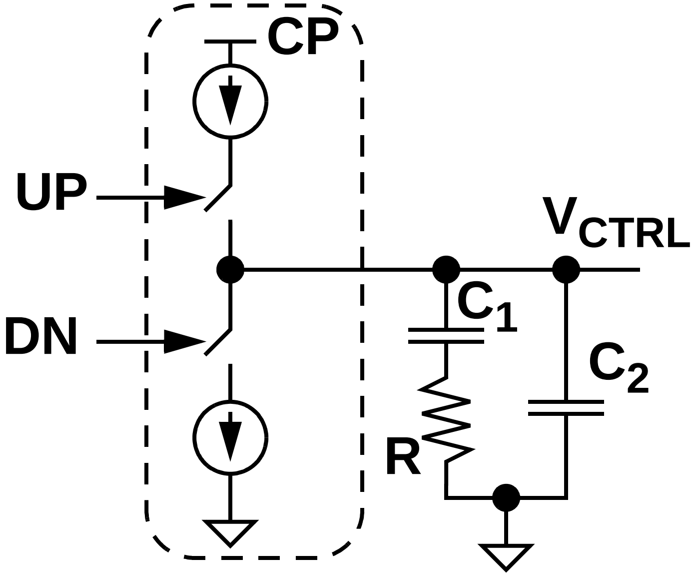
  - *Unfortunately, with above loop filter, the system becomes unstable*
    - Closed loop poles on imaginary axis

Loop BW and Type (cont'd)

- Need a stabilizing zero:

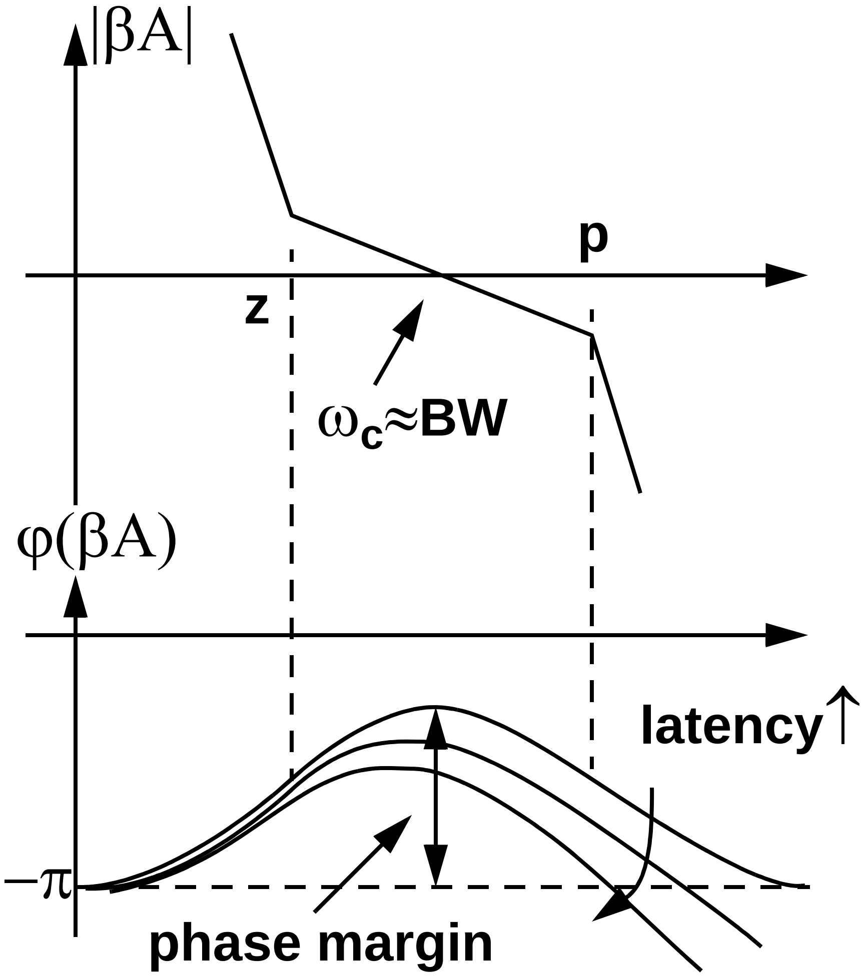
$$H_{LPF}(s) = \frac{K_{CP}\cdot(1+sC_1R)}{sC_1\cdot\left(1+s\left(\frac{C_1C_2}{C_1+C_2}\right)R\right)} = \frac{K_{CP}\cdot(1+s/z)}{sC_1\cdot\left(1+\frac{s}{p}\right)}$$

- High-frequency pole in the filter is due to parasitic capacitance at V_{CTRL}, also useful to suppress spurs



Design Strategy: Pole / Zero Positioning

- 6) Determine pole/zero position



For maximum phase margin:

$$\omega_C = \sqrt{zp}$$

$$PM = 2arctg\left(\sqrt{\frac{p}{z}}\right) - \frac{\pi}{2}$$

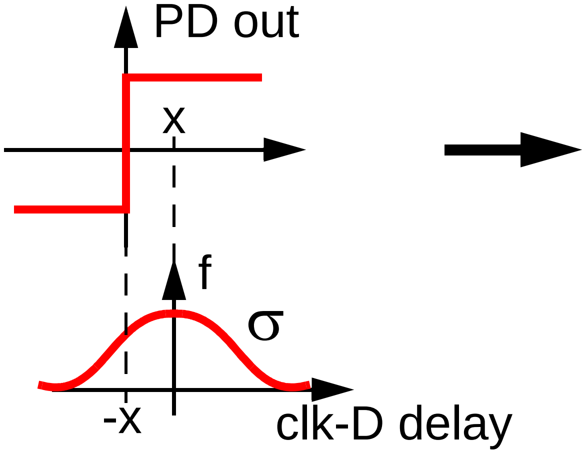
For PM=60º, ω_c=BW

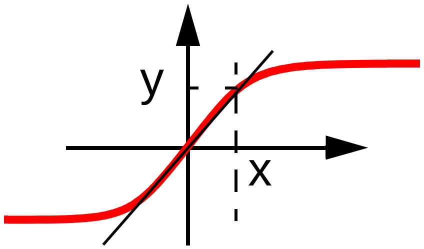
⇓

p/z≈14

Design Strategy: Pole / Zero Positioning (cont'd)

- **In a bang-bang system, concept of transfer function and bandwidth does not exist**
- **Still possible to design having in mind that bandwidth depends on amplitude of disturbance**
- **Statistically, gain of PD can be linearized through VCO jitter and/or input jitter**
  - *Implies the system parameters such as bandwidth, jitter transfer, peaking etc depend on noise !*
  - *A wide design margin should be allocated*

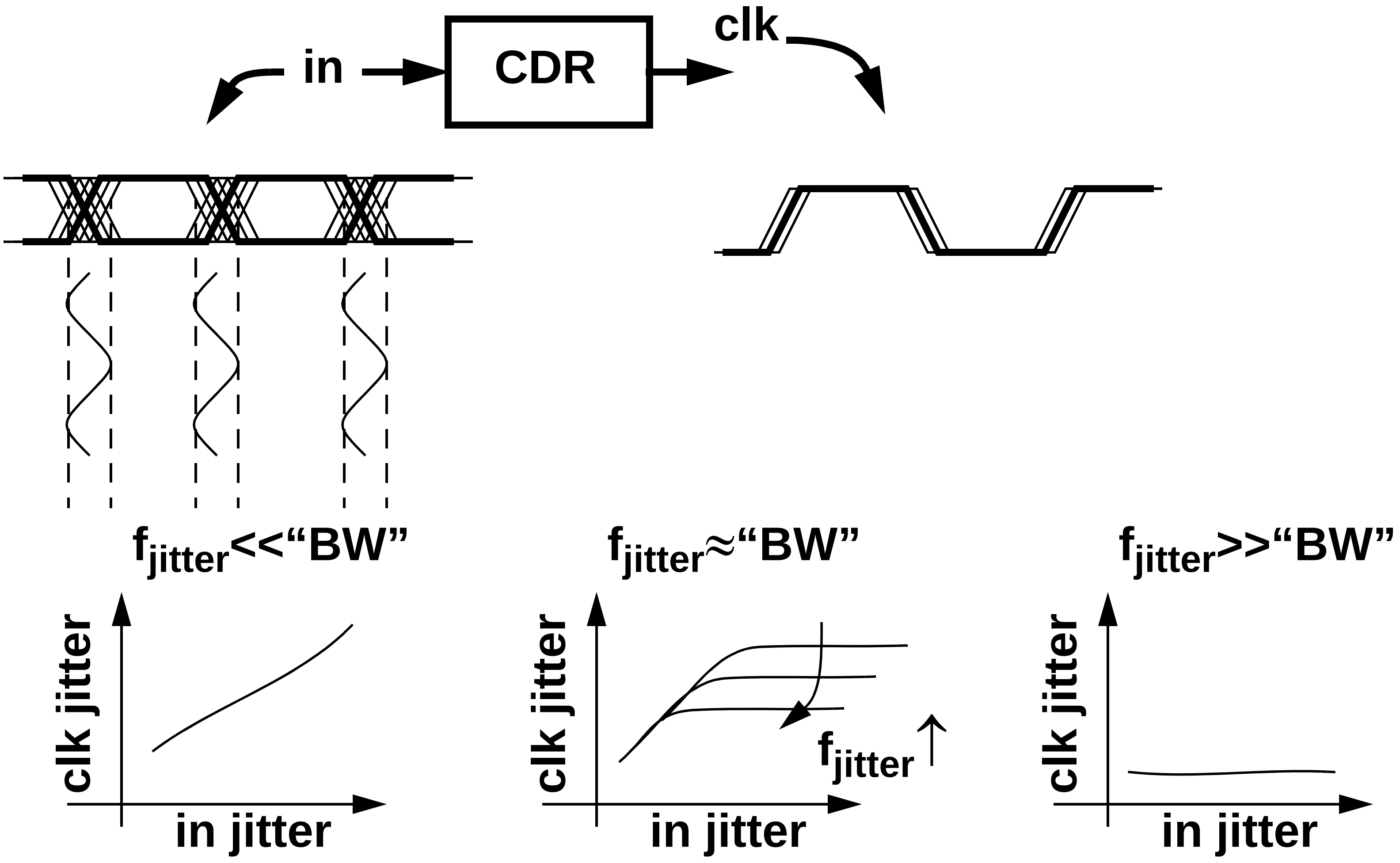




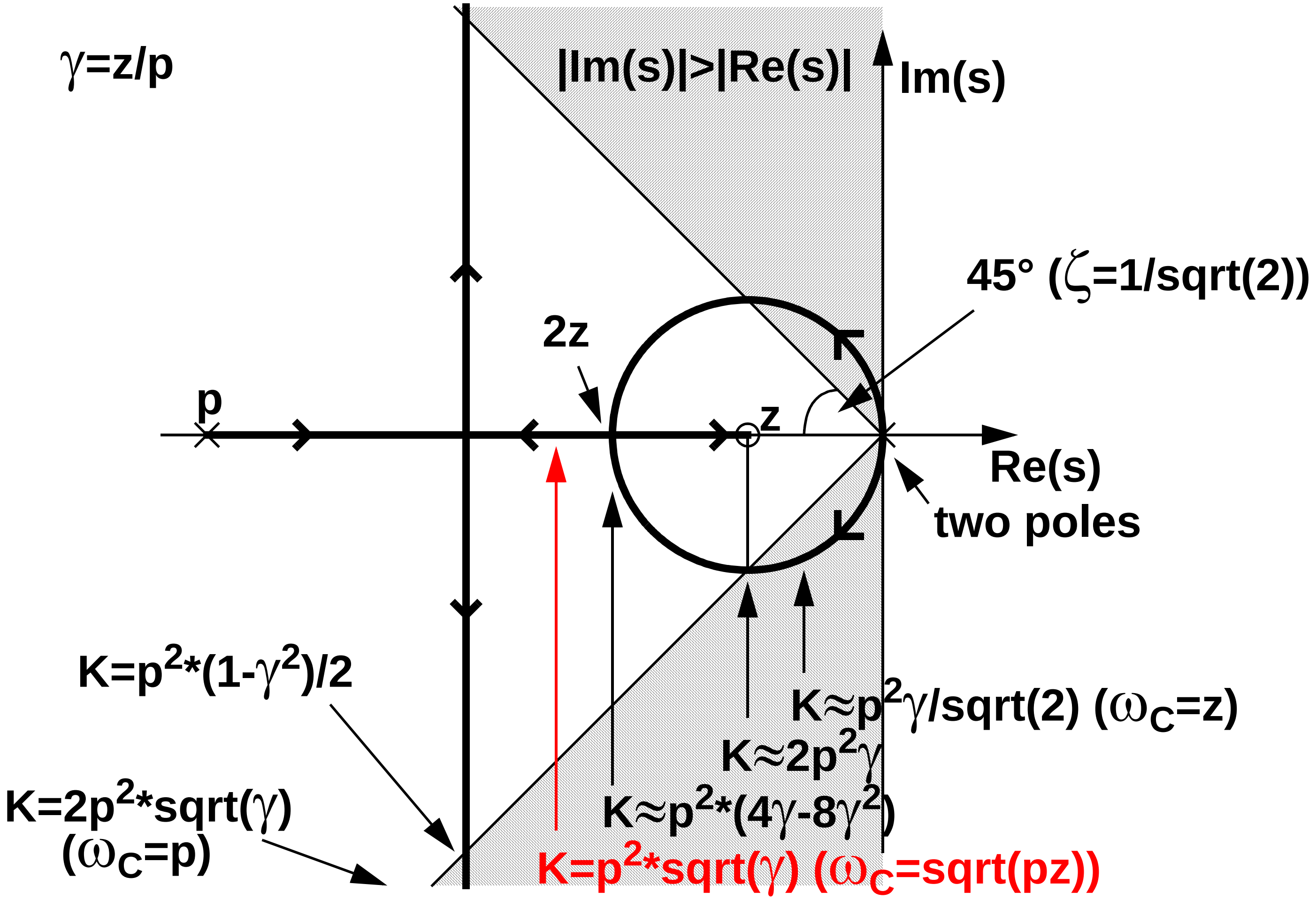
$$y(x) = -\int_{-\infty}^{-x} f(t)dt + \int_{-x}^{\infty} f(t)dt = 1 - 2F(-x)$$

$$gain \approx \left.\frac{\partial y}{\partial x}\right|_{x=0} = 2f(0) \xrightarrow{\text{gaussian}} gain \approx \frac{1}{\sigma}\cdot\sqrt{\frac{2}{\pi}}$$

Design Strategy: Pole / Zero Positioning (cont’d)



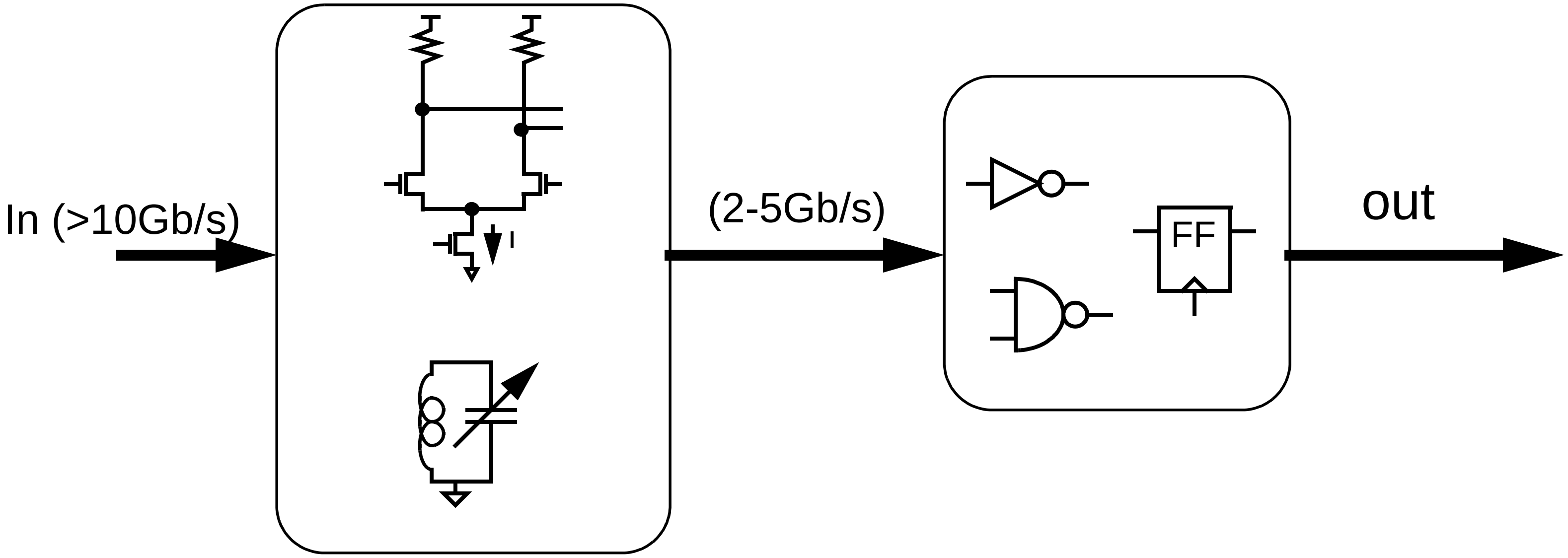
Design Strategy: Root Locus



- **K widely varies in non-linear CDR**
  - *Design for wide margin*
  - *About 4x span for K available for damping factor $\zeta>1/sqrt(2)$*

Design Strategy: Circuit Style

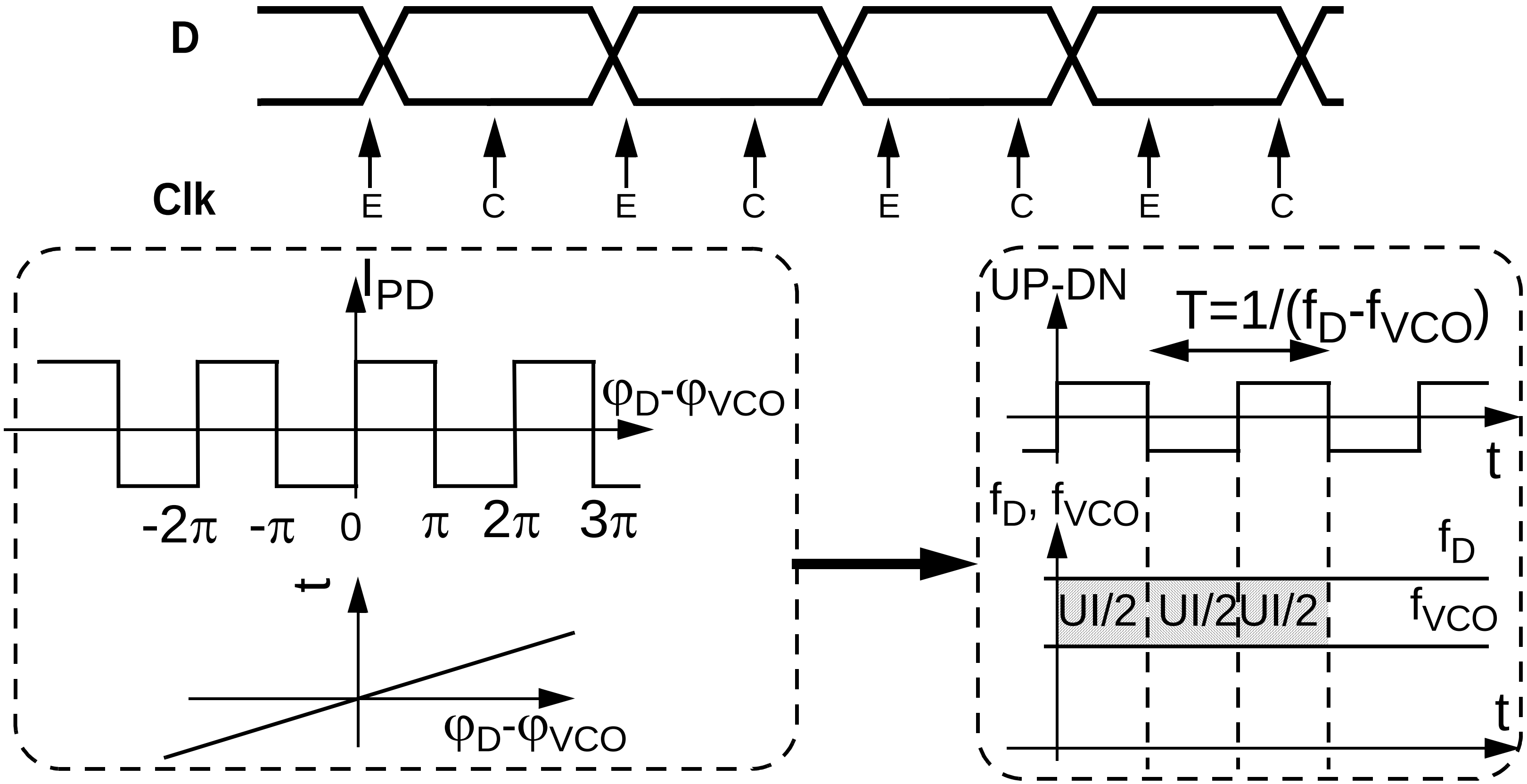
- **7) Choose circuit style**
  - *In bipolar technology, typically a current-mode logic (ECL)*
  - *In CMOS, choice between current mode logic (CML) and static CMOS*
    - Static CMOS very appealing choice as it can dramatically reduce power consumption [Toifl, ISSCC2007]
    - Very few processes today allow 10Gb/s+ operation in full static CMOS
    - Trade-off: use fast and power hungry CML in front-end, use static CMOS as soon as it can accommodate data rate (usually after DEMUX to two to eight bits).



Design Strategy: Architecture

- **8) Choose CDR transient locking behavior**
  - *Lock range is the maximum difference between VCO clock and data rate for which lock is achieved without a cycle slip*
    - All recovered data are valid
    - Useful for burst CDRs, less for continuous mode CDRs
  - *Pull-in range is the maximum difference between VCO clock and data rate for which lock is eventually achieved*
    - cycle slips allowed, some data may be invalid
    - Most important parameter for conventional continuous mode CDRs
  - *Plenty of literature on lock/pull-in properties of PLLs, most for first or second order loops and/or oversimplified*
  - *Pull-out range is maximum difference between VCO clock and data rate for which CDR stays in lock*

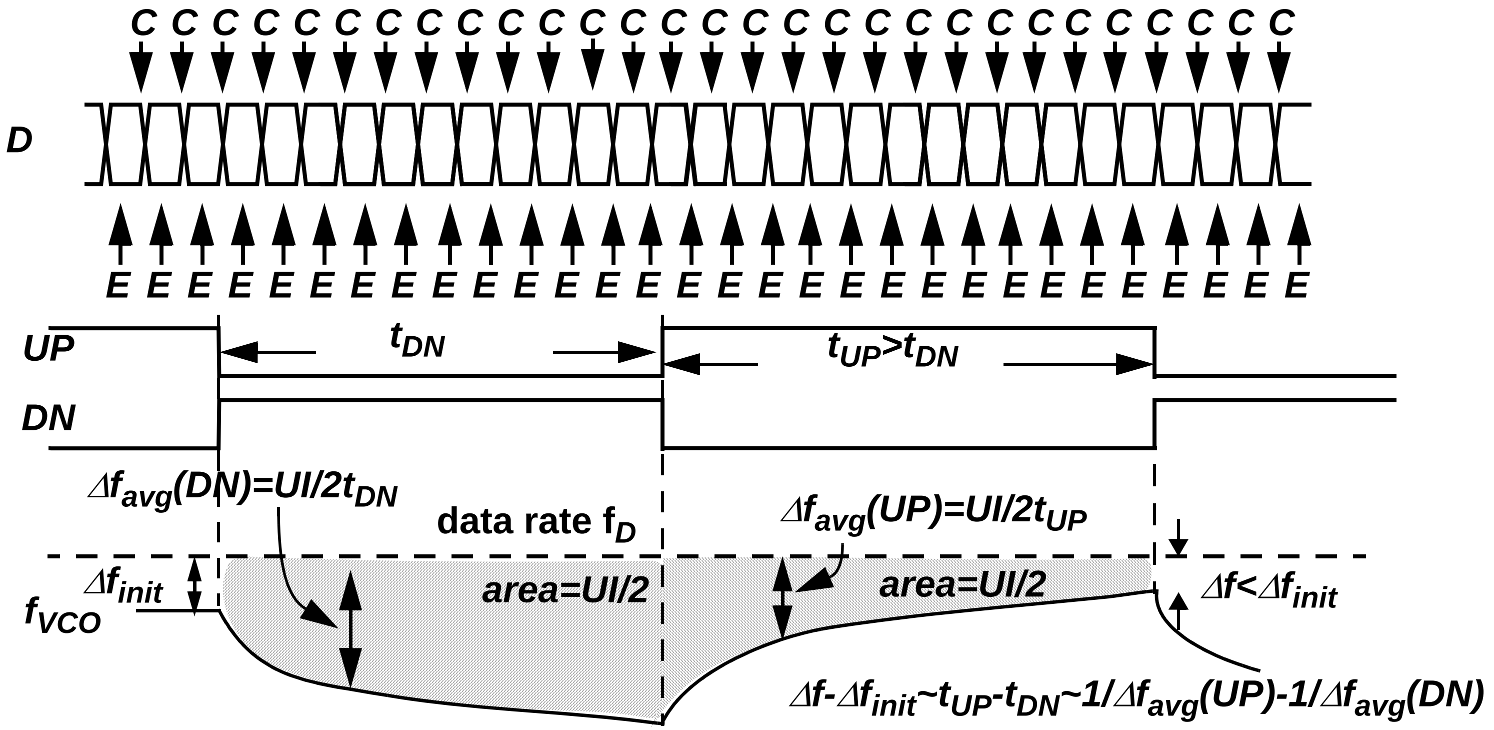
CDR Lock and Pull-In



- **If VCO and data frequencies differ, VCO clock "sweeps" data eye**
- **PD output has a beat frequency component equal to f_D-f_{VCO}**
- **Area between f_D and f_{VCO} is equal to one unit interval (UI) over one beat period**

CDR Lock and Pull-in

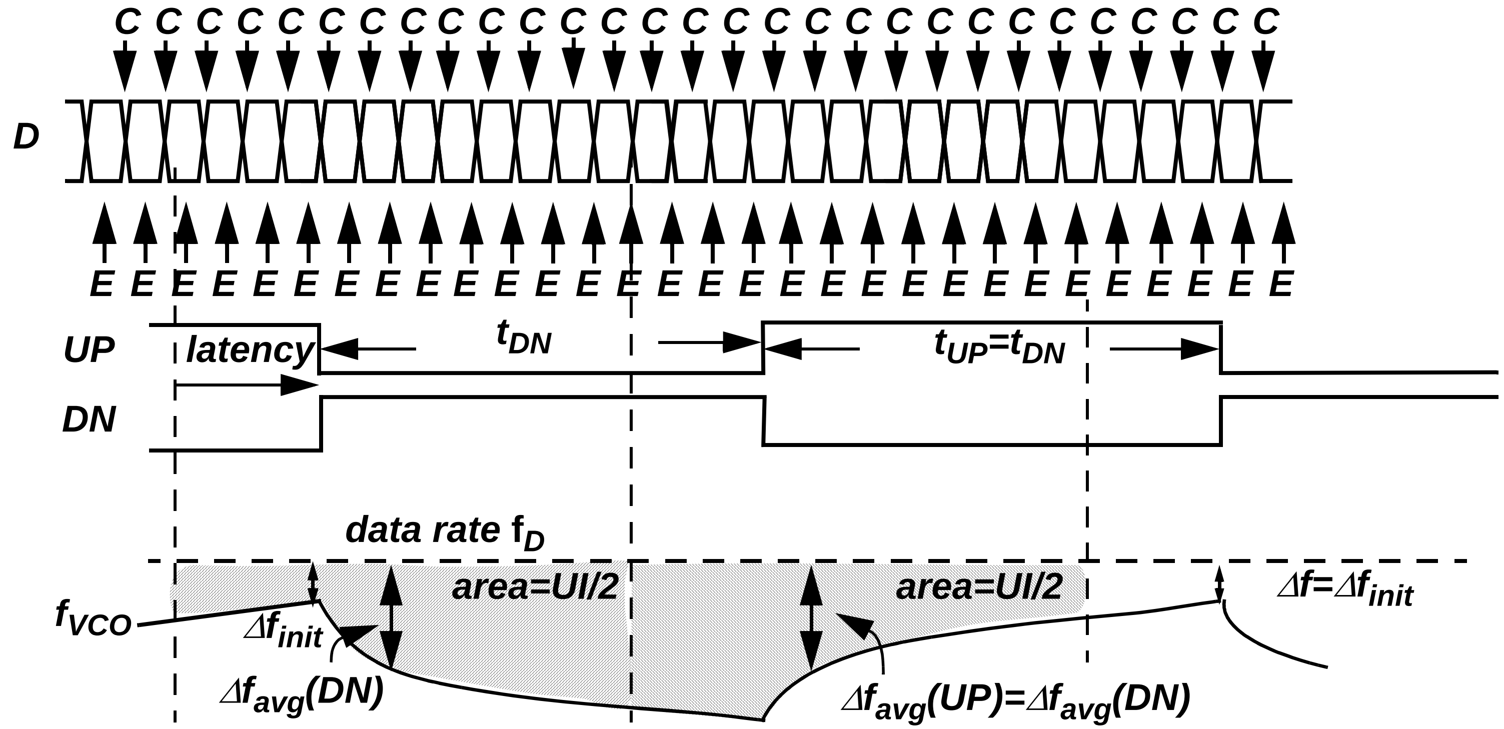
- 3rd order type-II bang-bang CDR, f_{VCO} slightly slower than f_D



- Pull-in happens when f_{VCO} converges towards f_D in one DN-UP cycle
- Change of f_{VCO} in one UP/DN cycle proportional to difference of inverses of average Δf's in UP and DN cycles.
  - *Ideally, $\varphi(PD\rightarrow V_{ctl})<\pi/2 \Rightarrow$ pull-in range is equal to tuning range*

CDR Pull-in with Latency in the Loop

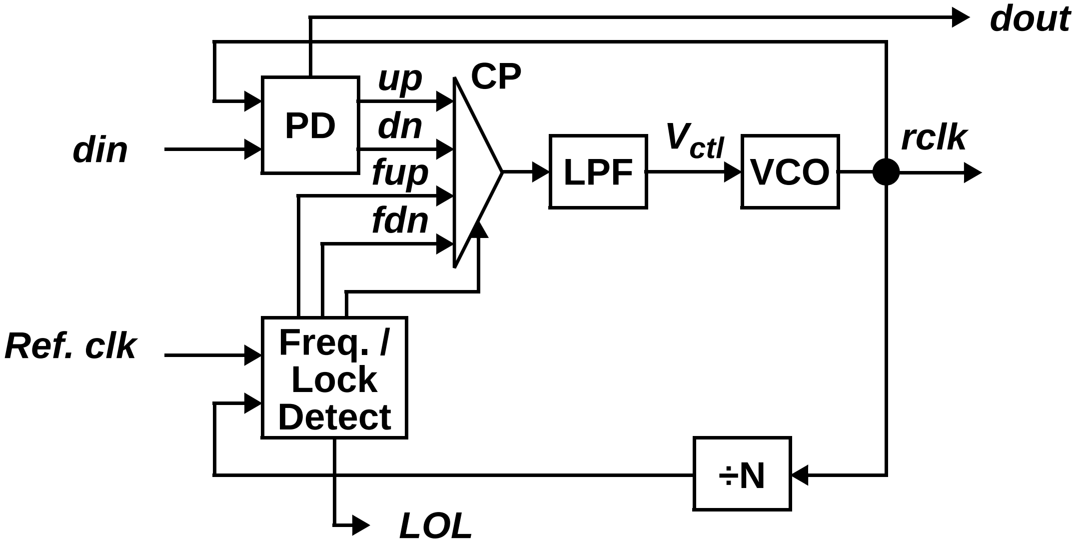
- **Pull-in in 3rd order type-II CDR with latency in the loop**



- **Pull-in depends on the phase of the loop gain**
  - *If* $\varphi(\beta A(s=j|\omega_{VCO}-\omega_D|))=-\pi$*, there is no pull-in (false lock)*
- **Pull-in limited by latency of PD/DEMUX**
  - *A safe pull-in range is about loop bandwidth as there is a defined phase margin for stability (latency acounted for)*

Aided Frequency Acquisition

- As pull-in can be guaranteed only for a few hundred ppm around data rate, phase tracking CDR's use aided frequency acquisition
- Most common: dual loop



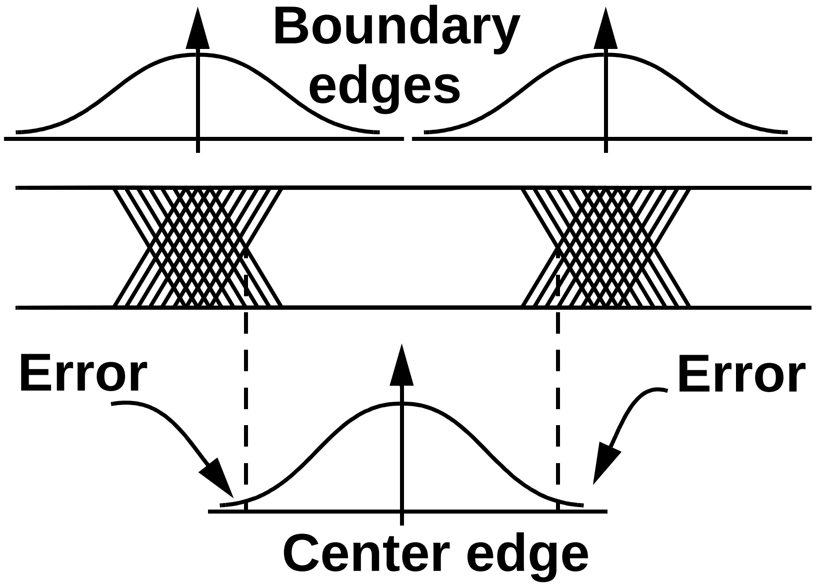
- Frequency detector monitors the frequency difference between rclk and Ref. clk
  - *Switch to frequency acquisition loop if greater than a threshold*
  - *Switch to phase loop if less than a threshold*

Design Strategy: Architecture (cont’d)

- **9) Determine specifications for key circuit blocks**
  - *Sampler*
    - Frequency = data rate / CDR rate
    - **Aperture << unit interval (UI)**
    - Power
    - Offset
  - *VCO*
    - Tuning range. Typically 10% of the center frequency for LCVCO, wider for ring VCO
    - **Phase noise ↔ cycle-to-cycle jitter. Typical target -100dBc/Hz @ 1MHz offset**
    - Phase deviation and phase adjustment
    - Power
  - *Demultiplexer (optional)*
    - Timing
    - **Power**
  - *Charge pump*
    - ON current - depends on the value of filter capacitances
    - **Output resistance >> filter resistor, VDD/I_{CP}**
    - **Operating range**
    - Leakage
- **Behavioral simulation essential!**

Effect of Circuit Parameters on CDR System Performance

- **Bit error ocurrs when the center edge samples adjacent (wrong) bit due to**
  - *Random VCO jitter*
  - *input jitter (assumed deterministic)*
  - *VCO phase deviation*
  - *Sampler aperture*
  - *Sampler offset*
  - *Sampler history*
- **For BER=10^{-12}, jit$_{in}$=0.3UI, k=0.7 → σ_{CL}<0.028UI**
  - *About 700fs @ 40Gb/s*
- **σ_{CL} is a function of loop BW and cycle-to-cycle VCO jitter $\sigma_{c\text{-}c}$**
  - *Typically $\sigma_{c\text{-}c}$=x10fs*



$$BER = erfc\left(\frac{k \cdot UI - jit_{in}}{2\sigma_{CL}\sqrt{2}}\right)$$

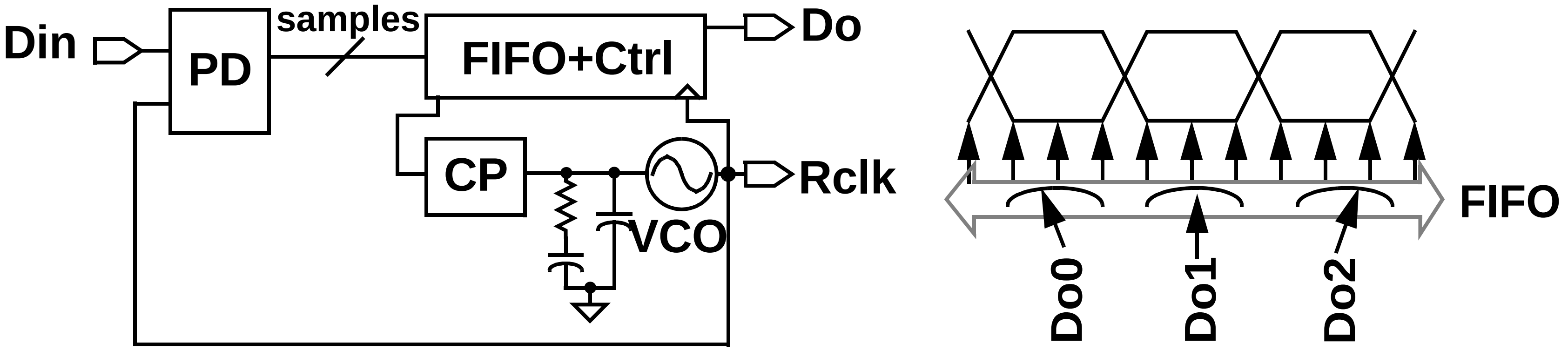
$$\sigma_{cl} = \sigma_{c-c}\sqrt{\frac{f_{OSC}}{\pi BW}}$$

Summary - Part I

- **CDR linear model useful but one must be aware of limitations**
- **High-speed design - severe nonlinearities**
- **Concurrent system, architecture, and circuit design needed**
  - *Circuit specifications depend on architecture, system specifications*
  - *Loop dynamics depends on circuit non-idealities*
- **Behavioral simulation necessary**

Hybrid Oversampling CDR

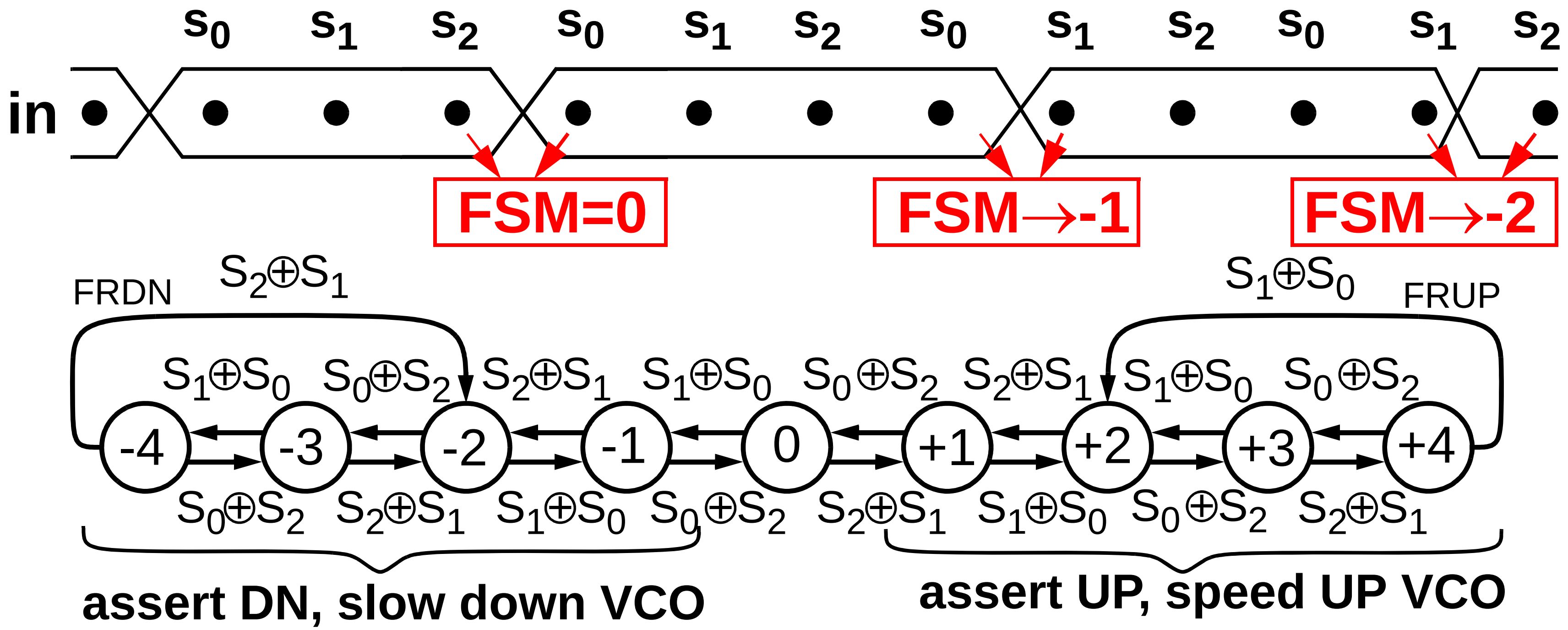
Hybrid CDR Architecture



- **Detect edge positions as in blind oversampling and lock to these edges as in phase tracking CDRs**
- **Output data are the samples furthest from the transition**
- **CDR loop only needs to loosely track low-frequency jitter**
  - FIFO tracks high-frequency jitter
  - Maximum tolerable phase error > 1UI, depends on FIFO depth
- **Oversampling allows seamless lock directly from data and suppresses some VCO jitter**

Hybrid CDR: Principle of Operation

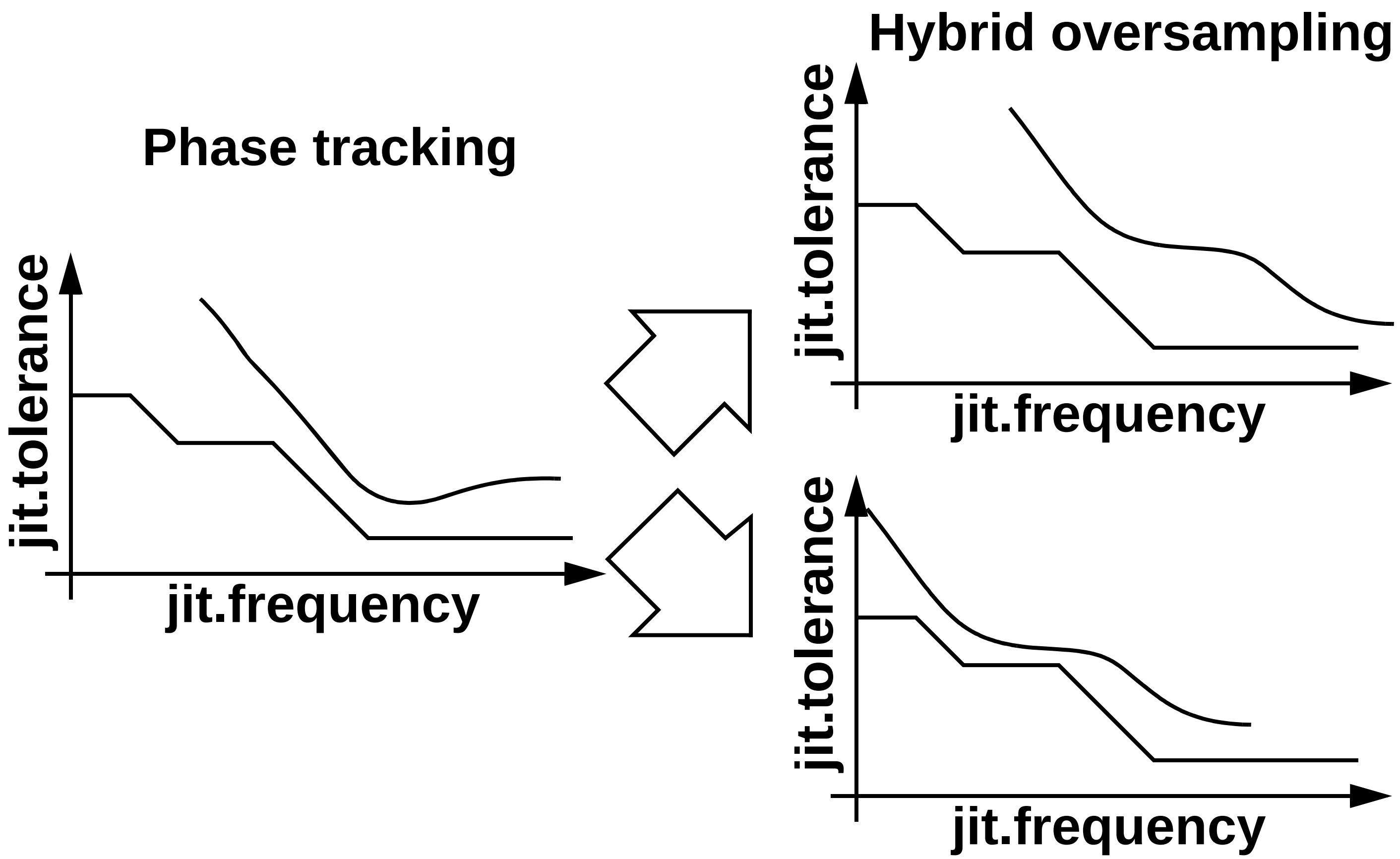
- **Sample more than two times per UI, detect phase by comparing adjacent samples**
  - *Detect the **direction** of the phase error*
  - *Operating range of the phase detector > 2π*
- **Keep track of the detected phase in Finite State Machine (FSM)**
  - *Each position in FSM represents a discrete amount of phase error*
- **Send the phase information to VCO for clock recovery**



assert DN, slow down VCO

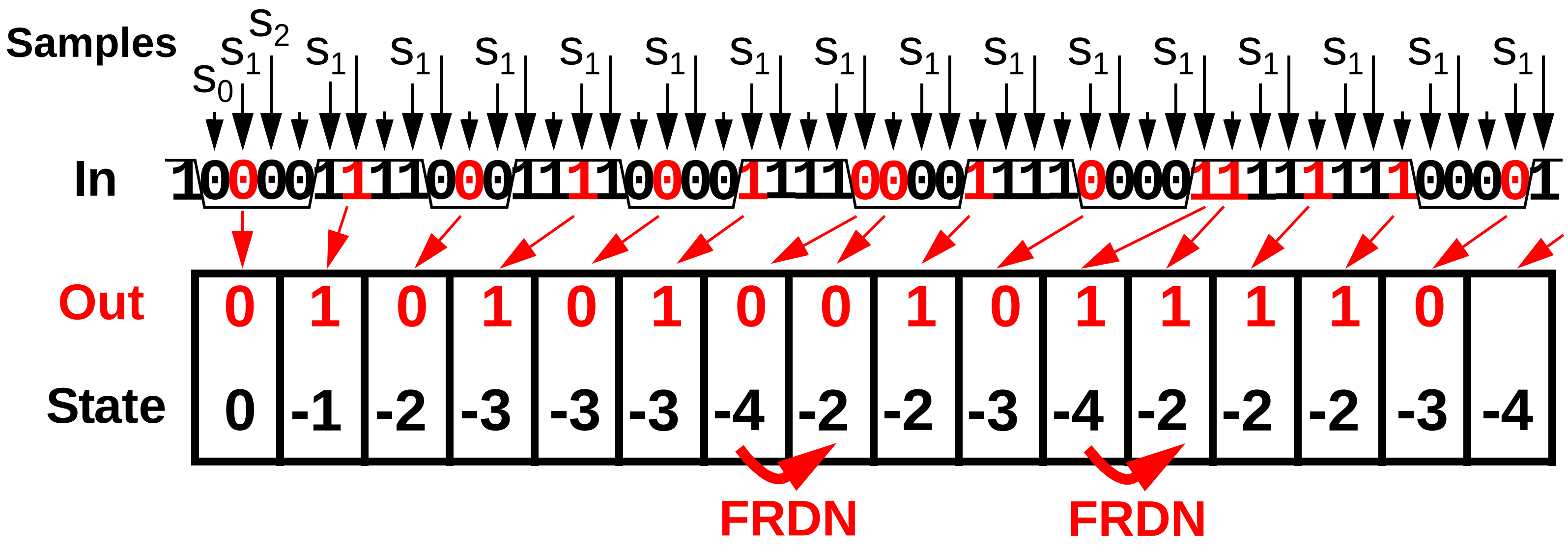
assert UP, speed UP VCO

Hybrid Oversampling CDR: Strategy Revision

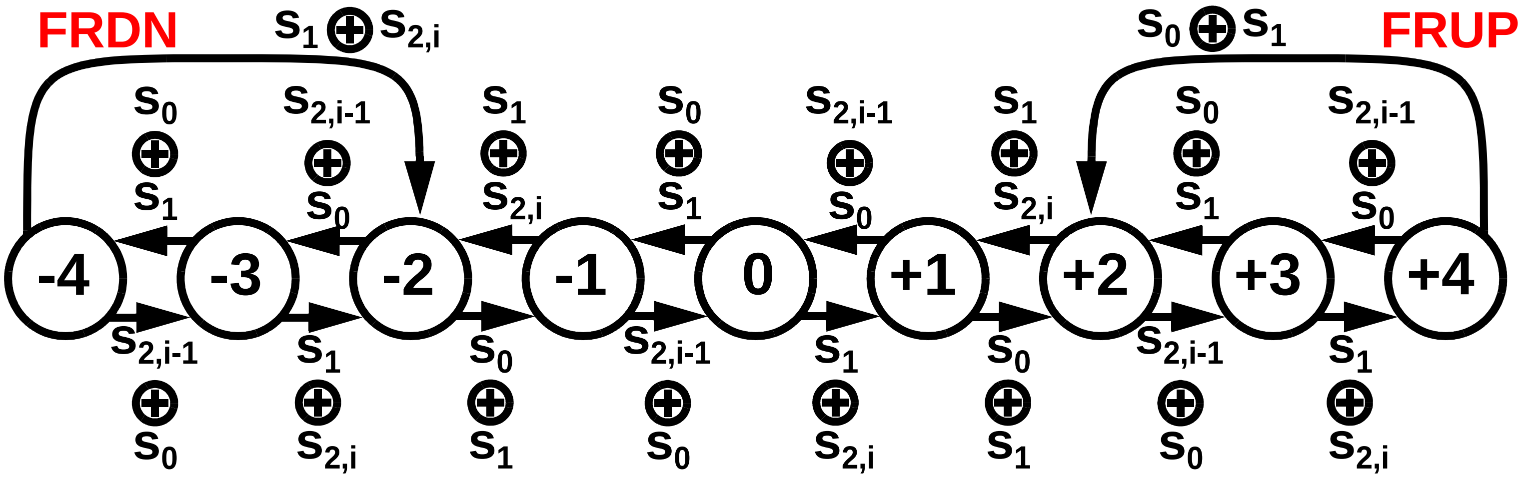


- **Loop bandwidth can stay same for more design margin, or it can be reduced for better input jitter tolerance**

Hybrid Oversampling CDR: Frequency Acquisition

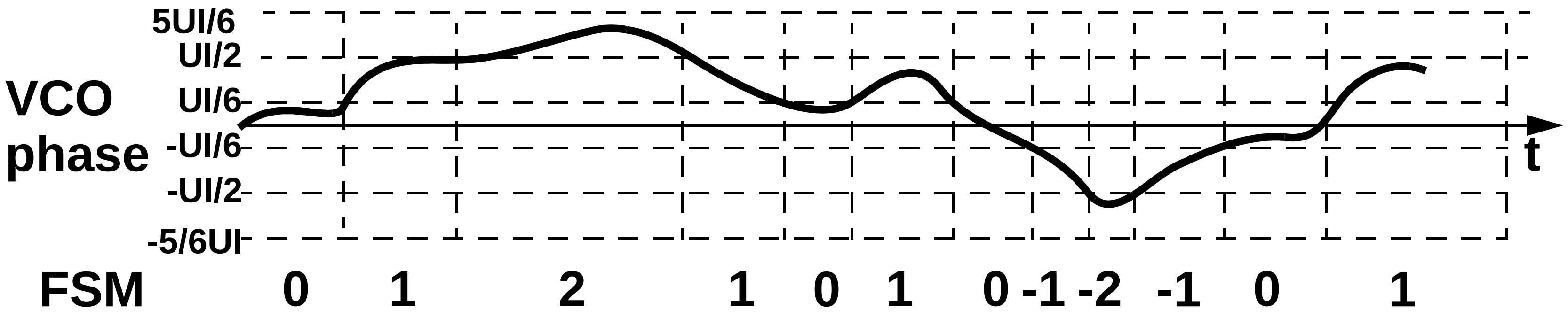


Out	0	1	0	1	0	1	0	0	1	0	1	1	1	1	0	
State	0	-1	-2	-3	-3	-3	-4	-2	-2	-3	-4	-2	-2	-2	-3	-4



Hybrid Oversampling CDR: Effect of Circuit Parameters on Performance

- **Bit error ocurrs when the VCO wanders during CID so phase tracking direction is erroneous (bit skip)**

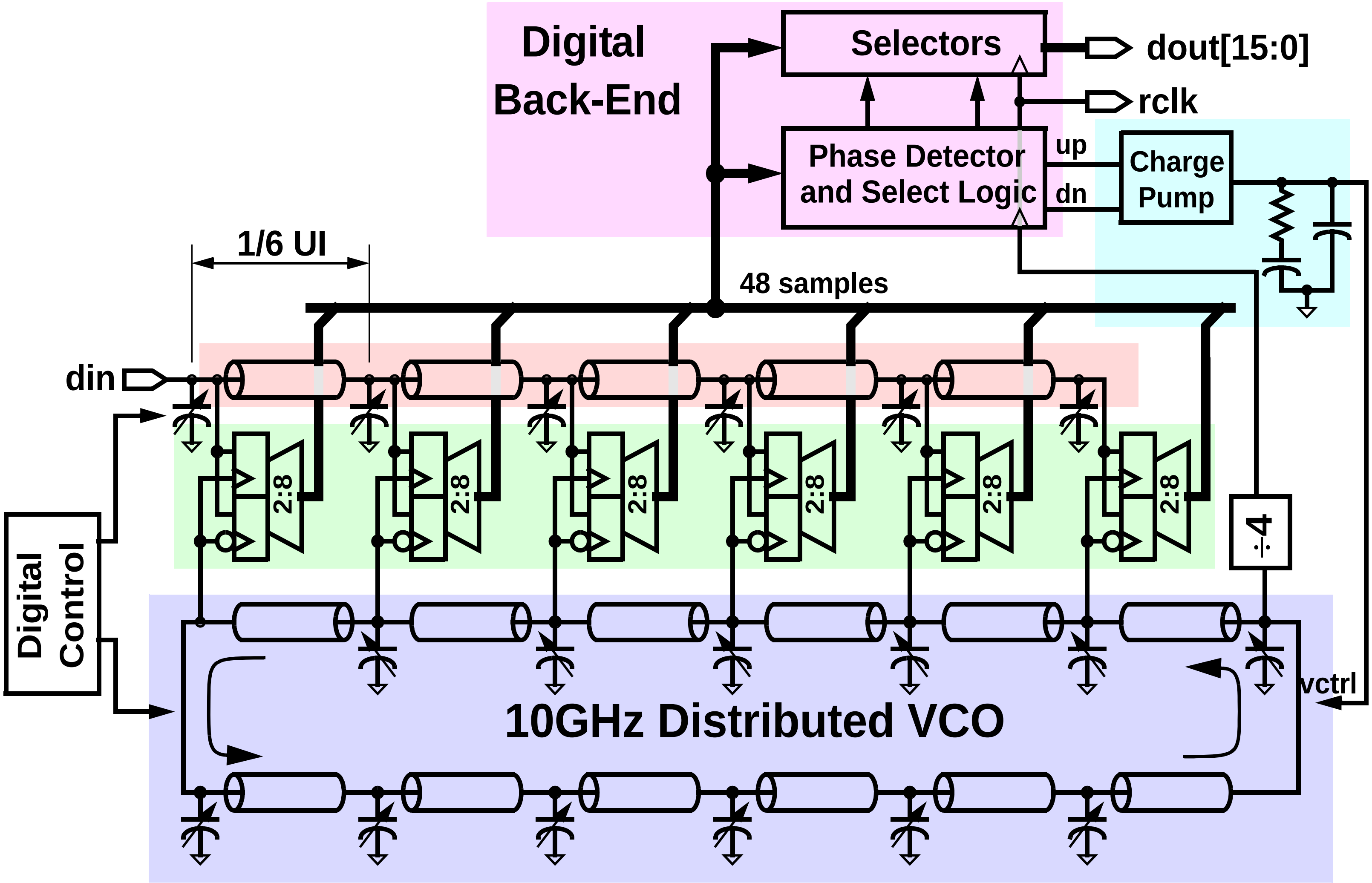


- **Expression for VCO jitter tolerance is complex and not enlightening, however some insight is possible**
  - *Gradual changes in phase due to accumulating VCO jitter tracked by the FSM*
  - *Break dependency of BER on loop bandwidth*
    - Hybrid scheme has much higher tolerance to VCO jitter than phase tracking CDR
    - Potential direction for deep submicron technologies that suffer from relative increase of noise, jitter
- **Tighter specification for sampler aperture**

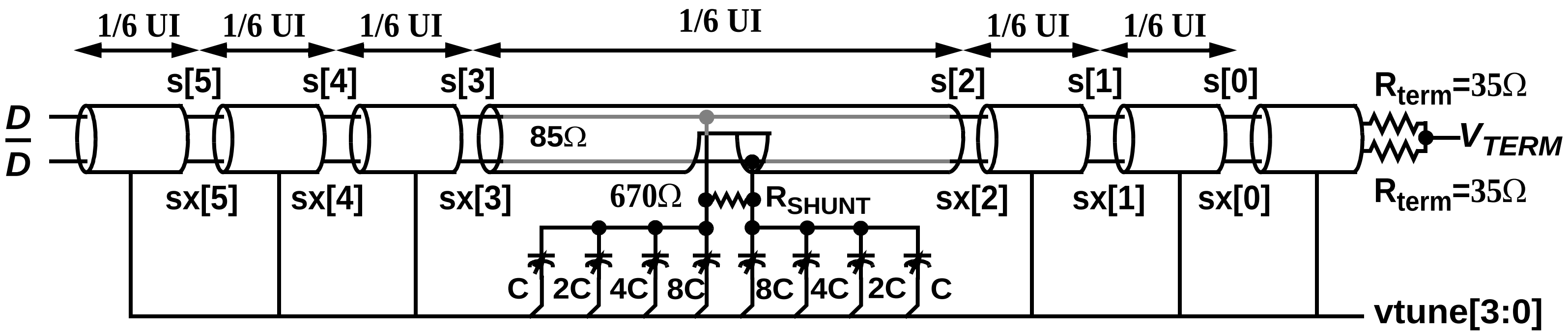
Design Example

Circuits: Design Example

- **40Gb/s 3x oversampling hybrid CDR**



Circuits: Input Data Line



- **208µm long T-line segments between DEMUX taps**
- **Digitally controlled varactors in the middle of the segments**
  - Avoid large discontinuities, reduce distortion
- **Parallel loss R_{SHUNT} to reduce ISI**
  - Distortionless line:

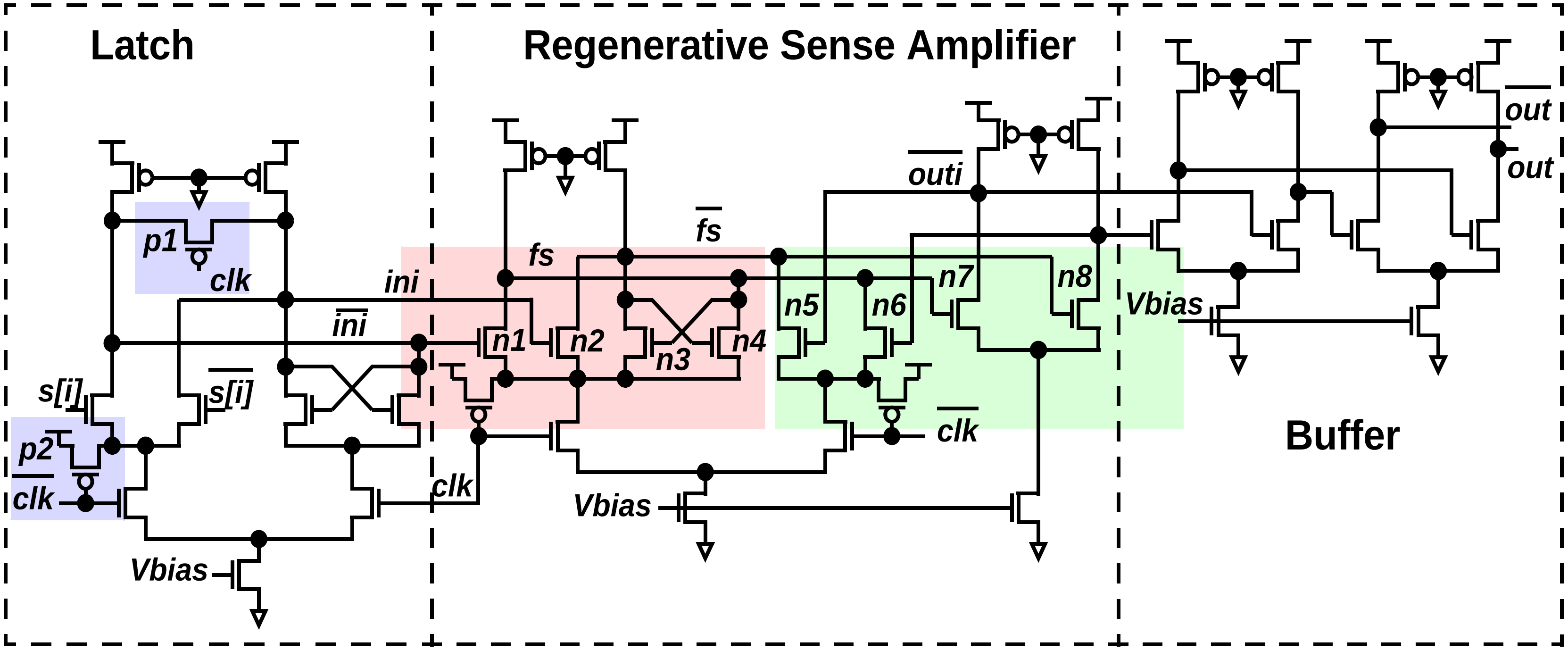
$$\frac{R}{L} = \frac{G}{C}$$

$$loss = \sqrt{RG} \neq f(\omega)$$

$$delay = \sqrt{LC} \neq f(\omega)$$

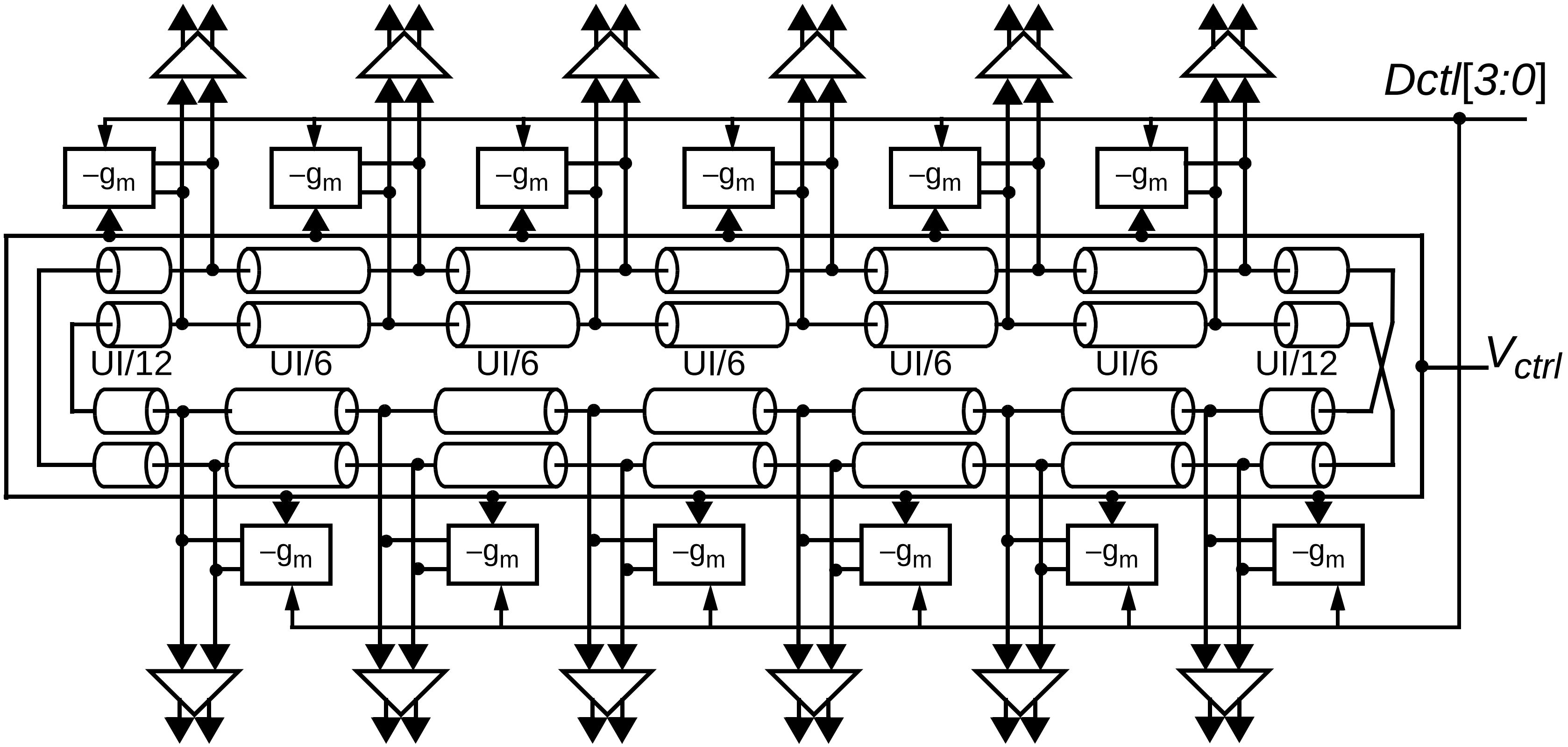
  - R_{SHUNT}=670Ω as a compromise between ISI and loss
- **Analogous to Pupin coils from early days of telephone industry**

Circuits: Sampler



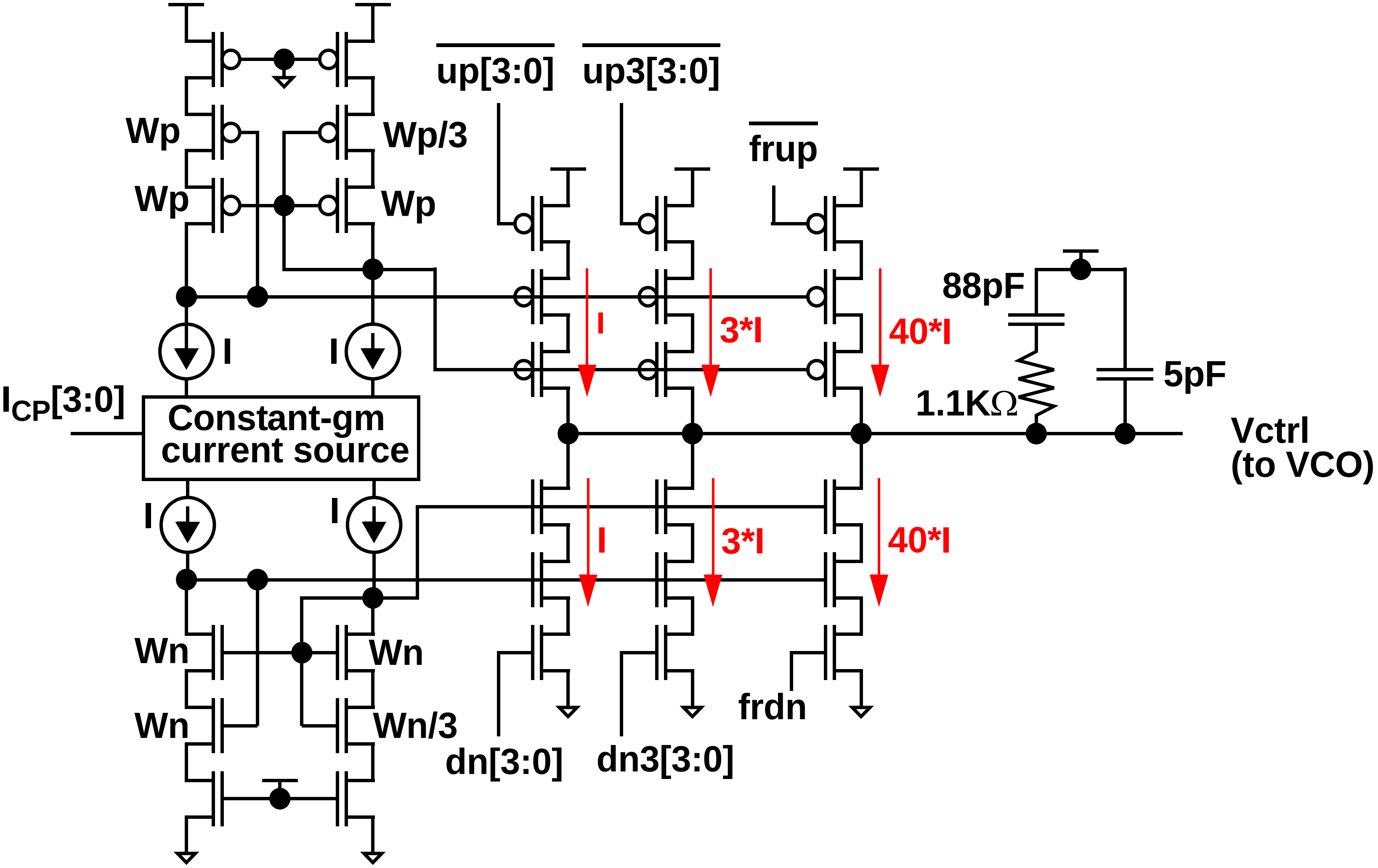
- **CML latch**
  - Transistors p1 and p2 to improve bandwidth and shut off input differential pair
- **Sense Amplifier**
  - Reset in the off-phase through feedback n5-n8
  - Compare input with output using quad n1-n4 to reduce aperture
- **Two-stage buffer**

Circuits: VCO

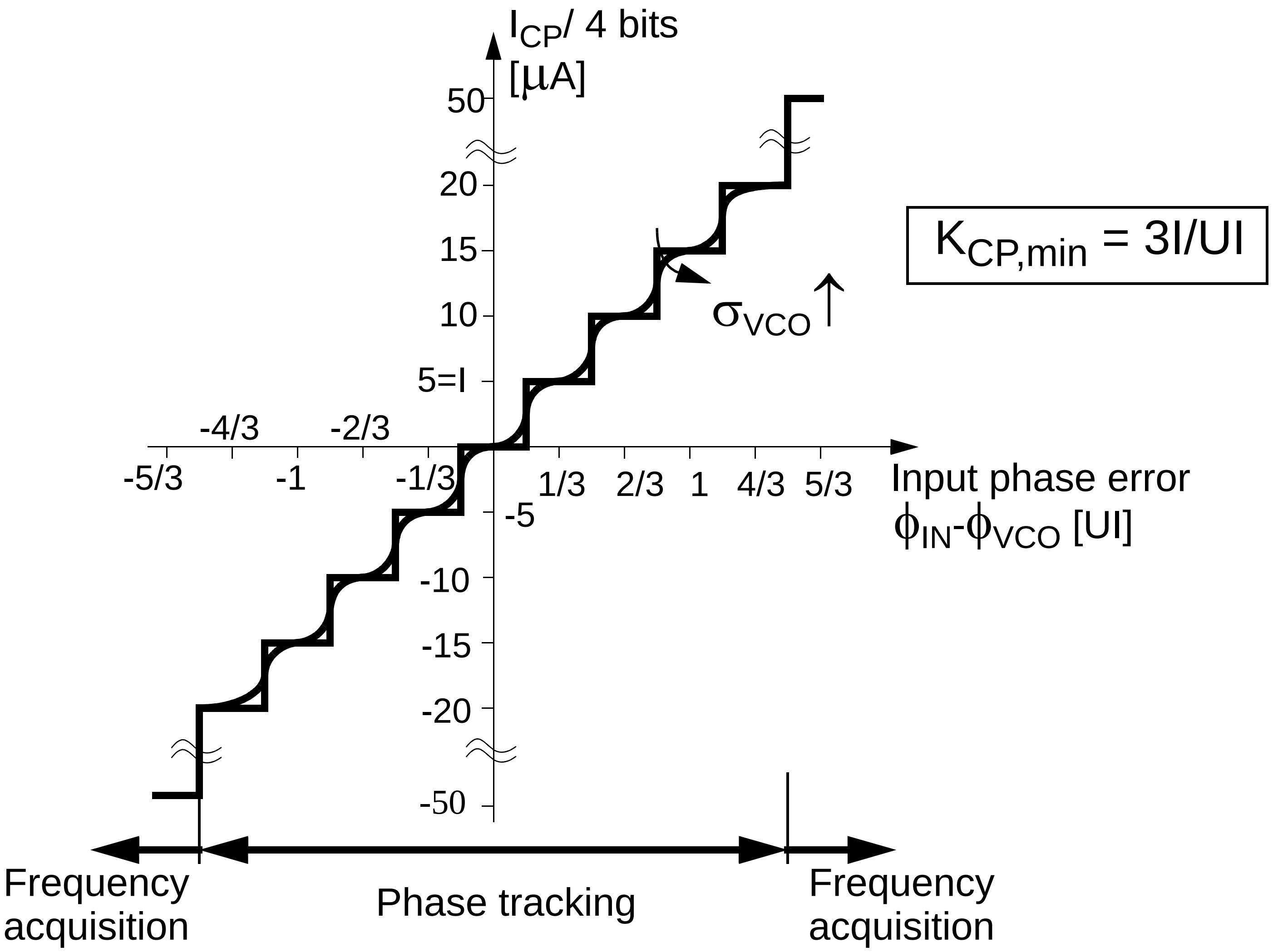


- **Distributed closed-loop VCO with built-in mechanism to set the clock direction counter-clockwise [Tzartzanis et al, ISSCC’06]**

Circuits: Charge Pump / Loop Filter



Charge Pump Characteristic



Summary - Part I + Part II

- **CDR linear model useful but one must be aware of limitations**
- **High-speed design - severe nonlinearities**
- **Concurrent system, architecture, and circuit design needed**
  - *Circuit specifications depend on architecture, system specifications*
  - *Loop dynamics depends on circuit non-idealities*
- **Behavioral simulation necessary**
- **Hybrid oversampling CDR takes more than two samples per unit interval in PLL-like loop**
  - *Detect the direction of the phase error*
  - *Improves jitter tolerance - jitter generation tradeoff*
  - *Improve pull-in range*
  - *Improve immunity to VCO noise*