MODELING OF HVDC-MMC TRANSMISSION SYSTEM FOR ELECTROMAGNETIC TRANSIENTS

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Plan:

1. Introduction
2. MMC topology overview
3. MMC models
4. HVDC-MMC model in EMTP-RV
5. Real time simulations
6. Conclusion

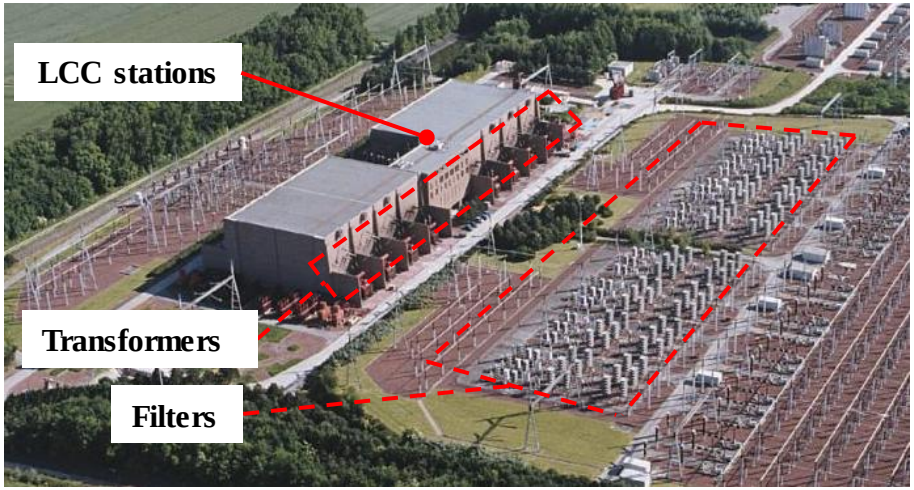
1. Introduction
HVDC technologies:

Around 145 HVDC installations worldwide (in operation or planned for very near future). Two distinct technologies exists:

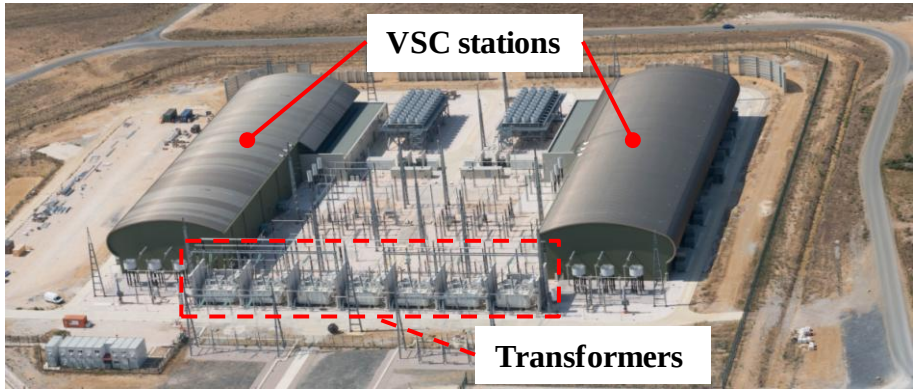
- Line-commutated current-source converters (LCCs):
  - Thyristor type
  - Technology well established for high power. It's also referred to as "Classic" HVDC
  - The most power transmission line installed in the word transmit 7200MW, with a voltage rated at 800kV DC and 1000kV AC (China)
- Forced-commutated voltage-source converter (VSCs)
  - GTO or in most industrial cases IGBT type
  - It represents the recent technology in DC power transmission
  - First VSC-based PWM-controlled HVDC system was installed in Sweden in 1997 (3MW, 10km distance and 20kV DC)

1. Introduction
Advantages of VSC over LCC:

- Independent control of the reactive and active powers of each converter
- Avoidance of commutation failures due to disturbances in the AC network
- Ability to connect the VSC-HVDC system to a weak ac network or even to a passive network (when no generation source is available)
- Faster dynamic response due to higher PWM, which result to smaller filter size



HVDC-LCC link, IFA2000 project

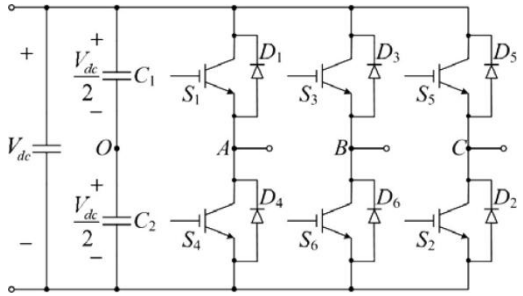


HVDC-VSC link, INELFE project

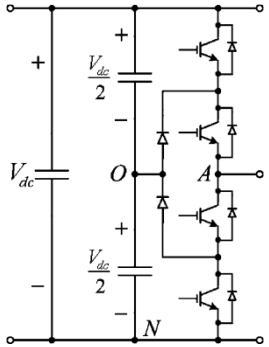
1. Introduction
VSC topologies:

Numerous converter topologies exists for VSC. Four main categories can be established:

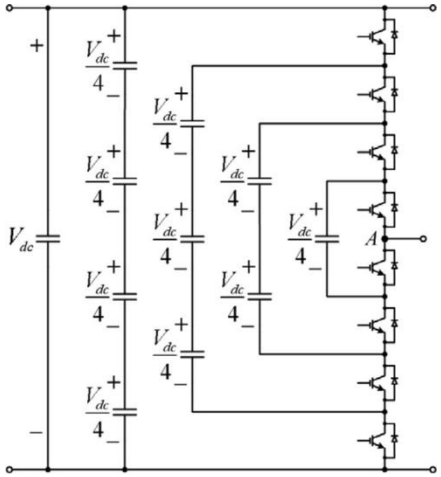
Two-Level



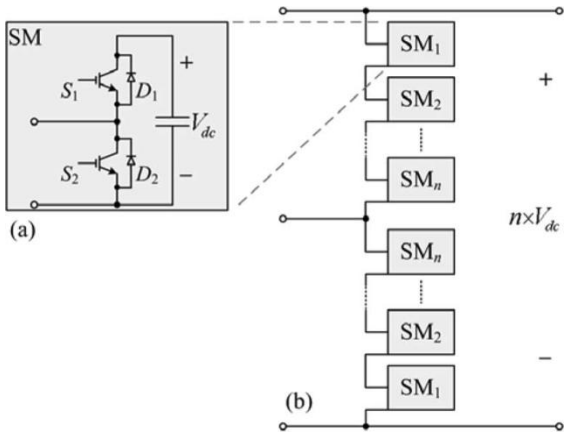
Multilevel diode-clamped



Multilevel floating-capacitor (FC)



Modular multilevel converter (MMC)

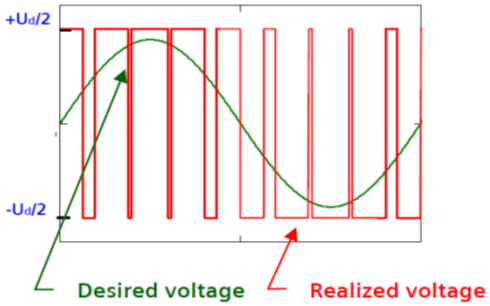


1. Introduction
MMC advantages:

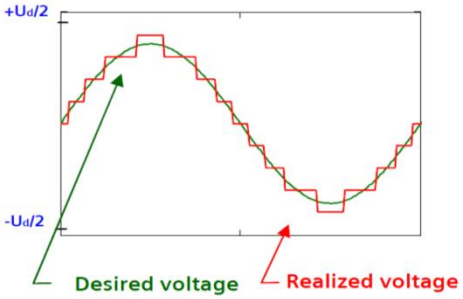
Advantages of Modular Multilevel Converter (MMC):

- Low frequency modulation
- Lower transient peak voltages on IGBT, which will lead to a lower losses
- Very low THD, hence no need for High-pass filters or very small size
- Modular structure, scalable to different power and voltage levels

VSC 2 levels



MMC 5 levels



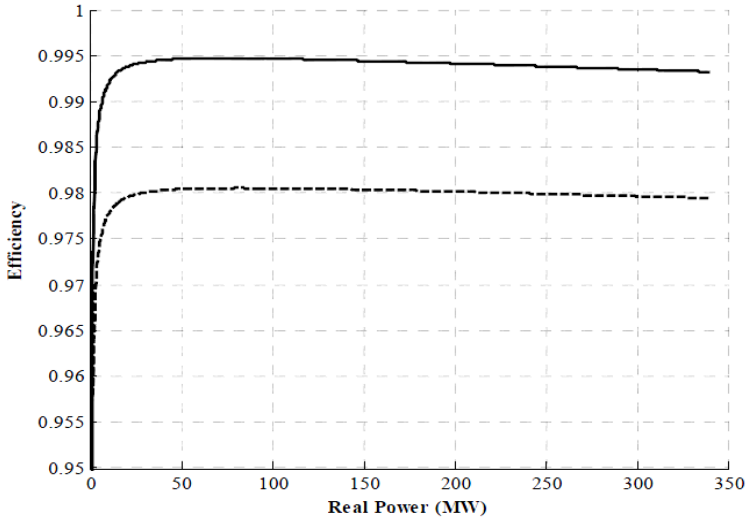
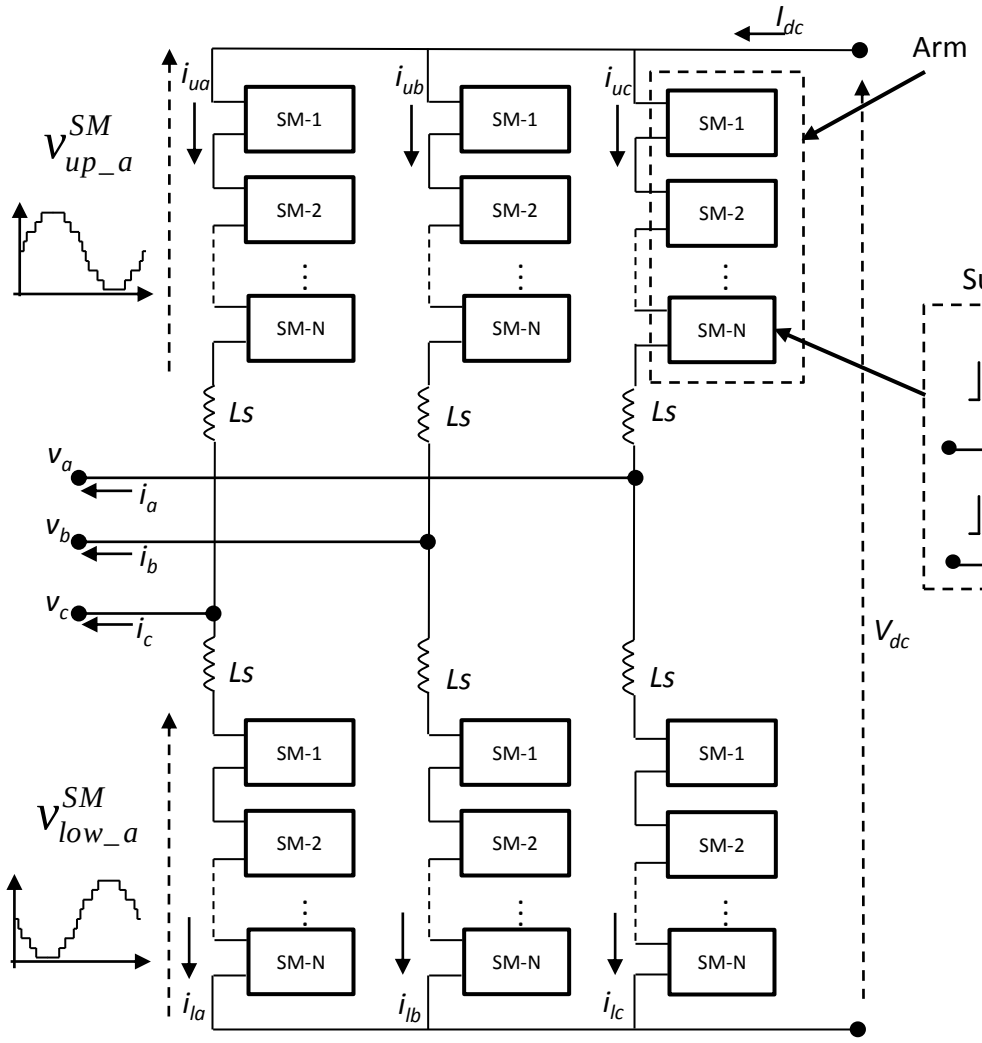


Fig. 10: Efficiency of the 2level and M2C (cos φ = 0.88)
- Solid line: M2C
- Dashed line: 2level

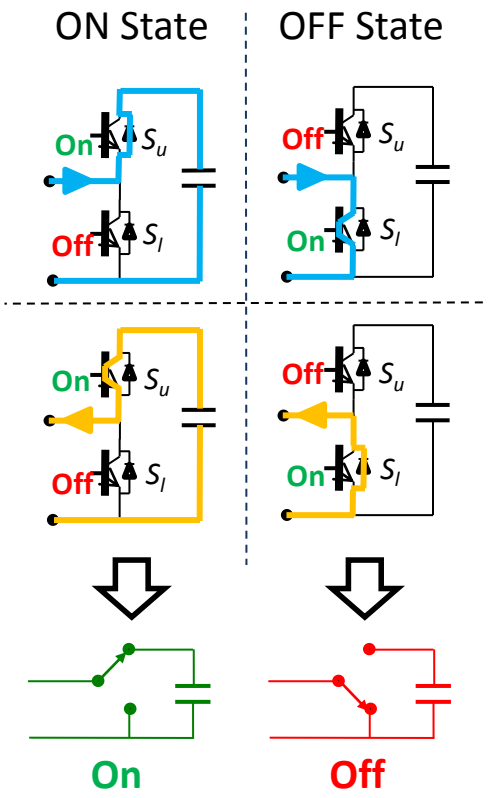
S. Allebrod, R. Hammerski, and R. Marquardt, "New transformerless scalable modular multilevel converters for HVDC-Transmission," *Power electronics specialtists Conference (PESC),* 2008.

2. MMC topology overview



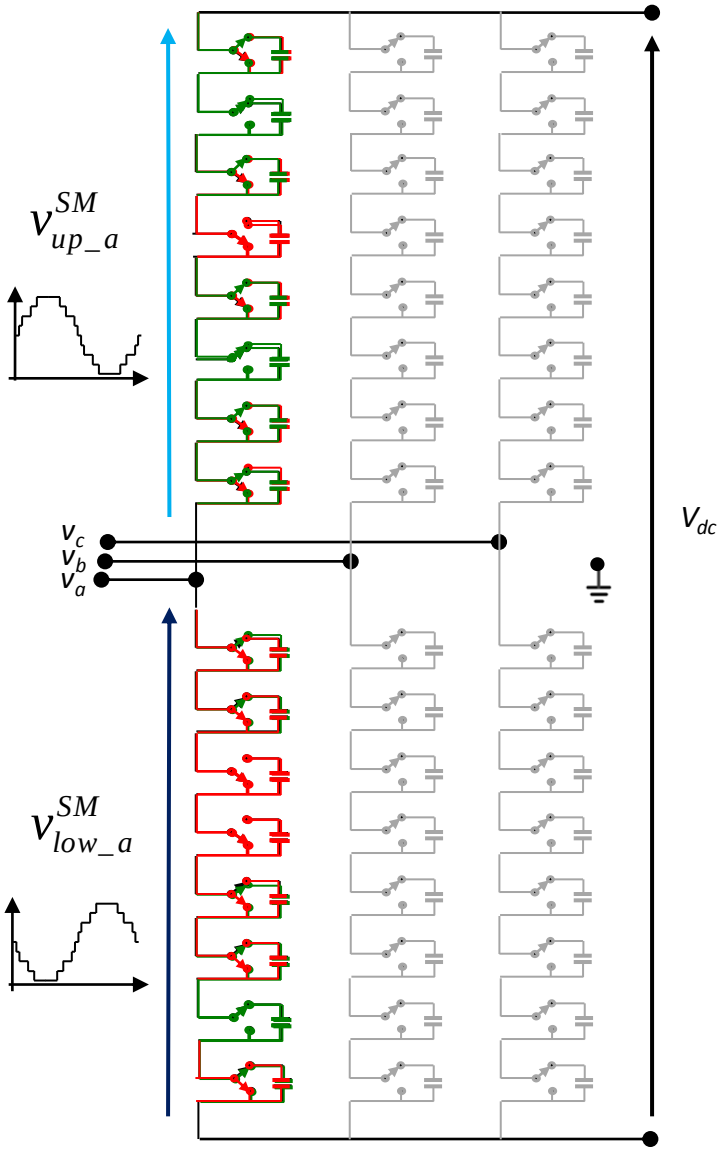
At normal operation, S1 and S2 are complementary

- The sub-module consist of two states:
  - S_u->on and S_l->off
  - S_u->off and S_l->on



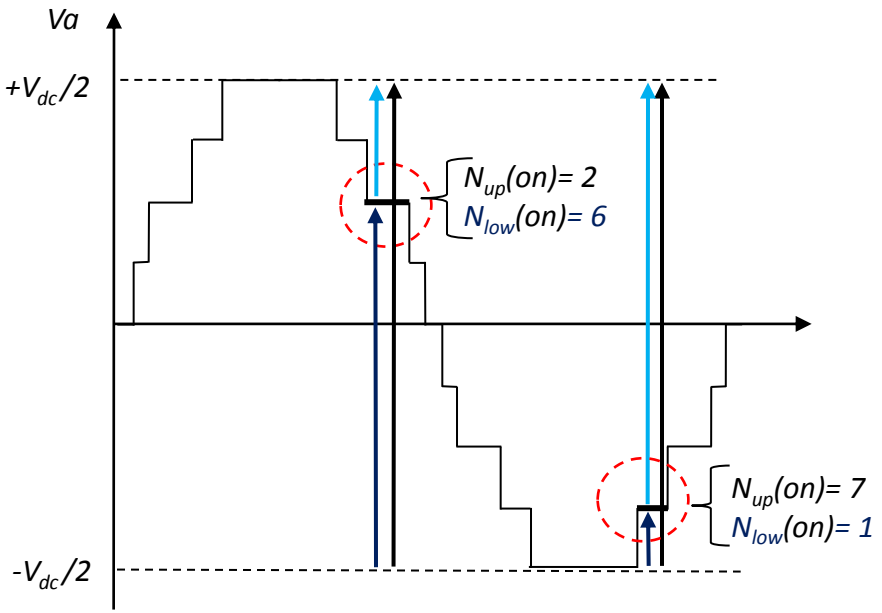
2. MMC converter overview

Example: Suppose we have a MMC-9levels (i.e. 8 SMs/arm)



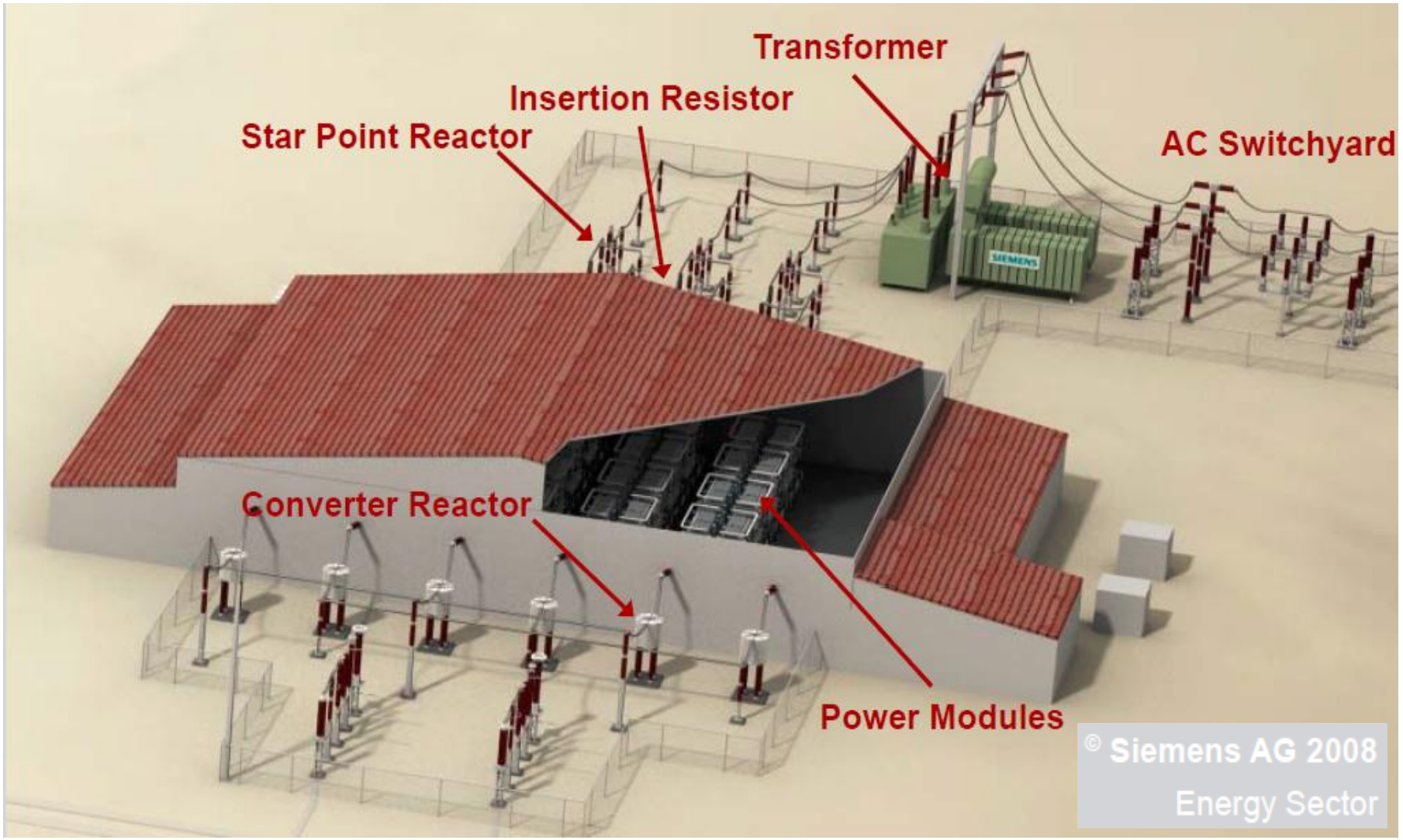
$$v_{up\_a}^{SM} = \sum_{i=1}^{N_{up}} (S_{up\_ai} \cdot vc_{up\_ai})$$

$$v_a = -v_{up\_a}^{SM} + \frac{V_{dc}}{2} = v_{low\_a}^{SM} + \frac{V_{dc}}{2}$$



2. MMC converter overview

MMC overview:



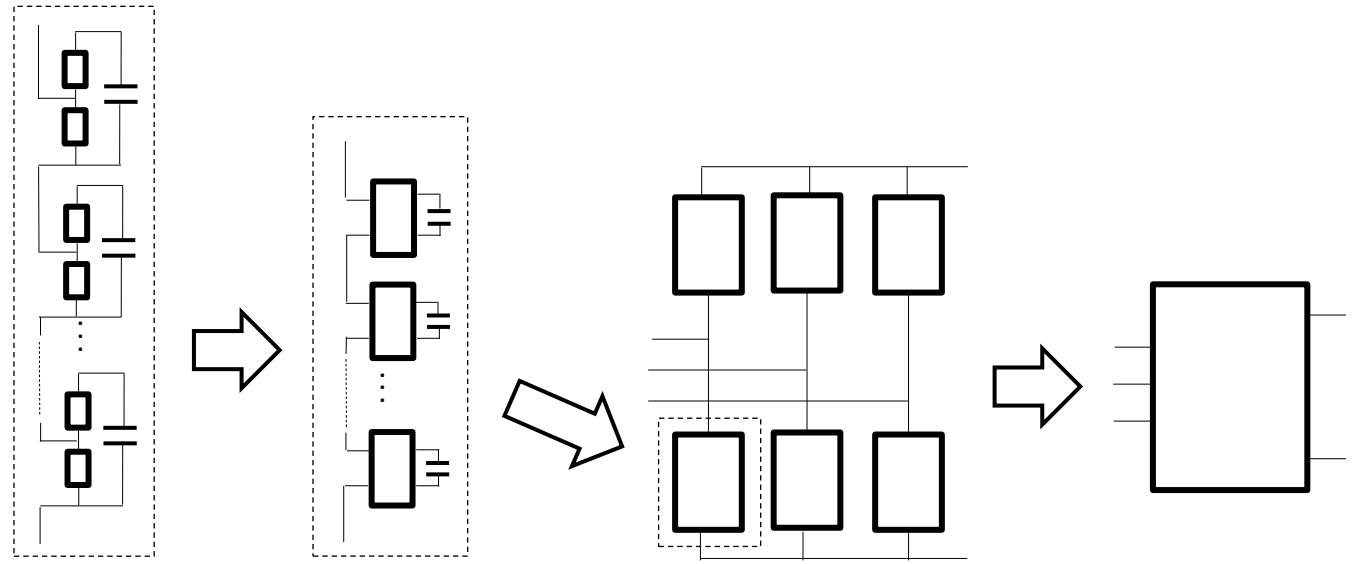
2. MMC converter overview

MMC overview:

3. MMC models

Depending on the type of study different type of modeling are presented:

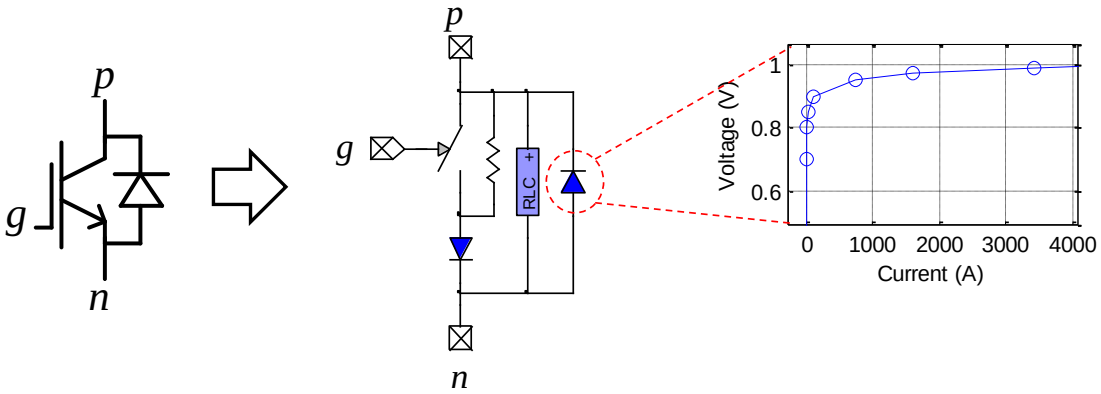
- Model 1 – Model based on nonlinear IGBT models
- Model 2 – Model based on simplified switchable resistance
- Model 3 – Switching Function of Arm (SF-arm)
- Model 4 – Average Value Model of MMC (AVM-MMC)

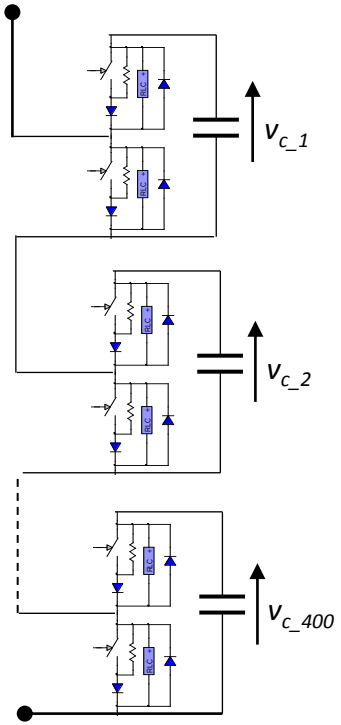


3. MMC models

Model 1 - Models based on nonlinear IGBT models

- In this case IGBT/diode are modeled by nonlinear resistor and an ideal switch.





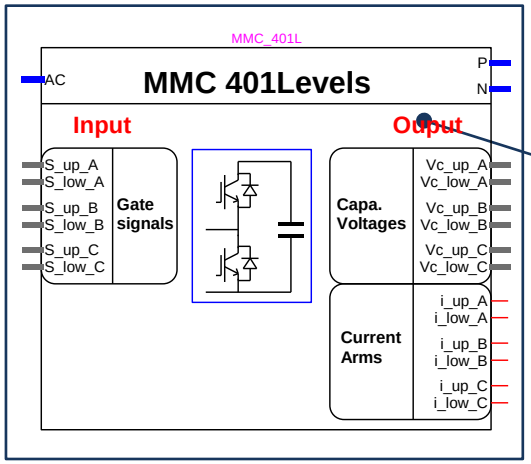
Advantages:

- Very easy to achieve, it preserve the main structure of the IGBT
- The V-I curve of the IGBT/diode is modeled.

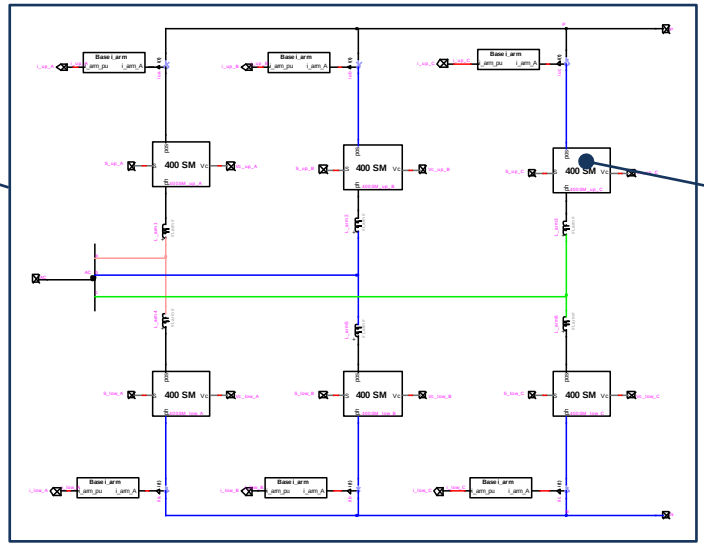
Inconvenient:

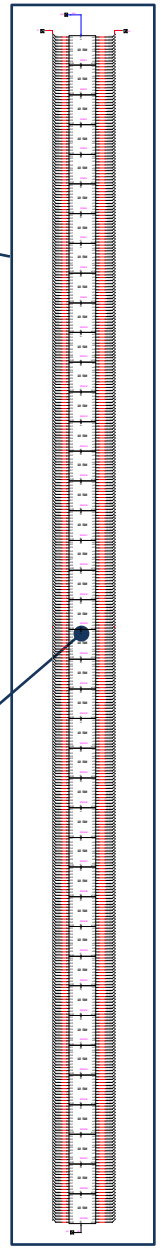
- Computation time is high

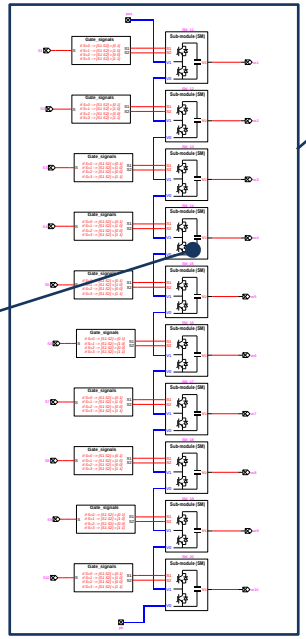
3. MMC models



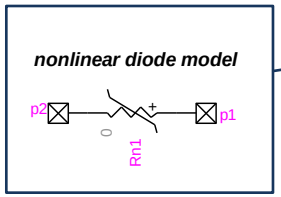
VSC-MMC 401 levels
Model 1

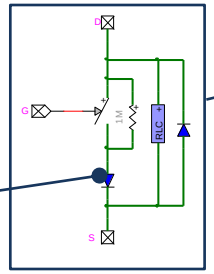


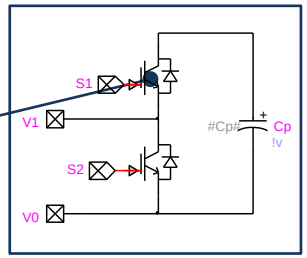




Total IGBT/diode in the HVDC-MMC 401 Level system:
2(IGBT/SM)*400(SM/arms)*2(arms/phase)*3(phases)*2(converters)
= 9 500 IGBTs/diodes



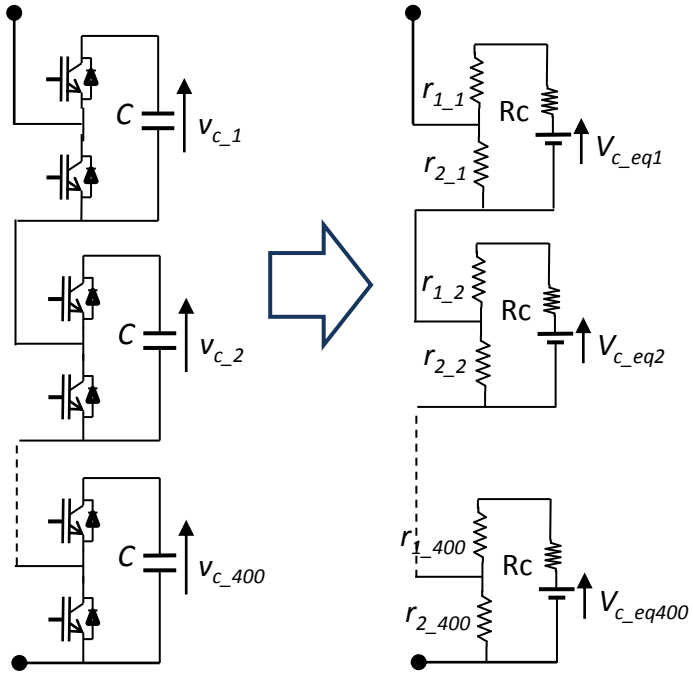


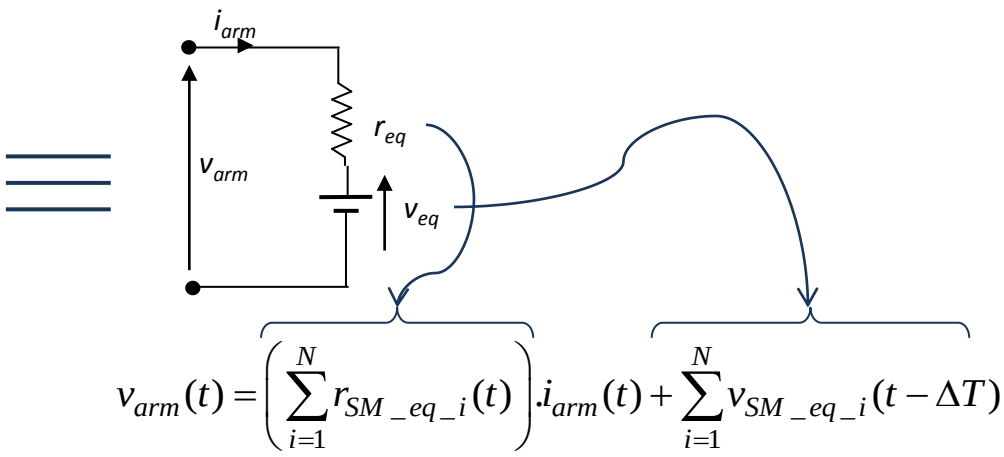


3. MMC models

Model 2 - Models based on simplified switchable resistance

IGBT and diodes are represented by two-value resistors (Ron and Roff). A reduction is performed to reduce the number of electrical nodes that describe converter.





$$v_{arm}(t) = \left(\sum_{i=1}^{N} r_{SM\_eq\_i}(t) \right) . i_{arm}(t) + \sum_{i=1}^{N} v_{SM\_eq\_i}(t - \Delta T)$$

$$\begin{cases} r_{SM\_eq}(t) = \dfrac{r2(t).\left(r1(t) + R_c\right)}{r2(t) + r1(t) + R_c} \\ v_{SM\_eq}(t - \Delta T) = v_{c\_eq}(t - \Delta T).\left(\dfrac{r2(t)}{r2(t) + r1(t) + R_c} \right) \end{cases}$$

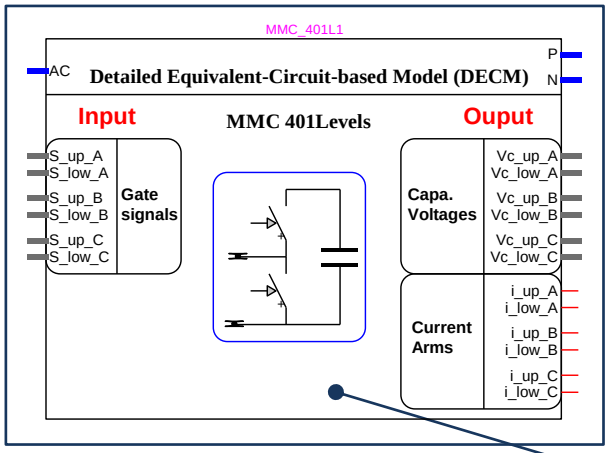
Advantages:

- Reduction of electrical nodes to 3 nodes, without loosing the variable information of each SM.
- Low computation time

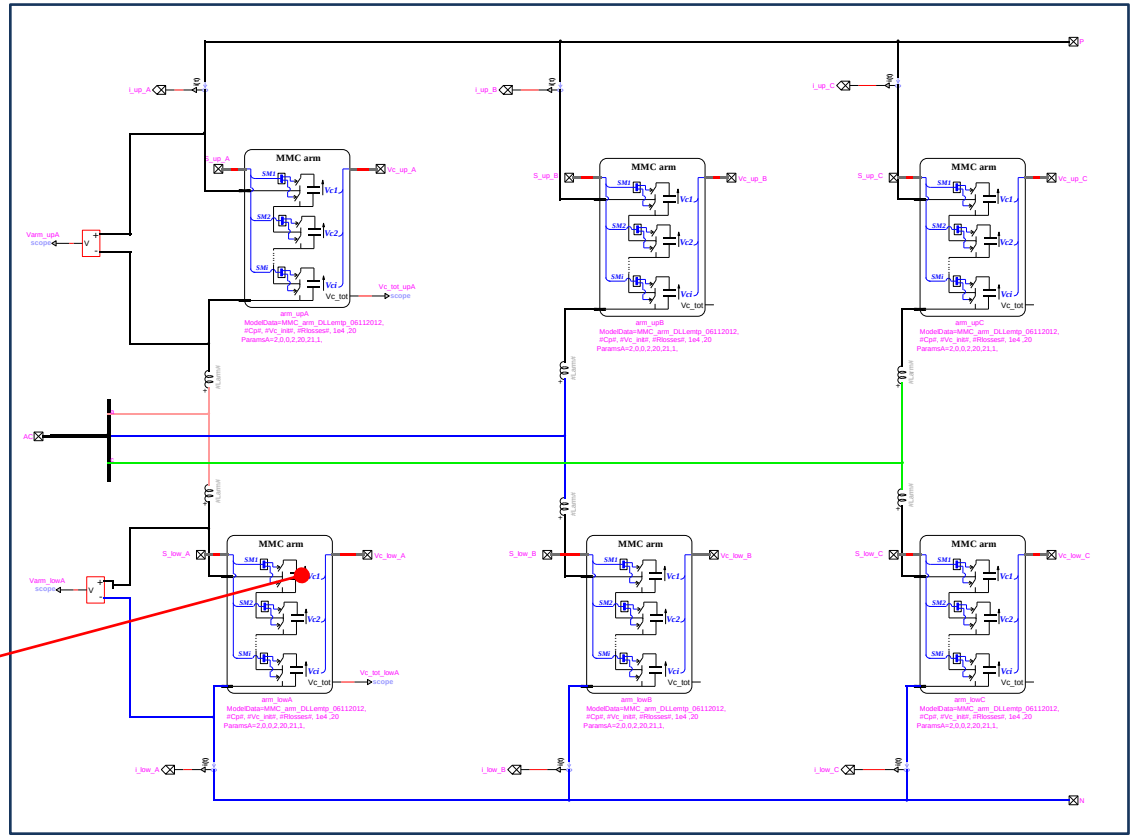
Inconvenient:

- The model is hard-coded, hence the user has no more access to SM circuits
- The V-I curve of IGBT/diode is not modeled

3. MMC models



MMC Model 2



DLL block
Fortran 95 code

3. MMC models

Model 3 – Switching function of Arm

- Each MMC arm are modeled as controlled current and voltage sources for ON/OFF states and half diode bridge for Blocked state.
- These models can be used to study harmonics generated and control system which account for energy regulation of MMC-arm.
- It suppose that Capacitor voltages balancing control operate correctly

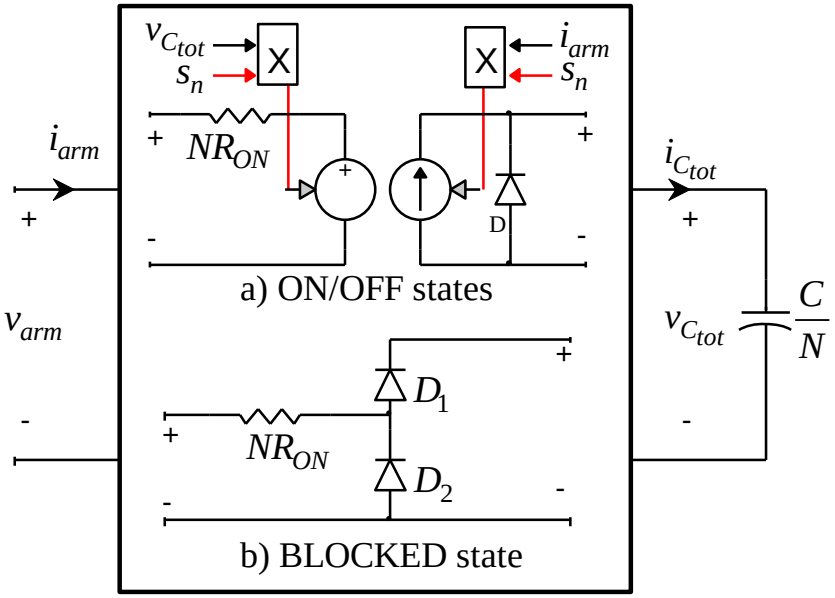
Assuming that: $\overline{v}_{C_1} = \overline{v}_{C_2} = \ldots = \overline{v}_{C_i} = \dfrac{v_{C_{tot}}}{N}$

$$\begin{cases} v_{arm} = s_n . v_{C_{tot}} + \left(NR_{ON} \right) i_{arm} \\ i_{C_{tot}} = s_n . i_{arm} \end{cases}$$

where: $s_n = \dfrac{\left(\sum_{i=1}^{N} S_i \right)}{N}$

$S_i = 1$ -> For ON state

$S_i = 0$ -> For OFF state



3. MMC models

Model 3 – Switching function of Arm

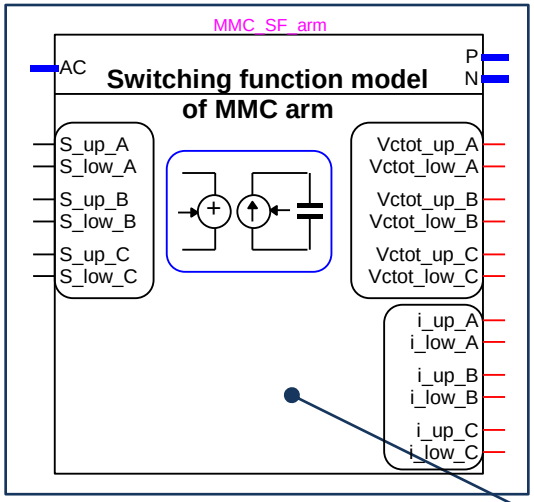
Advantages:

- Reduction of electrical nodes to 3 nodes, without loosing the variable information of each SM.
- Very Low computation time.
- Circulating currents and the linear conduction losses can be represented
- The energy transferred from ac and dc sides into each arm of the MMC is taken into account

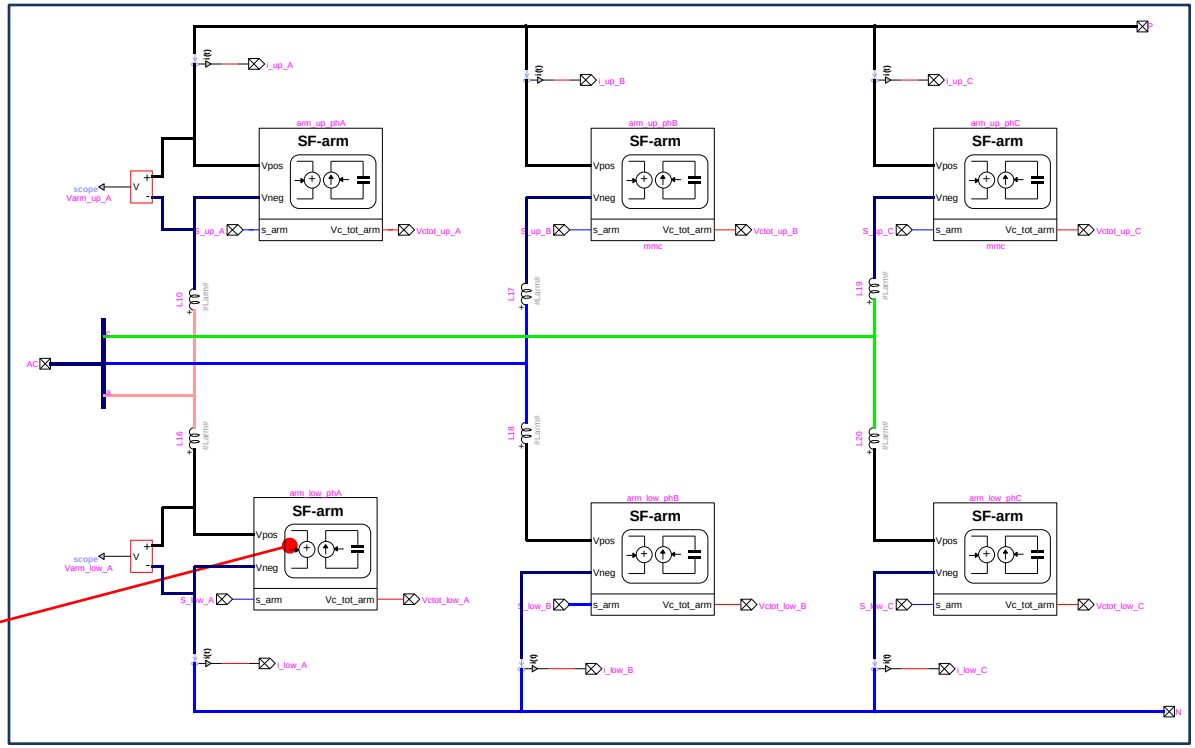
Inconvenient:

- SMs are no longer represented
- Balancing controls of capacitor voltages in each arm cannot be studied using this approach.
- Should be used with care when dealing with MMC having < 51Level

3. MMC models



MMC Model 3



DLL block
Fortran 95 code

3. MMC models

Model 4 – AVM (Average Value Model)

- The AC and DC side characteristics are modeled as controlled current and voltage sources.
- These models cannot be used to study harmonics generated by such converters.
- AVM model suppose that internal variables of MMC (Capacitor voltages and current of each arm) are controlled correctly

AC side:

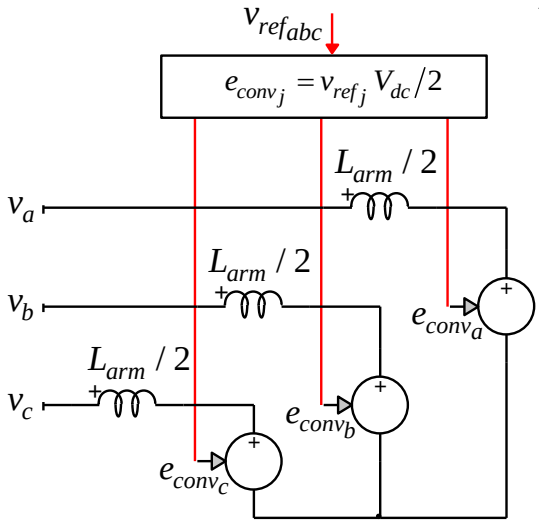
$$e_{conv_j} = \frac{L_{arm}}{2}\frac{di_j}{dt} - v_j \qquad j = a,b,c$$

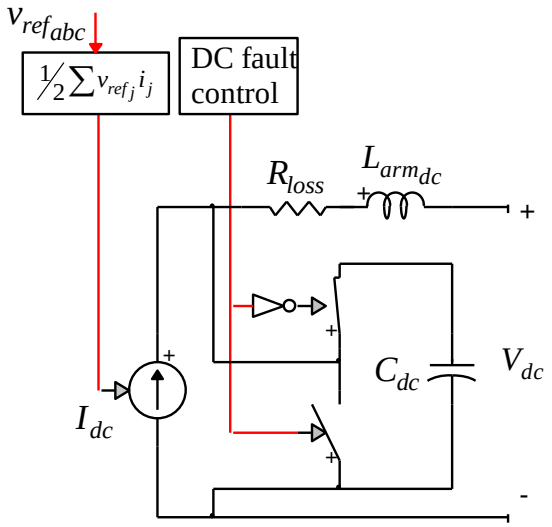
$$e_{conv_j} = v_{ref_j}\frac{V_{dc}}{2}$$

DC side:

$$P_{ac} = P_{dc}$$

$$I_{dc} = \frac{1}{2}\sum_{j=a,b,c} v_{ref_j} i_j$$





3. MMC models

Model 4 – AVM (Average Value Model)

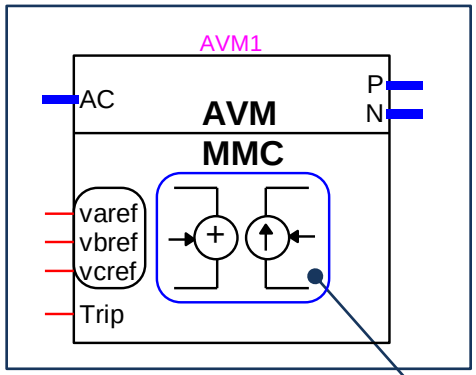
Advantages:

- Reduction of electrical nodes
- Very Low computation time.

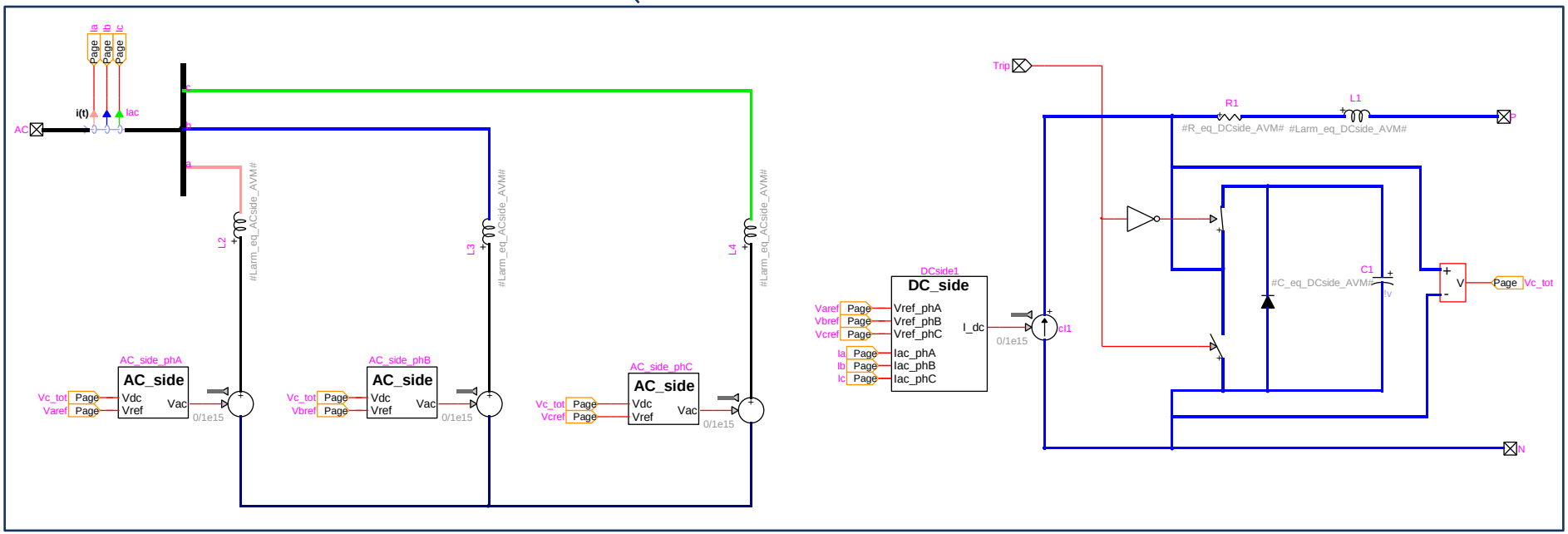
Inconvenient:

- MMC arm are no longer represented
- Lower level control cannot be studied using this approach.
- Blocked state behavior cannot be accurately modeled

3. MMC models



MMC Model 4

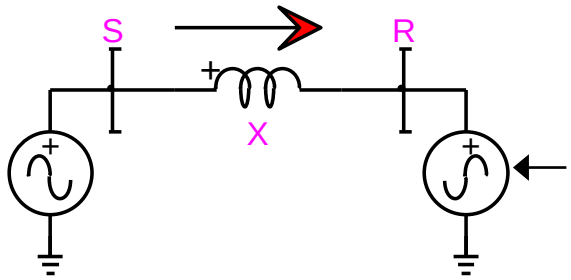


4. Control system

Basic idea:

By linearizing the power equation, active and reactive power can be decoupled, thus:

- Regulating the phase angle -> active power is controlled
- Regulating the voltage amplitude -> reactive power is controlled



$$\begin{cases} P_R = \dfrac{V_S V_R}{X}\sin(\delta) \\ Q_R = \dfrac{V_S V_R \cos(\delta) - V_R^2}{X} \end{cases}$$

$$\Leftrightarrow P_R = fct(\delta)$$

$$\Leftrightarrow Q_R = fct(V_R)$$

However the control system is much more complex

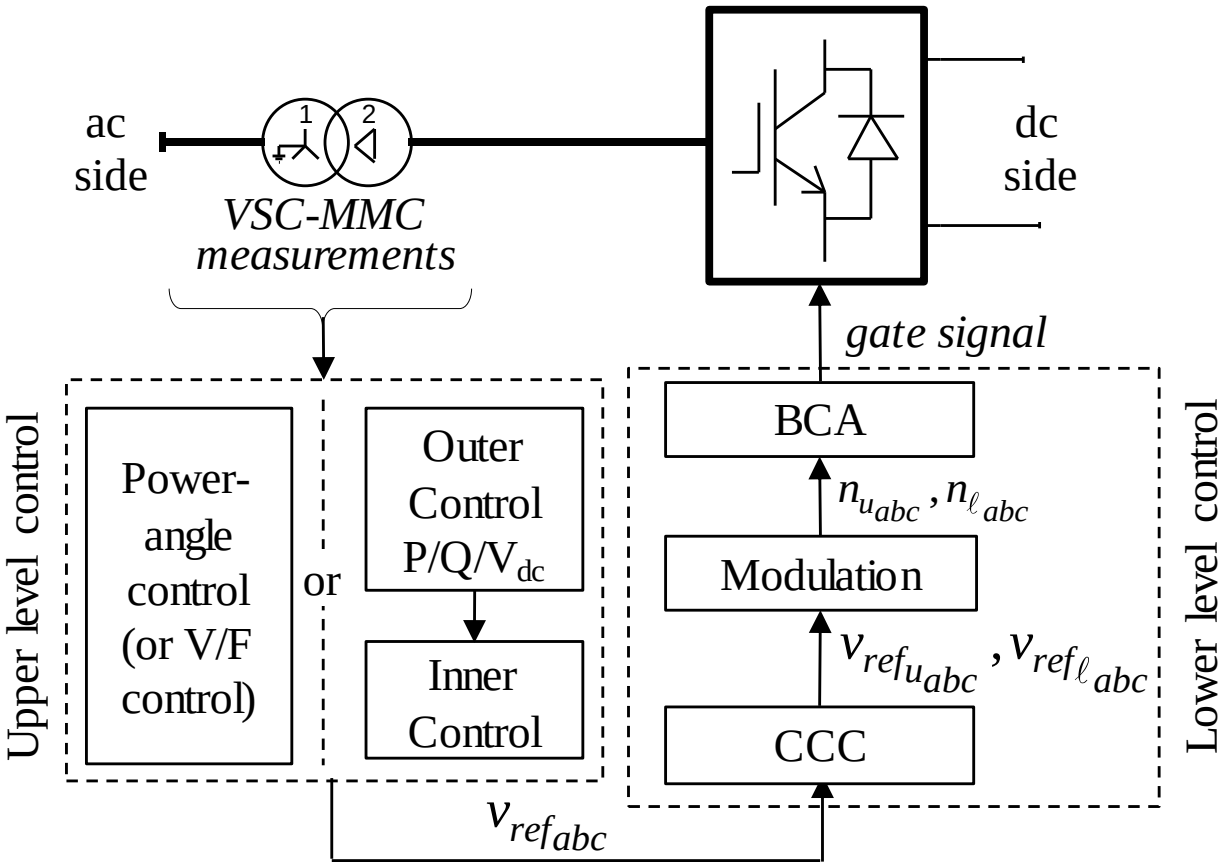
Upper control (VSC control)

Since MMC topology is a VSC type, the generic Outer/Inner Control can be used

Lower control (MMC control)

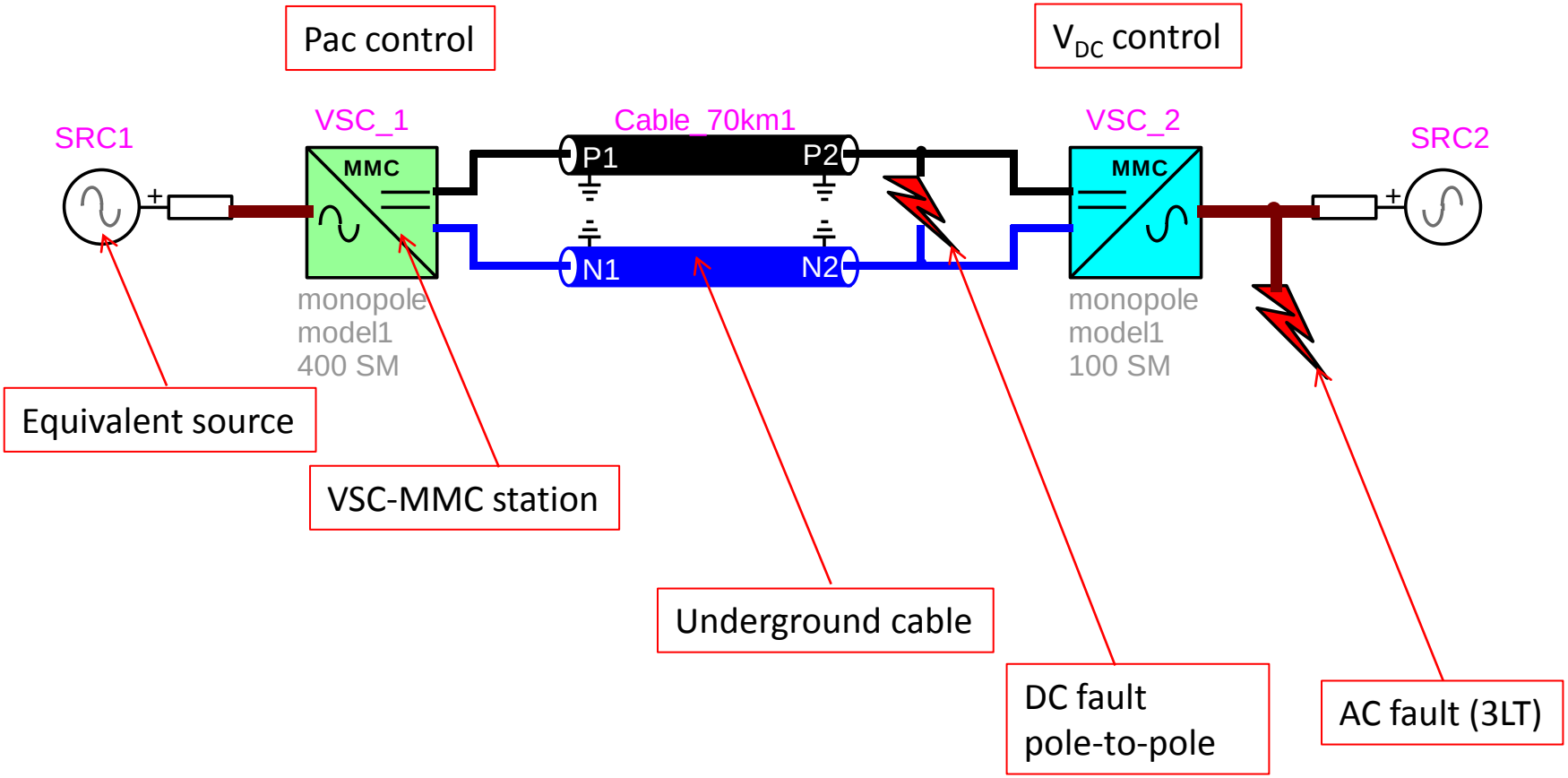
Controller related to the MMC topology, in order to control internal variables

4. Control system



5. HVDC-MMC model in EMTP-RV

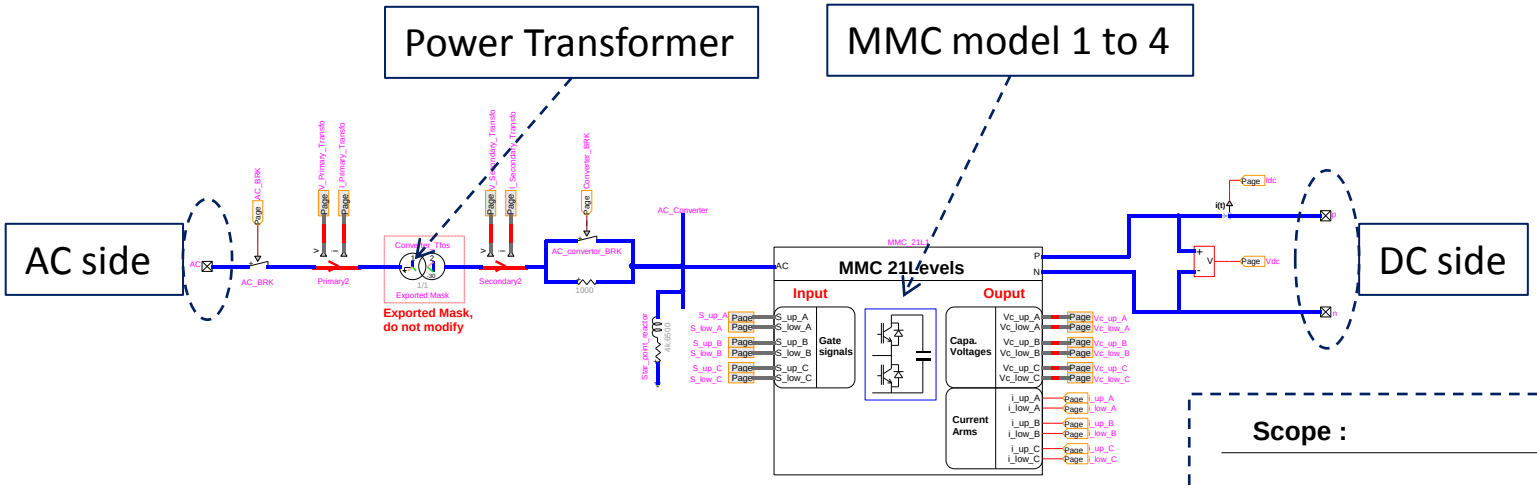
HVDC link modeled in EMTP-RV

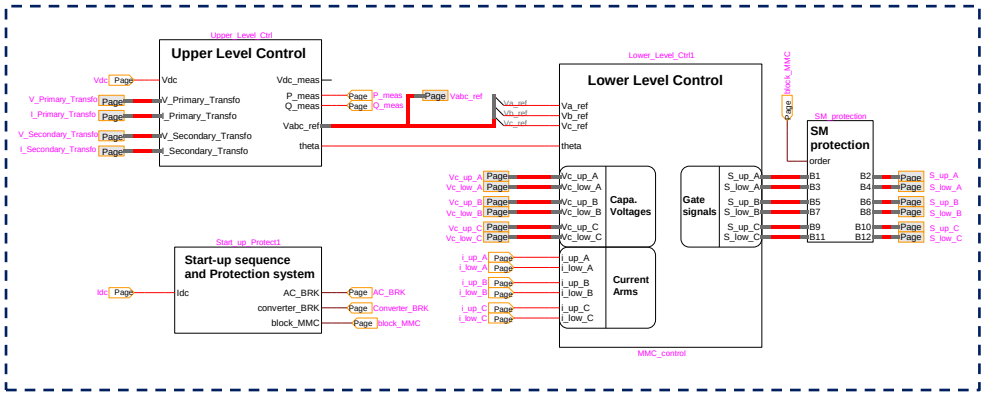


NB: This test case is included in the examples folder of EMTP-RV 2.5

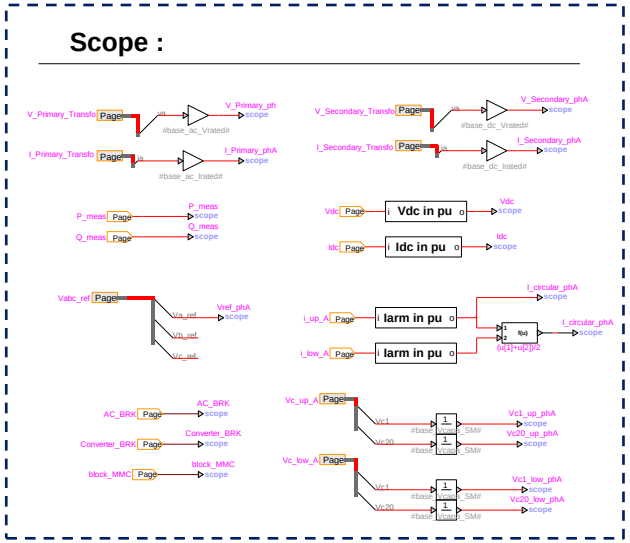
HVDC-MMC model in EMTP-RV

Subsystem structure of the VSC-MMC station





Control and Protection System



Acquisition system

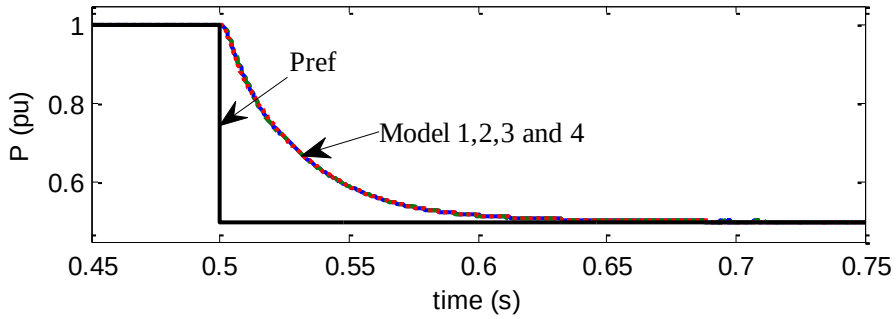
Model comparisons

Step change on active power reference

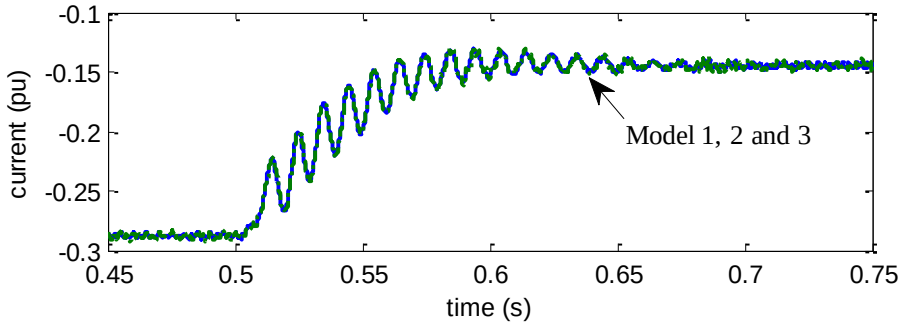
Simulation configuration:

MMC-401Level (*N* = 400SMs/arm)

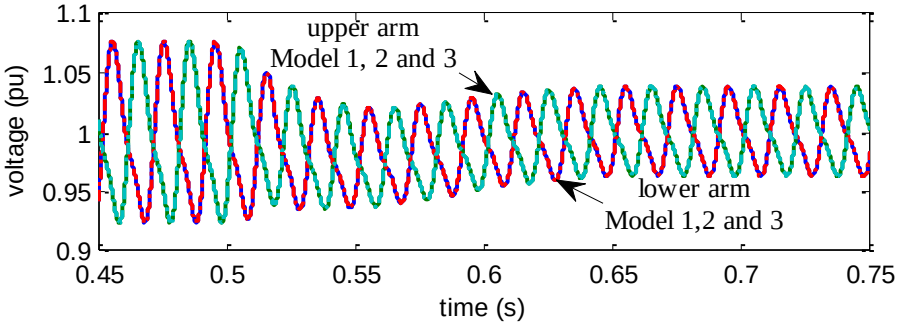
Active power reference (Pref) of MMC-1 is reduced from 1 to 0.5 pu at t=0.5s



MMC-1 Active power



MMC-1 phase A, difference current i_{diff_a}



MMC-1 phase A upper and lower arms, v_{Ctot}

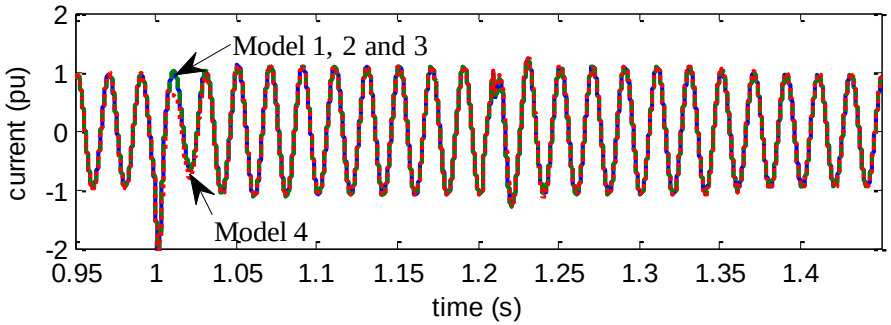
Model comparisons

3LG AC fault

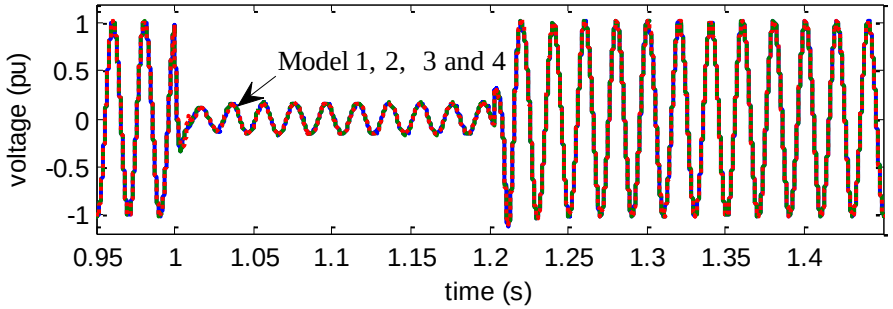
Simulation configuration:

MMC-401Level (*N* = 400SMs/arm)

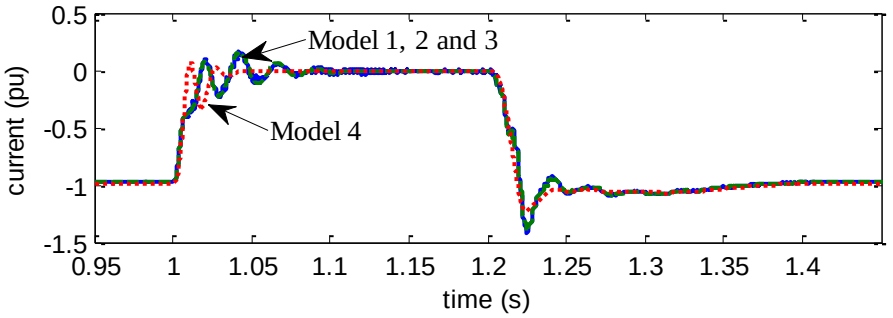
Three-phase to ground fault of 200ms after 1sec of simulation



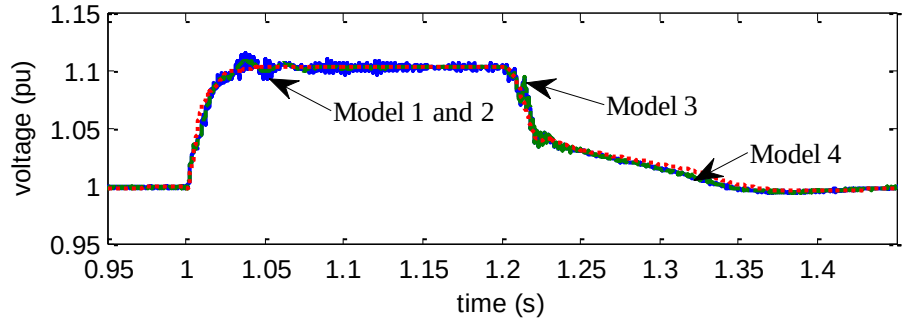
MMC-2 phase A current: i_a



MMC-2 phase A voltage: v_a



MMC-2 dc current: I_{dc}



MMC-2 dc voltage: V_{dc}

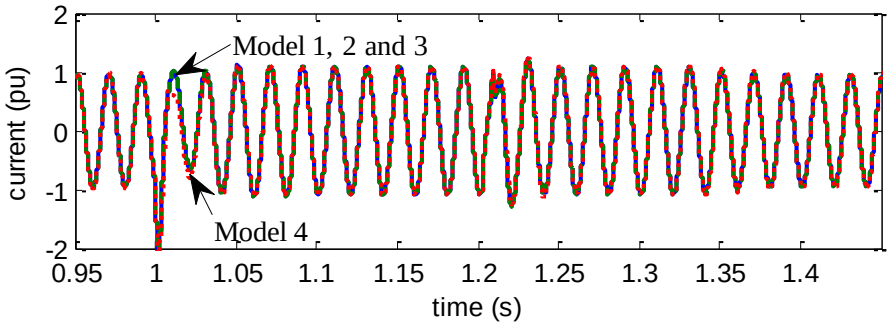
Model comparisons

3LG AC fault

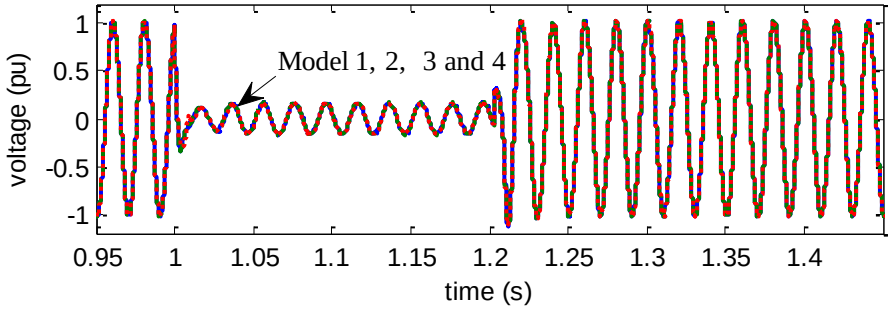
Simulation configuration:

MMC-51Level (N = 50SMs/arm)

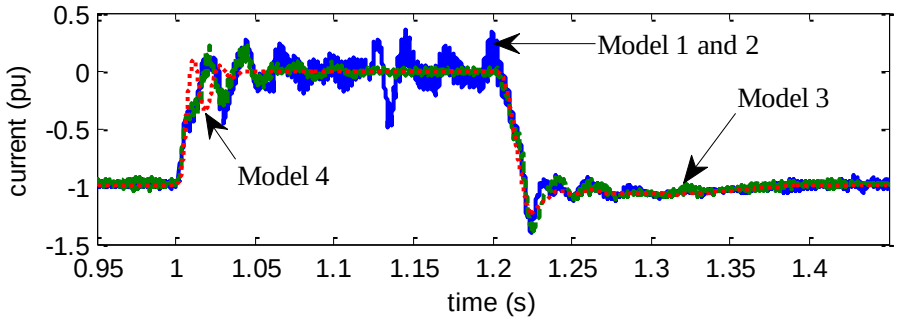
Three-phase to ground fault of 200ms after 1sec of simulation



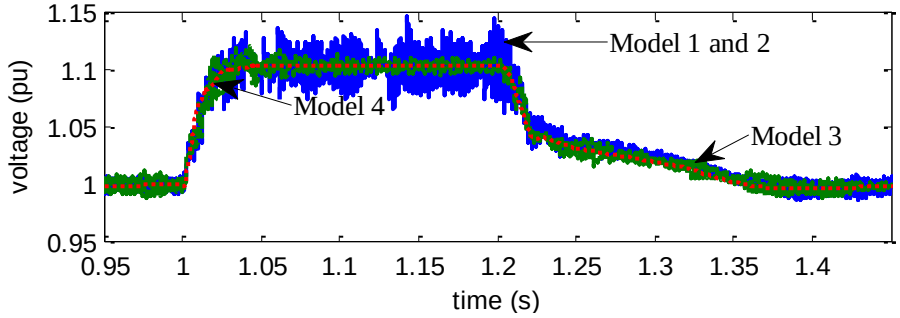
MMC-2 phase A current: i_a



MMC-2 phase A voltage: v_a



MMC-2 dc current: I_{dc}



MMC-2 dc voltage: V_{dc}

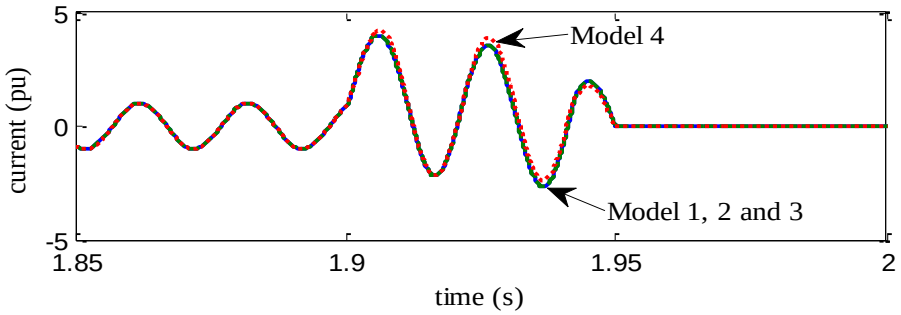
Model comparisons

DC pole-to-pole fault

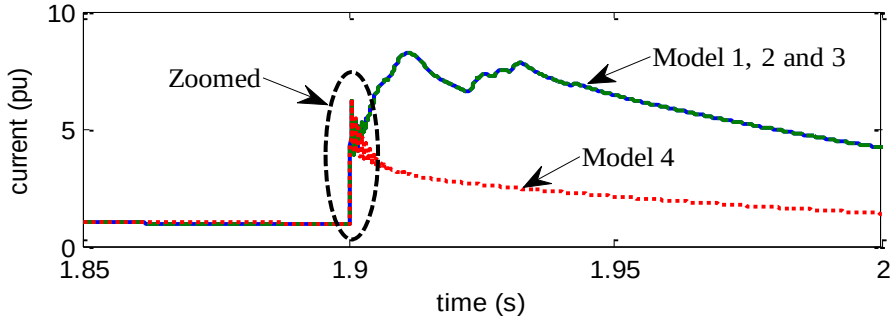
Simulation configuration:

MMC-401Level (*N* = 400SMs/arm)

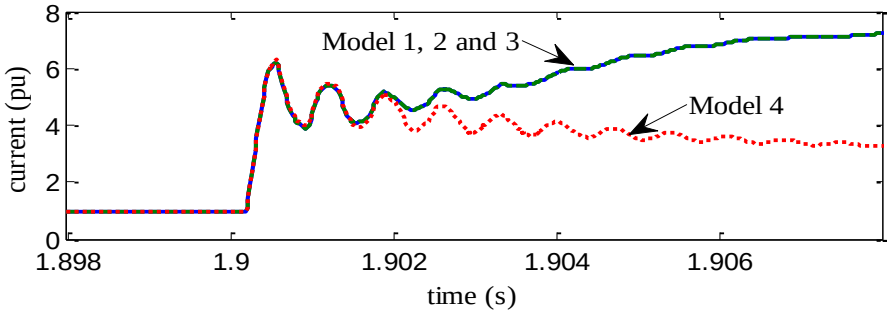
Permanent Pole-to-pole DC fault at 1.9sec of simulation



MMC-1 ac current: i_a



MMC-1 dc current: I_{dc}



Zoomed MMC-1 dc current: I_{dc}

Computation performances in EMTP-RV

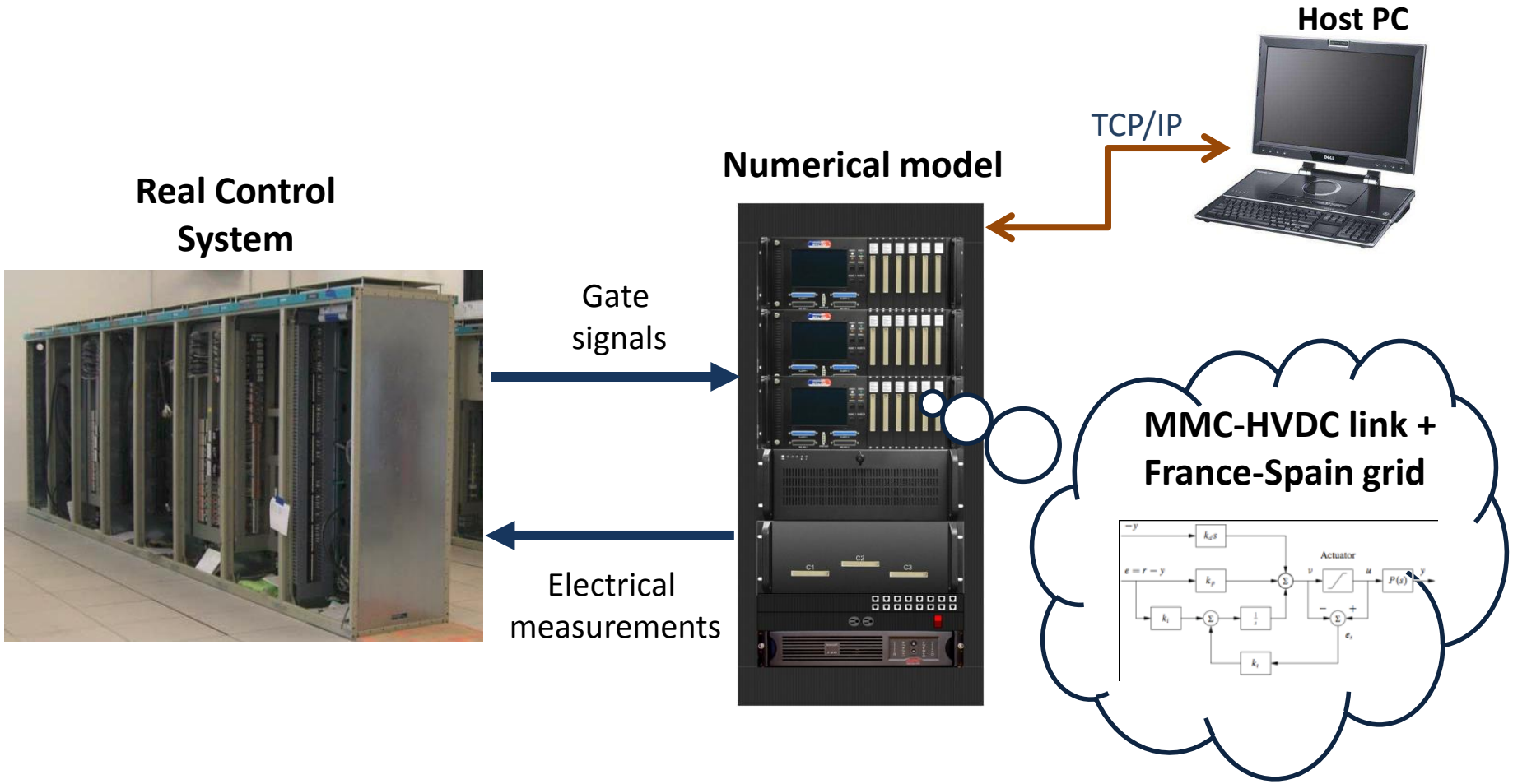
Computation performances

- 401-levels MMC based HVDC link was tested for 1sec simulation.
- The simulation time is compared for all models
- The best computing performance is given by Model 4, however Model 3 is very fast and more accurate. Model 1 and 2 dependent on the number of MMC levels simulated.

Model	Time step (µs)	Computation time (s) in function of SMs/arm			
		20 SMs/arm	50 SMs/arm	100 SMs/arm	400 SMs/arm
# 1	10	258	822	2,106	13,459
# 2	10	37	65	114	441
# 3	10	18	18	18	18
# 4	10	15	15	15	15
# 4	100	2	2	2	2

4. Real-time simulation
Introduction

Objective is to perform Hardware In the Loop (HIL) simulation.
By means of interfacing the real control system of SIEMENS with a numerical MMC-HVDC link + AC grid



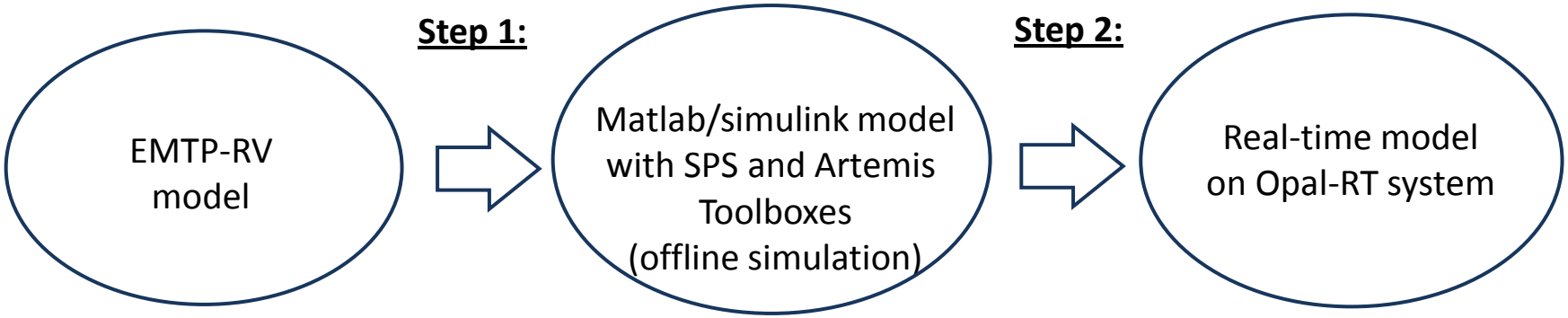
4. Real-time simulation

A HVDC-MMC transmission system is used to verify the SSN-MMC model proposed.

In order to achieve a real-time simulation, two steps are required:

Step 1: Transfer the original MMC based HVDC system model achieved in EMTP-RV to the Matlab/Simulink software using SimPowerSystem (SPS) and Artemis tools.

Step 2: Transfer from offline to real-time simulation (using Opal-RT simulator)



- The generic control system developed in Simulink is directly interfaced with EMTP-RV by means of a DLL
- Detail MMC model (reference model) is kept on EMTP-RV.

4. Real-time simulation
Offline to real-time simulation

Step 1: Transfer form EMTP-RV to Matlab/Simulink
Interfacing by mean of a DLL between these two programs is performed

Matlab/Simulink limitations:

- MMC model with non-linear IGBT/diode models (Model 1) can not be modelled. (Specially for high level MMC)
- France-Spain grid can not be modelled. A simplified model has to be used
- Small resistances have to be added between some connection (i.e. connection between the wideband Cable and the MMC)

Difference between the two programs:

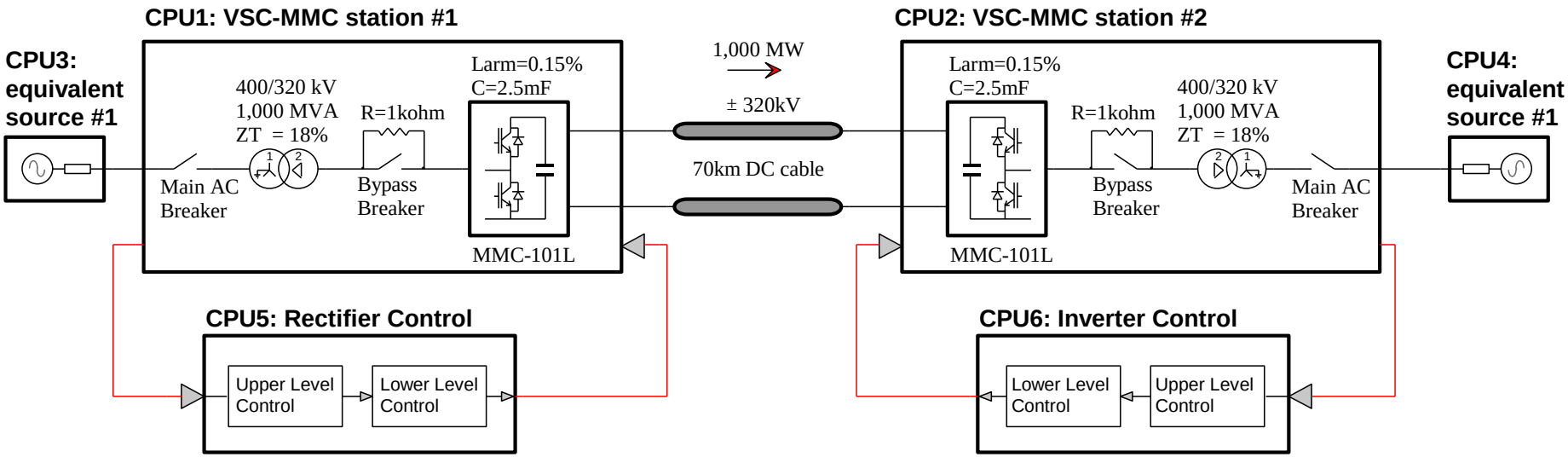
	EMTP-RV	**Matlab/simulink (SPS/ARTEMIS)**
Integration Method	Trapezoidal integration and Euler backward with half time step for discontinuities	SimPowerSystem: • Continuous • Discrete (trapezoidal rule) RT-Lab: • ARTEMIS art5 (order 5)
Equation type	Nodal equations	State space equations

4. Real-time simulation
Offline to real-time simulation

Step 2: Transfer form offline to real time simulation

1. Partitioning of the system is necessary for multiprocessor usage
    - Determine the most suited partition in order to optimize the computation time of each processor
    - Add stubline and delays where it's necessary in order to parallelize the CPU

Only MMC model 2 has been studied since Model 3 and 4 does have any technical challenge in real time modeling and performances

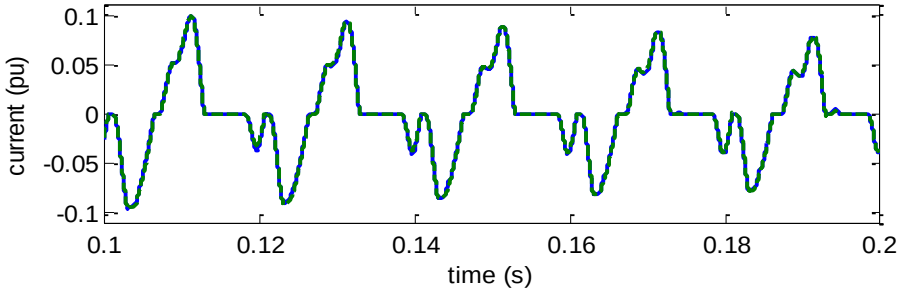


4. Real-time simulation
Offline to real-time simulation

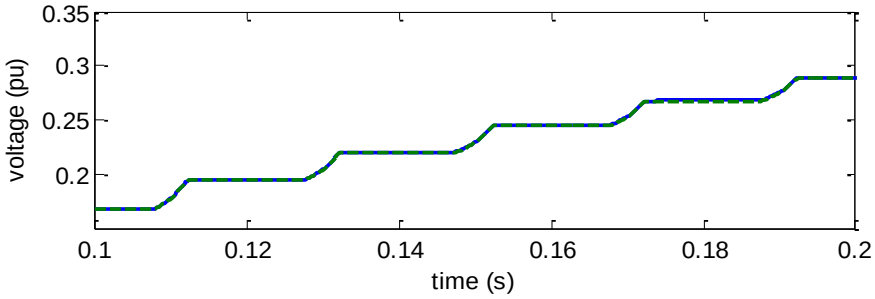
Real-time Model accuracy verification

Scenario 1: Start-up sequence

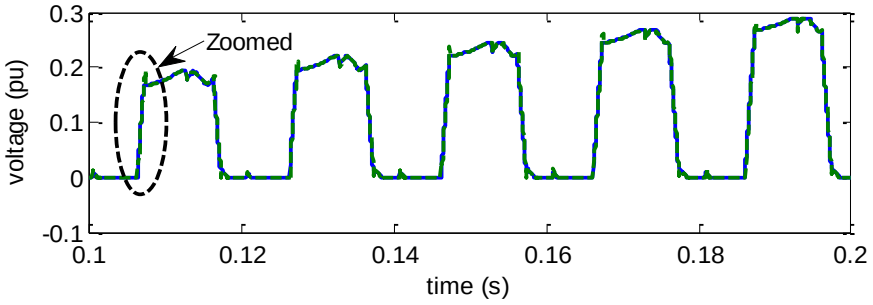
- All capacitor voltages are initially set to zero and all SMs are at BLOCKED state.
- "main AC breaker" devices are closed and "bypass breaker" devices are opened



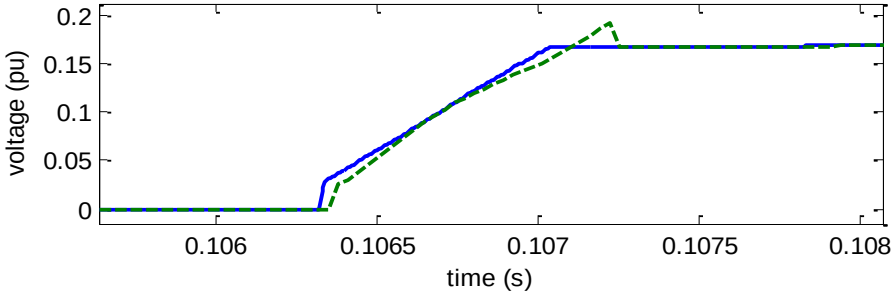
MMC current upper arm of phase A station #1



Sum of all capacitor voltages of MMC upper arm phase A station #1



MMC voltage upper arm of phase A station #1



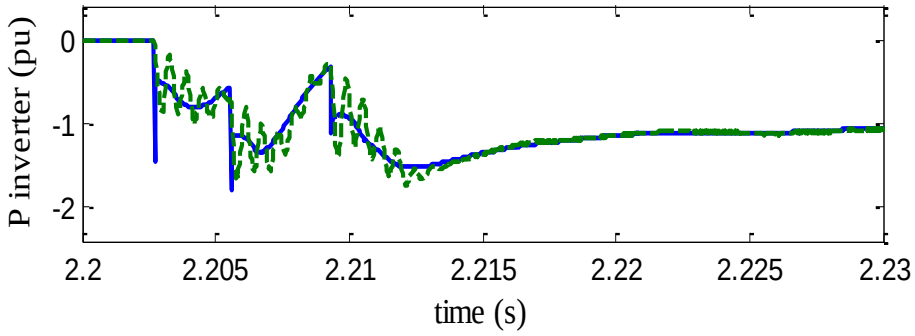
Zoomed waveforms, MMC voltage upper arm of phase A station #1

4. Real-time simulation
Offline to real-time simulation

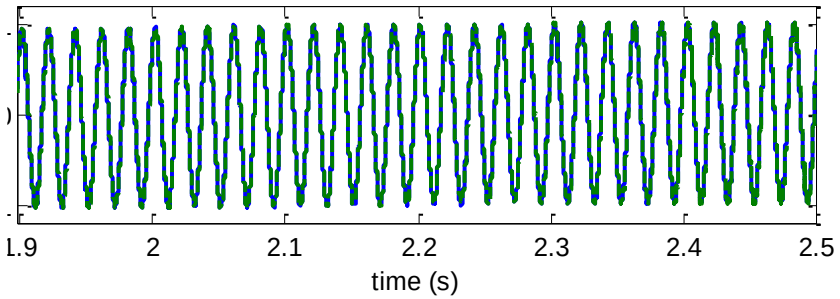
Real-time Model accuracy verification:

Scenario 2: Three-phase AC Fault

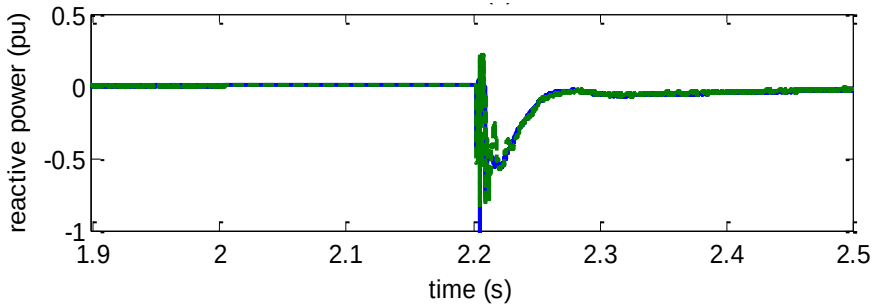
- A three-phase-to-ground fault is applied at T=2s on the ac side between CPU2 and PCU4



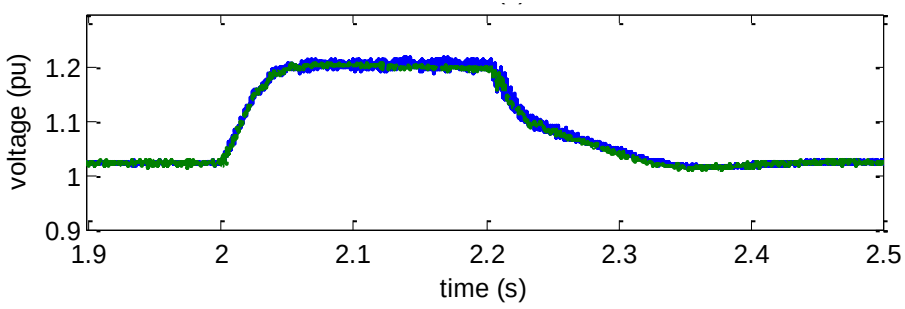
Active power flowing out of ac grid into the station#2



AC voltage, line-to-ground, Station#1, transformer secondary



Reactive power flowing out of ac grid into the station#2



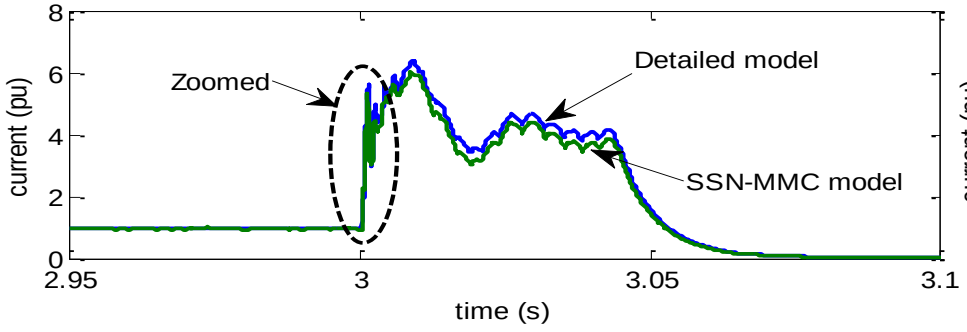
DC voltage, Station#1

4. Real-time simulation
Offline to real-time simulation

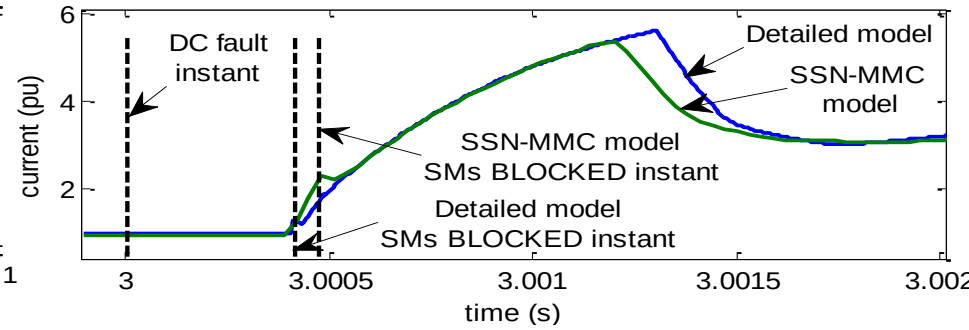
Real-time Model accuracy verification

Scenario 3: Pole-to-pole DC Fault

- Permanent DC fault between the positive and negative poles in Station #2 is applied at 3 s of simulation time
- clearing fault method:
  - All thyristors (K2) are fired and all IGBTs are blocked after the fault
  - The “Main AC Breakers” of both VSC-MMC stations are opened after two cycles



DC current flowing out of Station#1

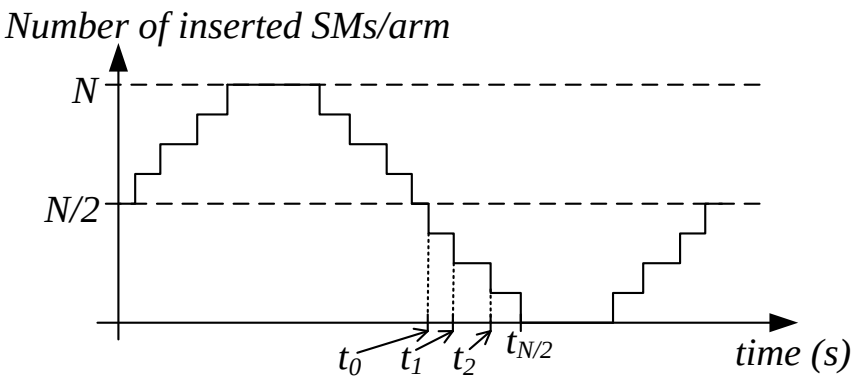


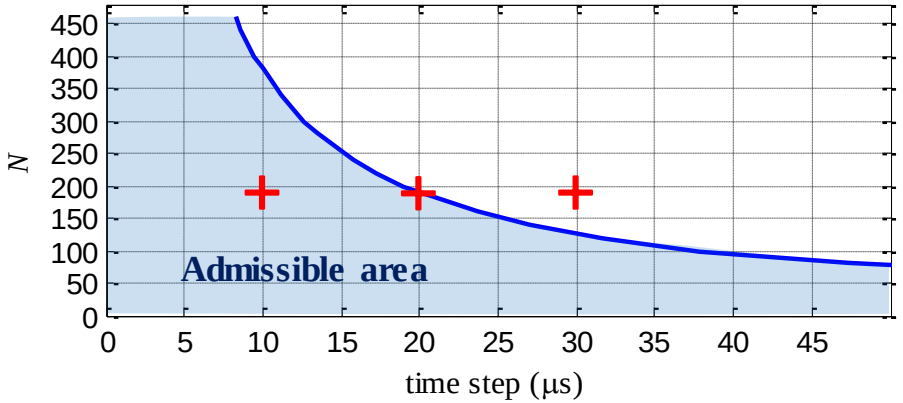
Zoomed waveform

4. Real-time simulation
MMC Performances

The objective of this study is to evaluate the feasibility and performance of the MMC model in real-time simulation.
In order to guarantee the passage through each level, the sampling time must respect certain criteria.
The smallest time interval between two different levels is found where the slope of the desired sine wave is the highest.
For NLC modulation, the controller sampling time-step should respect the following inequality in order to guarantee the replication of each MMC level:

$$\Delta t \leq \frac{1}{1.2(2\pi f)} \arcsin\left(\frac{2}{1.4N}\right)$$



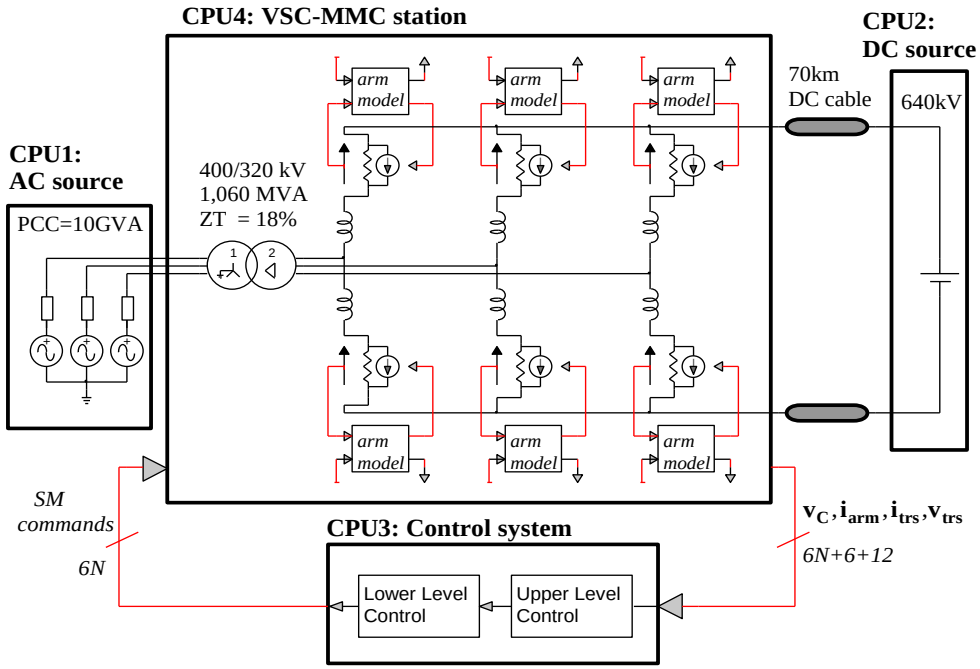


4. Real-time simulation
MMC Performances

CPU-based and FPGA-based implementations were developped for MMCs having up to 401 Levels

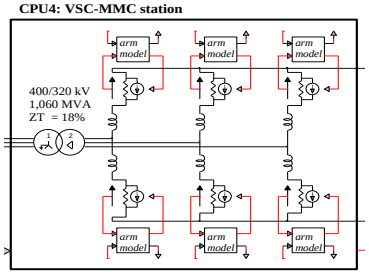
Details:

- Transmission capacity of the system is 1,000 MW.
- DC side is represented with a dc cable and a dc voltage source of 640kV.
- OP5600 real-time simulator from Opal-RT. 3 quad-core processors (for a total of 12 Intel Xeon CPUs) that communicate through a shared memory of 8 GB, and they are able to communicate with the FPGA board through a 2nd generation PCIe link.

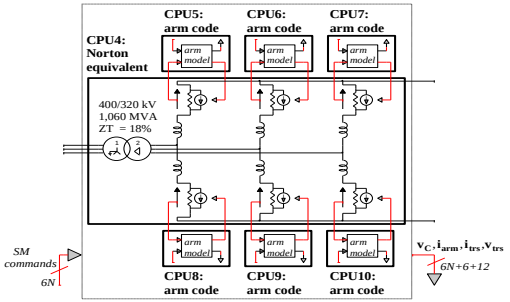


4. Real-time simulation
MMC Performances

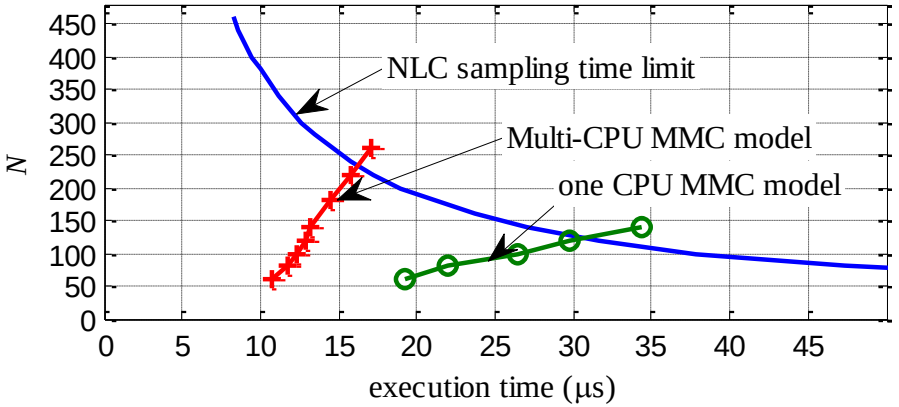
CPU-based model



One-CPU MMC model



Multi-CPU MMC model



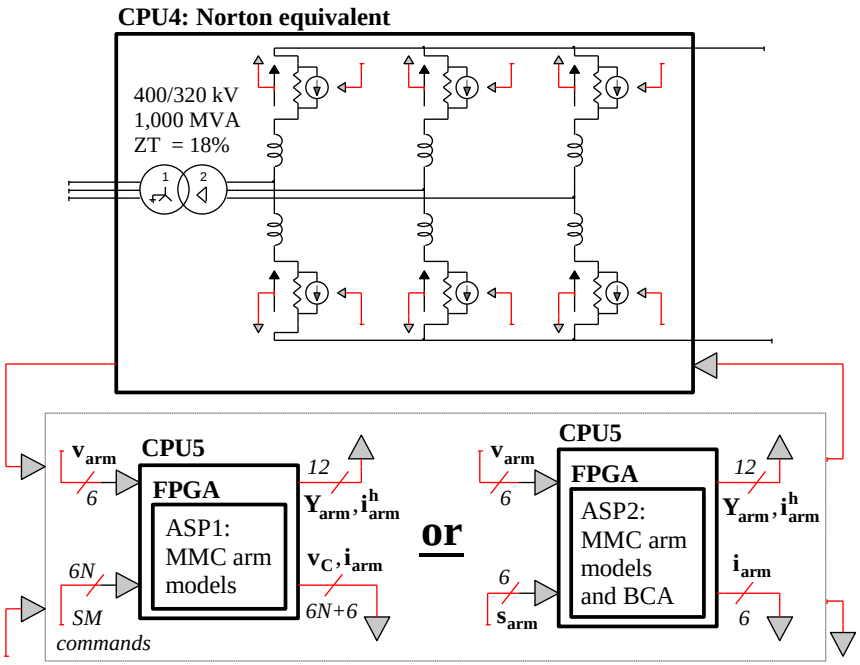
N as a function of execution time for CPU-based models

Maximum number of SMs/arm that can be simulated in real-time with the multi-CPU MMC setup is about 230 SMs/arm

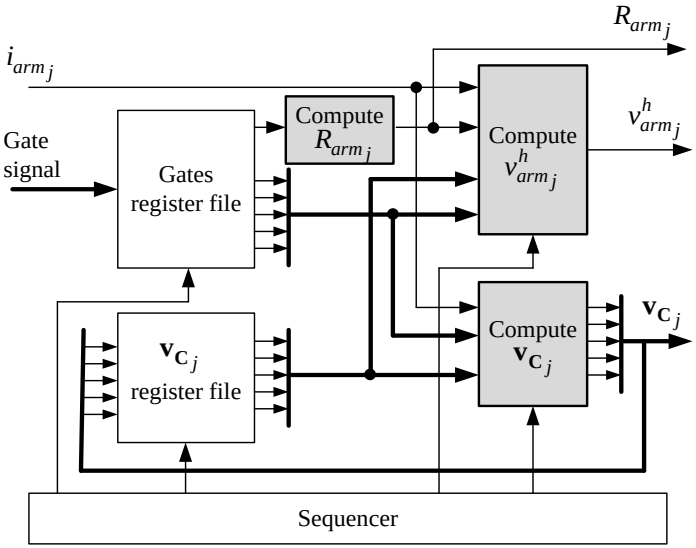
In HIL configuration, the latency produced by communication overhead and I/O management is estimated to reach 9us. The curves must be shifted and the maximum number of SMs/arm for real-time CPU-based simulations now reduces to 160 SMs/arm.

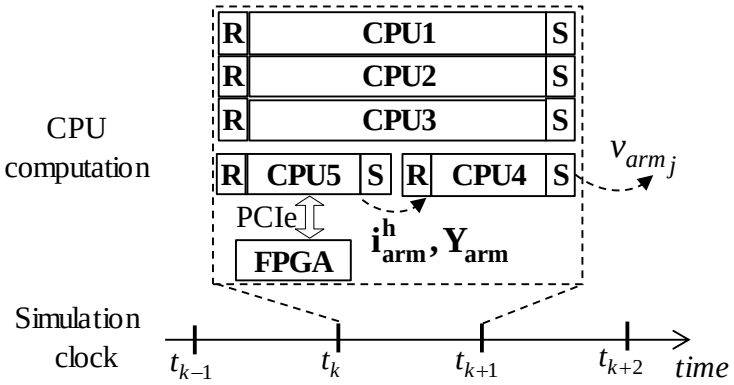
4. Real-time simulation
MMC Performances

FPGA-based MMC model implementation



FPGA-based MMC model with ASP1 and ASP2

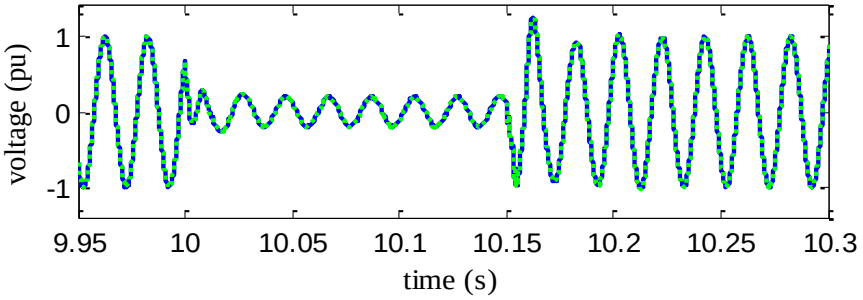




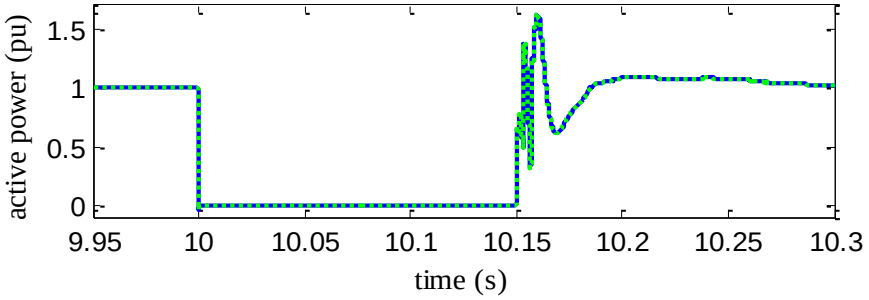
Real-time computation for FPGA-based MMC model

4. Real-time simulation
MMC Performances

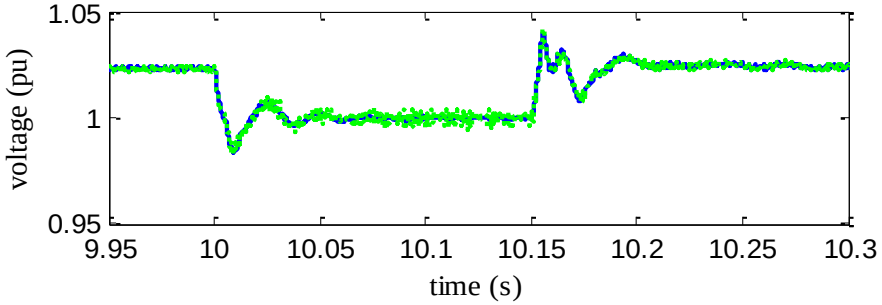
Model validation : Three phase to ground fault for 150ms at PCC. MMC 401 Level.



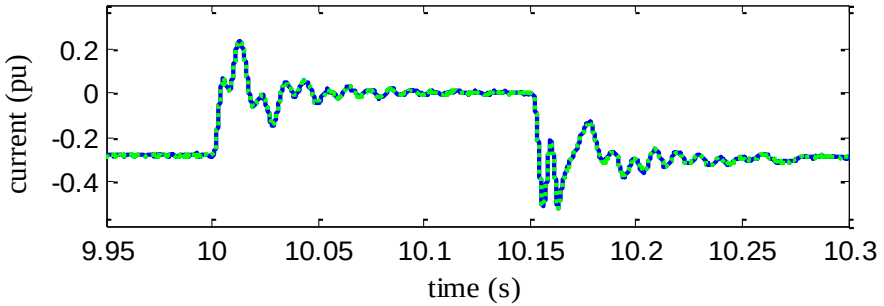
Phase voltage:



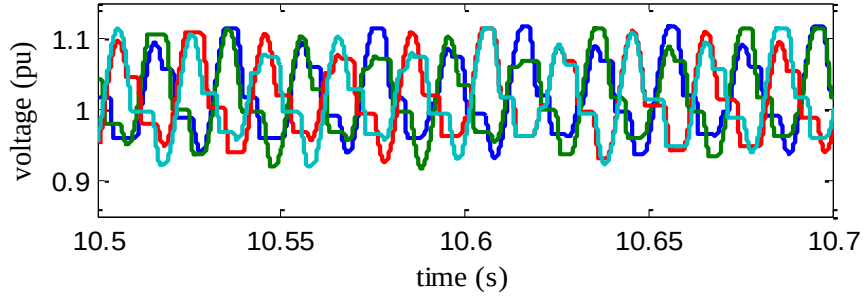
Active power: P



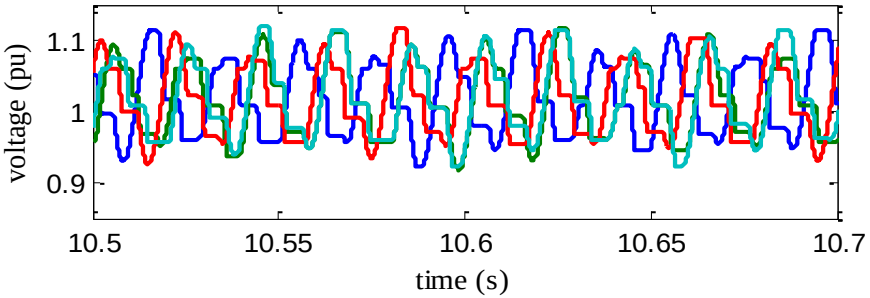
dc voltage



Circulating current



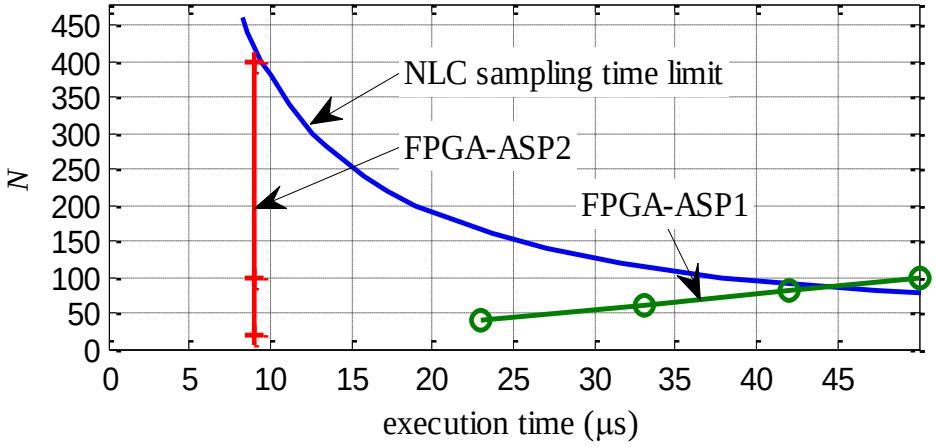
Capacitor voltages of the reference model (One-CPU model)



Capacitor voltages of the FPGA-ASP2 model

4. Real-time simulation
MMC Performances

•For both ASPs, the FPGA runs at 2.4 µs
•The execution times depicted in this figure include CPU4 and CPU5 since they are in series.
•FPGA-ASP1 MMC model has a poor performance in comparison with the CPU-based model. This is explained by the important amount of data that has to be exchanged between the FPGA and the CPU5 connected through the PCIe link (2×6N+6 values).
•FPGA-ASP2 model is the best among those reported in this paper. It is able to achieve an execution time of 9 µs. It does not depend on the number of SMs. The FPGA-ASP2 setup is more realistic within the context of HIL simulation, where the gating signals are provided by a physical controller to the FPGA through its low latency I/Os.



5. Conclusion

Four types of MMC model suited for EMT-type studies have been developed and presented:

- Model 1 is currently the most detailed model, but requires very high computing times with available numerical methods. It can be used as a highly accurate reference model and for calibrating simplified models.
- Model 2 allows reducing the converter circuit for achieving much higher computing speeds. This model provides accurate results when the balancing control of each capacitor has to be analyzed.
- Model 3 delivers further improvements in computational performance. It should be used with caution when the number of levels decreases (<101 Level). This model can account for circulating currents and energy storage in each arm.
- Model 4 is based on average value method. It allows increasing the time-step to speed up computing times. DC side modeling remains less accurate.

Real time simulation for MMC has been developed:

- It has been shown that the CPU-based MMC model is limited to 231 levels. This limit is reduced to 161 levels for HIL simulations due to latencies in communications and I/Os.
- Two different FPGA-based MMC model setups has been presented. In the second setup (ASP2) the BCA is implemented on the FPGA and the lowest execution time of 9 µs is achieved. Moreover, the FPGA based MMC arm models run at 2.4 µs. These execution times do not depend on the number of MMC levels and can go up to 400 SMs/arms.

6. References

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Questions?