Designing low phase noise integrated VCOs

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5. Oscillator combining

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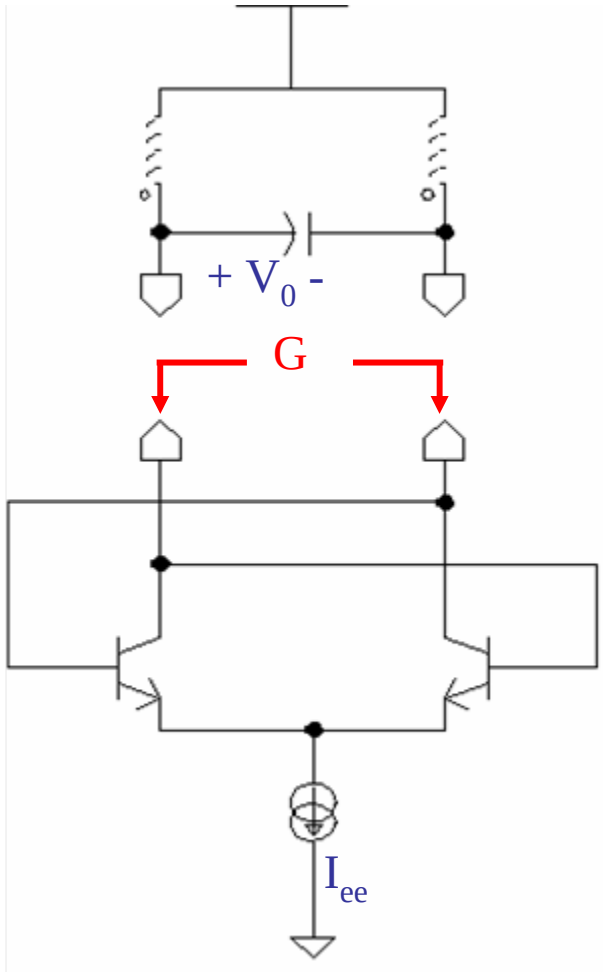
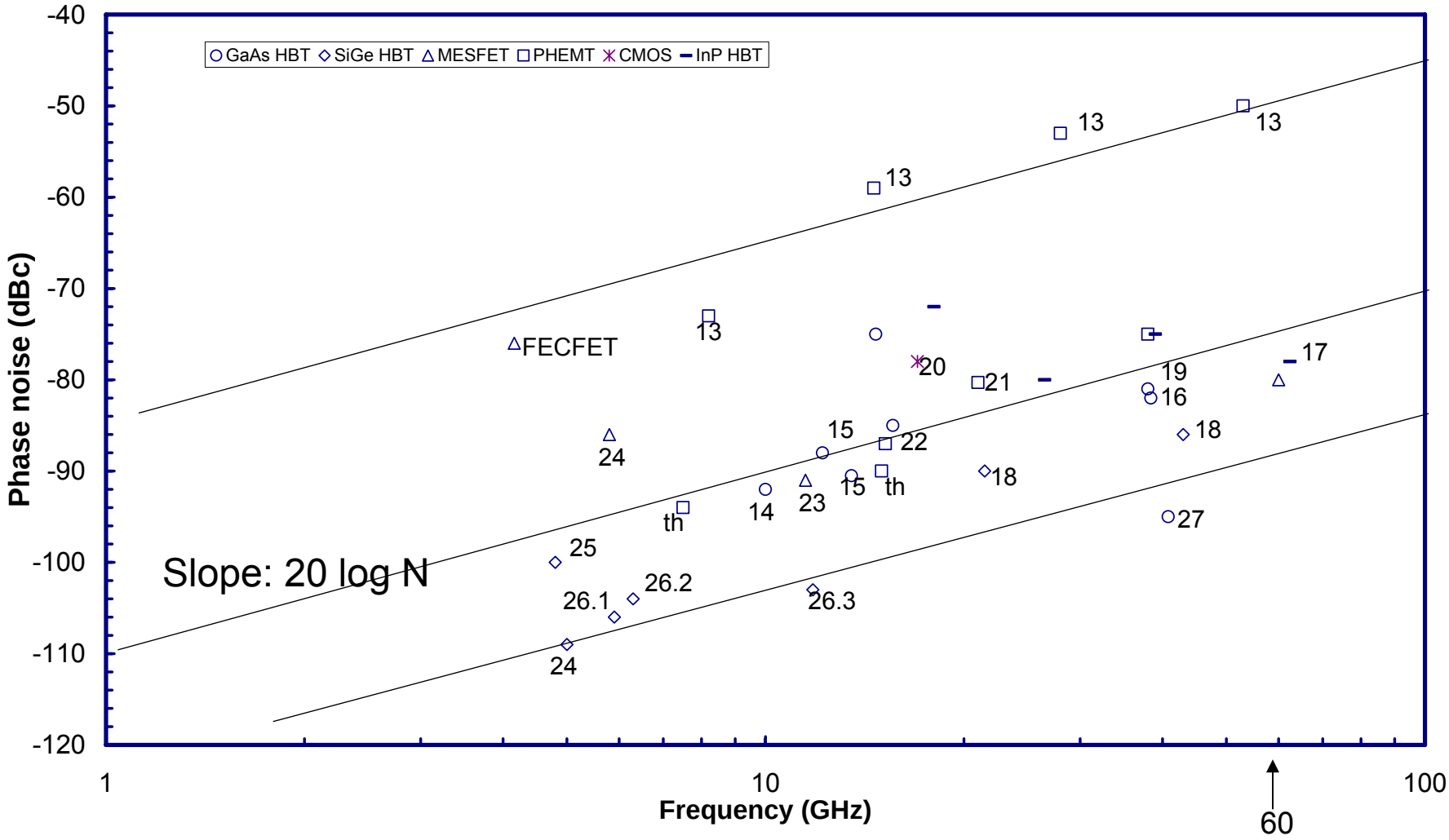
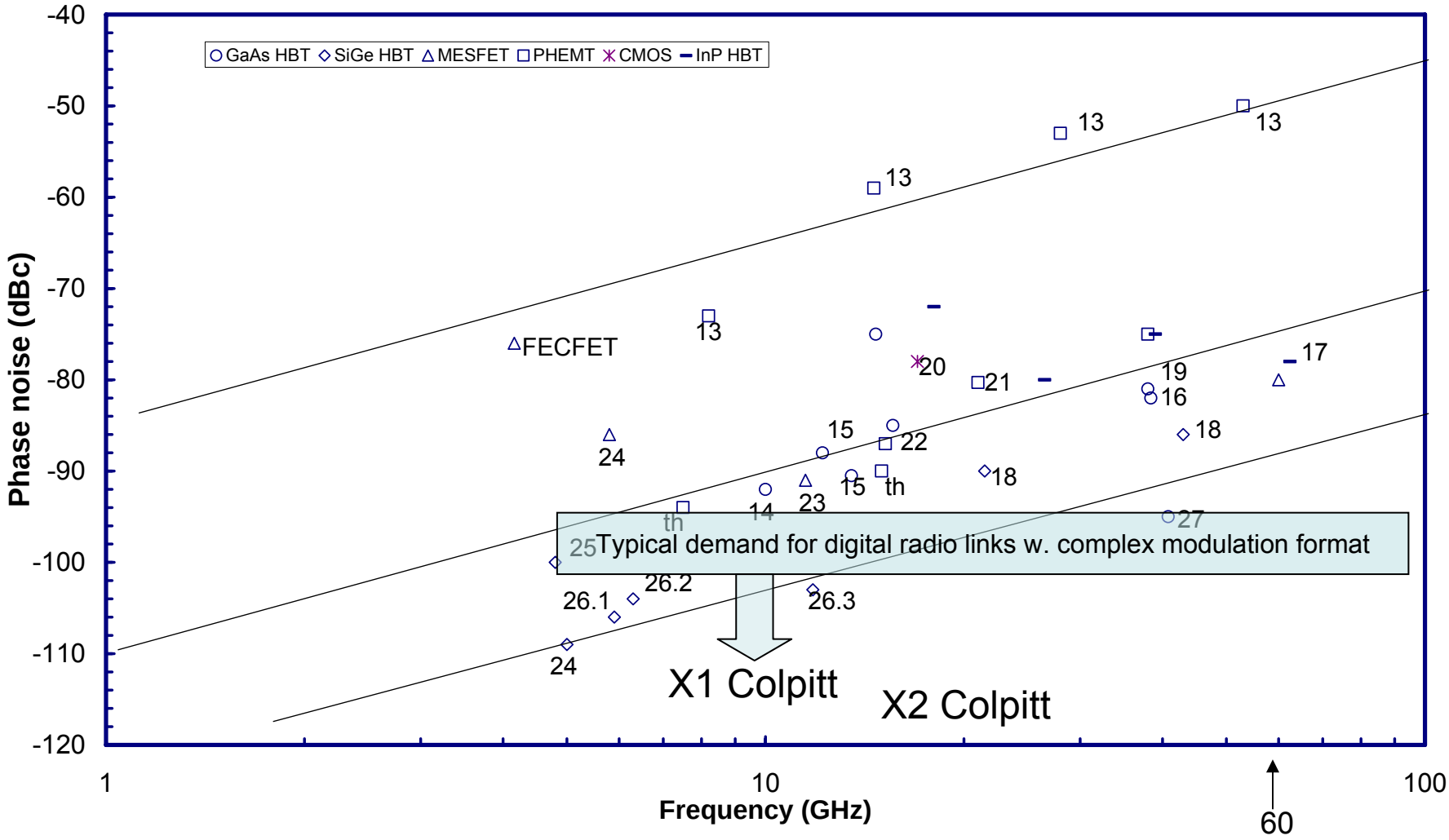
2. Balanced Colpitt
3. Second harmonic Balanced Colpitt
4. Hartley

-Conclusions



Published data phase noise versus frequency @100kHz offset frequency



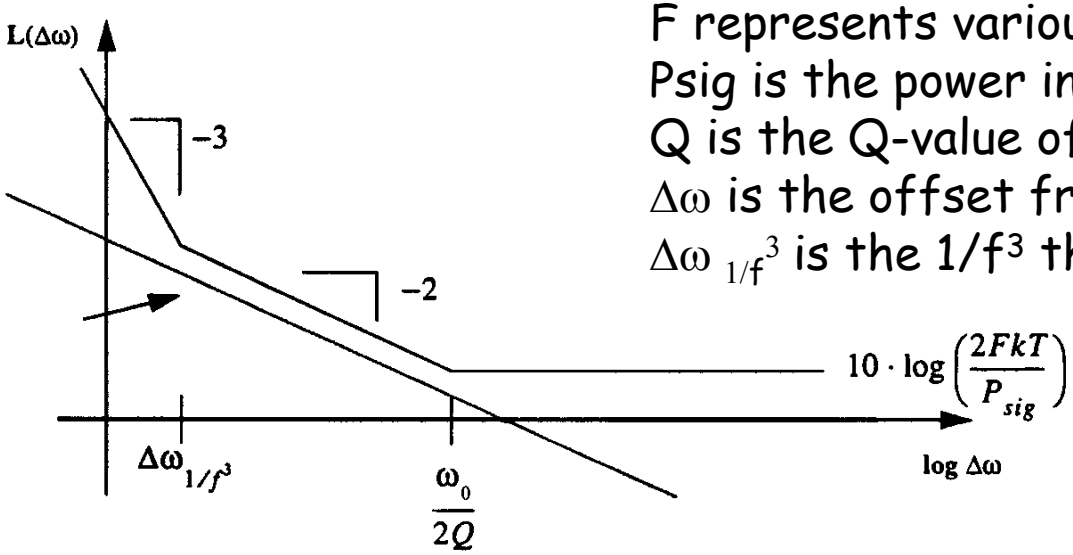


See IEEE JSSC, Vol. 40, no 10, October 2005

Leeson's model for phasenoise

Leeson described the variation of the phase noise 1966

$$L(\Delta\omega) = 10 \cdot \log\left\{ \frac{2 \cdot F \cdot k \cdot T}{Psig} \left[1 + \left(\frac{\omega_0}{2 \cdot Q \cdot \Delta\omega} \right)^2 \right] \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|} \right) \right\}$$



F represents various noise mechanisms
Psig is the power in the resonator
Q is the Q-value of the resonance circuit
$\Delta\omega$ is the offset frequency
$\Delta\omega_{1/f^3}$ is the 1/f³ the corner frequency

Technologies used in this work and associated critical parameters

Technology	BV	f_T GHz	f_{max} GHz	manufacturer
InGaP-GaAs HBT	10	60	110	K*ON
SiGe HBT	2.5	70	90	STM
SiGe HBT	3.3	48	65	IBM
CMOS	1.2	170	240	IMEC
PHEMT	8	70	180	OMMIC
MHEMT	8	90	210	WIN

Tank design: Choice of L and C: **High tank energy design**

Maximize the ***tank energy*** for lowest phase noise*

$$E_{\text{tank}} = \frac{1}{2} C \cdot V_{\text{tank}}^2 = \frac{1}{2} L \cdot I_{\text{tank}}^2 \qquad \omega_0 = \frac{1}{\sqrt{L \cdot C}}$$

V_{tank} is set by the breakdown voltage of the transistor, maximize C

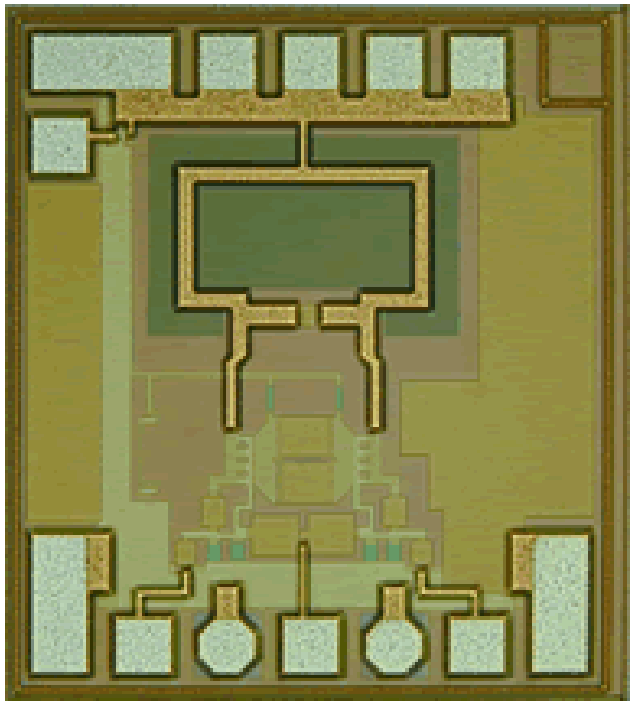
->L have to be decreased to maintain the oscillation frequency
->I_{tank} have to be increased in order to increase the tank energy

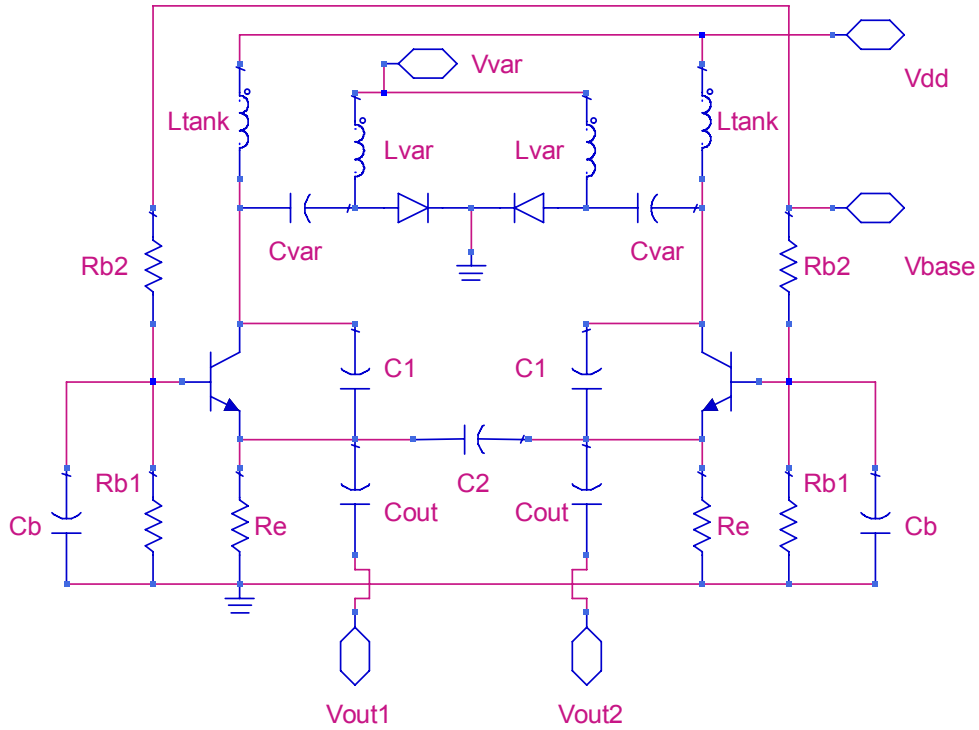
For high tank energy design, it becomes critical that the transistor can deliver a high current, depends on the Q-value of the tank

Don't forget to design the tank for large circulating currents, be careful not exceeding the current density specs for transmission lines, coupling capacitors etc

*D Ham, A Hajimiri, IEEE JSSC Vol 36, no. 6, pp. 896-909, June 2001

Example 1: 5 GHz SiGe Balanced Colpitt oscillator





Why Colpitt ?

-Can be designed for high efficiency -> VCO-operation at a lower temperature for a certain tank energy, less dc-power consumption

-excellent impulse sensitivity characteristics* -> favorable for low phase noise

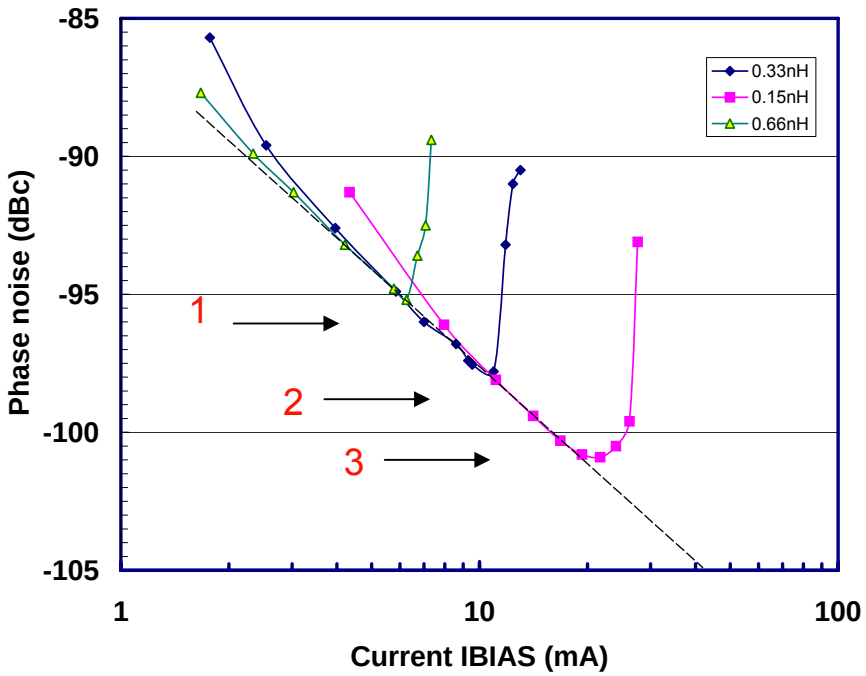
However:

-frequency dependent negative resistance

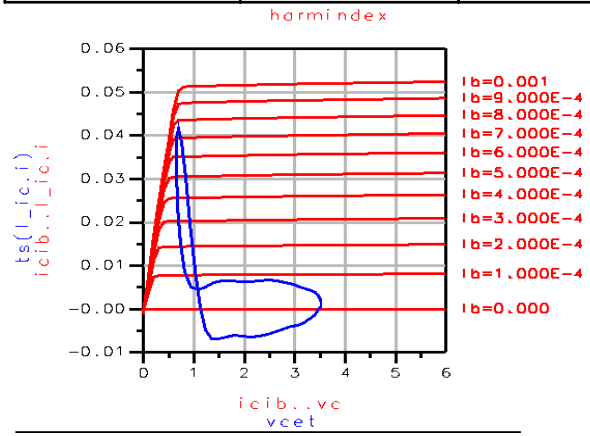
-amplitude control not straightforward

*Ali Hajimiri, Thomas H. Lee,'Low noise oscillators', ISBN 0-7923-8455-5, 1999, Kluver Academic Publishers

Example: Simulation of a single Colpitt oscillator

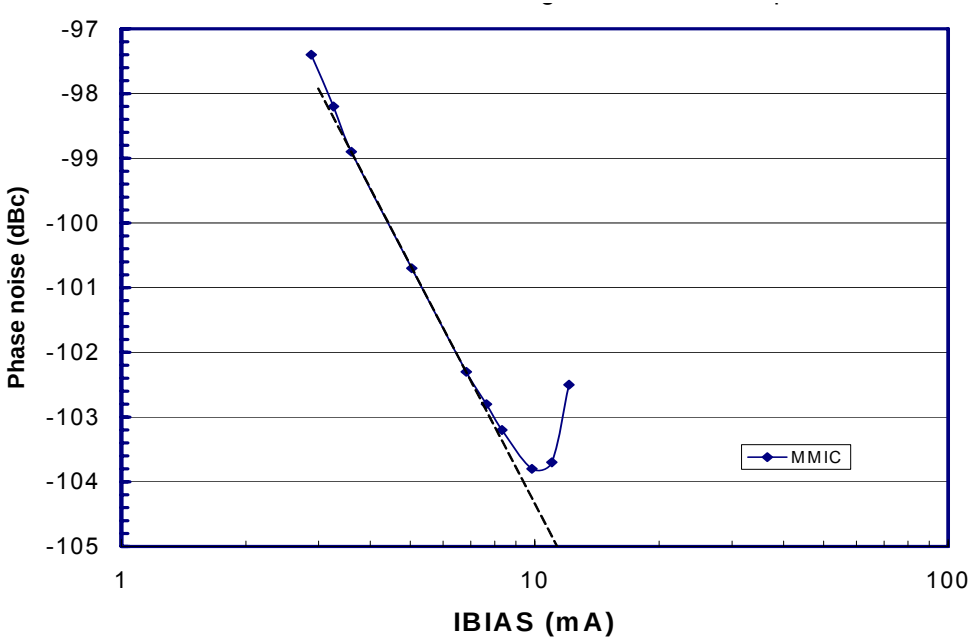


inductance nH	Series - resistance of inductor	Inductor Q-value	transistor size
0.15	0.41	11.5	6x20
0.33	0.9	11.5	3x20
0.66	1.8	11.5	2x20

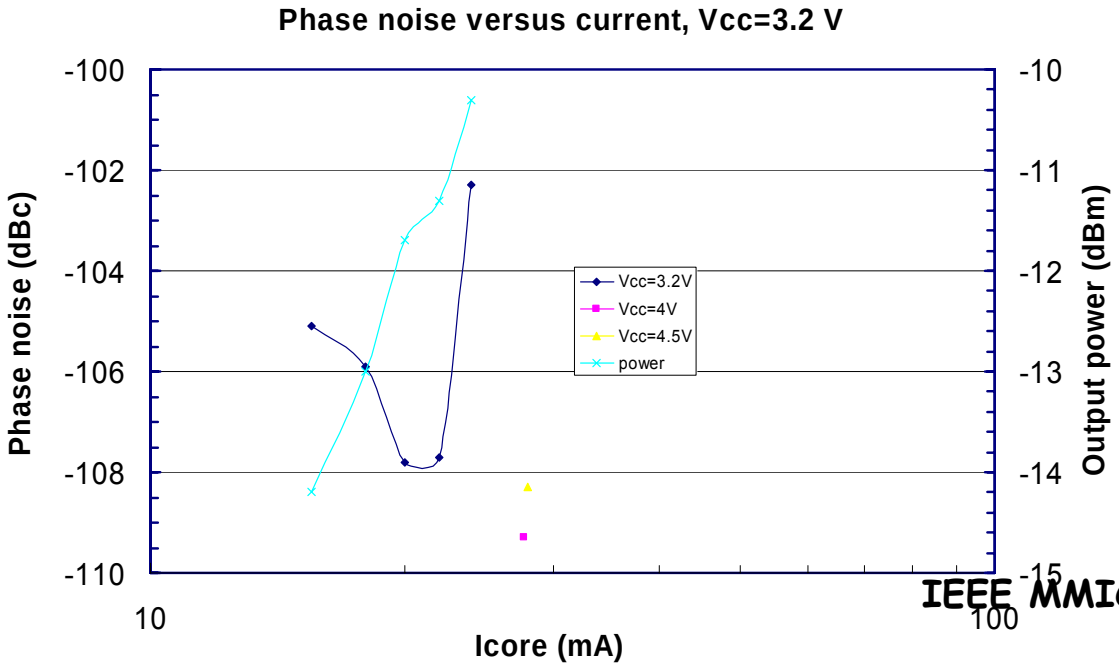


The tank inductor for the Colpitt oscillator is varied from 0.15 nH to 0.66nH, the oscillation frequency is kept constant.

The dc-current I_{BIAS}, controls the ac amplitude of the oscillation and at some current, the ac tank voltage gets voltage limited, the phase noise is increasing at this bias (1). By increasing the maximum tank energy i e by decreasing the tank inductance and increasing the tank-capacitance, we can reach a new, lower level of minimum phase noise at the onset of voltage saturation (2 and 3)



Simulated phase noise @100kHz offset for the coupled SiGe oscillator versus the biascurrent (emitter current in one of the transistors).

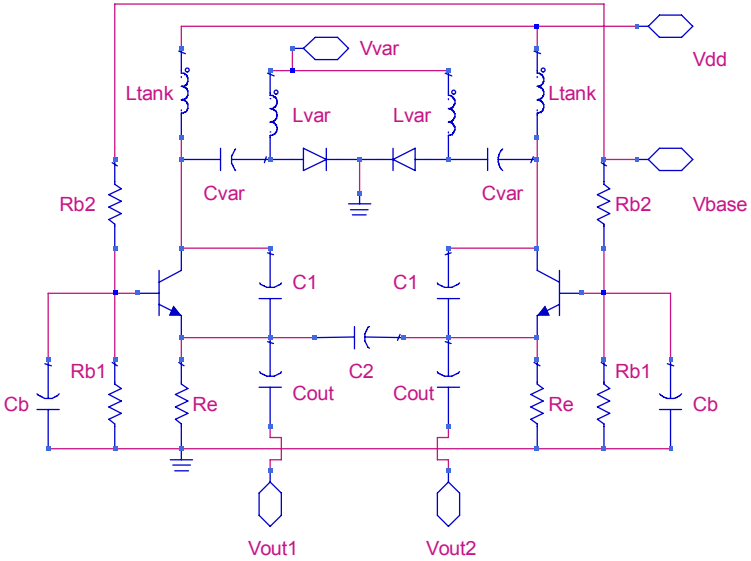


Measured phase noise @100kHz offset for the coupled SiGe oscillator versus the bias current (sum of the emitter currents for both transistors).

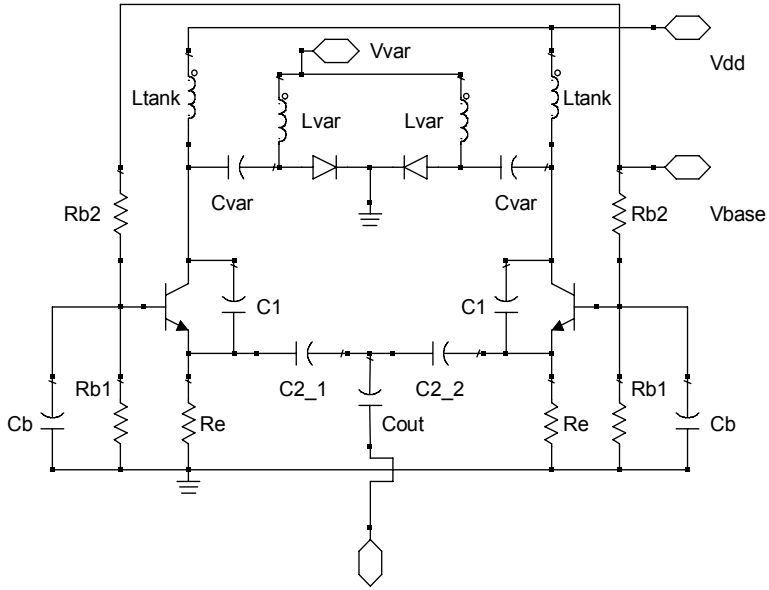
A minimum of -109dBc is obtained at Vcc=4.5V

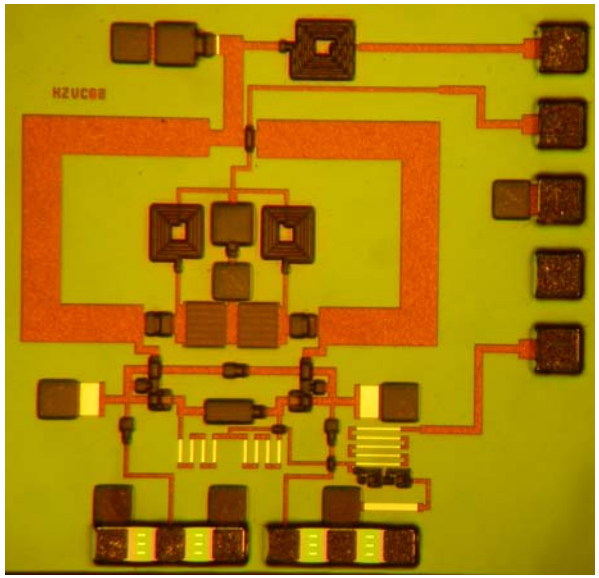
Example 2: InGaP-GaAs Coupled Colpitt VCO with interdigitated varactor

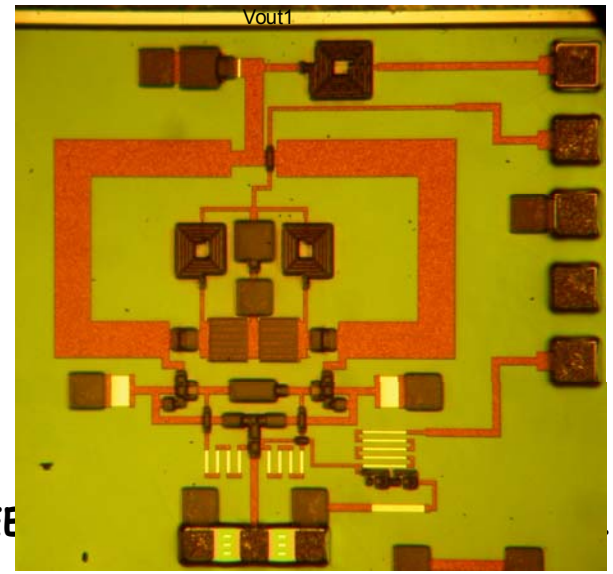
Fundamental frequency, VCO1



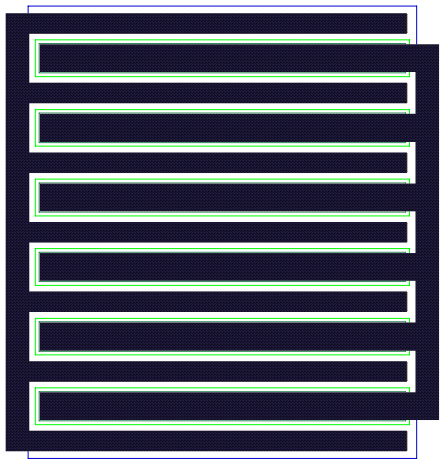
Second harmonic, VCO2

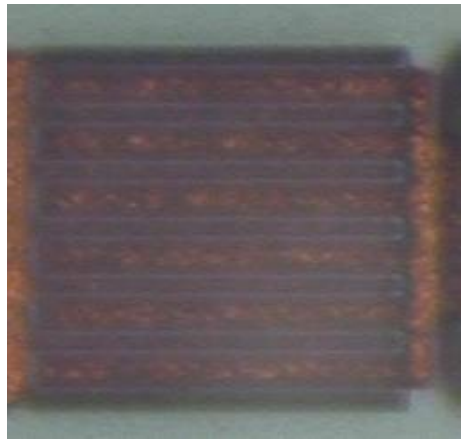


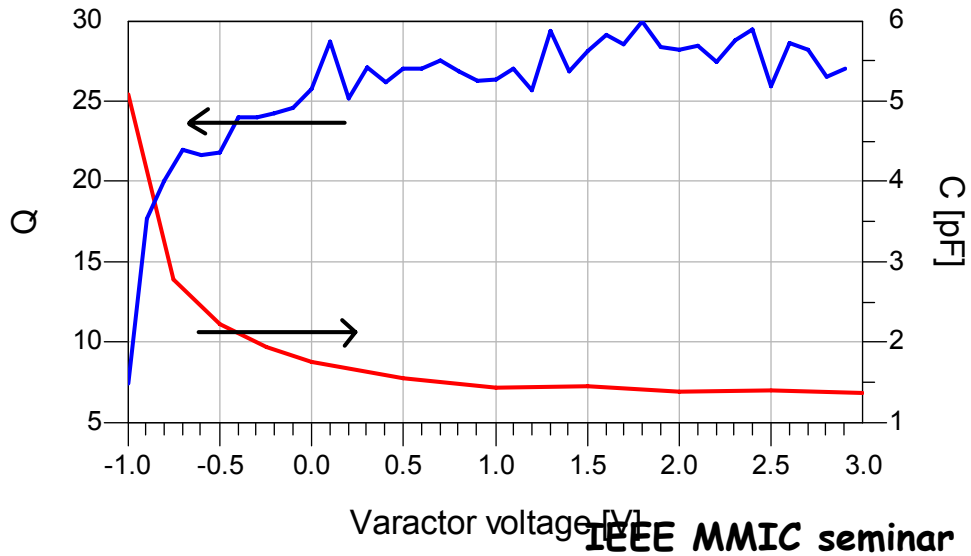




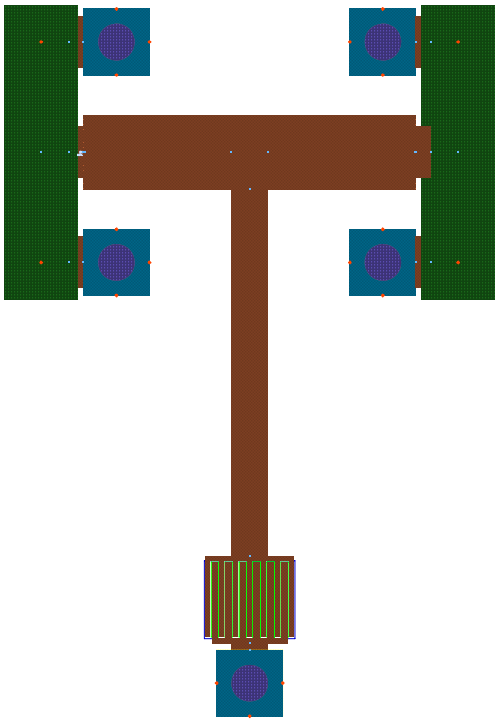
Varactor design 6x10x100 um B-C junction for optimized Q-value

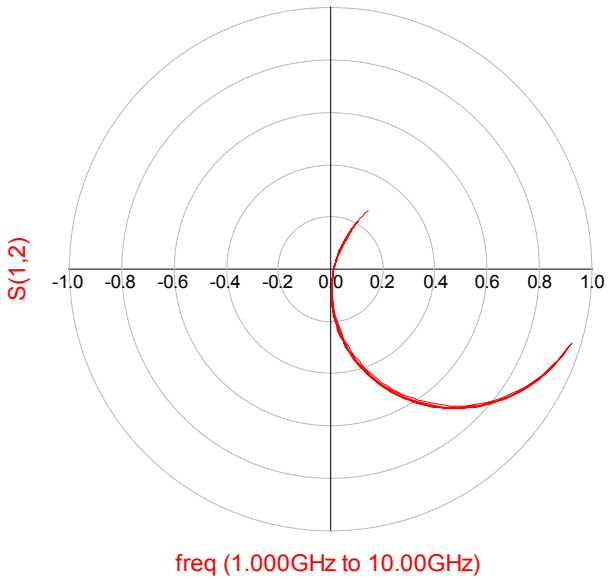


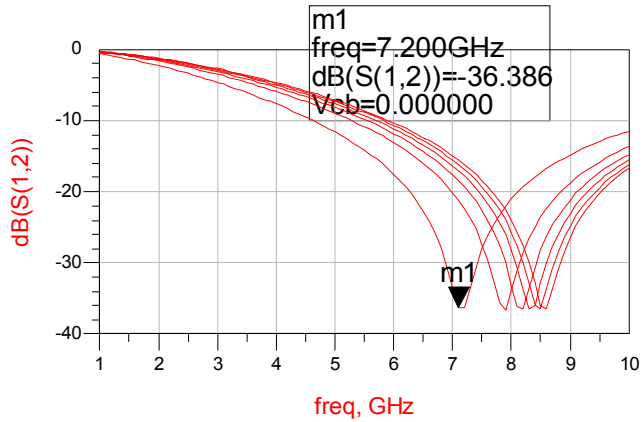


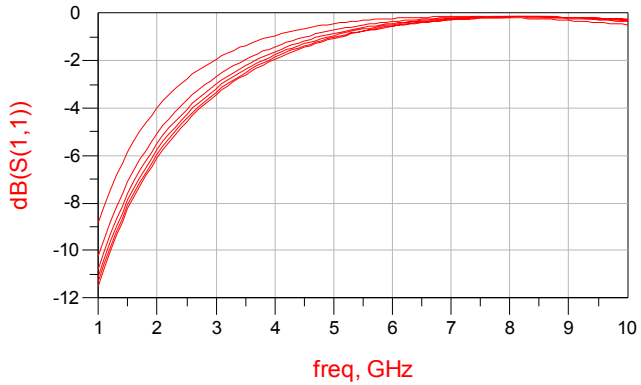


DeLoach varactor test circuit for C and Q-value evaluation



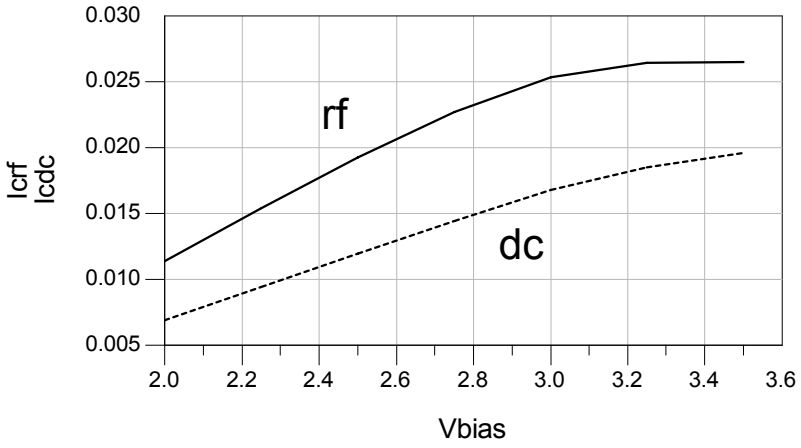




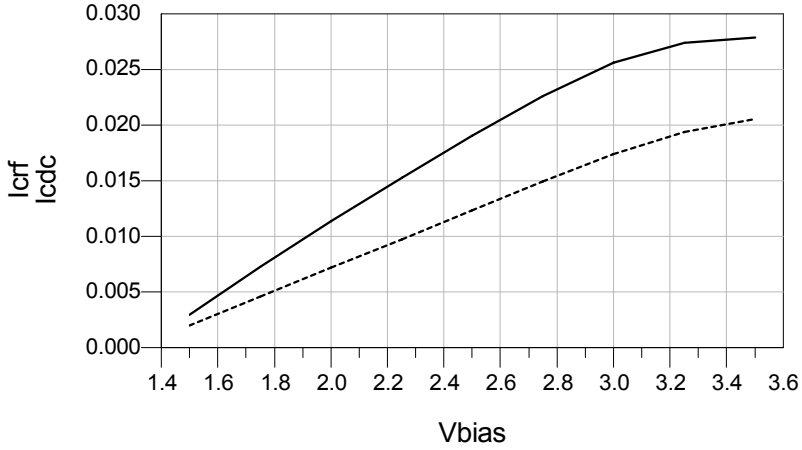


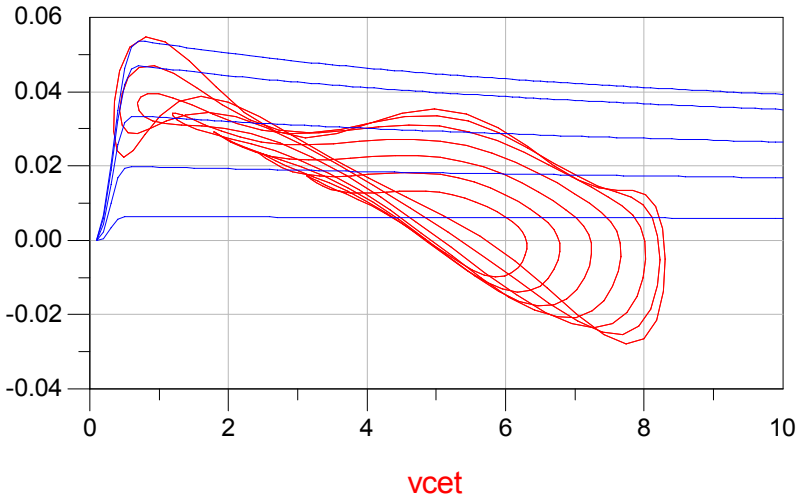
RF and DC collector current versus bias voltage, Ic-Vce trajectories

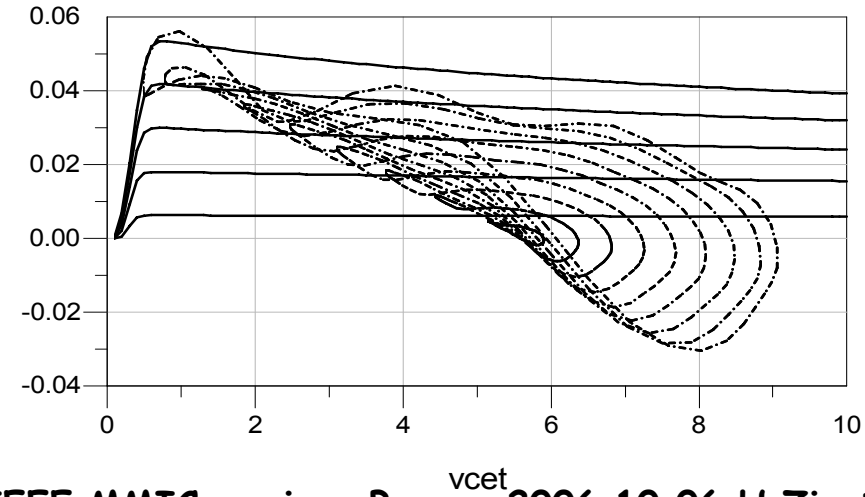
Fundamental (VCO1)



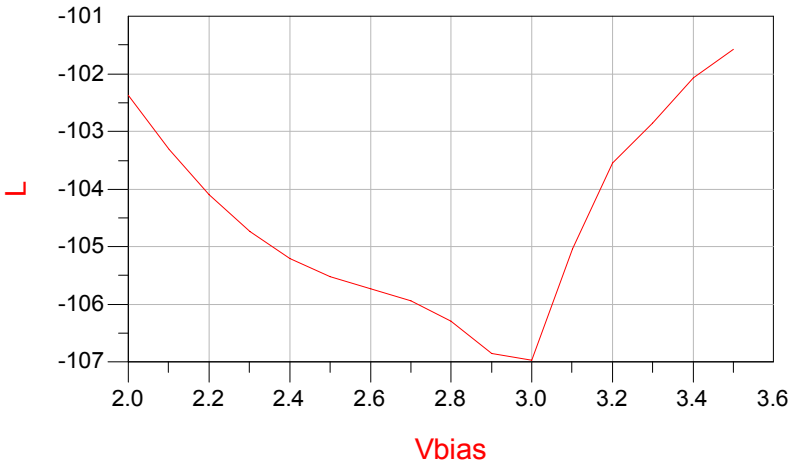
X2 (VCO2)



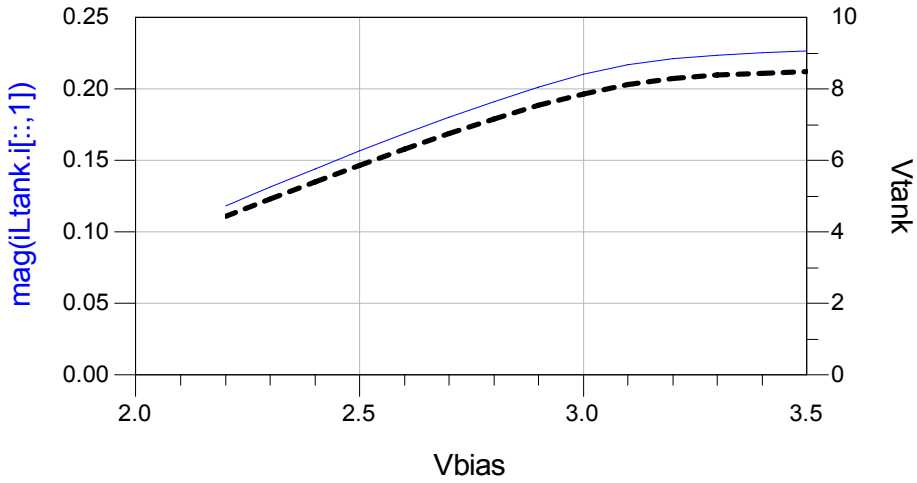




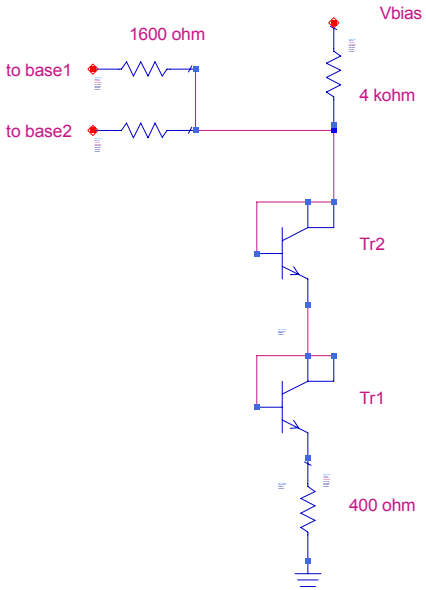
The simulated phase noise at an offset frequency of 100kHz (fundamental VCO).



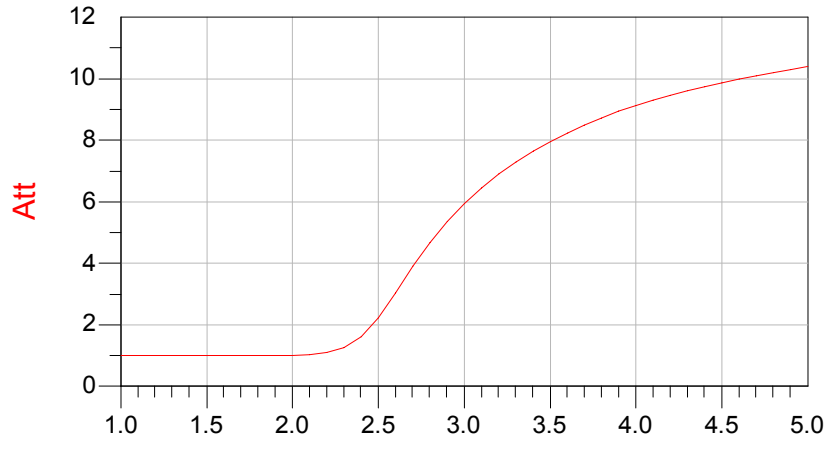
The simulated tank inductor current and the tank voltage (dashed line) versus Vbias.



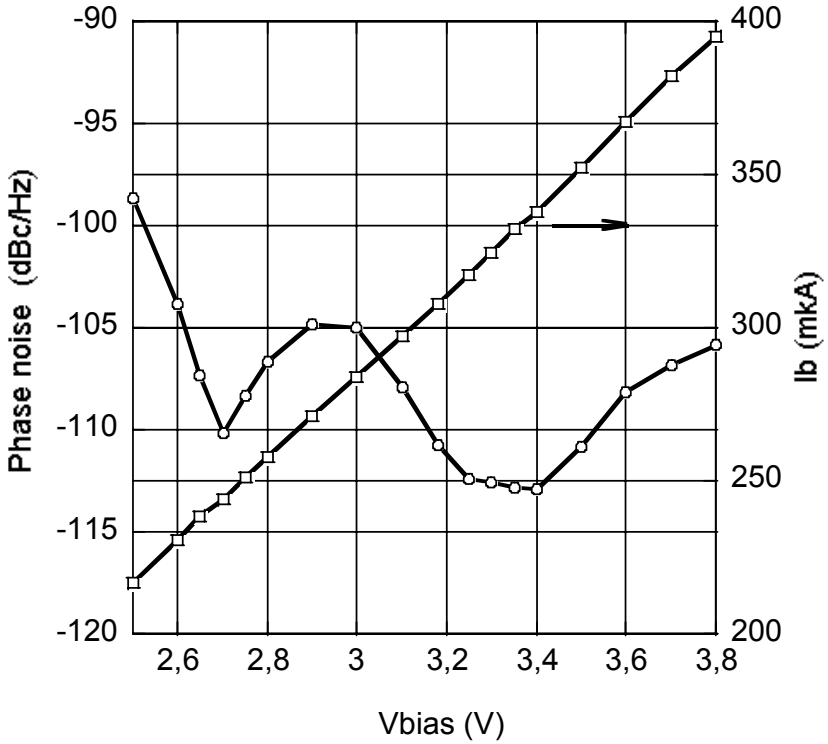
The base-current bias circuit

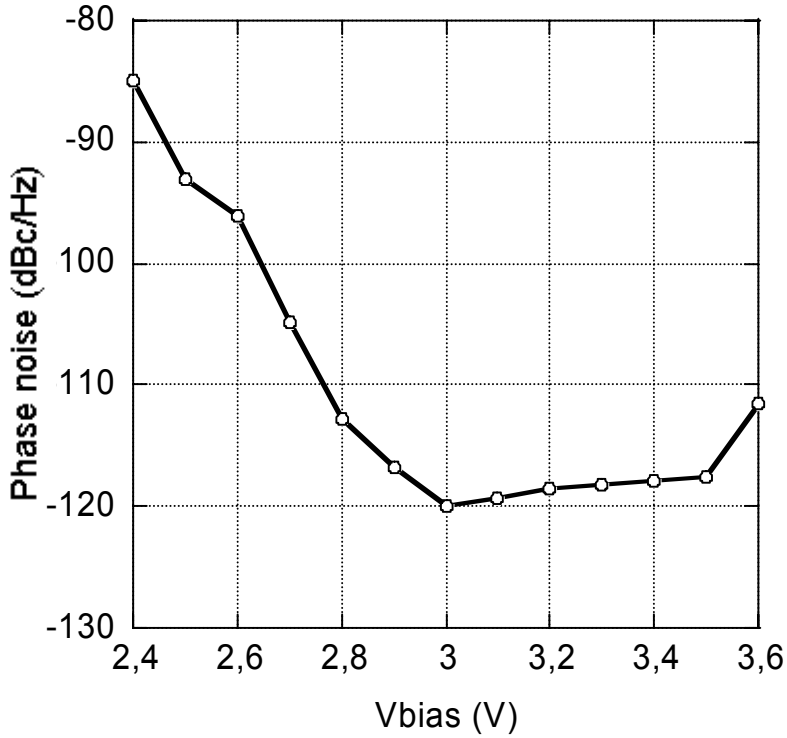


Attenuation of a noise signal at the bias terminal versus Vbias



Phase noise and core current versus base bias voltage for VCO1 and VCO2.

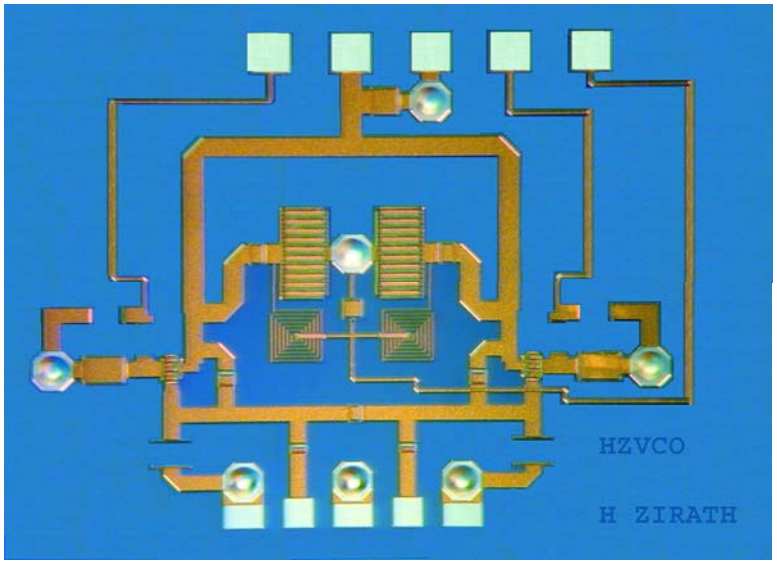


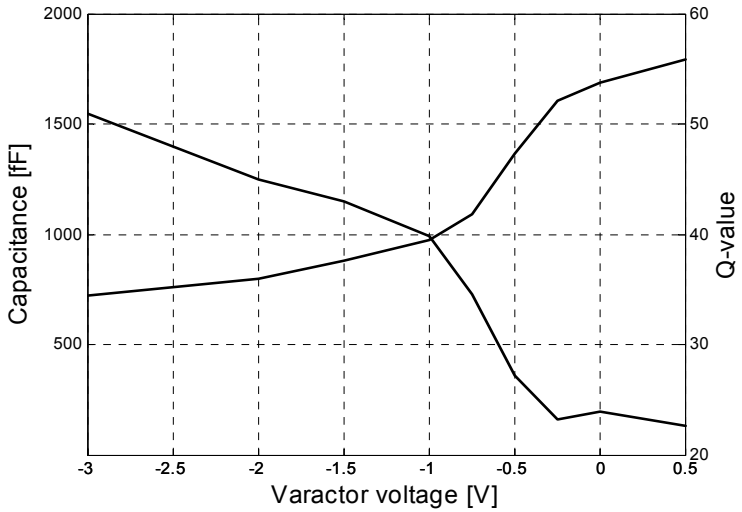


PHEMT and mHEMT technologies are very suitable for mm-wave systems but HEMT-based VCOs have usually high phase noise ?

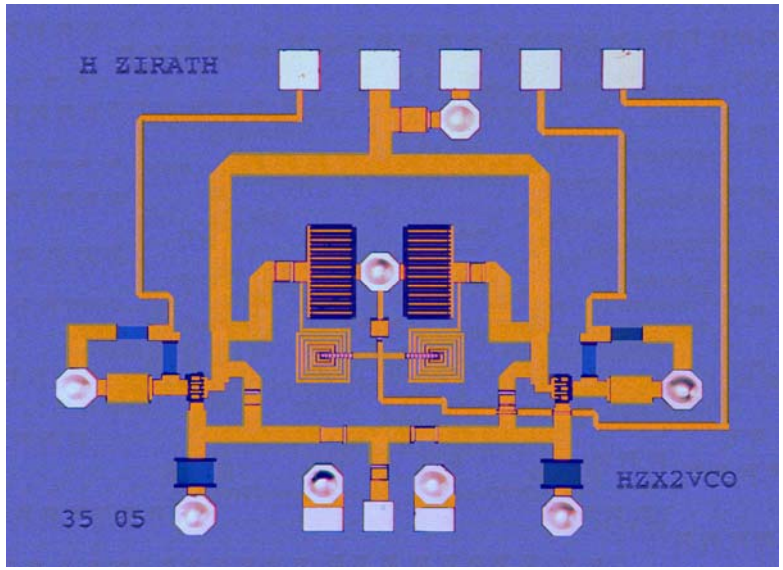
Example 3: PHEMT Coupled Colpitt VCO with interdigitated varactor

7.5-7.88 GHz, Pout >4 dBm
$\mathbf{L_{min}}$=-90 to -95 dBc @100kHz
P_{DC}=150 mW



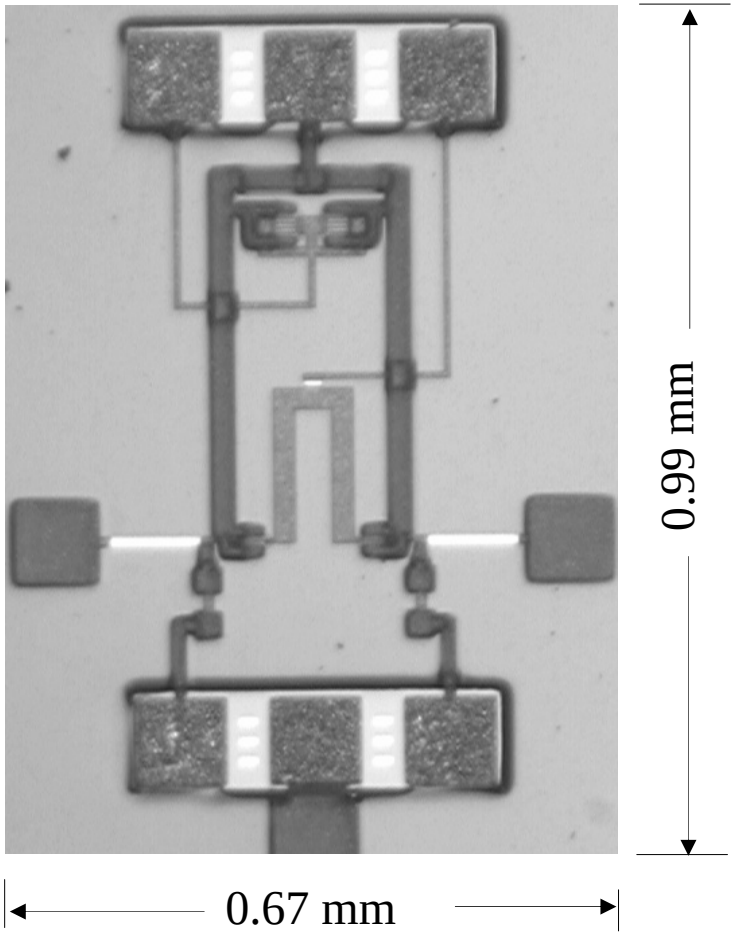


14.9-15.8 GHz, Pout= -2 to 2dBm
$\mathbf{L_{min}}$=-104 dBc @100kHz at 14.9 GHz,
P_{DC}=150 mW, large **L**-variation



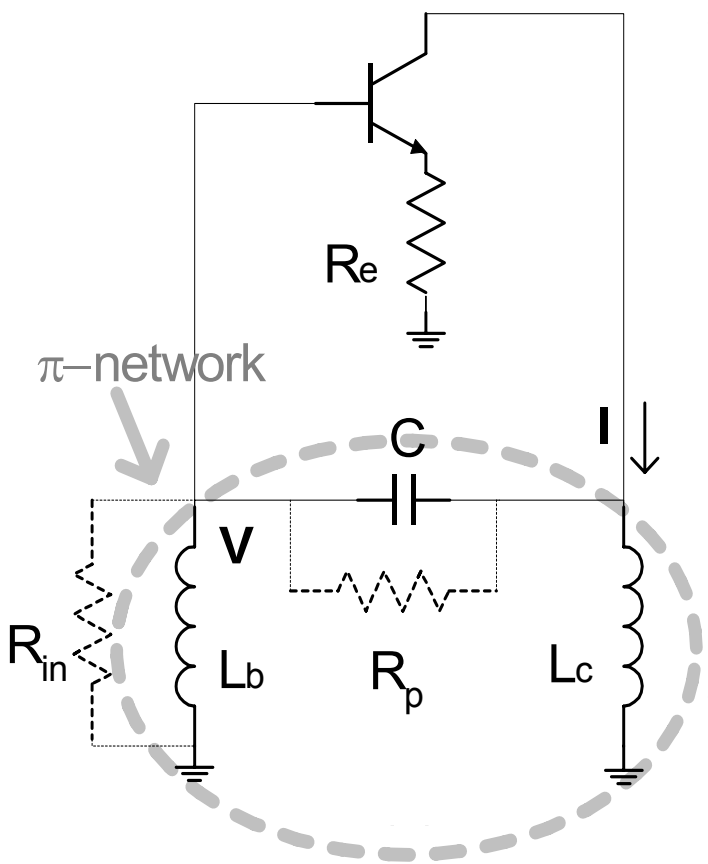
High Q-values of varactor achieved:
40-50 for V_{var}< -1V
20 parallel gate-fingers Lw=100um

Example 4: InGaP-GaAs HBT Coupled Hartley VCO

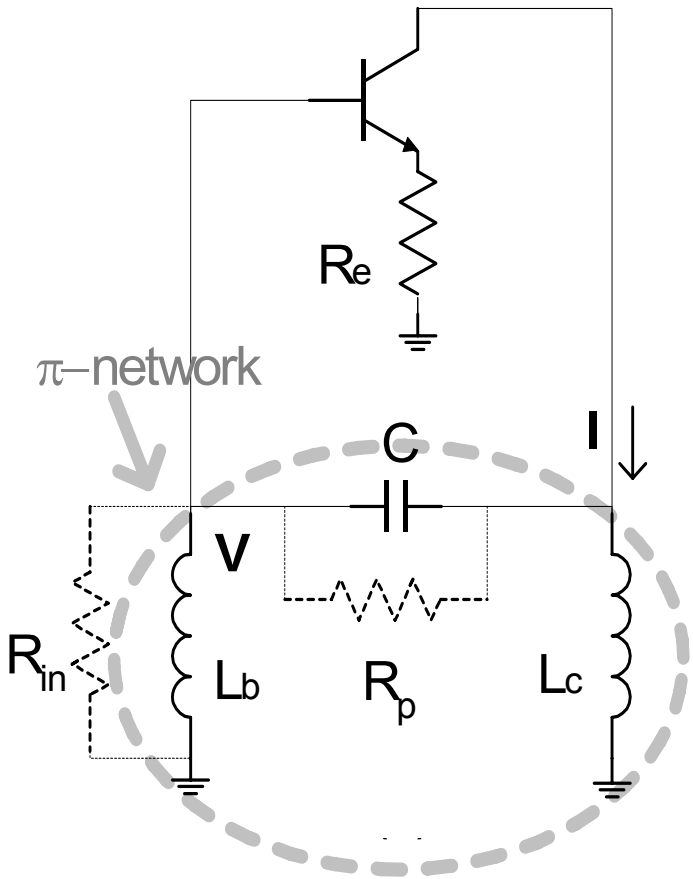


Bao

Single-ended Hartley VCO



- At high frequency, a Hartley VCO has a better phase noise performance than a Colpitts VCO, because
  - the resonator of Hartley VCO consists of two inductors and one capacitor, instead of two capacitors and one inductor for Colpitts VCO
  - Inductors has higher Q value than that of capacitors, thus, the reasonator of Hartley VCO has higher Q value than that of Colpitts VCO.
- The π-network in a Hartley VCO
  - acts as a resonator
  - offers 180-phase shift to compensate phase shift between base-collector
  - transforms impedance.

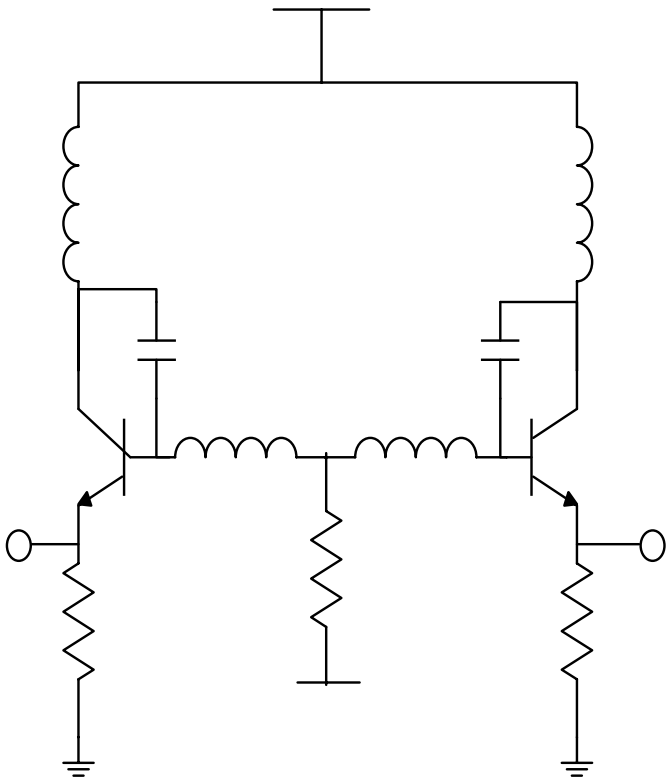


- Transistor in common-emitter configuration is used, which has high collector resistance and moderate base resistance

  ⇒ loading resonator slightly comparing to CB or CC configuration where a small emitter resistor would load resonator heavily.

- The transistor in CE configuration also has the highest gain comparing with other configurations

  ⇒ less DC current is needed to sustain an oscillation, and less noise is generated by active device

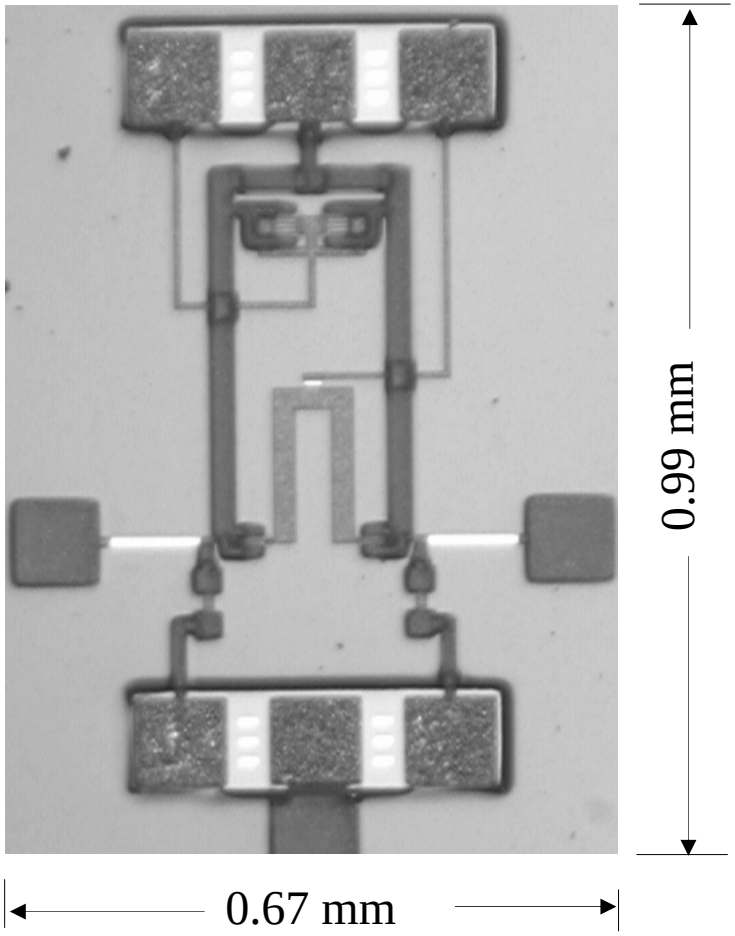


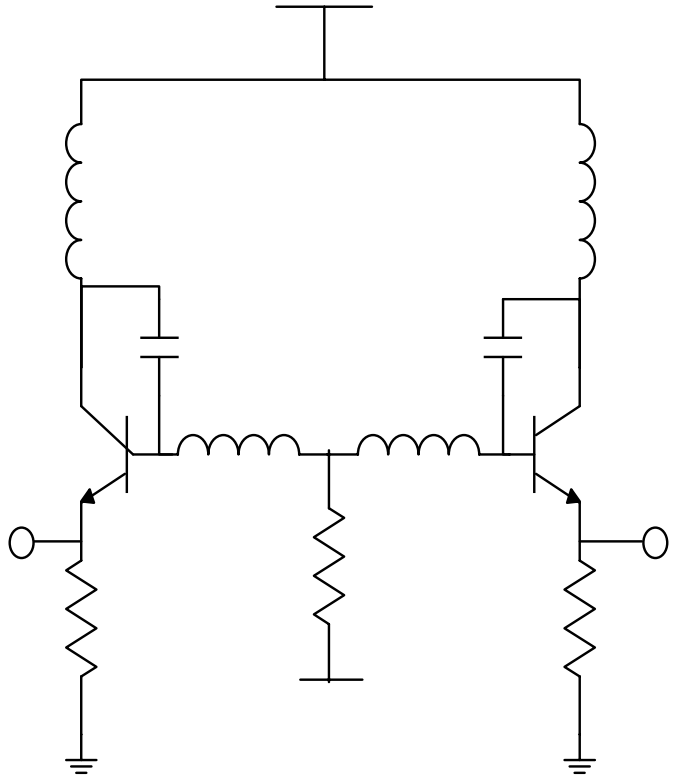
- Two single-ended Hartley VCOs consists of a balanced Hartley VCO
- The differential output signals are taken from emitters
  - outside load does not connect with resonator directly
  - transistors acts as a buffers

⇒ reducing load-pull effect and phase noise

Bao

A 25GHz VCO in InGaP/GaAs HBT technology





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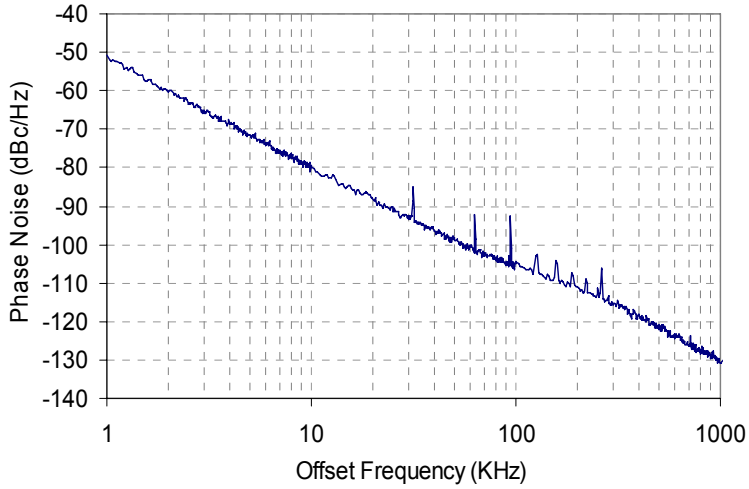
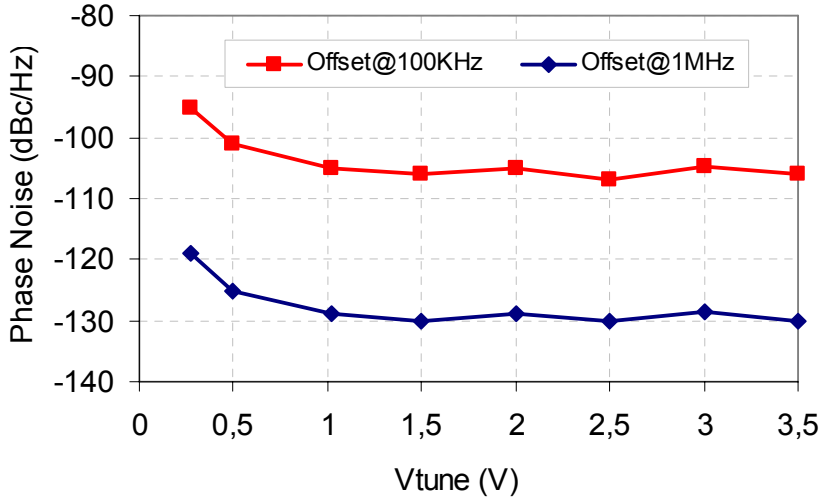
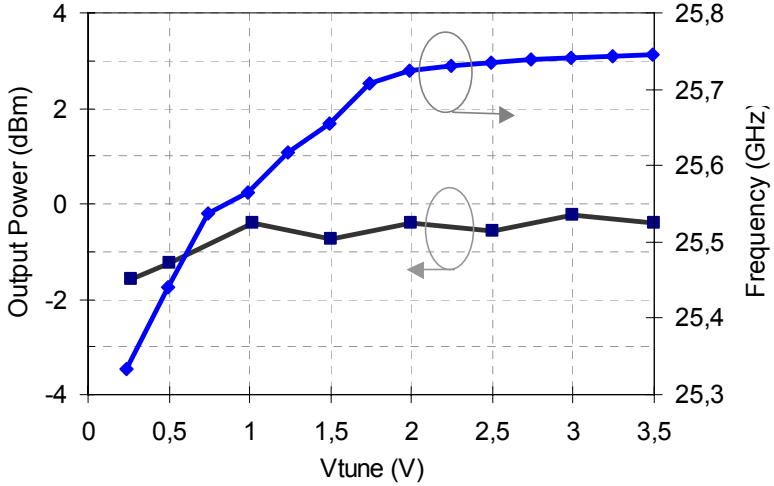
Phase noise versus offset frequency at *Vtune=2V*



Phase noise at 100 KHz and 1 MHz offset versus V_{tune}



Oscillation frequency and output power versus V_{tune}



Dr Ming X Bao

P_{dc}=90 mW
I_c=10 mA, V_c=9 V
FOM=-195 dBc/Hz

$$FOM = L(f_{off}) - 20\log\left[\left(\frac{f_o}{f_{off}}\right)\right] + 10\log(P_{DC})$$

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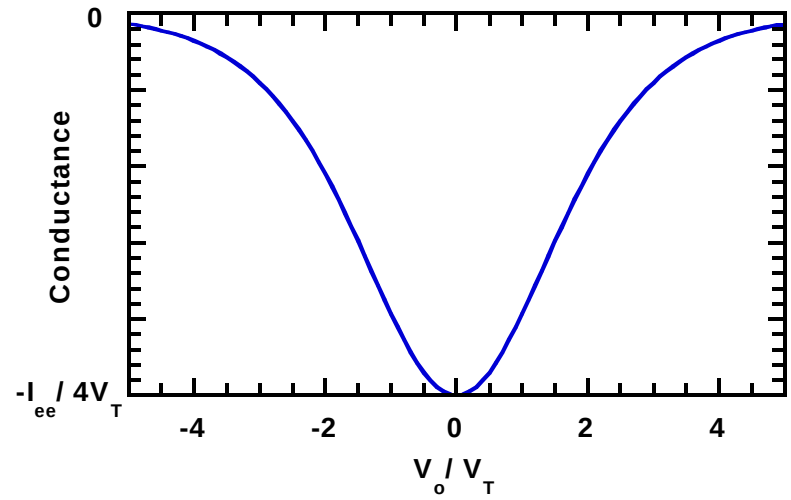
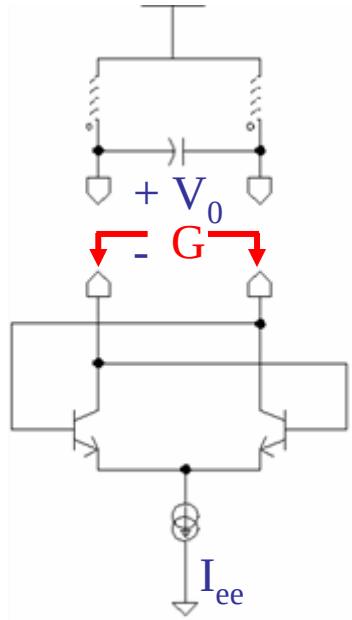
Example 5: SiGe HBT CCDP VCO



- Cross-coupled differential amplifier generates negative conductance
- Wide frequency band negative conductance
- Similar for CMOS

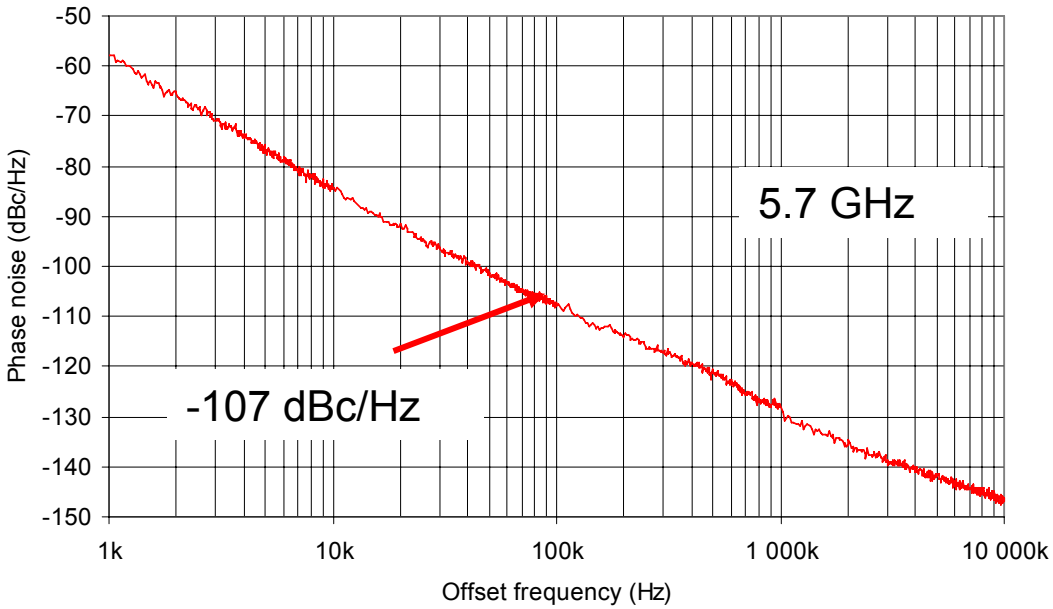
$$G = -\frac{I_{ee}}{4V_T}\cosh^{-2}\left(\frac{V_0}{2V_T}\right)$$

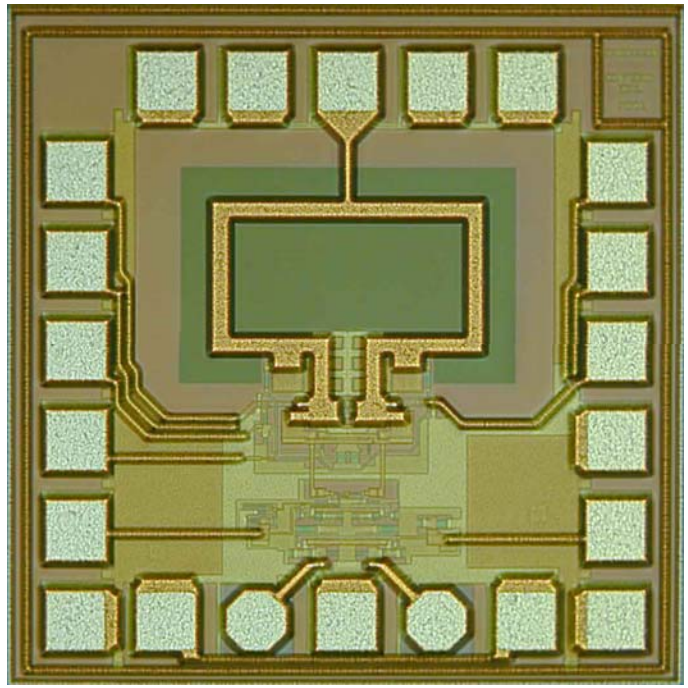
$$G^{small} = -\frac{g_m}{2}$$



SiGe VCO Measurements

- Single differential VCO
  - Tuning: 5.56 GHz - 5.78 GHz
  - Power consumption: 30 mW (excluding buffers)
  - -3dBm output power (differential from buffers, P_{DC}=135mW incl buffers)





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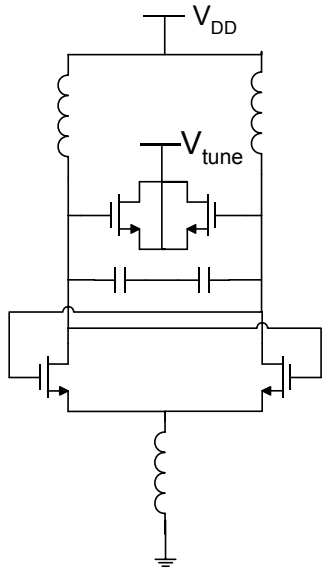
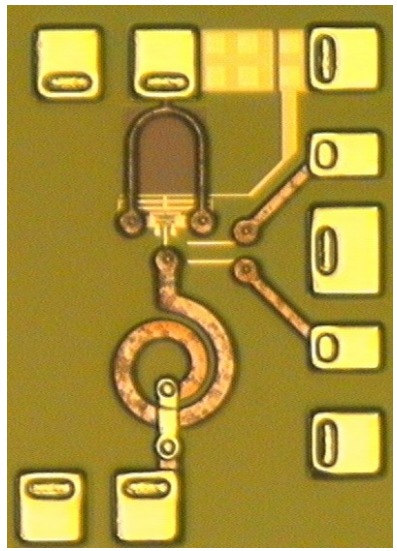
Example 6: CMOS CCDP VCO

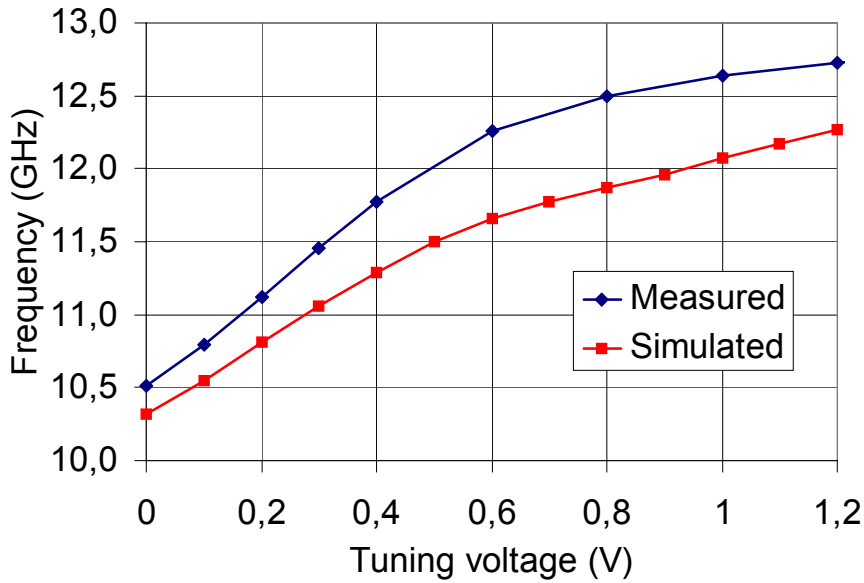
10-12 GHz CMOS VCO (i)





- Cross-coupled differential pair nmos-only with DC-feedback
- Nmos varactor
- Inductor ”current source”
- ~20 % tuning range
- V_{supply} down to 0.6 V

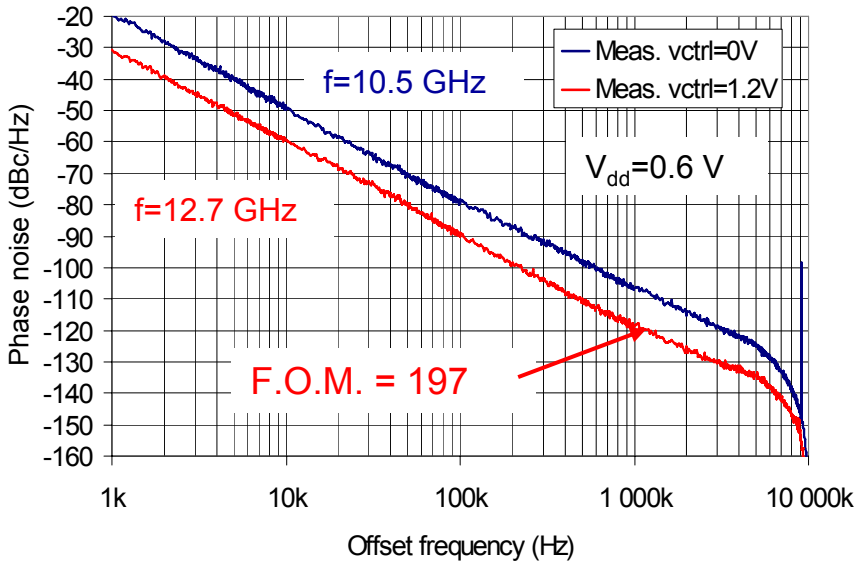
- Pout=-13dBm at P_{DC} = 1.6 mW
- Pout=-8dBm at P_{DC} = 5 mW



10-12 GHz VCO (ii)

- moderate phase noise, -81 to -91dBc/Hz @100kHz offset
- Very clean noise spectrum – no spurioses
- Record F.O.M. = 197
- Phase noise deteriorates with tuning voltage

  reduced Q of nmos varactor in inversion



How can phase noise be further reduced with one and the same technology?

- Couple N VCOs - the phase noise is reduced to 1/N

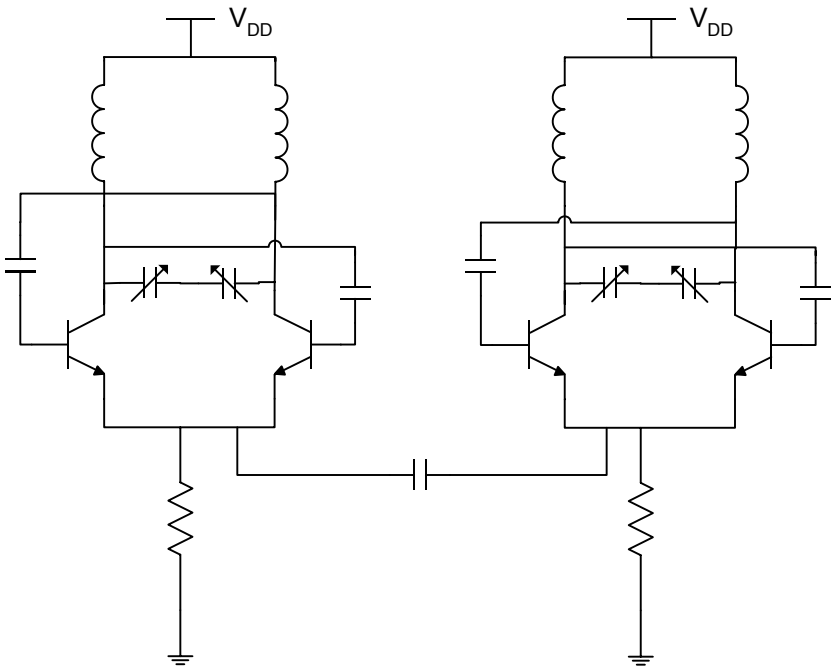
Why?

- Signal power increases as N^2
- Noise power increases as N (uncorrelated)

- S/N ratio increases as N

Coupled CCDP VCOs

1. Inductive coupling
2. Superharmonic coupling



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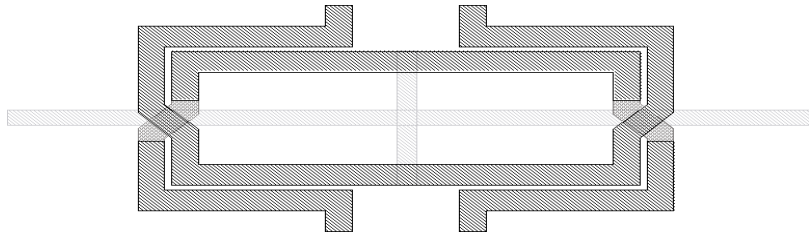
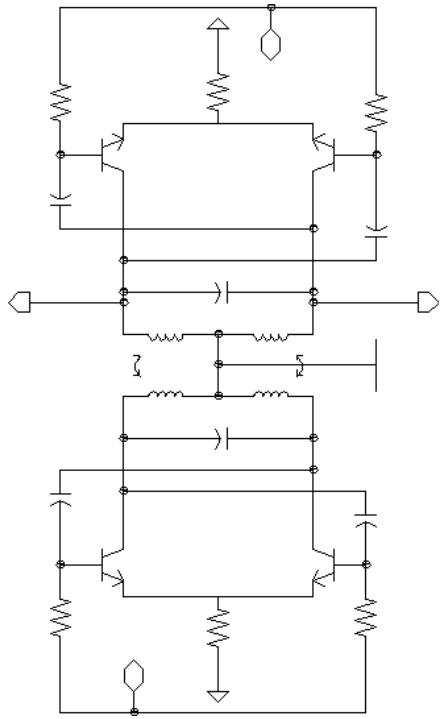
VCO 1

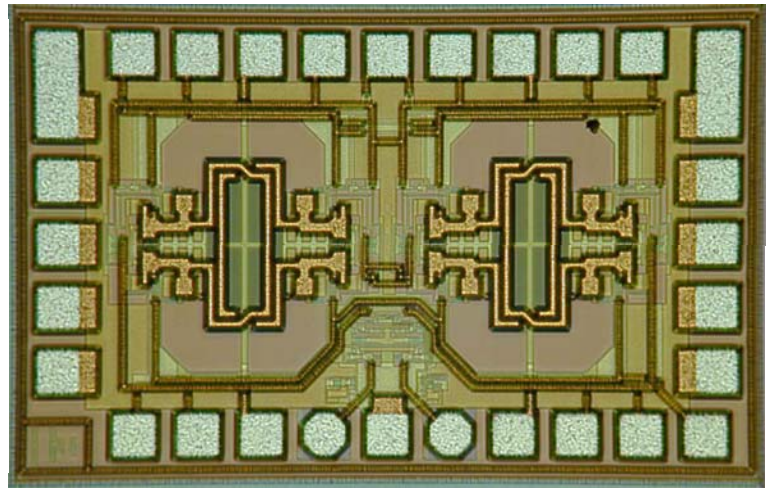


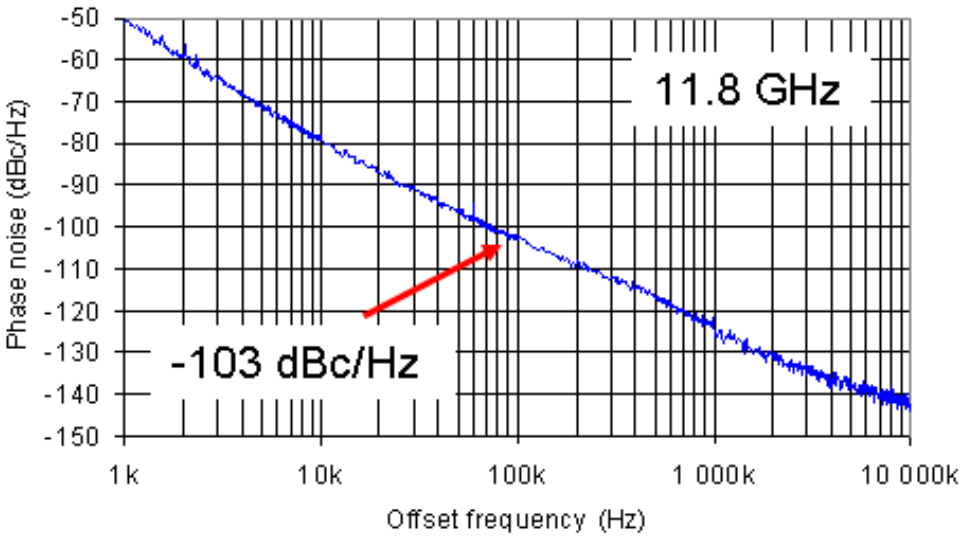
VCO 2

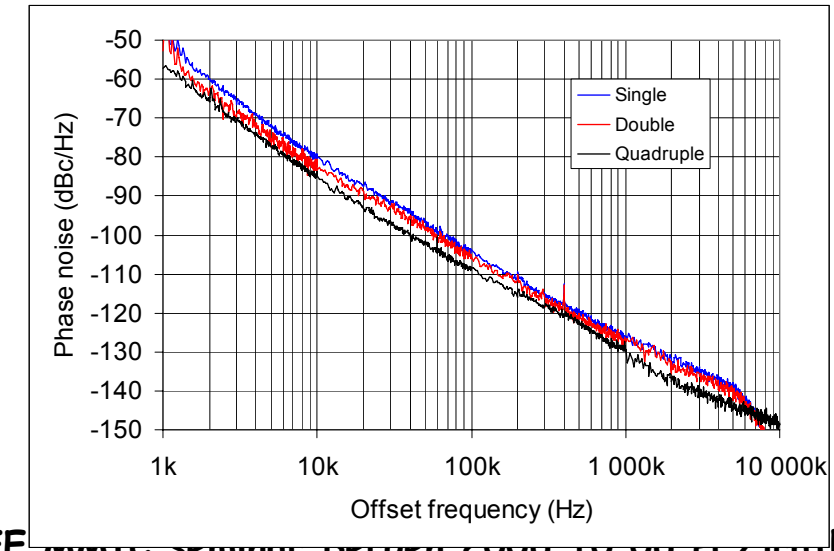


Example 7: Coupled SiGe HBT CCDP VCO

- Four coupled VCOs
  - Tuning: 10.0 GHz - 11.9 GHz
  - Continuous tuning: 500 MHz
  - Power consumption: 110 mW (excluding buffers)







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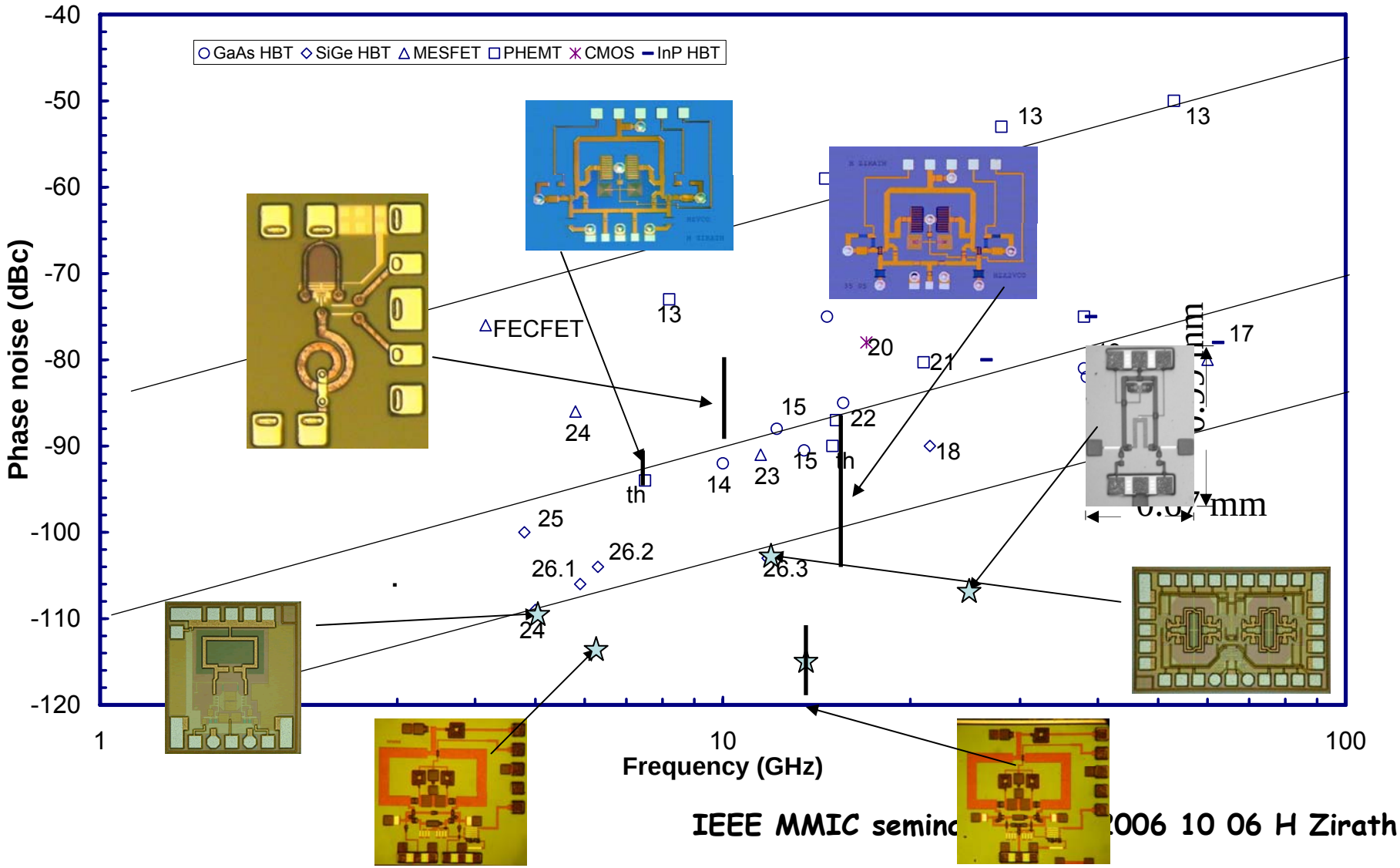
Summary of presented oscillators: Phase noise at 100kHz offset



Conclusion

Low noise VCOs based on Colpitt, Hartley, and crosscoupled differential pairs have been presented utilizing PHEMT, SiGe HBT, InGaP-GaAs HBT, and CMOS technologies

-Lowest phase noise obtained by InGaP-GaAs HBT based Colpitt design
-InGaP-GaAs HBT Hartley excellent at higher frequencies

-Excellent performance also by SiGe HBT Colpitt and CCDP VCOs

Future work:

-extended tuning range
-optimized varactors
-amplitude stabilization
-increased tankenergy for lower PN
-investigate symmetry and second harmonic sensitivity on phase noise