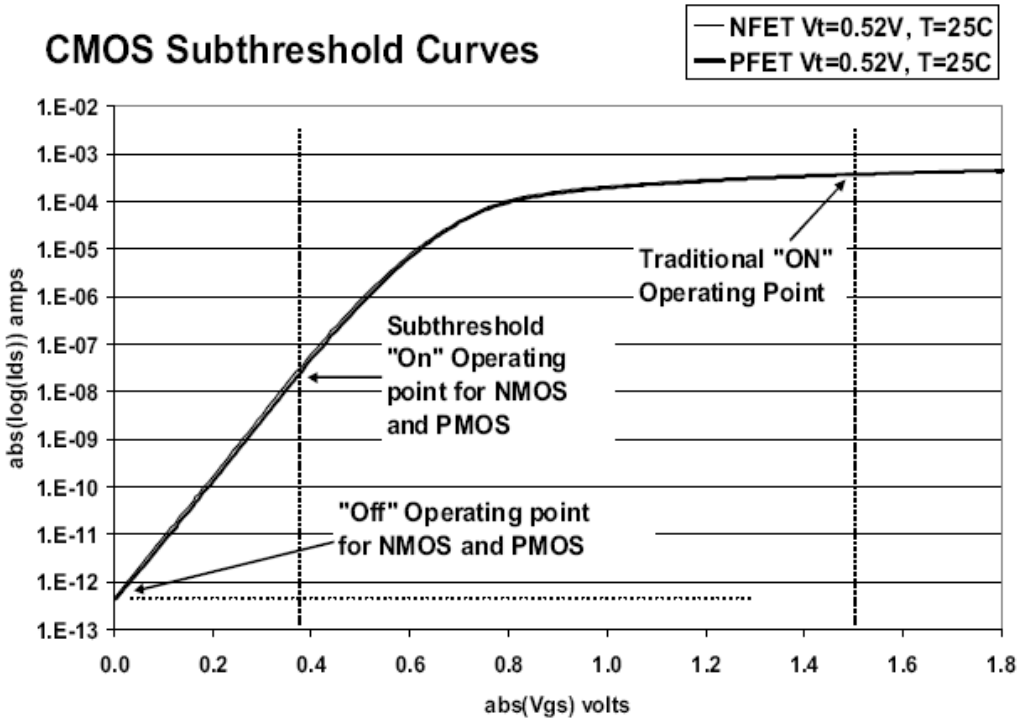
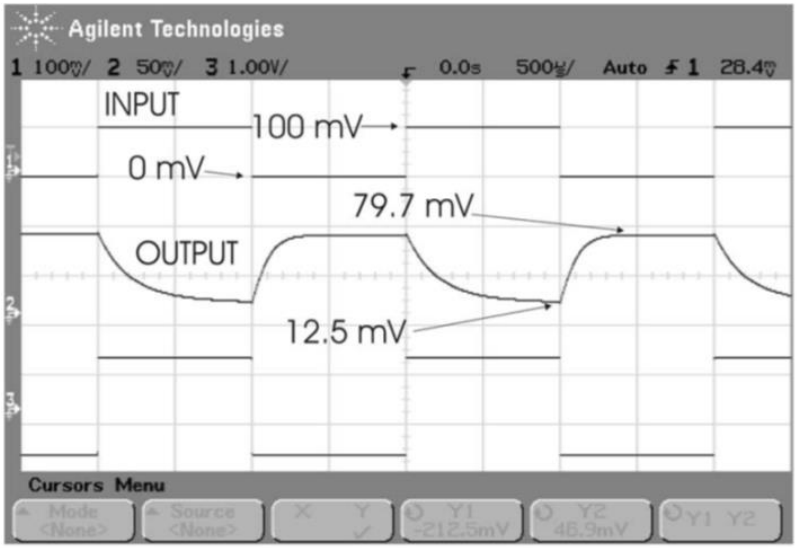
Low Voltage / Low Energy CMOS





Measurements of inverting function for $V_{dd} = 100$ mV.

IEEE TRANSACTIONS ON NEURAL NETWORKS, VOL. 19, NO. 4, APRIL 2008

Real-Time Reconfigurable Subthreshold CMOS Perceptron

Snorre Aunet, *Senior Member, IEEE*, Bengt Oelmann, Per Andreas Norseng, and Yngvar Berg

IEEE MTP/AP seminar, Oslo, 2013.03.08

Snorre Aunet, Prof., Dr. Ing., Department of Electronics and Telecommunications, NTNU / Department of informatics, University of Oslo (part time).

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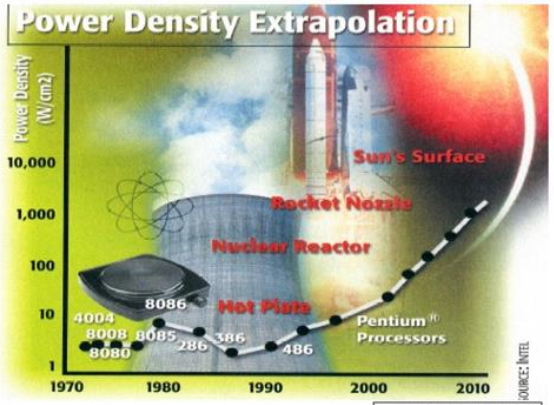
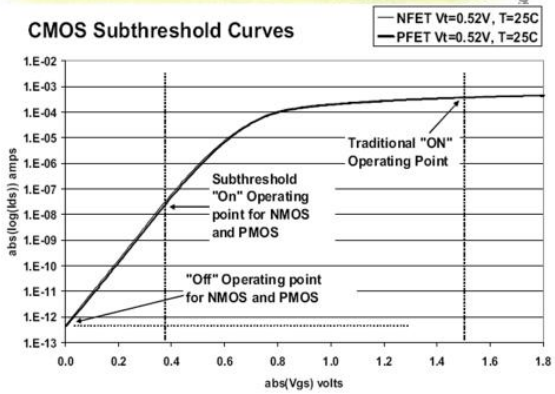
Outline

- Subthreshold CMOS providing the lowest power- and energy consumption attainable.
- Subthreshold operation, definition.
- Reducing the power supply voltage as the most direct and dramatic means of reducing the overall power consumption.
- Intel and UC Berkeley predict bright future for ultra low voltage CMOS.
- Ultra low voltage CMOS reducing power consumption up to several orders of magnitude, or energy per switching up to 1-2 orders of magnitude.
- Examples from practical («full custom») chip implementations demonstrating the «green» statements above:
- 1) 32-bit adder functioning for a supply voltage down to 106 mV, thus being able to reduce power consumption by thousands of times, when compared to what the same technology normally would provide for 32-bit addition.
- 2) 32-bit microprocessor having 90.9 % reduction in energy per operation when the power supply voltage is reduced from the standard 1.2 V, to about 0.3 V.
- 3) ««RX» and «TX» functionalities» operating with supply voltage down to 185 mV, consisting of about 1500 transistors, having power consumption of 145 nW@185 mV («RX») and 131.4 nW («TX»).
- Pointers to litterature and research within ultra low voltage / low power CMOS

Ultra Low Voltage («Subthreshold») operation as the most radical low power technique

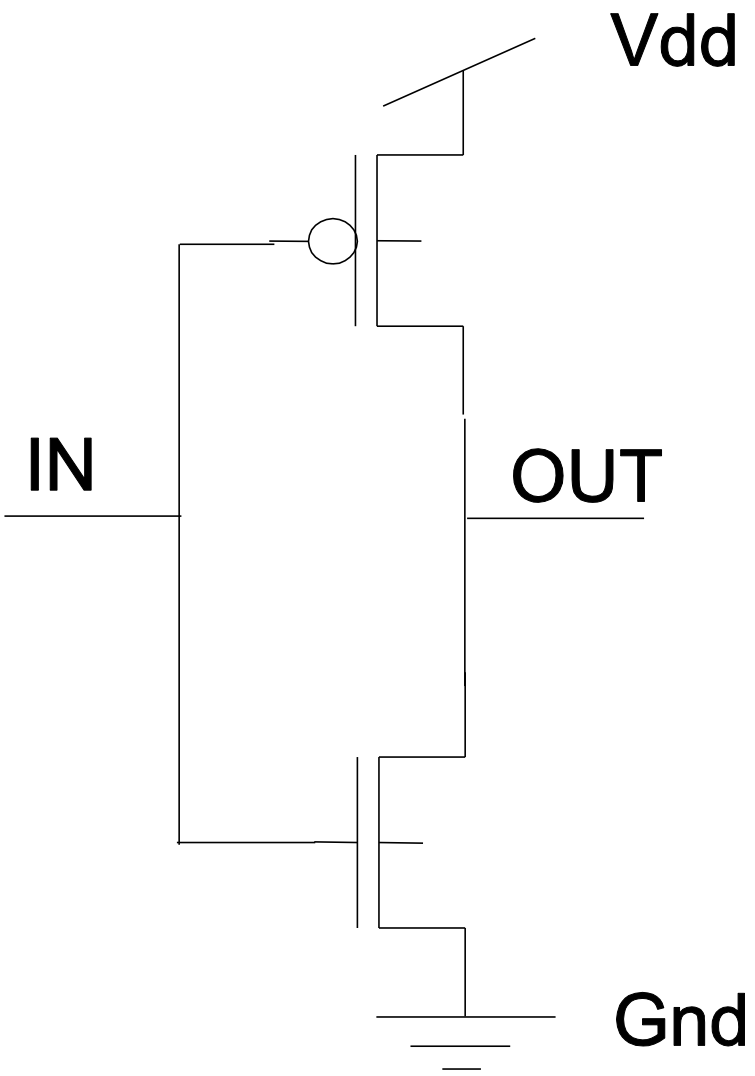




- Reducing the power supply voltage is the most direct and dramatic means of reducing the overall power consumption.

•Subthreshold operation: lower power consumption than other known techniques

Subthreshold is attained by using a supply voltage below the absolute value of the inherent threshold voltages of the PMOS and NMOS transistors



- Normal operation, example: Vtp = -0.3 V, Vtn = 0.3 V. Supply voltage, Vdd = 1.2 V.
- Subthreshold operation, example: |Vtp| = |Vtn| = 0.3 V, Vdd = 0.180 V

- Subthreshold currents may be used for computations in ultra low power / low energy circuits and systems.
- Inverter shown left. OUT = IN'

; IN = Vdd → OUT = Gnd.
IN = Gnd → OUT = Vdd.
Vdd = «1», Gnd = «0»

Intel's top 10 technology predictions: Subthreshold circuits will enable new classes of portable devices with ten times more battery life and personal mobile internet devices being able to run all day.

Prediction One - new classes of portable devices with ten times more battery life
Sub-threshold integrated circuit technology requires only 300mV to operate.

Intel showed 4-way SIMD (single instruction multiple data) vector processing accelerator in 45nm in CMOS operated below its gate threshold voltage at the ISSCC technology conference.

"This will lead to new classes of portable devices designed to take advantage of greater battery life, which in turn will drive popularity and uptake."

Prediction six - personal internet devices will be truly personal
Mobile internet devices (Mids) are already powerful enough to be useful and the introduction of sub-threshold devices (prediction one) mean these will run all day.

Add this to a continuous Internet connection and users will, for example, be able translate words into other languages and hear then pronounced, or with GPS get a constant geographically-based pollen prediction for that day.

Ten years from now Mids will be ubiquitous and application developers will flood the market with all sorts of ingenious ideas.

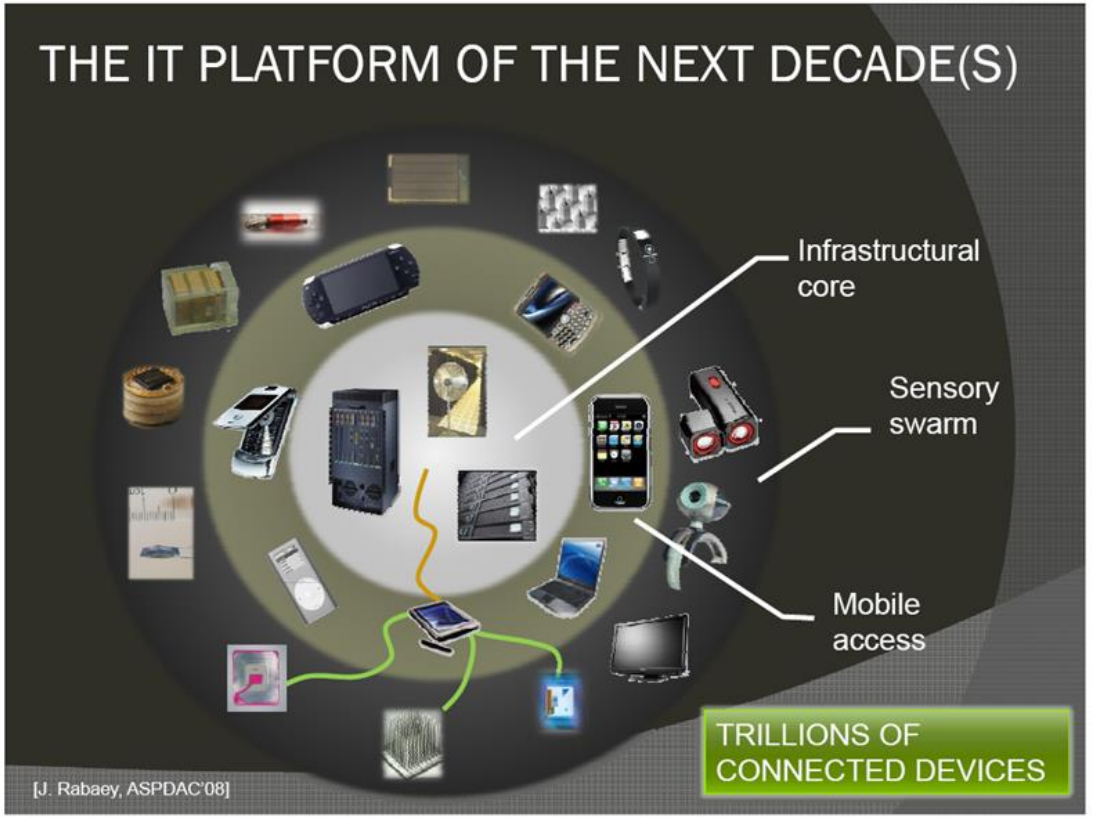
"*Ten years from now Mids (Mobile Internet Devices) will be ubiquitous and application developers will flood the market with all sorts of ingenious ideas*"

- Steve Bush: **Intel makes its top ten technology predictions for next decade**

http://www.electronicsweekly.com/Articles/2009/05/13/45950/intel-makes-its-top-ten-technology-predictions-for-next-decade.htm

New information acquisition and processing devices enabled by ultra-low power technologies – the sensory swarm

- Sensory swarm «… *will have a tremendous impact in domains such as advanced healthcare, improved energy efficiency, environmentally-friendly living, mobility management, enhanced security, and many others*.»



The Swarm at the Edge of the Cloud – A New Perspective on Wireless

Jan M. Rabaey

University of California at Berkeley

Reducing the supply voltage into the subthreshold regime may reduce power consumption by several orders of magnitude, or energy per operation by typically 10 to 30 x

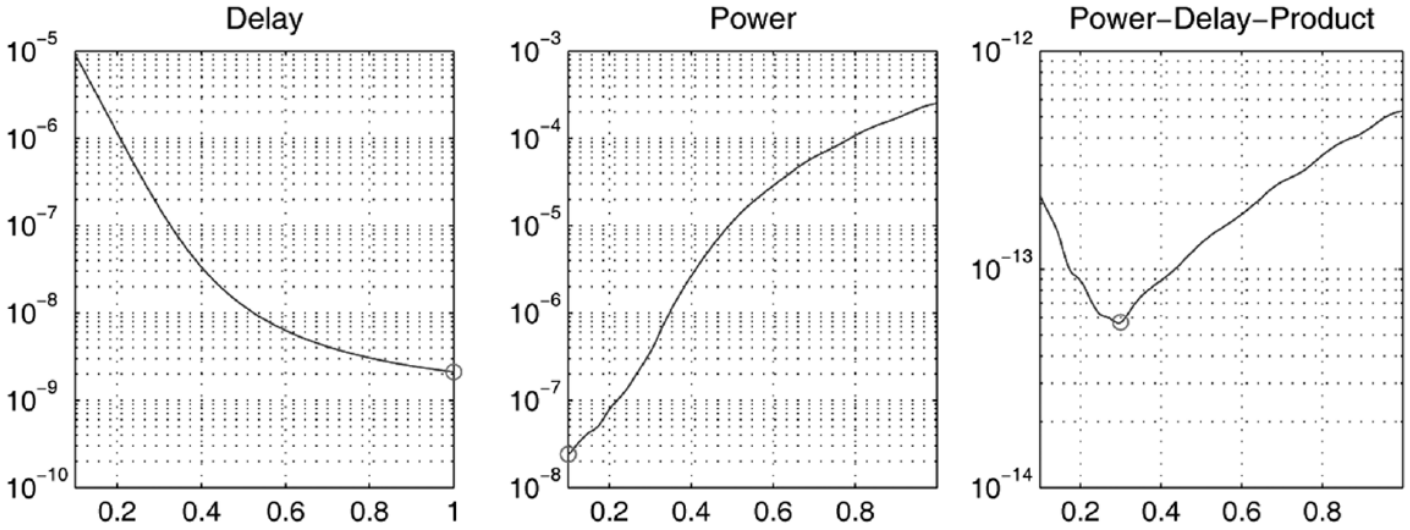


Fig. 10. Effect of varying V_{DD} (32-bit RC) on power, PDP, and EDP Optimum operating point is marked with a circle.

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 54, NO. 11, NOVEMBER 2007

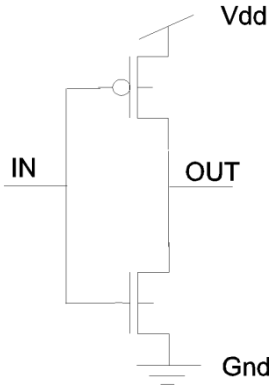
Serial Addition: Locally Connected Architectures

Valeriu Beiu, *Senior Member, IEEE*, Snorre Aunet, *Senior Member, IEEE*, Jabulani Nyathi, *Member, IEEE*, Robert R. Rydberg III, *Student Member, IEEE*, and Walid Ibrahim, *Member, IEEE*

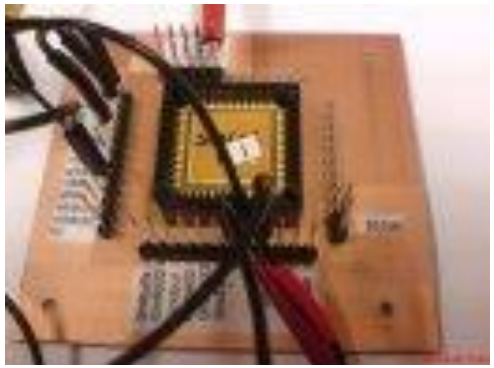
Power = Voltage x Current

Energy = Power x Delay

- $P = P_{static} + P_{dyn} + P_{sc} = V_{DD}I_{leak} + \alpha V_{swing}V_{DD}C_L f_{CLK} + I_{SC}V_{DD}$



Chip measurements, full custom implementation of 32-bit addition, supply voltage 106 mV - close to predicted practical lower limit of 100 mV.



"..to allow for some tolerance to process and design margins, operation at VDD 100 mV may prove a practical lower bound."
(Nowak, IBM, '02)

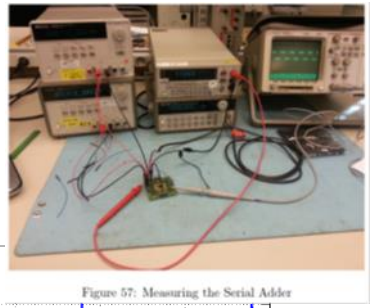
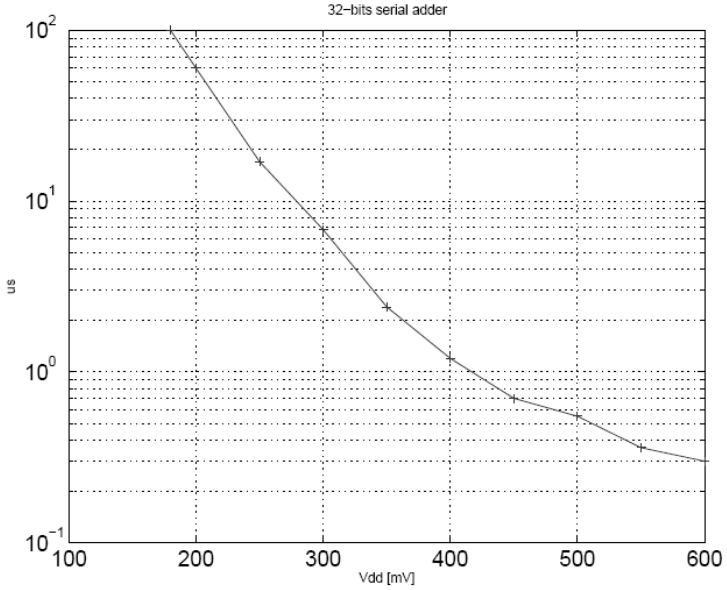


Figure 57: Measuring the Serial Adder



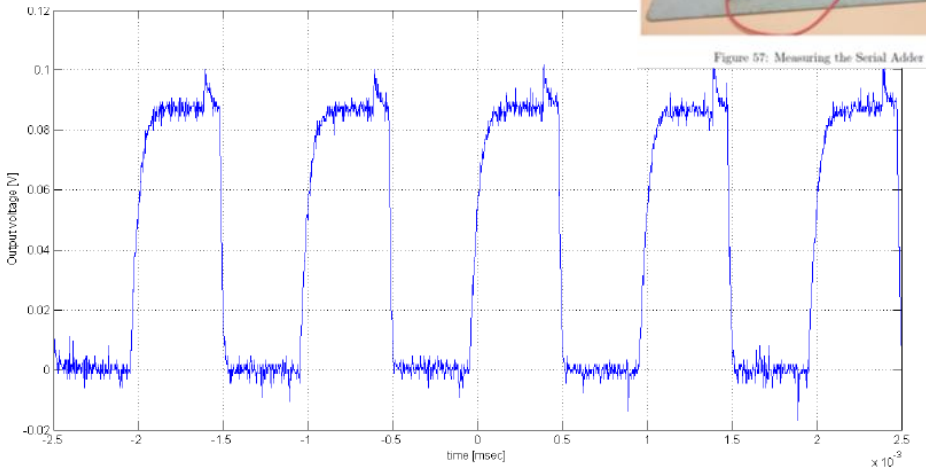


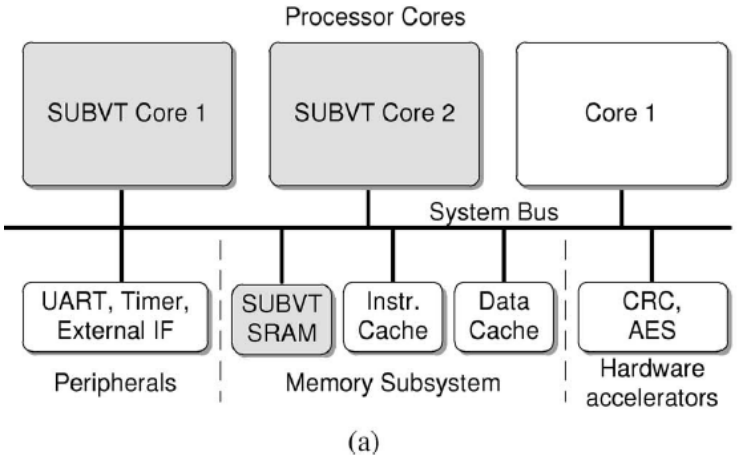
Figure 55: The Serial Adder output at the lowest possible Supply Voltage, 106mV input

14. Delay, capacitively loaded 32-bit serial adder as a function of V_{dd}.

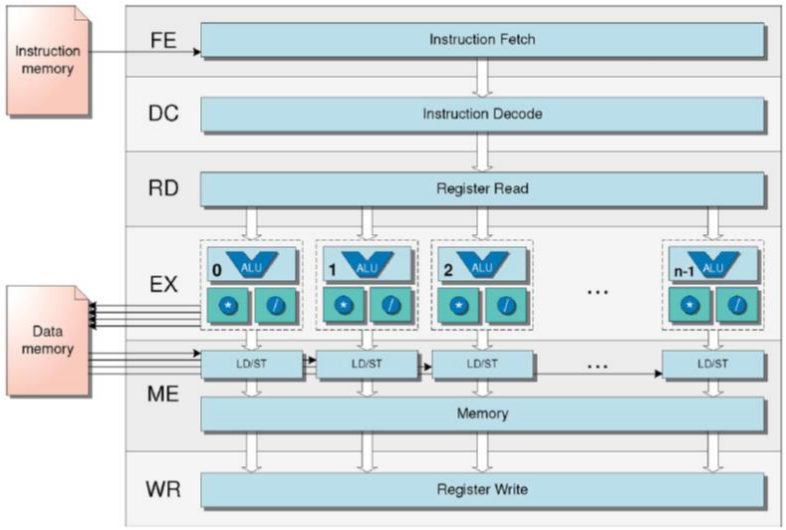
Measurements for 32-bit serial adder, above (S. A., Norchip 2009)

Upper , right: 32-bit addition CARRY, Vdd = 106 mV (unpublished measurements, Nov. 2012). Thanks to siv. ing. student Magne Værnes!

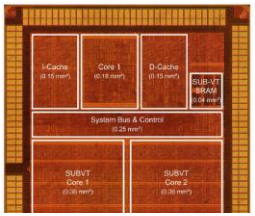
Energy per operation reduced to 1/11 when reducing supply voltage from 1.2 to about 0.3 V, demonstrated by chip measurements (or 90.1 % reduction) .

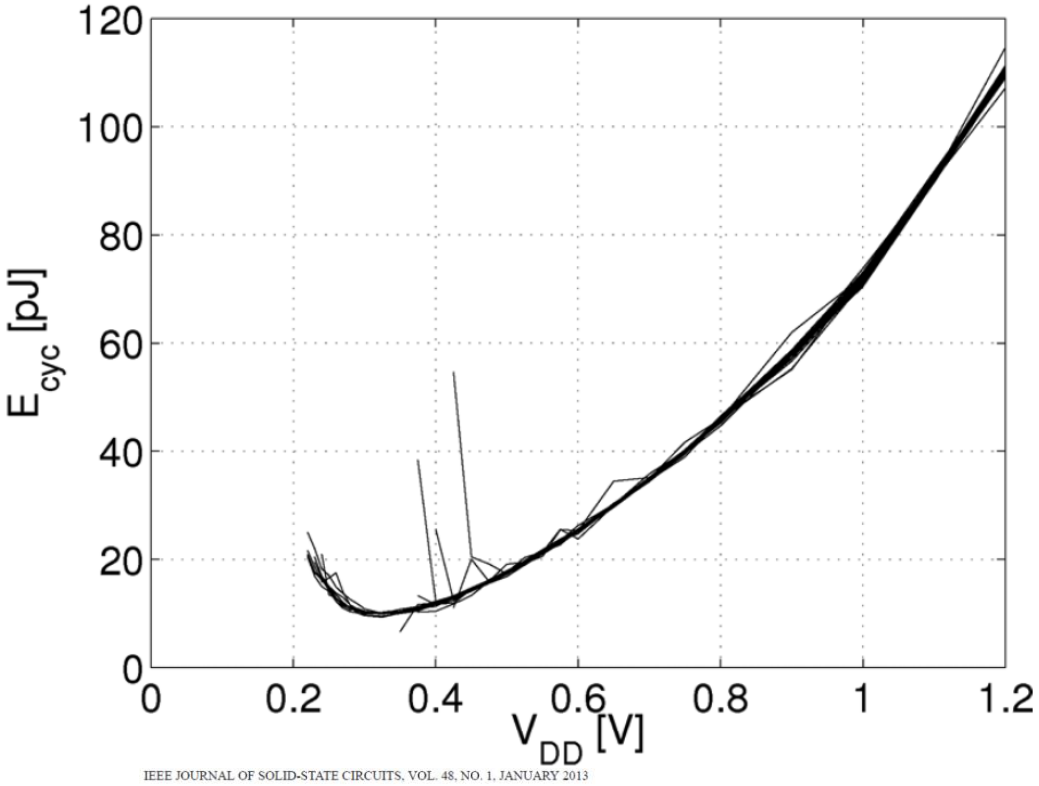


(a)



Generic pipeline structure of the CoreVA processor.





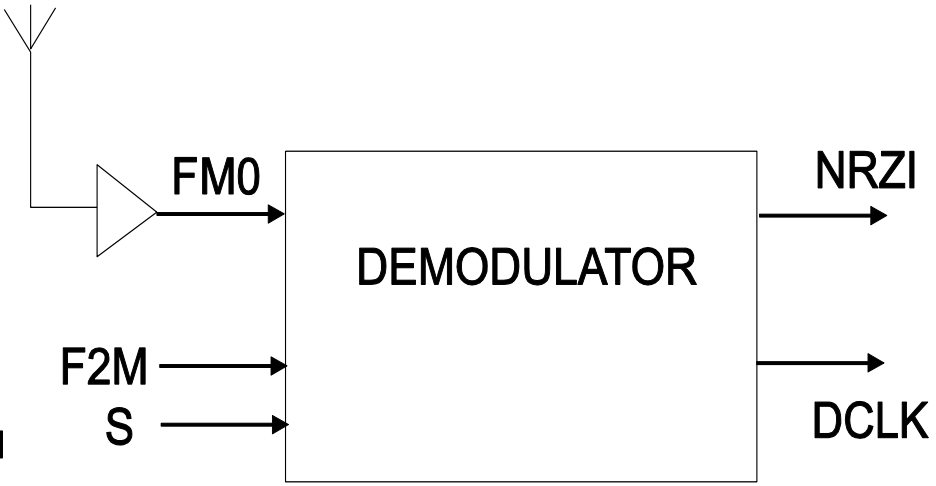
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 48, NO. 1, JANUARY 2013

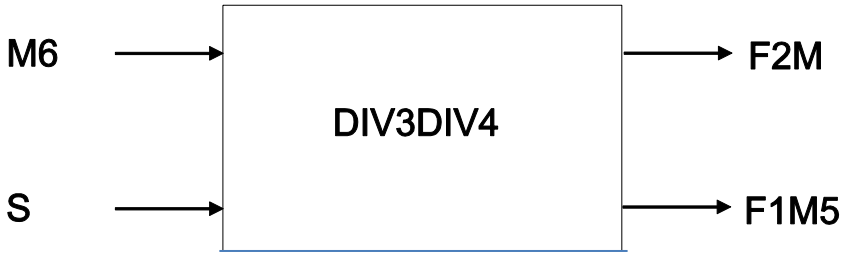
A 65 nm 32 b Subthreshold Processor With 9T Multi-Vt SRAM and Adaptive Supply Voltage Control

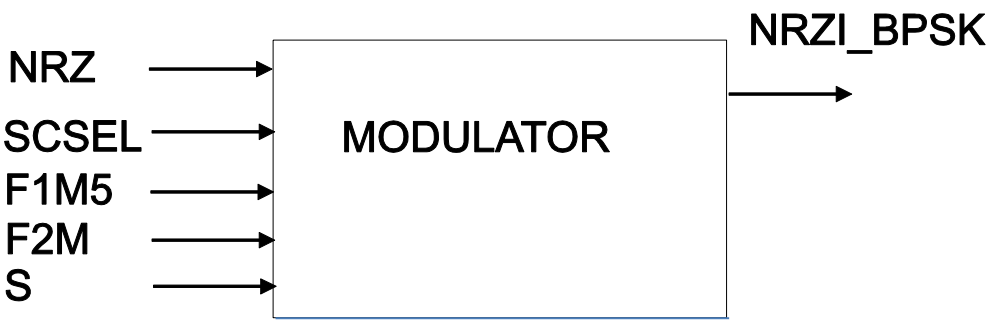
Sven Lütkemeier, *Student Member, IEEE*, Thorsten Jungeblut, *Member, IEEE*, Hans Kristian Otnes Berge, *Student Member, IEEE*, Snorre Aunet, *Senior Member, IEEE*, Mario Porrmann, *Member, IEEE*, and Ulrich Rückert, *Member, IEEE*

RX/TX modules implemented in 90 nm CMOS

The demodulator receives a 500 kbit/s FM0 signal and produces a demodulated signal and a 500 kHz clock signal.

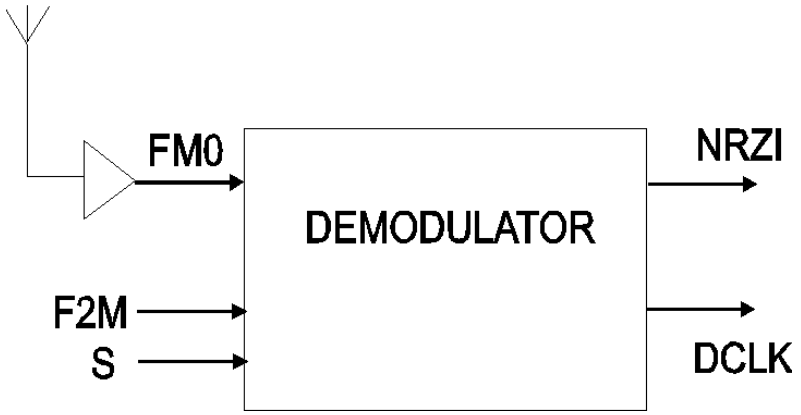




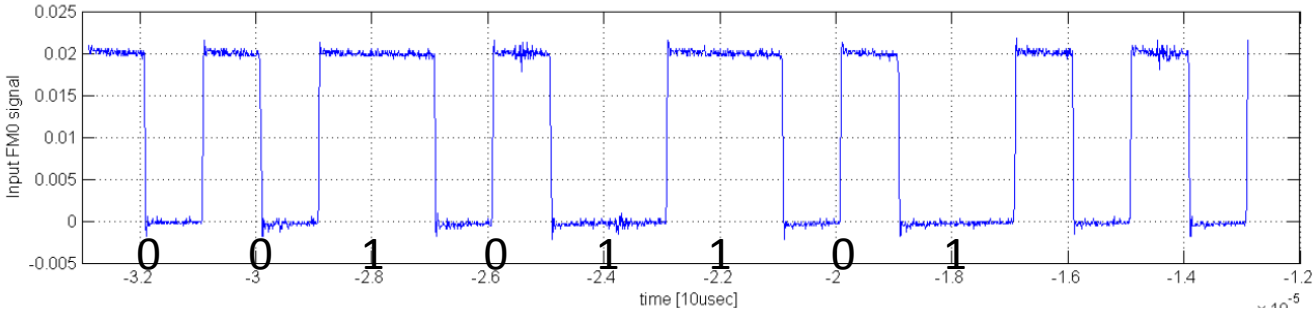


The modulator takes an NRZ input And modulates into NRZI_BPSK, using a chosen sub-carrier .

Chip measurements, «RX», demonstrating decoding of «…00101101…»



- About 700 MOSFETs
- Power consumption 114.7 nW
- Supply voltage down to 0.185 V.



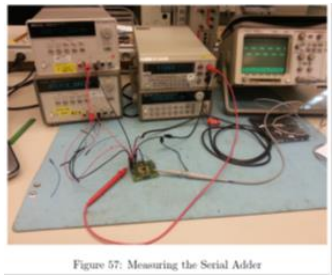
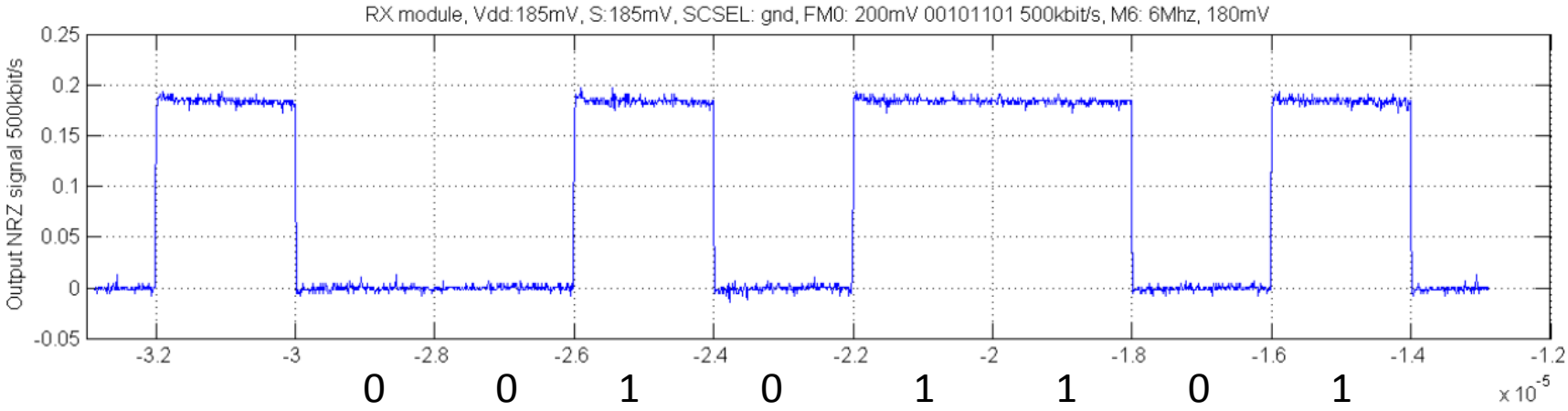
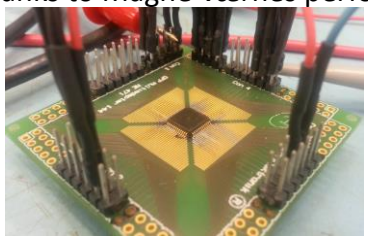


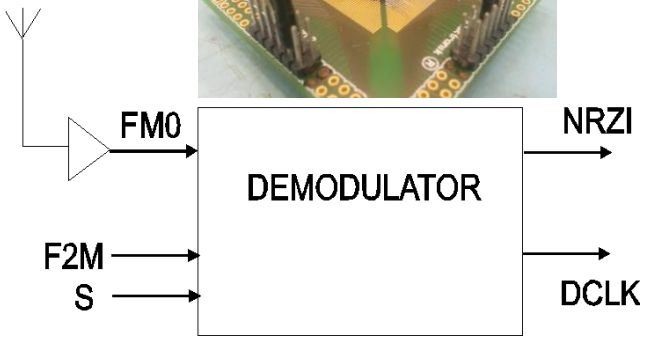
Figure 57: Measuring the Serial Adder

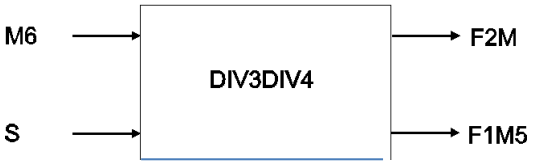


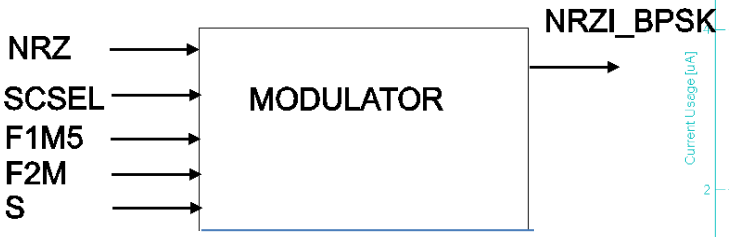
Chip measurements, «RX» and «TX».

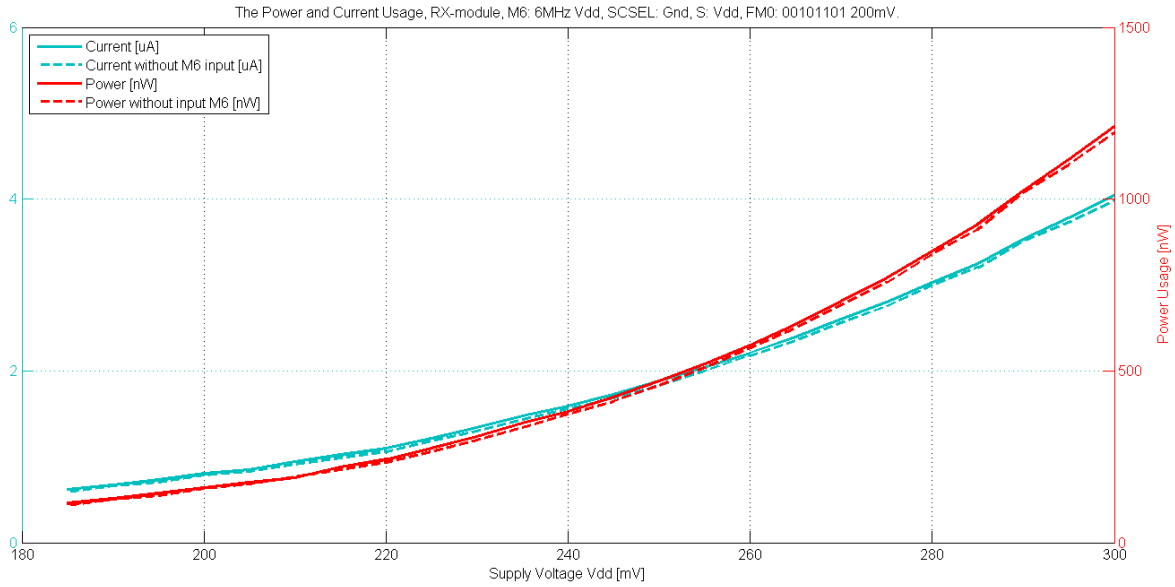
Thanks to Magne Værnes performing the measurments, and Q-Free ASA for lending out their laboratory equipment

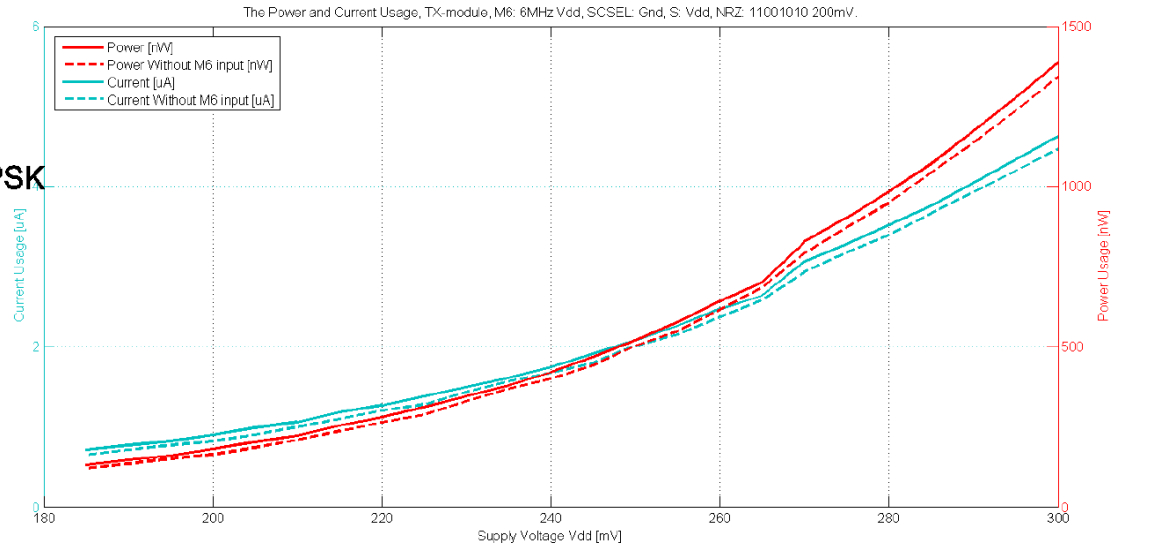












Literature / pointers

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- http://www.ambiqmicro.com , http://iridiumtec.com/ .

Thank you for your attention!

Questions?

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He worked with ASIC design at Nordic VLSI (now Nordic Semiconductor) from 1994 to 1997, afterwards starting his doctoral studies. Since 2002 he held different positions at NTNU and the Department of Informatics (Ifi), UiO, and is currently a Professor at the Department of Electronics and Telecommunications, NTNU. He holds an adjunct professorship at the Nanoelectronics group, Ifi, UiO. He has been a visiting researcher at the Circuits and Systems Group, University of Paderborn, from 2004. He has two patents and has published about 85 scientific papers, several book chapters and books on floating-gate circuits and ultra-low-voltage mixed-signal circuits and microarchitectures.