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für Höchstfrequenztechnik

Flip-Chip for MM-Wave and Broadband Packaging

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with contributions by F. J. Schmückle

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Motivation

Growing markets for mm-wave systems,
e.g.

- 77 GHz automotive radar
- 60 GHz wireless communications
- 40 GHz radio links
- high bit-rate electronics
(40 Gbps and beyond)

ICs are available: GaAs, SiGe, (CMOS)

What about packaging (low cost !)



DAIMLERCHRYSLER

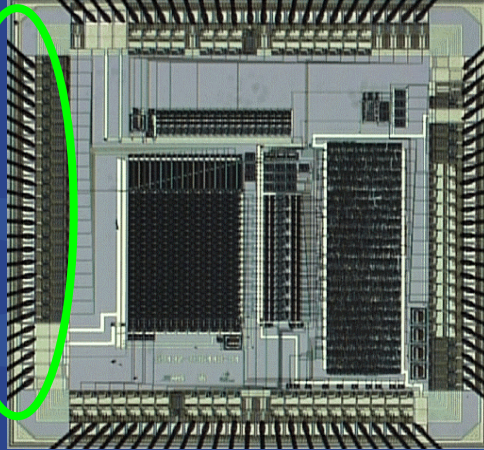
DISTRONIC
DTR



Packaging a mm-wave IC (I)

As conventional
- same as for VLSI chips ?

High frequency
-> increased parasitics
at interconnects



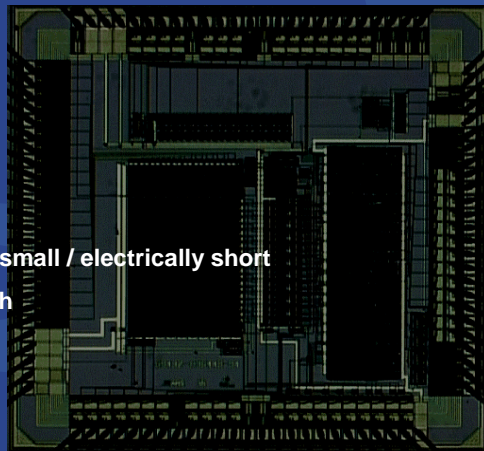
Packaging a mm-wave IC (II)

As conventional
- same as for VLSI chips ?

High frequency
-> increased parasitics
at interconnects

General rule: keep dimensions small / electrically short

- compact mounting approach
- miniaturized interconnects



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Techniques available

Wire bonding (up to 40 GHz and beyond)

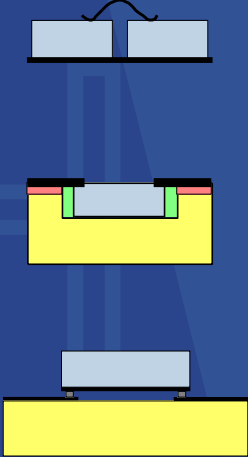
- tight tolerances
- narrow-band (compensation)

Embedded chips

- interconnect smaller than for wire bonding
- impedance mismatch due to gap (tolerances!)

Flip-chip

- smallest interconnect
- well-controlled geometry



The diagrams show: 1. Wire bonding: two grey rectangular pads on a substrate with a thin wire connecting them. 2. Embedded chips: a grey chip with two green pads on top, embedded in a yellow substrate. 3. Flip-chip: a grey chip with two red pads on its bottom surface, mounted on a yellow substrate.

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Packaging is more than just the interconnect

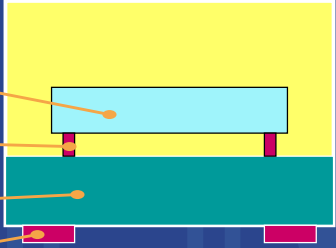
The generic structure

Chips: GaAs, SiGe
- microstrip, coplanar, TFMSL

0-level interconnect
(e.g. flip-chip)

Carrier substrate

1-level interconnect
(flip-chip, ball grids)

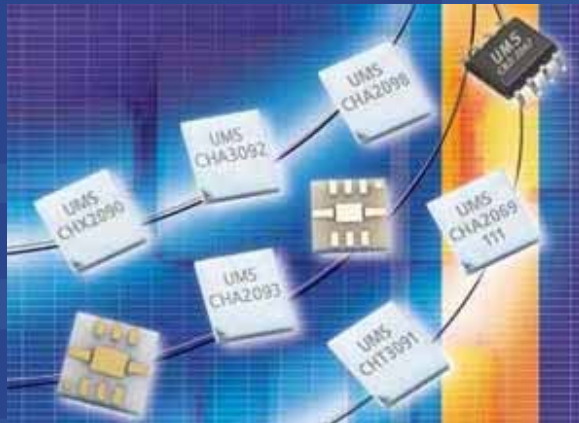


The diagram shows a cross-section of a packaging structure. It consists of a yellow top layer (chip), a green middle layer (carrier substrate), and a pink bottom layer (1-level interconnect). A light blue chip is mounted on the yellow layer. Two red pads are on the bottom surface of the chip, connected to the pink layer. Two red pads are also on the top surface of the chip, connected to the green layer. Labels with orange arrows point to these components: 'Chips: GaAs, SiGe - microstrip, coplanar, TFMSL' points to the light blue chip; '0-level interconnect (e.g. flip-chip)' points to the red pads on the top of the chip; 'Carrier substrate' points to the green layer; and '1-level interconnect (flip-chip, ball grids)' points to the red pads on the bottom of the chip.

Example: SMD chips at mm waves

United Monolithic Semiconductors (UMS)

- Very attractive, but general approach for mm-waves ?



This talk

Flip-chip for mm-wave and broadband packaging

- identify key issues from electrical / em design point of view
- provide understanding of mechanisms

Needs comprehensive view

- flip-chip interconnect
- carrier substrate & housing

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The flip-chip interconnect

- overview on processes
- mm-wave & broad-band characteristics
- parasitic moding
- hot-via interconnect

The package

- thin-film & flip chip
- LTCC as carrier substrate

Conclusions



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Flip-chip processes for mm-waves

Chip interconnect by means of bumps

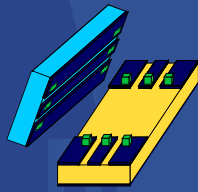


Two technologies:

(i) Thermocompression

- Au bumps (using electroplating or stud bumps)
- bonding by thermocompression

(ii) Soldering

- e.g., AuSn bumps
- chip bonding & soldering in reflow oven


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Which issues need to be considered?

Electrical characteristics

Thermal behavior

- heat-sinking (incl. additional thermal bumps)
- CTE mismatch (materials, chip size, underfiller?)




Manufacturability / cost

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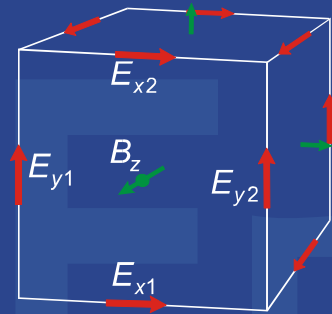


The package

- thin-film & flip chip
- LTCC as carrier substrate

Conclusions

A remark on 3D electromagnetic simulation



Tools used

- Based on finite-difference / finite-integration method
- F3D: FBH in-house code
 - frequency domain (FDFD)
- Microwave Studio (CST)
 - time domain (FDTD)



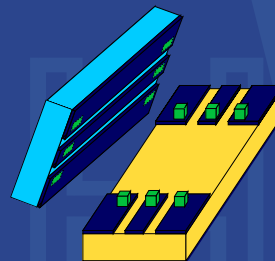
The flip-chip interconnect: mm-wave characteristics

Flip-chip approach

- well-known for lower frequencies
- suitable also for mm-waves because of small dimensions

Two main RF effects

- detuning of on-chip circuit
- reflections at bump transition



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Detuning

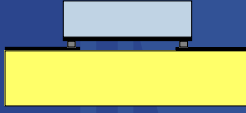
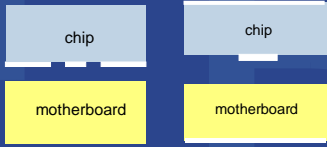
Changes of circuit behavior due to flip-chip mounting

Most critical elements: passives

- transmission lines
- spiral inductors

Underfiller has a particular influence

Transmission lines can be used as a benchmark

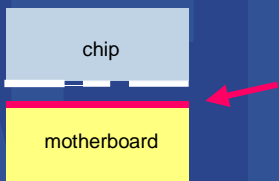
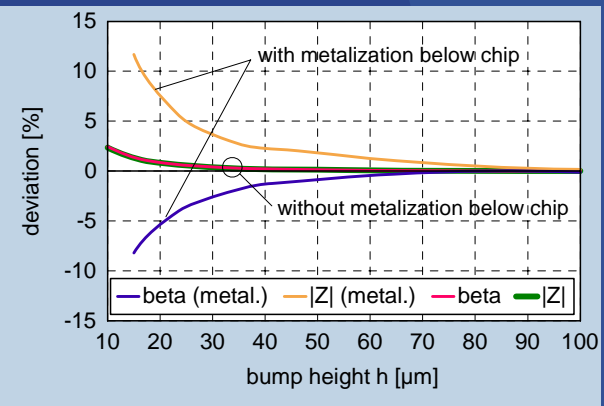
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CPW : deviation β/β_0 and Z vs. bump height h

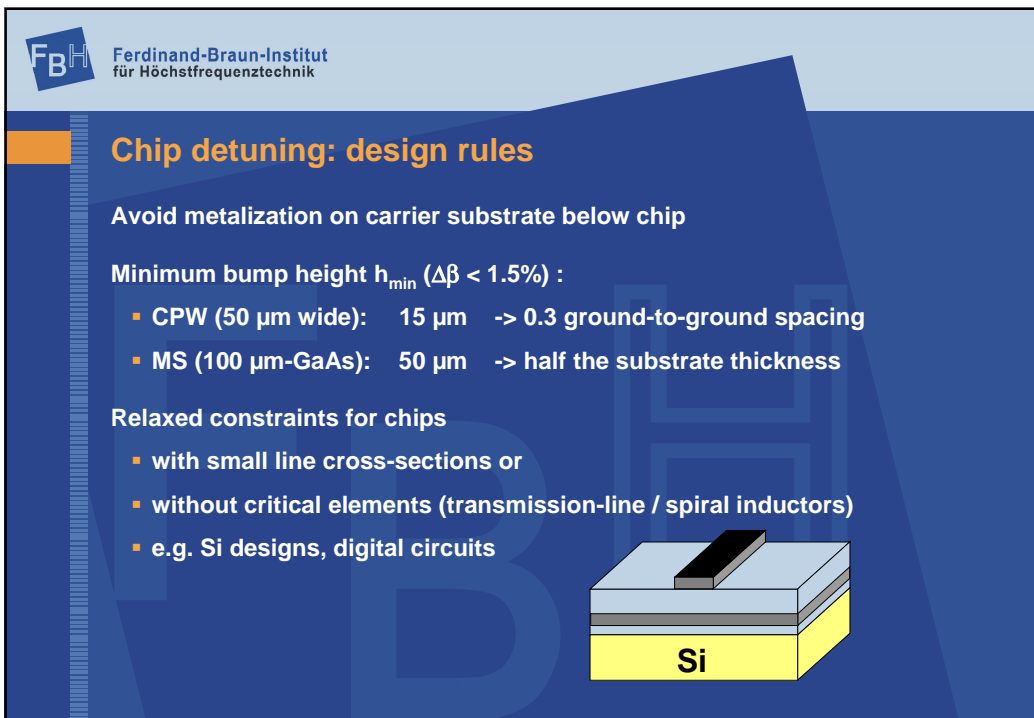
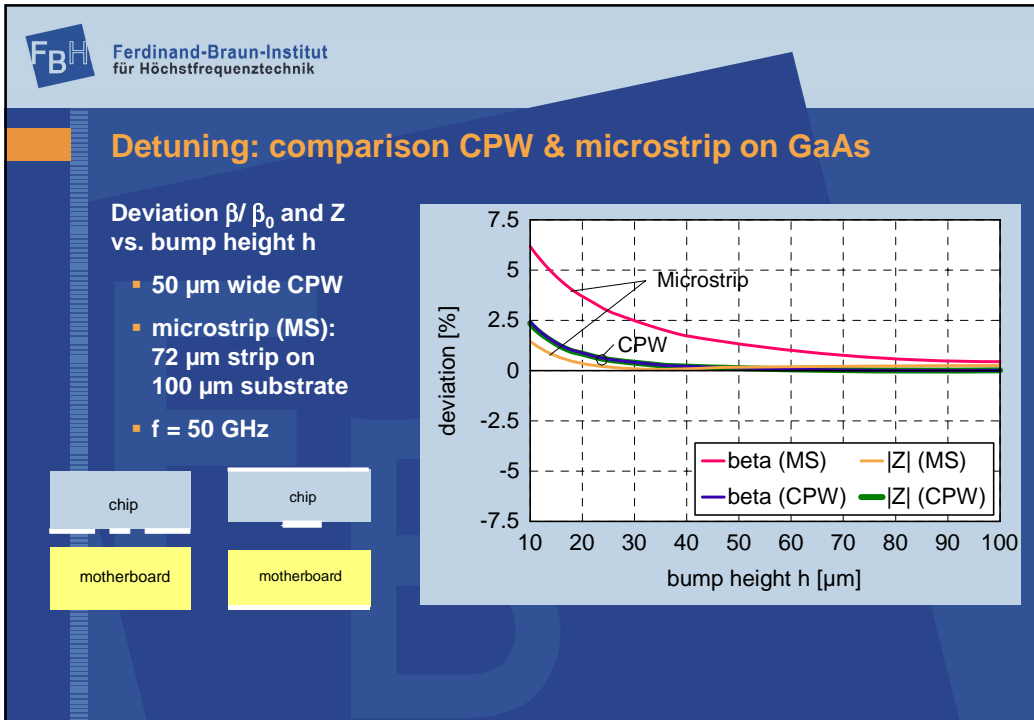
Chip: 50 μm wide CPW

With/without metalization on motherboard below chip

$f = 50 \text{ GHz}$

Bump height h [μm]	beta (metal.) [%]	Z (metal.) [%]	beta (no metal.) [%]	Z (no metal.) [%]
10	-8	12	2	2
20	-5	8	1	1
30	-3	5	0.5	0.5
40	-2	3	0.2	0.2
50	-1.5	2	0.1	0.1
60	-1.2	1.5	0.05	0.05
70	-1	1.2	0.02	0.02
80	-0.8	1	0.01	0.01
90	-0.7	0.8	0.005	0.005
100	-0.6	0.7	0.002	0.002

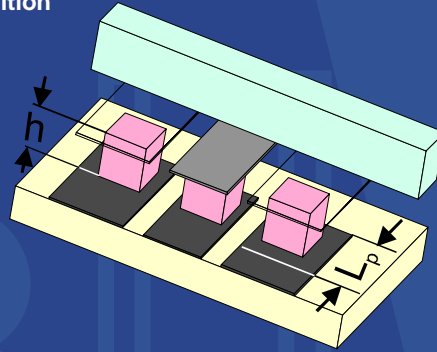


Reflections at the interconnect

Basic structure: CPW-to-CPW transition

Bump geometry

- height h
- diameter l
and related quantities
 - pad size l_p
 - total width of transition



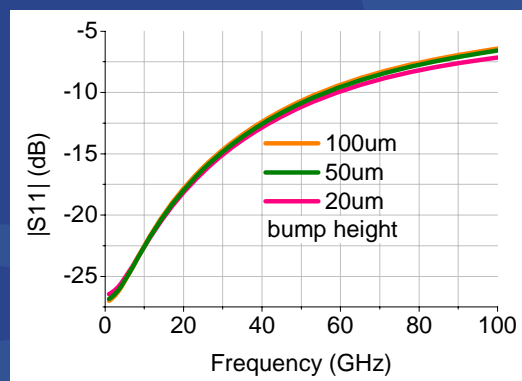
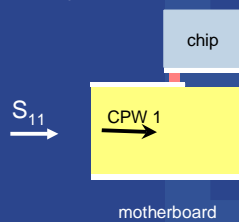
S_{11} for 80 μm bumps: Influence of bump height

3D FDFD simulations

Bump geometry

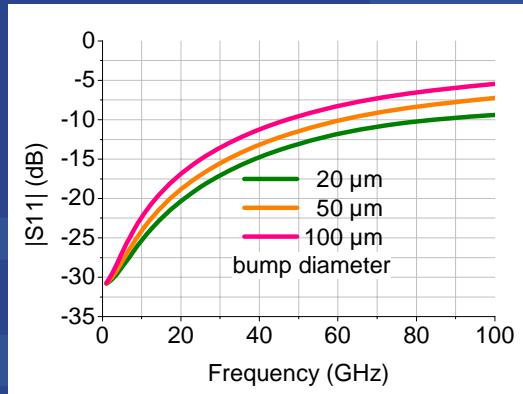
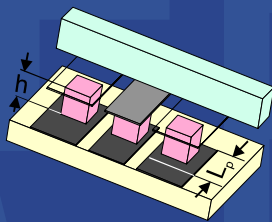
- diameter $l = 80 \mu\text{m}$
- pad size $l_p = 100 \mu\text{m}$
- height $h = 20 \dots 100 \mu\text{m}$

$|S_{11}|$ for CPW mode
vs. frequency



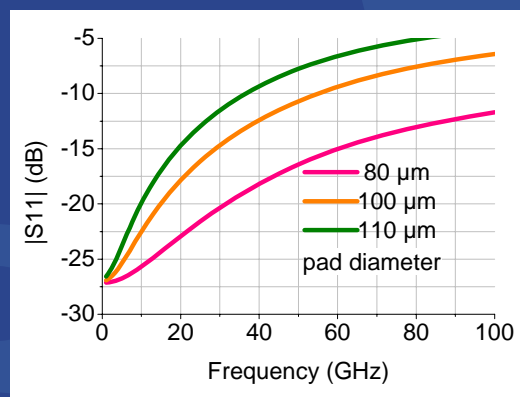
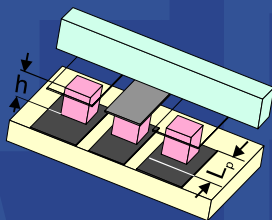
Influence of bump diameter

- constant pad size: 100 μm
- bump height = 50 μm
- bump diameter 20...100 μm
- Small deviations



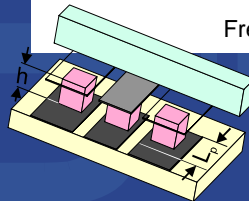
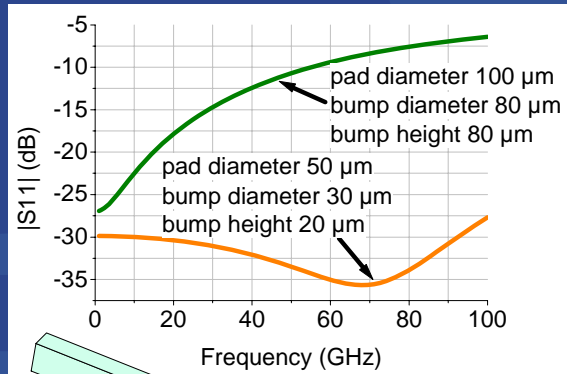
Influence of pad size

- bump height = 80 μm
- bump diameter = 80 μm
- pad size 80...110 μm
- most sensitive parameter



Comparison small / large bumps

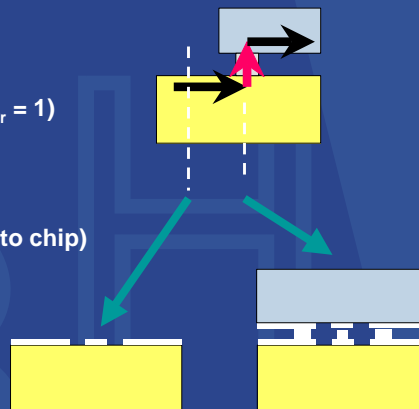
- High-frequency performance depends on interconnect size
- 30 μm bumps: excellent broadband characteristics over 100 GHz
- In practice: 2 parameters dictate overall dimensions
 - bump size
 - min. pad size & spacing on carrier substrate



Electrical characteristics: capacitive or inductive ?

Two effects

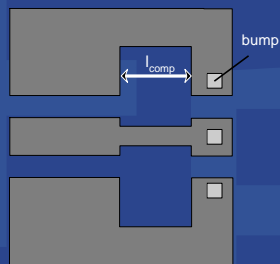
- **inductive** (bumps: coplanar structure with $\epsilon_r = 1$)
- **capacitive** (dielectric loading due to chip)



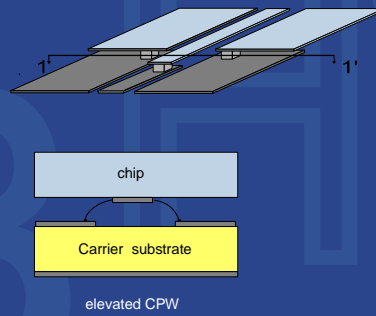
Optimized designs

Reduced reflection by means of compensation:

(i) high-impedance line section on motherboard



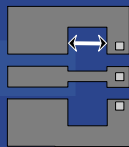
(ii) staggered bumps



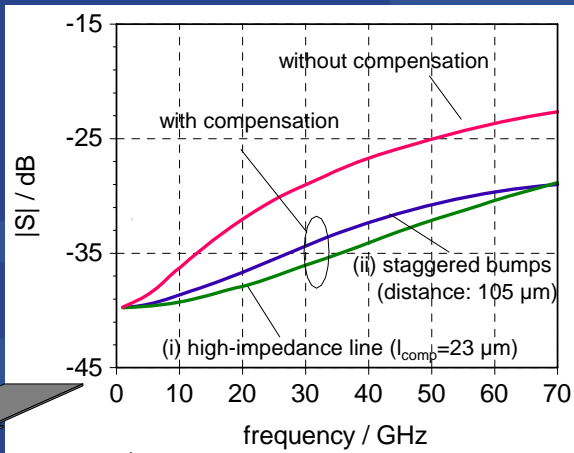
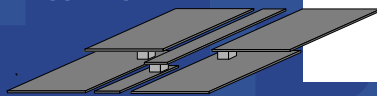
Reflection S_{11} w/o compensation

Bump height and diameter:
 $h = l = 25 \mu\text{m}$
Pad length: $l_p = 50 \mu\text{m}$

high-impedance line



staggering



Flip-chip interconnect: design rules

Bump diameter and pad dimension critical parameter,
not height (only detuning)

Capacitive behavior dominates

Bump / pad diameter

- 20...30 μm : good broadband mm-wave properties
- up to about 100 μm : possible with compensation

Verification by test structures

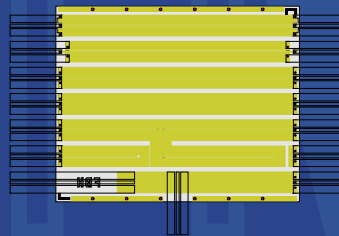
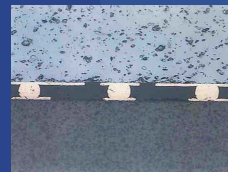
FC process by Alcatel (Stuttgart / Germany)

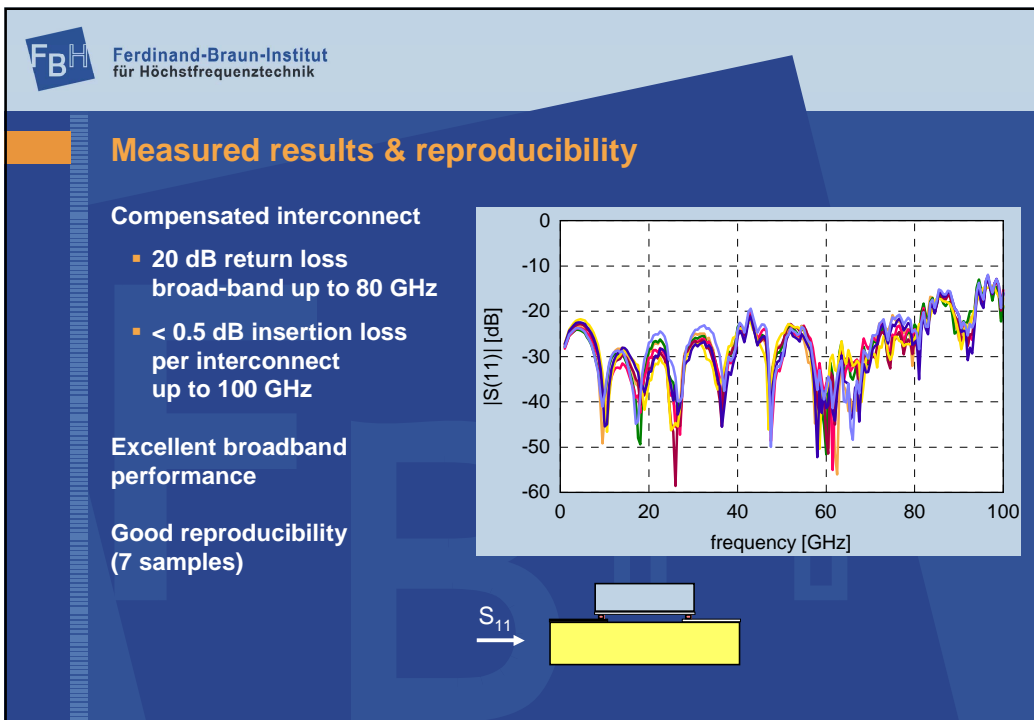
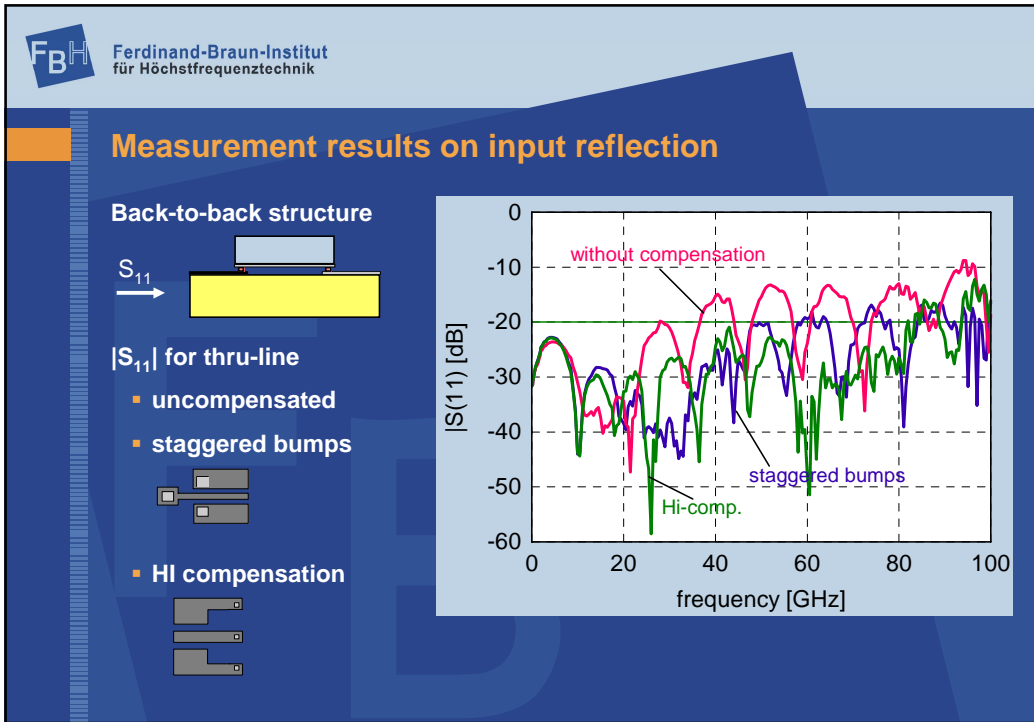
- electroplated Au bumps
- thermo-compression bonding

Bump geometry

- diameter $l = 35 \mu\text{m}$
- pad length $l_p = 60 \mu\text{m}$
- height $h = 22 \mu\text{m}$

GaAs test chips with passive structures






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 - **parasitic moding**
 - hot-via interconnect
- The package
 - thin-film & flip chip
 - LTCC as carrier substrate
- Conclusions

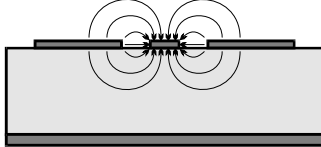


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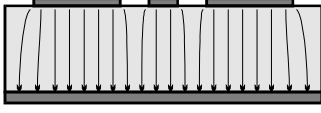
Be aware of parasitic modes

- Substrate modes due to multiple grounds
- Well known: PPL mode for conductor-backed CPW
- Package design must account for parasitic modes

CPW mode



Parallel-plate line mode (PPL)



Parasitic substrate modes

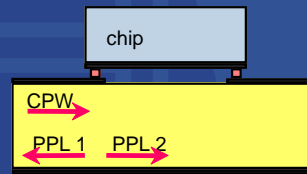
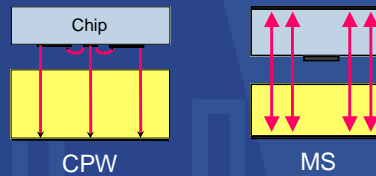
Parallel-plate line (PPL) modes
in flip-chip environment (below chip)

- for conductor-backed carriers
- present also in microstrip case

Excitation at interconnects & discontinuities

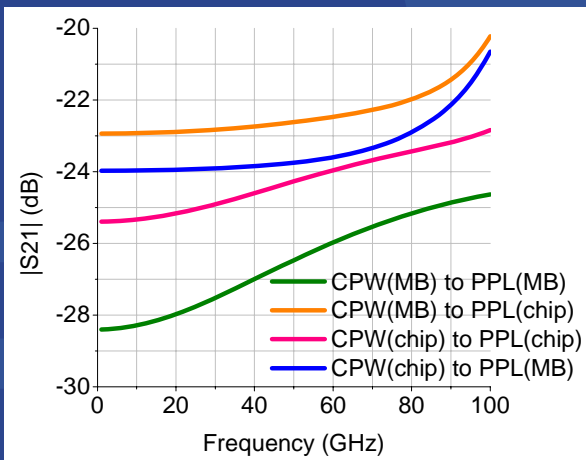
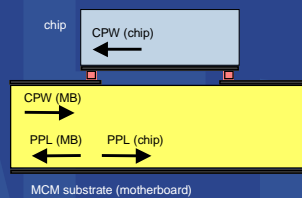
Result: unwanted crosstalk / coupling between
chip interconnects and housing feedthroughs

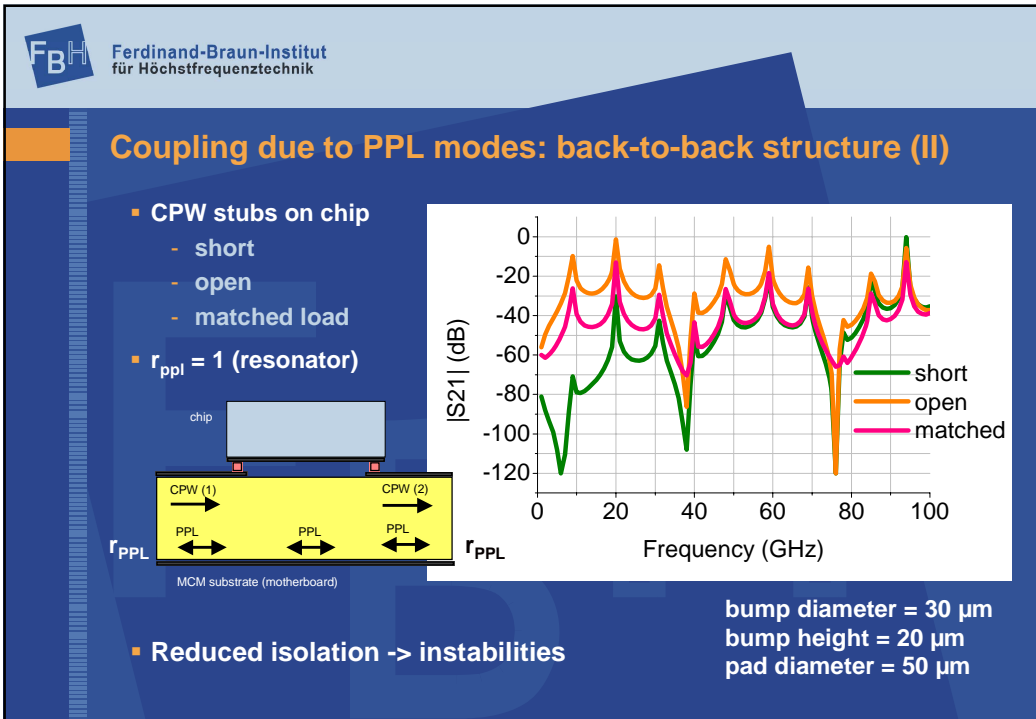
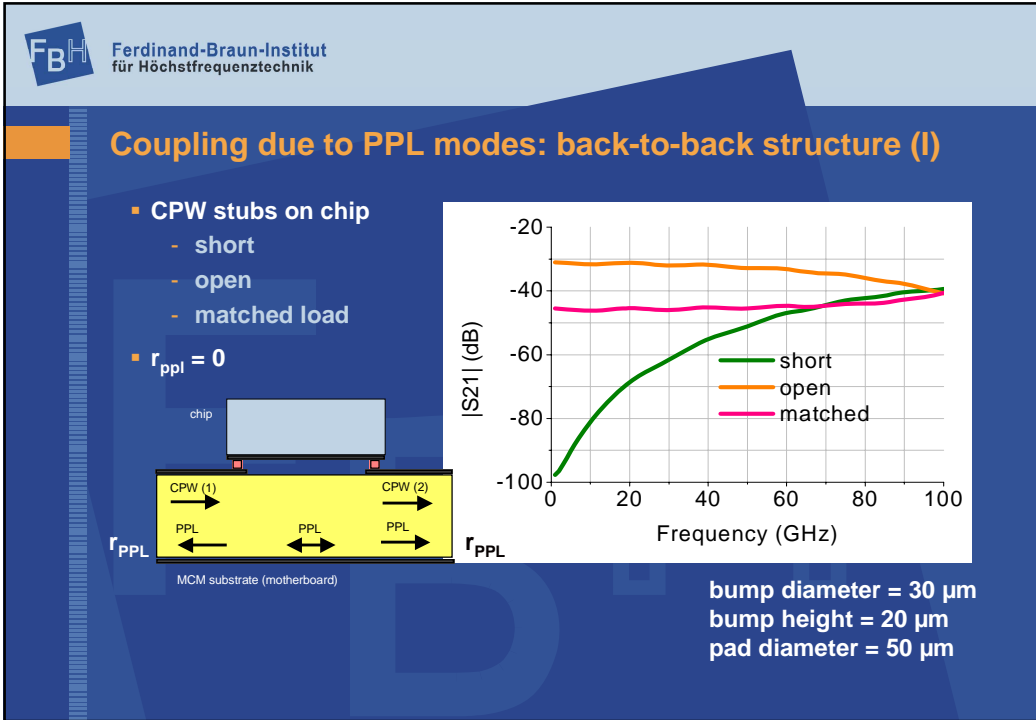
- reduced isolation
- stability problems



Coupling CPW to PPL modes : single transition

- bump diameter = 30 μm
- bump height = 20 μm
- pad diameter = 50 μm





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- parasitic modeling
- **hot-via interconnect**



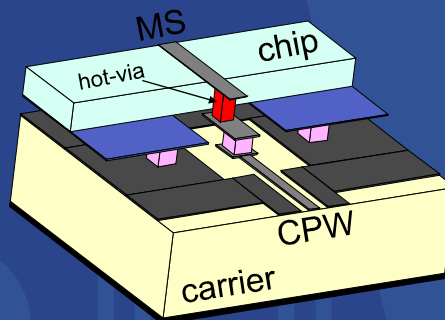
The package

- thin-film & flip chip
- LTCC as carrier substrate

Conclusions

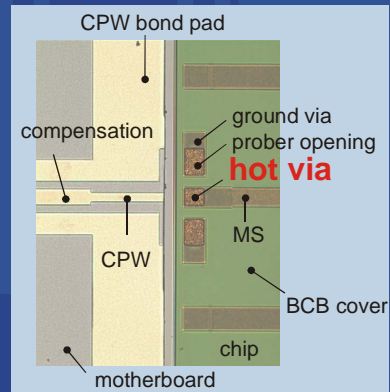
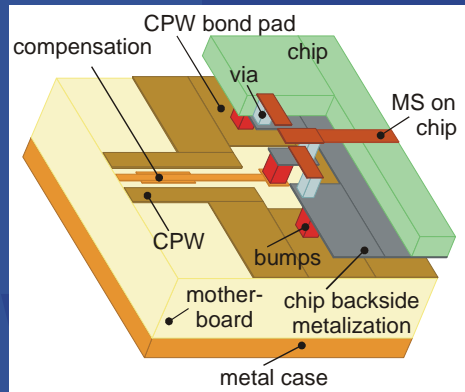
Flip-chip: The hot-via alternative

- Chip mounted frontside up
- Adapted to microstrip chips
- No detuning
- Requires chip backside process
- Higher reflections due to via interconnect



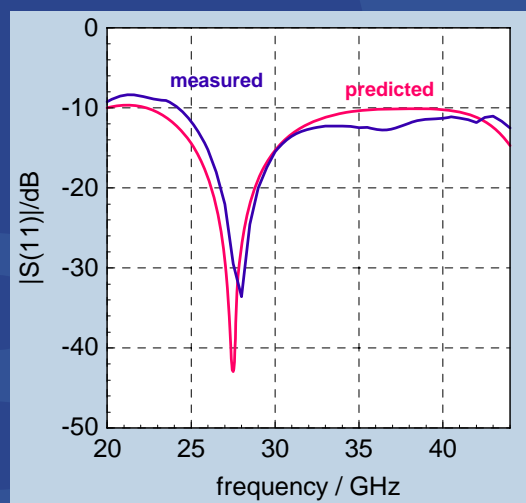
Hot-via design for 40 GHz (UMS / Ulm)

- Chip: in-out cell with on-wafer probing pads
- Compensation for 40 GHz



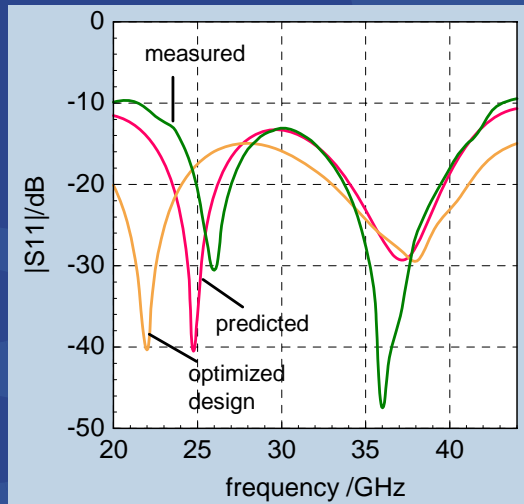
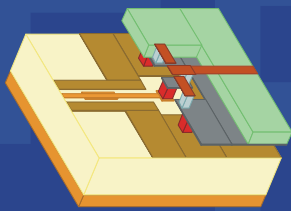
Hot-via: reflection (I)

- back-to-back structure;
without compensation



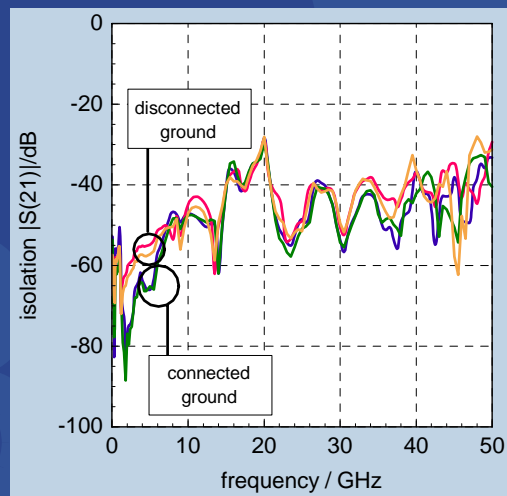
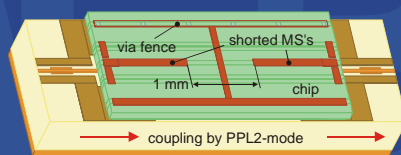
Hot-via: reflection (II)

- Back-to-back structure
- Compensation for 40 GHz
- Potential for frequencies beyond 40 GHz



Hot-via: isolation

- Microstrip stubs on chip
- Ground on motherboard connected/non-connected
- Measured transmission below -30 dB up to 50 GHz



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Why thin-film (on carrier)?

Main limitation of frequency / bandwidth potential of carrier-substrate approaches:

design rules for minimum dimensions

- strip width & spacing
- via diameter & pitch

Scaling

- Conventional ceramics (e.g. 127 μm thick Al_2O_3):
300 μm diameter vias, 600 μm pitch $\rightarrow \lambda/2$ at 80 GHz
- LTCC: 130 μm vias, 400 μm pitch
- Thin-film substrate (e.g. 20 μm thick BCB):
40...60 μm vias, 100 μm pitch

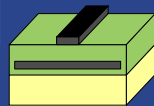
Thin-film & flip-chip

Thin-film microstrip (TFMSL) on carrier

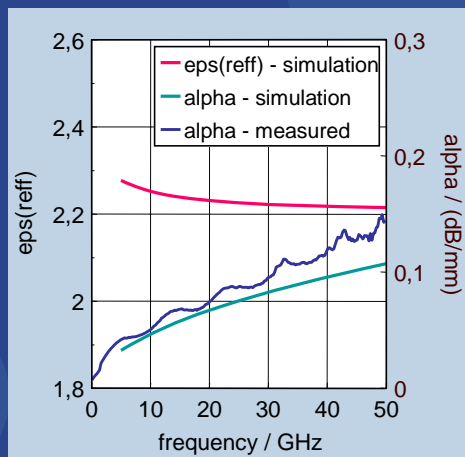
- surface-oriented as CPW
- suppression of parasitic modes (e.g. low-resistivity Si substrate)

Effective permittivity and attenuation vs. frequency (simulated & measured)

- quasi-TEM characteristics
- acceptable loss level

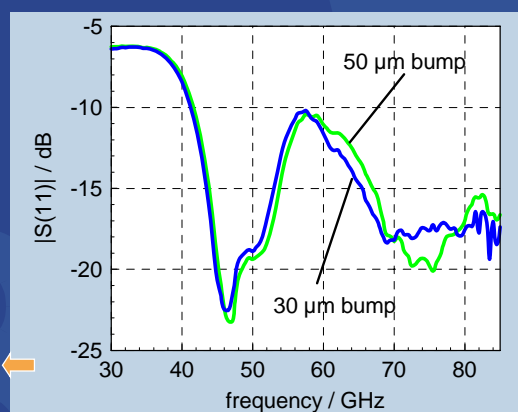
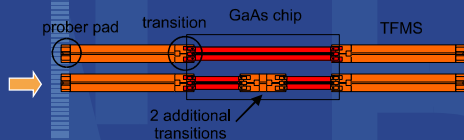


$d = 25 \mu\text{m}$
 $w = 64 \mu\text{m}$
 $\epsilon_r = 2.7$



Approach with thin-film carrier for 77 GHz (UMS)

- Compensated flip-chip interconnect (design by 3D em simulation)
- Thin-film carrier (BCB on Si)
- Chips: GaAs, coplanar, bumped chips can be probed
- Measurement results for 4-interconnect structure

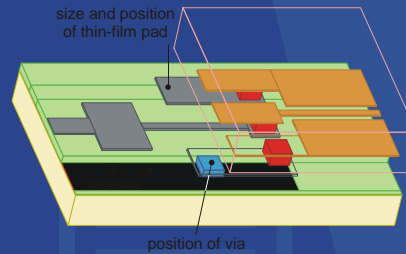


Thin-film & flip-chip: summary

Interesting solution

- feasible up to W band
- good isolation properties (lossy substrate)

To be clarified: CTE mismatch (chip - carrier substrate)



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LTCC as carrier substrate

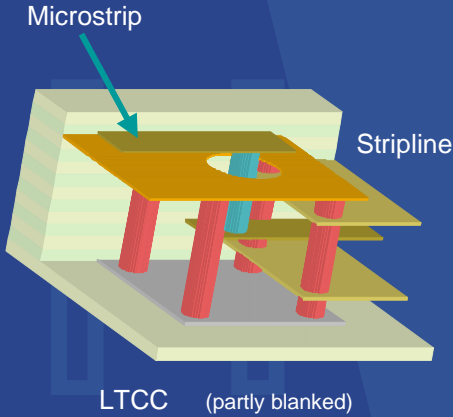
LTCC & thick-film process:
cost-efficient solution

Pros

- multi-layer flexibility (line structures, routing, DC)
- low cost

Cons

- thick-film design rules dictate large dimensions (100 μm line width & spacing)
-> reduced frequency limits



Microstrip

Stripline

LTCC (partly blanked)

FBH Ferdinand-Braun-Institut
für Höchstfrequenztechnik

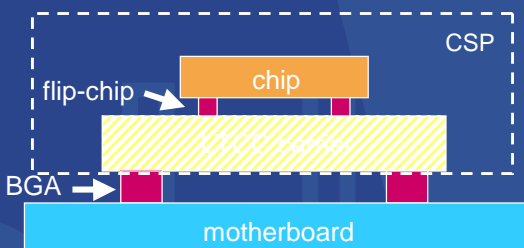
Example for LTCC solution: chip-scale package (CSP)

Approach

- flip-chip mounted coplanar chips
- LTCC intermediate substrate
- connected by BGA

Characteristics

- SMD compatible
- frequency limit: 40...50 GHz



flip-chip

chip

LTCC carrier

BGA

motherboard

CSP

Conclusions (I)

Flip-chip: clearly excellent potential for mm-waves

Broad-band interconnects up to 80 GHz and more realized

Linked to concepts for carrier substrate

- thin-film (BCB)
 - small dimensions
 - frequencies up to W band
- LTCC
 - low-cost
 - but frequency limitations (ca. 40 GHz so far)

Conclusions (II)

Status

- flip-chip of great interest, but not yet the standard

Transition to flip-chip requires decisions and additional efforts

- MCM assembly:
 - which flip-chip process?
 - which substrate?
 - needs qualification.
- Chip designer
 - GaAs: coplanar MMICs?
 - Si: thin-film microstrip is compatible!
- foundries: provide bumped chips?



Conclusions (III)

Flip-chip is gaining ground !

