Modeling the Package of a GaN Power Transistor

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- Introduction: GaN Power HEMTs at FBH
- Package and modelling approach
- Element extraction
- Measurements
- Conclusions
GaN Power HEMTs at FBH: Applications

Base stations (mobile communications, WIMAX, 1...4 GHz)
- Discretes
- Switch-mode amplifiers
- Focus on:
  - power
  - efficiency
  - linearity

Satcom, radar
- X-band discrete power devices and MMICs
- C- and Ka-band robust LNAs
- Focus on:
  - linearity & efficiency
  - robust LNAs

FBH GaN Technology: Full MMIC Capability

- GaN/AlGaN epitaxial growth on 3” SiC wafers
- Complete 3” HFET process
  - power bars and MMICs
  - 0.5 µm down to 0.15 µm gate technology
  - via technology (dry etched and laser assisted)
- Passive components:
  - 3 metal levels
  - electroplated Au air bridge
  - MIM capacitors
  - NiCr resistors
  - spiral inductors
Packaged Power Bar: 30 W

- **Geometry:** 5 x 8 x 250 µm
- **P_{max}** = 29 W
- **Linear gain:** 20 dB
- **P_{1dB}** = 14 W
- **Very high gain-power product**

Packaged Power Bar: 60 W

- **Geometry:** 11 x 8 x 250 µm
- **P_{max}** = 60 W @ 28 V_{DS}, 2 GHz
- **PAE:** 41%
- **Linear gain:** 15 dB
- **80 W heat dissipation**
Single Chip 100 W Power Bar (Feed-line, 40 mm)

- Design:
  - 10x8x500 μm
  - field-plate
- $P_{\text{max}}$ at 27 V$_{\text{DS}}$: 50 dBm (101 W) cw
- Gain: 14 dB
- PAE 39%

![Graph showing the relationship between input power (dBm) and output power (dBm), PAE (%), and gain (dB).](image)

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The Package under Consideration

- Kyocera power package
- Chip soldered to flange (heat sinking)
- Wire bonding
  - gate and drain
  - source: to ground (base plate)

Statement of Problem (I)

Task
- describe packaged power HEMT
- for: circuit design, package optimization

- 2 GHz type, 60 W
- frequency range up to 4 / 6 GHz of interest
Statement of Problem (II)

Challenges

- **Low impedance levels of transistors (large gate width)**
  - Extraction from S parameter measurements becomes inaccurate

- **Package description needs em simulation**
  - no simple models available
  - coupling effects cannot be neglected a priori

- **Measurement possible only in test fixture**
  - Deembedding of transistor data not straightforward

Approach

- **3D electromagnetic simulation of package**
  - multi-port analysis -> N-port
  - yields S and Z matrix (up to 10 GHz)
  - additional runs: varying bond wire length

- Define suitable equivalent-circuit topology

- Extract circuit elements from em simulation data

- Verify by measurements

- Combine package model with small-signal / large-signal model of HEMT unit cell
The N-Port Description (I)

For 11 unit cells: $22 + 2$ ports
**Equivalent Circuit Topology**

- Equivalent-circuit topology
  - single capacitor @ gate and drain
  - inductors along the feeding line
  - bond-wire inductances
    ▶ including coupling gate/drain
    ▶ inductance matrix

**EM Simulations**

The structure under investigation

- software: CST MWS (FDTD method)
- internal (lumped) ports at transistor cells
- parasitics of internal ports deembedded
**EM Simulations: Surface Currents (I)**

- Assists in understanding
- Impedances at internal ports: 1 Ω (gate), 50 Ω (drain)

**EM Simulations: Surface Currents (II)**

- Excitation at gate lead (top view)
EM Simulations: Surface Currents (III)

- Excitation at gate lead (bottom view)

EM Simulations: Surface Currents (IV)

- Excitation at drain lead (top view)
EM Simulations: Surface Currents (V)

- Excitation at drain lead (bottom view)

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Element Extraction

Procedure

- simulate structure with all unit cells connected
  - result: S and Z matrix (24 x 24)
- consider 2 port between single cell (i) and gate or drain lead
  - all remaining ports open

- extract C from Z matrix
- extract \( L_{ij} \)
  - varying bond wire length in order to check \( L(\text{bond}) \)

Element values: Capacitance C

Extraction as described before from 2-ports for each unit cell (i)

- topology with a single C on gate and drain is validated
- frequency dependence: allows description by constant value
Gate Inductances (I)

Bond wire inductance (25 µm single wire), when varying wire length
- extracted value: 916 pH / mm (rule of thumb 1nH/mm)

![Graph showing Gate Inductances (I)]

- Example
  - $L(\text{bond}) = 940$ pH
  - $L(p34) = 50$ pH
  - $L(p34) = 45$ pH
  - ....

causes uneven distribution
power vs. unit cell
**Drain Inductances**

Bond wire inductance (3 x 25µm-wires, ca. 25 µm apart), when varying wire length

- extracted value: 716 pH / mm (gate: 916 pH / mm)

**Mutual Inductances (I)**

Gate side (pitch 400 µm)

- mutual inductance up to 40% of L(bond)
- only next 2 neighbours relevant
Mutual Inductances (II)

Gate side to drain side
- self inductances ca. 900 pH
- dependence on distance
  - "3" next to "11": highest value
- magnitude: max. 5%
  - compared to 40% on same side

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Comparison with Measurements (I)

Simulation
- measured S parameters of unit cells (on-wafer)
- equivalent circuit model above

vs. measurement of packaged transistor in test fixture

Comparison with Measurements (II)

S(11): magnitude and phase
Comparison with Measurements (III)

$S(21)$: magnitude and phase

Comparison with Measurements (IV)

$S(22)$: magnitude and phase
Comparison with Measurements (V)

- Agreement in $S_{ij}$ good up to 4...5 GHz
- Remaining deviations may be due to
  - non-uniformity of unit cells
  - restriction to the model topology
    - lumped/distributed characteristics
  - imperfections of the em simulation

Conclusions

- Lumped equivalent-circuit modeling OK up to 4...5 GHz
- but: em simulation is needed to determine element values

- Mutual inductances play important role
  - between neighbouring bond wires: 40%
  - between different sides: 5%

- Feeding structure causes uneven power distribution over cells
  - at 2 GHz still moderate
  - pronounced at higher frequencies
  - optimizing the package is important (e.g., widen the lead)