Simulation and Modeling of Large Microwave and Millimeter-Wave Systems, Part 2

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with
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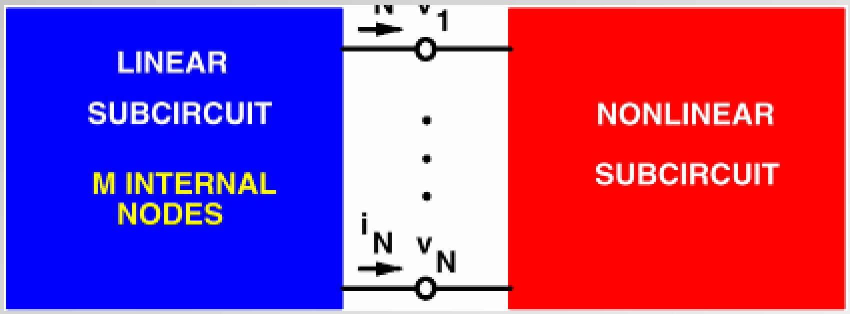
http://www.freeda.org

Outline

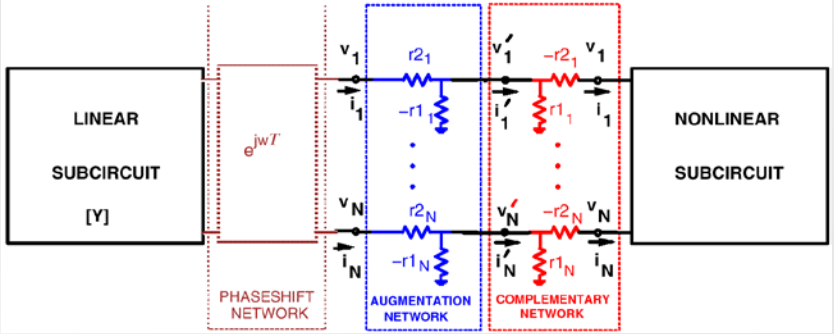
- ***fREEDA^{TM} Modeling Code***
- ***Simple device modeling***
- ***Noise Modeling***
- ***Transistor Model***
- ***Quasi-Optical Modeling***
- ***Parallel Circuit Simulation***
- ***Distributions***
- ***Commercialization***

Circuit-Level Behavioral Modeling

Linear Sub-Circuit Behavioral Modeling



Transient Analysis of Microwave Circuit



Behavioral Model is the Linear Subcircuit Described by

(*M* + *N*) x (*M* + *N*) *Y* Parameters

Reduce to *N* x *N* *Y* Parameters

Harmonic Balance

Use *N* x *N* Parameters Directly

SPICE

Use Impulse Response ✓

or Use Pole-Zero Approximation

Behavioral Model is an Impulse Response

Augmentation Network Used to Facilitate Incorporation of Behavioral Model

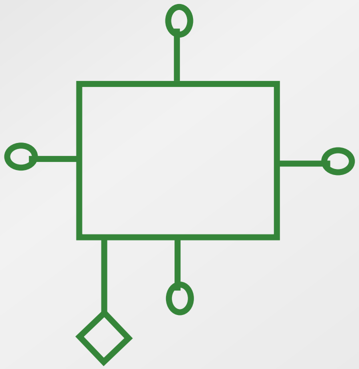
Frequency and Time Banding

Effect of the augmentation network removed during simulation.

Response of linear network is limited in time and frequency.

Coding Example

Modeling Scope



Can handle

$$y(t) = F\left[\begin{matrix} x_1(t),\ldots,x_n(t),\dfrac{dx_1(t)}{dt},\ldots,\dfrac{dx_n(t)}{dt}, \\ \dfrac{d^2x_1(t)}{dt^2},\ldots,\dfrac{d^2x_n(t)}{dt^2},\dfrac{d^3x_1(t)}{dt^3},\ldots,\dfrac{d^3x_n(t)}{dt^3}, \\ x_1(t-\tau_1),\ldots,x_n(t-\tau_1) \end{matrix}\right]$$

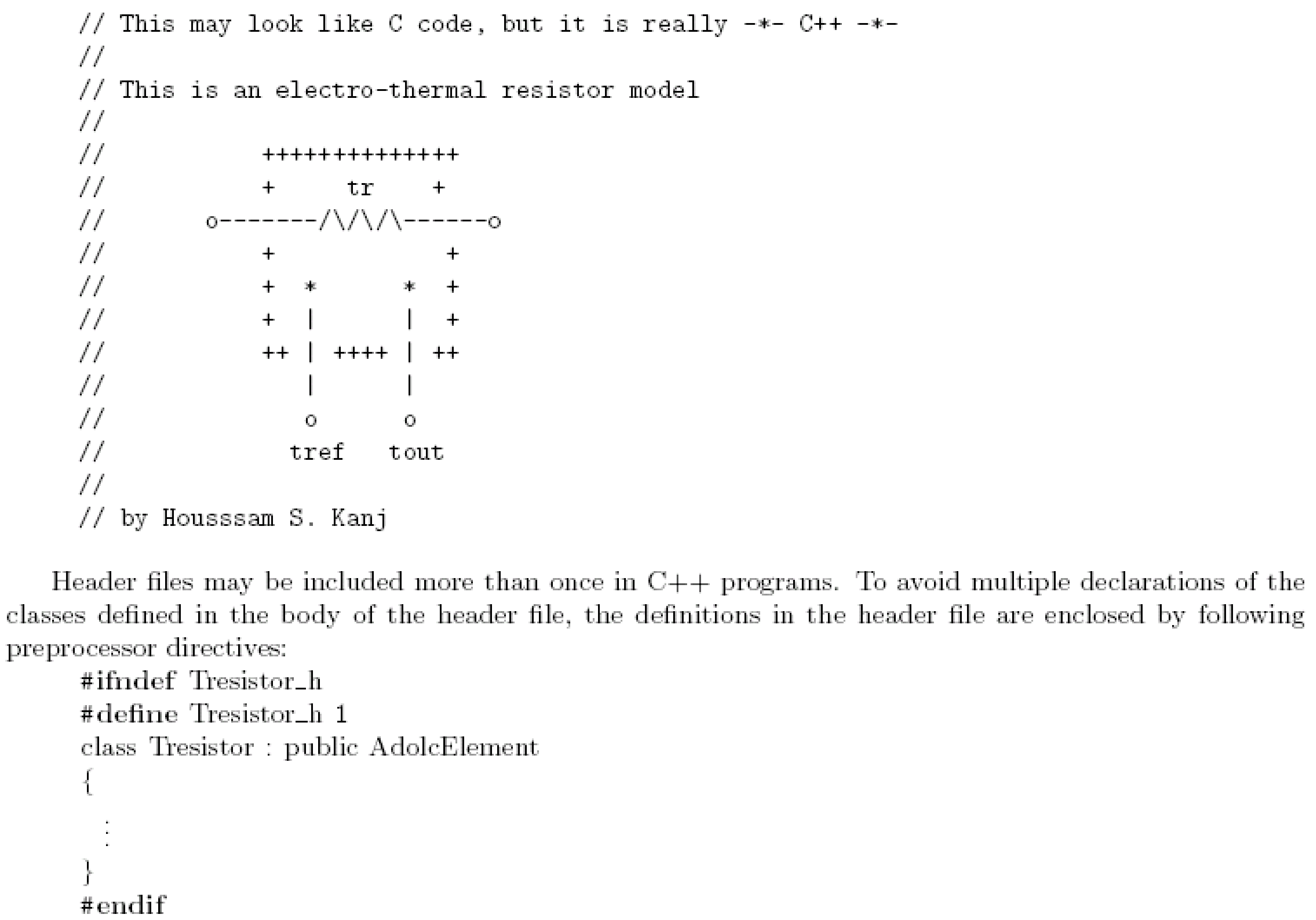
Where *y*(t) is either an *i(t*) or a *v*(*t*).

Also in any type of analysis we want *dy/dx* The exact derivatives (w.r.t. time or frequency etc.) we want depend on the type of analysis we are doing (transient, wavelet, harmonic balance). The derivatives needed are calculated using ADOL-C under control of the analysis routines. This is why the same model can be used in any type of analysis.

ADOL-C is one of the many support libraries.

Quick Once Over of Element Code

Electro-Thermal Resistor Code



```
// This may look like C code, but it is really -*- C++ -*-
//
// This is an electro-thermal resistor model
//
//           ++++++++++++++
//           +     tr    +
//       o-------/\/\/\------o
//           +            +
//           +  *      *  +
//           +  |      |  +
//           ++ | ++++ | ++
//              |      |
//              o      o
//             tref   tout
//
// by Housssam S. Kanj
```

Header files may be included more than once in C++ programs. To avoid multiple declarations of the classes defined in the body of the header file, the definitions in the header file are enclosed by following preprocessor directives:

```
#ifndef Tresistor_h
#define Tresistor_h 1
class Tresistor : public AdolcElement
{
  ⋮
}
#endif
```

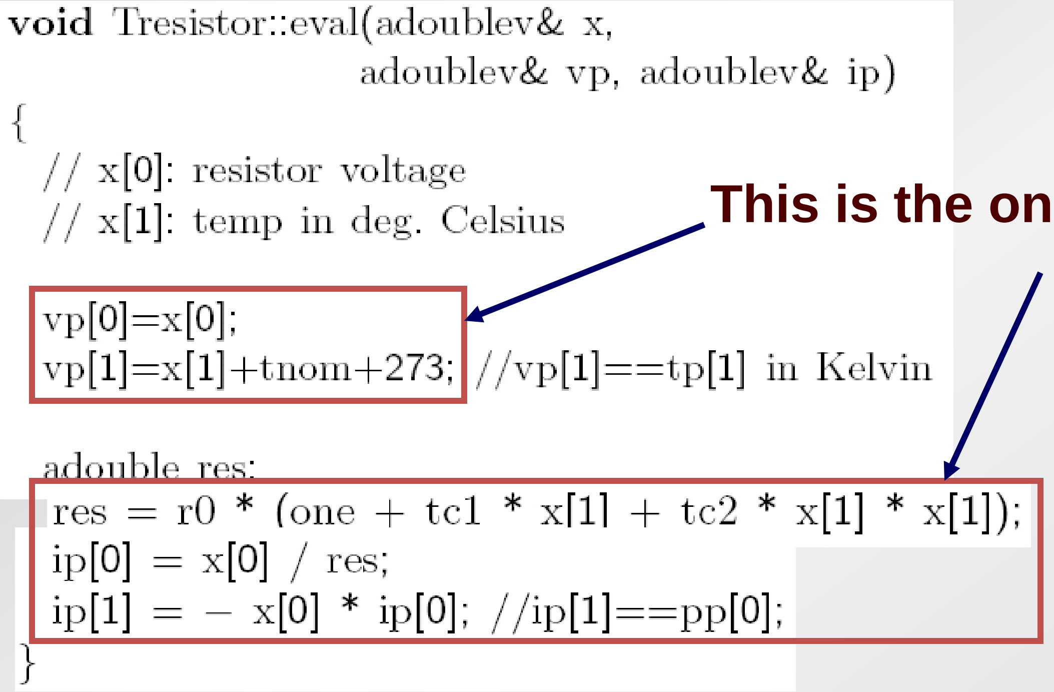
Electro-Thermal Resistor Code

```
#include "../network/ElementManager.h"
#include "../network/AdolcElement.h"
#include "../analysis/FreqMNAM.h"
#include "../analysis/TimeMNAM.h"
#include "Tresistor.h"
```

Now we must define the static member variables:

```
// Static members
const unsigned Resistor::n_par = 11‘;

// Element information
ItemInfo Resistor::einfo = {
  "tr",
  "Tresistor",
  "Houssam S. Kanj",
  DEFAULT_ADDRESS"elements/Resistor.h.html"
};
// Parameter information
ParmInfo Tresistor::pinfo[] = {
  {"r0", "Resistance value (Ohms)", TR_DOUBLE, false},
  {"l", "length (meters)", TR_DOUBLE, false},
  {"w", "width (meters)", TR_DOUBLE, false},
  {"t", "system Temperature (Celsius)", TR_DOUBLE, false},
  {"rsh", "sheet resistance (Ohms/sq)", TR_DOUBLE, false},
  {"defw", "default device width (meters)", TR_DOUBLE, false},
  {"narrow", "narrowing due to side etching (meters)", TR_DOUBLE, false},
  {"tnom", "initial Temperature (Celsius)", TR_DOUBLE, false},
  {"tc1", "Temperature Coefficient (1/Celsius)", TR_DOUBLE, false},
  {"tc2", "Temperature Coefficient (1/Celsius)", TR_DOUBLE, false},
  {"pdr", "Power Depenent Resistor", TR_BOOLEAN, false}
 };
```

Evaluation Routine



```
void Tresistor::eval(adoublev& x,
                     adoublev& vp, adoublev& ip)
{
  // x[0]: resistor voltage
  // x[1]: temp in deg. Celsius

  vp[0]=x[0];
  vp[1]=x[1]+tnom+273; //vp[1]==tp[1] in Kelvin

  adouble res;
  res = r0 * (one + tc1 * x[1] + tc2 * x[1] * x[1]);
  ip[0] = x[0] / res;
  ip[1] = − x[0] * ip[0]; //ip[1]==pp[0];
}
```

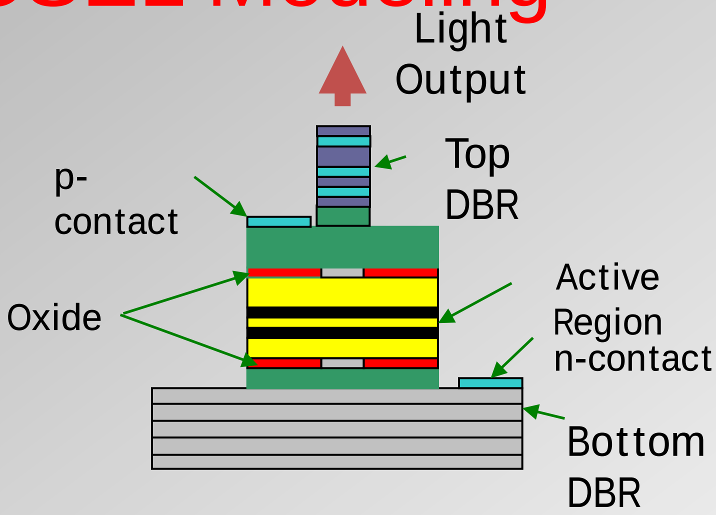
This is the only executable code

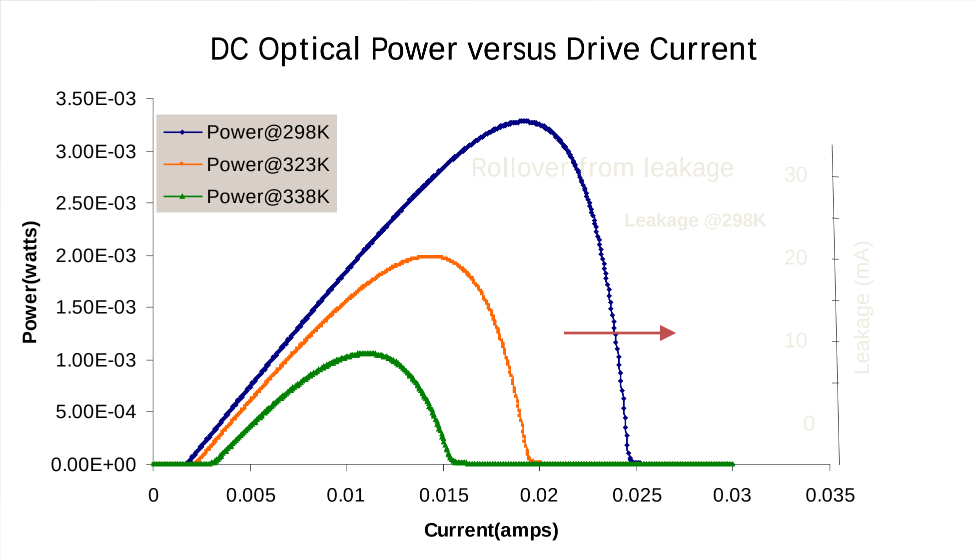
The same model close is used in all analyses: DC, Transient; Wavelet; Large Signal Noise, Harmonic balance; Analyses (32 altogether).

What can be Modeled that Could not be Modeled Before

VCSEL

VCSEL Modeling





Single Mode Rate Equations

Carrier density

$dN(t)/dt = \eta_i(I(t)-I_L(T))/\tau - N(t)/\tau_{nr} - G(T)(N(t)-N_0(T))S(t)/(1+\varepsilon S(t))$

Photon density

$dS(t)/dt = -S(t)/\tau_p + \beta N(t)/\tau_r + G(T)(N(t)-N_0(T))S(t)/(1+\varepsilon S(t))$

Temperature

$dT(t)/dt = -T(t)/\tau_{th} + (T_0+(I(t)V(t)-P_0(t))R_{th})/\tau_{th}$

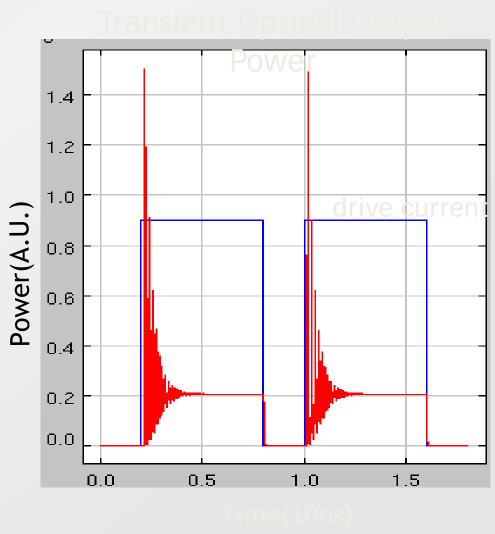
Temperature dependence of Gain and Transparency

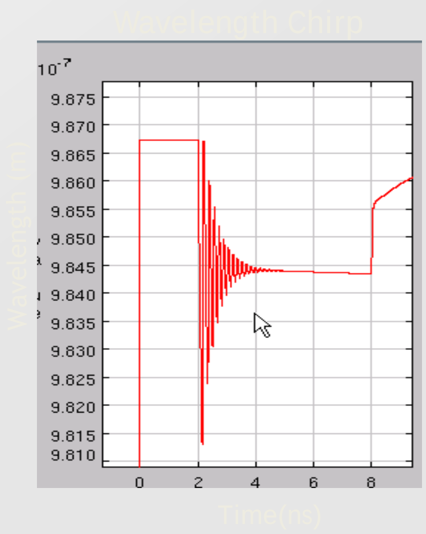
$G(T) = G_0(a_{g0} + a_{g1}T + a_{g2}T^2) / (b_{g0} + b_{g1}T + b_{g2}T^2)$

$N_0(T) = N_{t0}(c_{n0}+c_{n1}T+c_{n2}T^2)$

Leakage Current

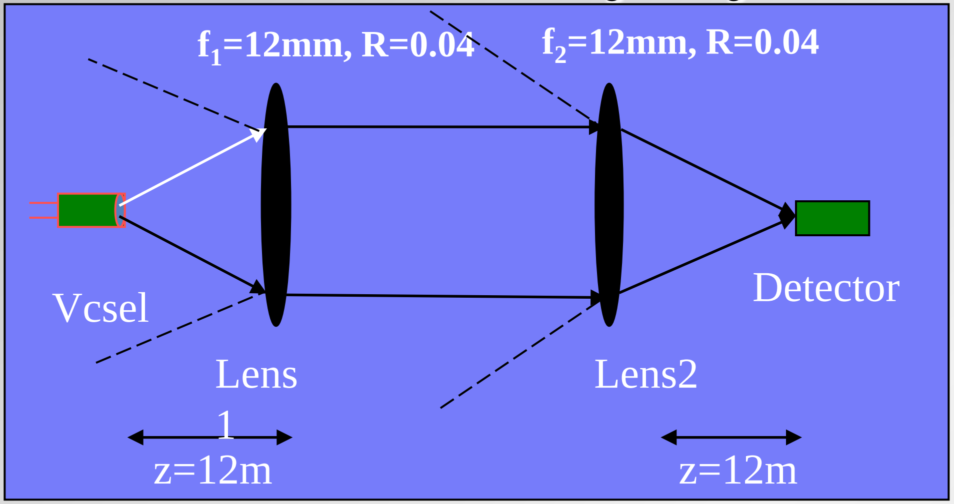
$I_L = I_{L0}\exp[(-a_0 + a_1N_0 + a_2N_0T - a_3/N_0)/T]$





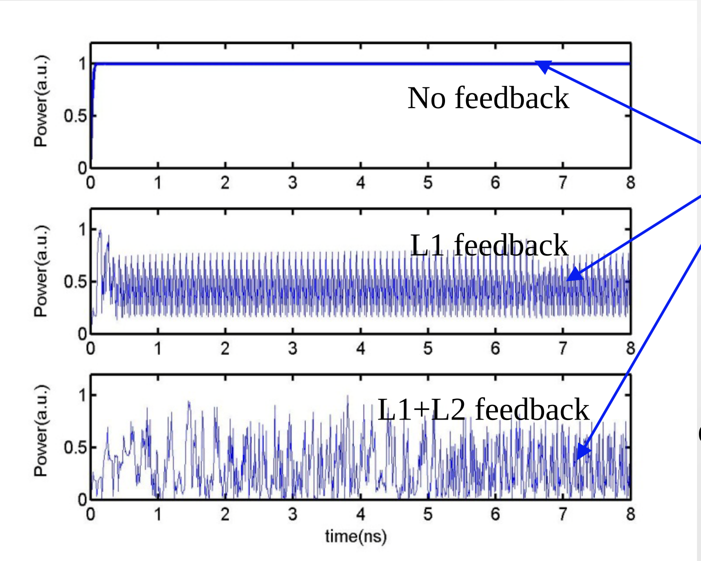
Feedback Results:

- Power and Wavelength degradation due to two components



With:
Mark Niefeld
Ravi Pant
Univ. of Arizona

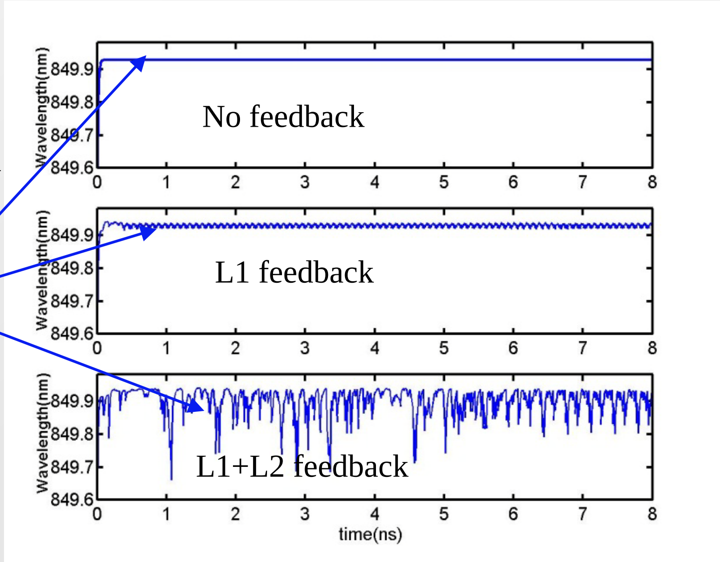
Optical Power



Output power degradation due to single and double lens feedback

Output wavelength degradation due to single and double lens feedback

Wavelength



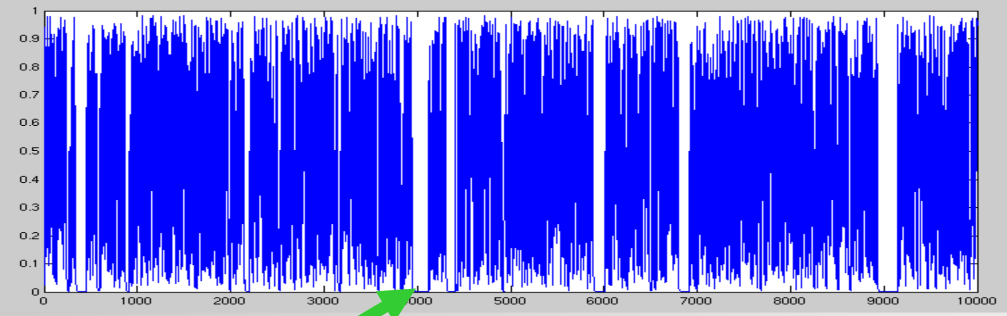
Code

$$f\left(x(t), \frac{dx}{dt}, \frac{d^2x}{dt^2}, x(t-\tau)\right)$$

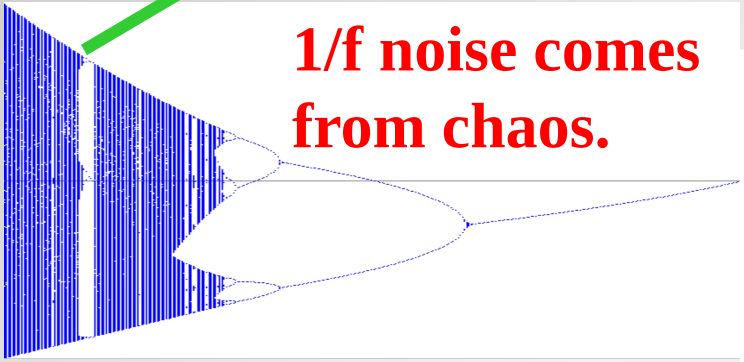
```
void Vcsel::eval(adoublev& x, adoublev& vp, adoublev& ip)
{
  // x[0]: terminal current, I
  // x[1]: photon density, vm0
  // x[2]: carrier density, vn0
  // x[3]: temperature, T
  // x[4]: dI/dt
  // x[5]: dvm0/dt
  // x[6]: dvn0/dt
  // x[7]: dT/dt
  adouble delta = 1e-8;
  adouble zn = 1e7;
  adouble q = 1.6e-19;
  vp[0] = 1.721 + 275*x[0] - 2.439e4*x[0]*x[0] + 1.338e6*x[0]*x[0]*x[0]
          - 4.154e7*x[0]*x[0]*x[0]*x[0] + 6.683e8*x[0]*x[0]*x[0]*x[0]*x[0]
          - 4.296e9*x[0]*x[0]*x[0]*x[0]*x[0]*x[0];
  ip[0] = x[0];
  adouble T = t0 + x[0];
  adouble G = g0 * (ag0 + ag1*T + ag2*T*T)/(bg0 + bg1*T + bg2*T*T);
  adouble Nt = nt0 * (cn0 + cn1*T + cn2*T*T);
   adouble Il = il0 * exp((-a0 + a1*zn*vn0+a2*zn*vn0*T - a3/(zn*vn0))/T);
}
```

Large Signal Noise Modeling

Flicker Noise



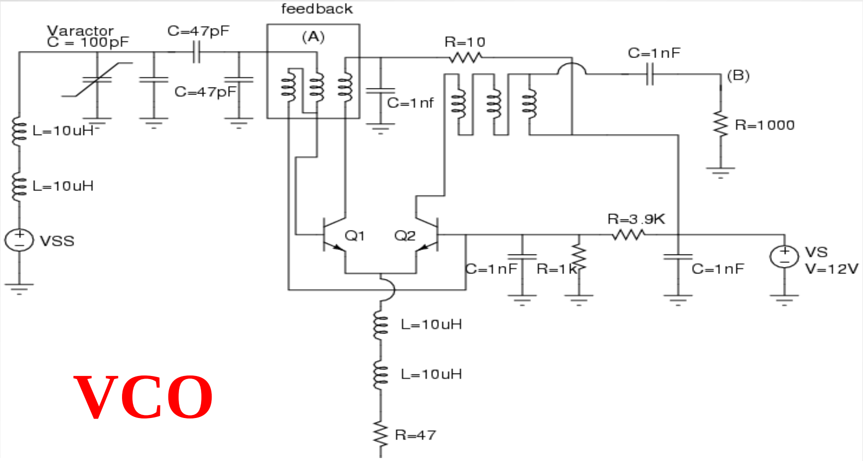
Laminar Regions



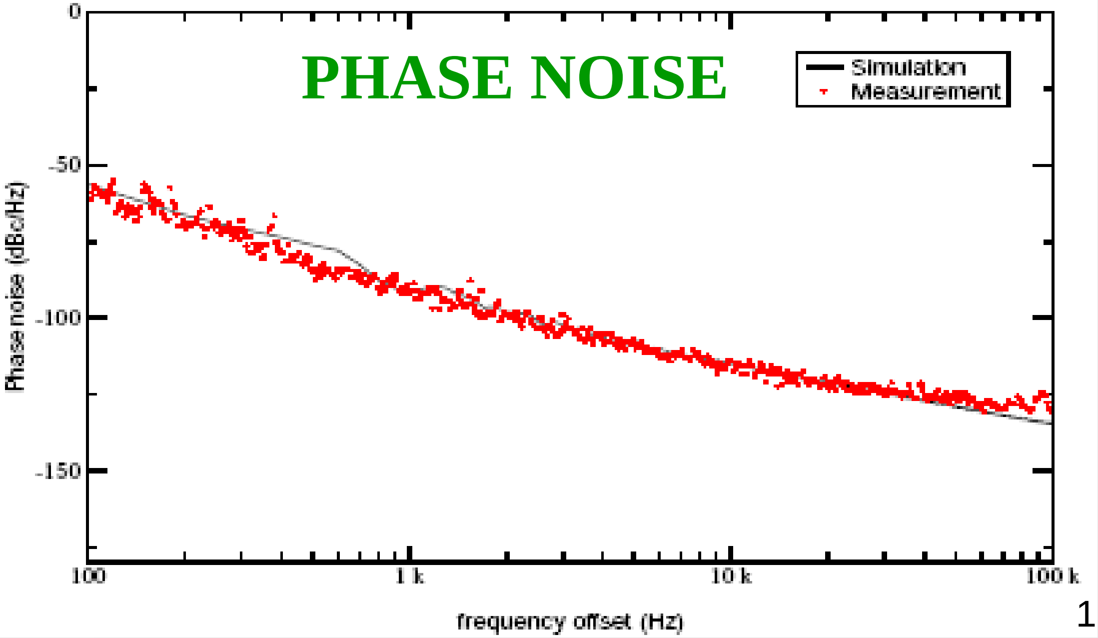
1/f noise comes from chaos.

Phase noise modeled in the time domain.

+ Large Signal Noise

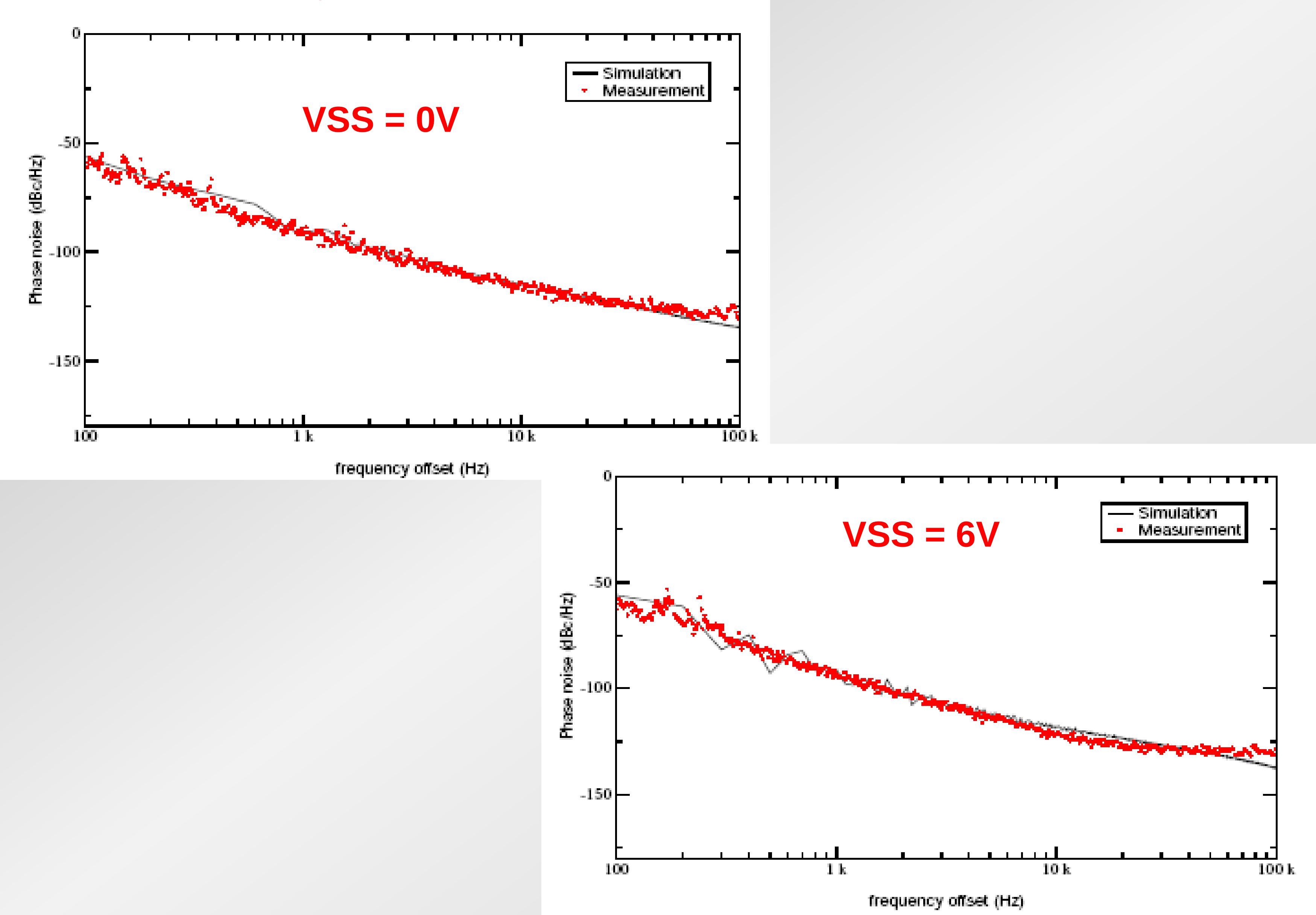


VCO



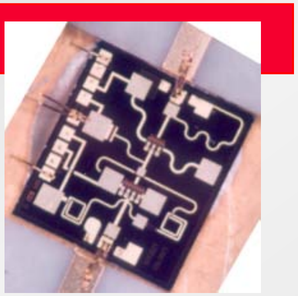
PHASE NOISE

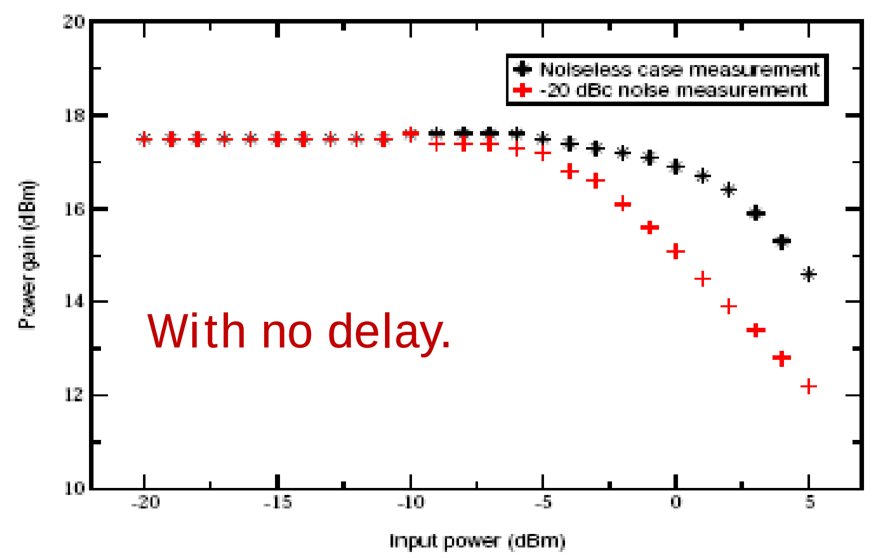
Phase Noise is Fully Predictive



Large Signal Noise

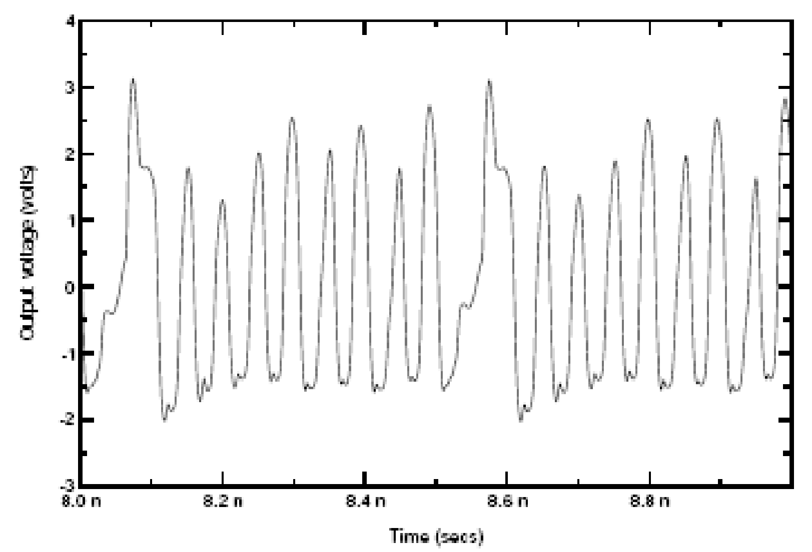
X-band MMIC

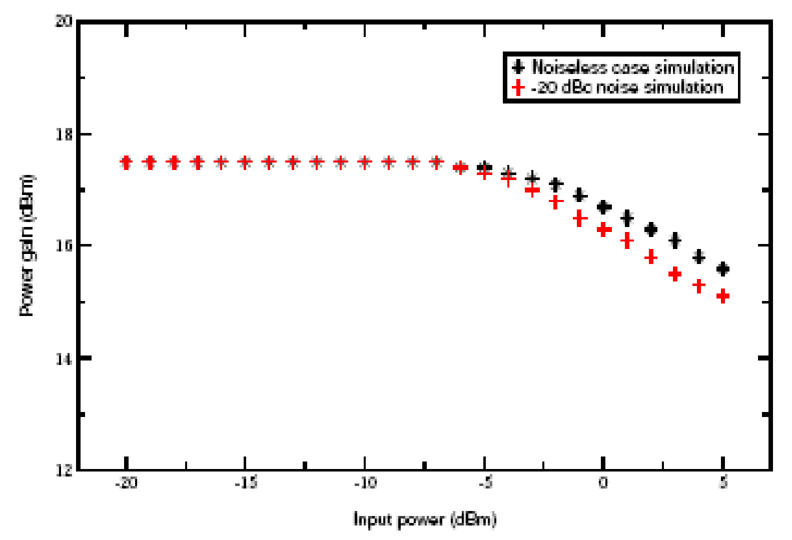




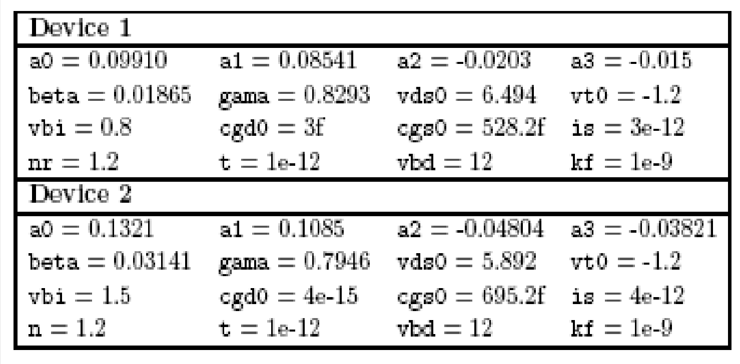
With no delay.

Measurement of power gain v/s input power





With 1 ps delay for each transistor



Device 1			
a0 = 0.09910	a1 = 0.08541	a2 = -0.0203	a3 = -0.015
beta = 0.01865	gama = 0.8293	vds0 = 6.494	vt0 = -1.2
vbi = 0.8	cgd0 = 3f	cgs0 = 528.2f	is = 3e-12
nr = 1.2	t = 1e-12	vbd = 12	kf = 1e-9
Device 2			
a0 = 0.1321	a1 = 0.1085	a2 = -0.04804	a3 = -0.03821
beta = 0.03141	gama = 0.7946	vds0 = 5.892	vt0 = -1.2
vbi = 1.5	cgd0 = 4e-15	cgs0 = 695.2f	is = 4e-12
n = 1.2	t = 1e-12	vbd = 12	kf = 1e-9

Modeling Noise

Deterministic differential equation:

$$\frac{dx}{dt} = a(t, x)$$

Stochastic differential equation

$$\frac{d}{dt}X_t = a(t, X_t) + b(t, X_t)\xi_t.$$

The Ito form

- **Named after Japanese mathematician K. Ito in the late 40s. He formulated the theory of Stochastic integration.**
- **Evaluation at the starting point on each interval.**
- **Requires no estimation of future values.**
- **Used in models where stochastic processes are assumed purely white.**

The Stratonovich form

- **Named after Russian engineer R. L. Stratonovich in the mid 60s.**
- **Evaluation at the mid-point on each interval.**
- **Requires estimation of future values.**
- **Used in models where stochastic processes are not purely white.**

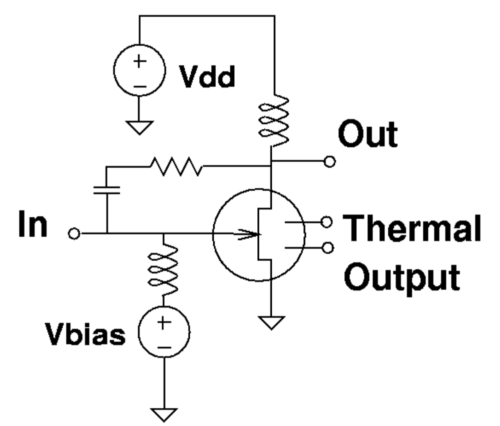
Either form will produce different end results but are both mathematically “right”.

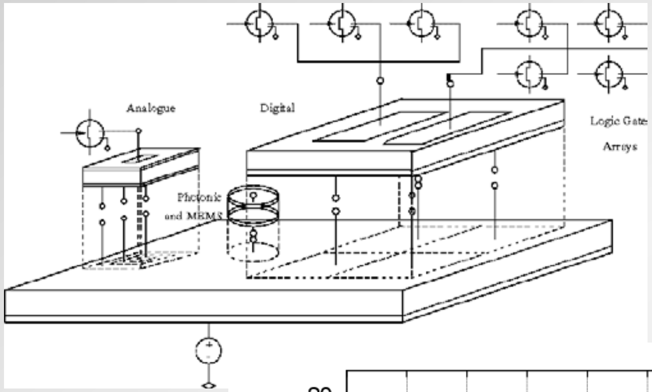
Which form to use is a modeling issue.

The Ito form requires new numerical techniques for solving an SDE. The Stratonovich form can be solved using techniques of classical calculus which is a significant advantage.

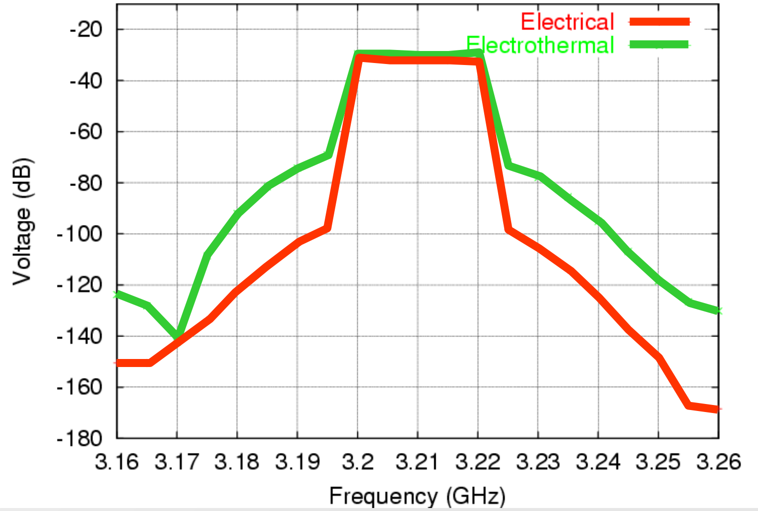
Electro-Thermal Physical Transistor Model

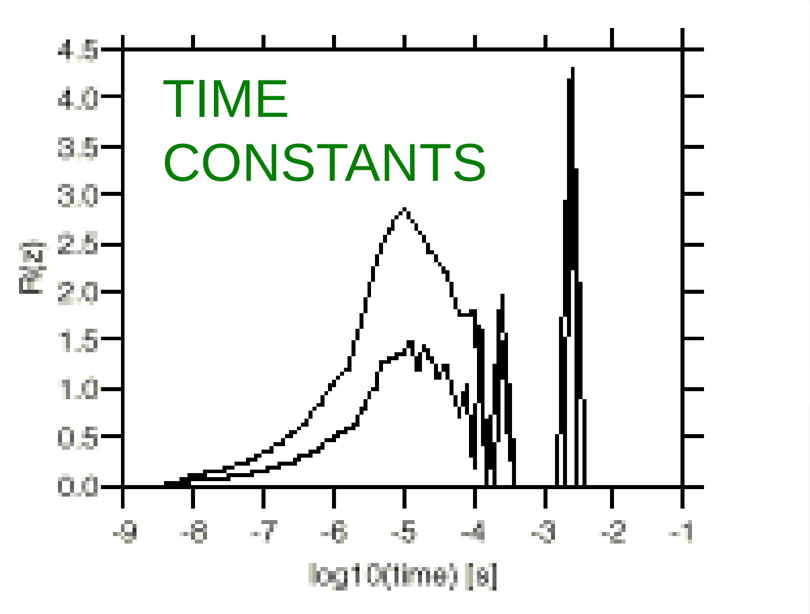
Electro-Thermal Modeling of PA





Batty/Snowden
Univ. Leeds



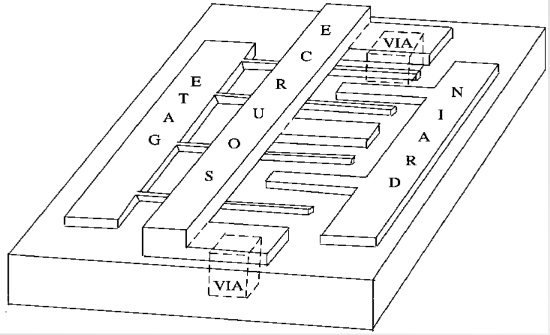


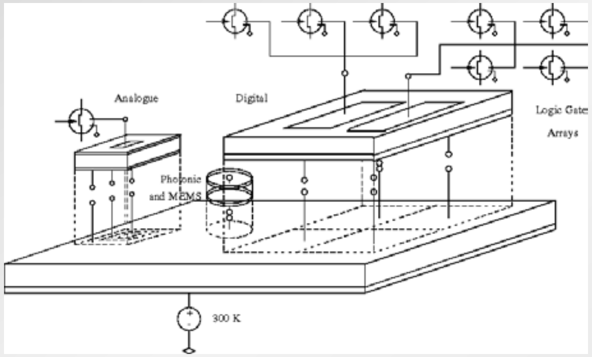
CONVERT NONLINEAR THERMAL PROBLEM INTO A LINEAR PROBLEM

KEY CONCEPT IS TIME DILATION

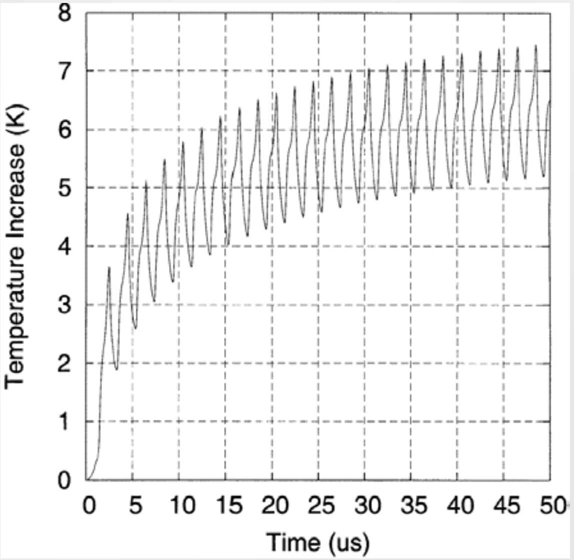
The first implementation of a Physical Transistor Model directly into a general purpose simulator: LPM (Leed's Physical Model) (implementation by University of Leeds in fREEDA). This is a full electro-thermal model of MESFETs and pHEMTs. Full device physics.

This can only be done in fREEDA because of state variables and universal error concepts (not just KCL).





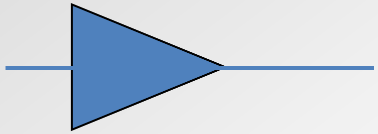
Electro-thermal model construction.



Temperature rise in junction of MMIC with 500 kHz tone.

Gain of MMIC is a function of temperature.

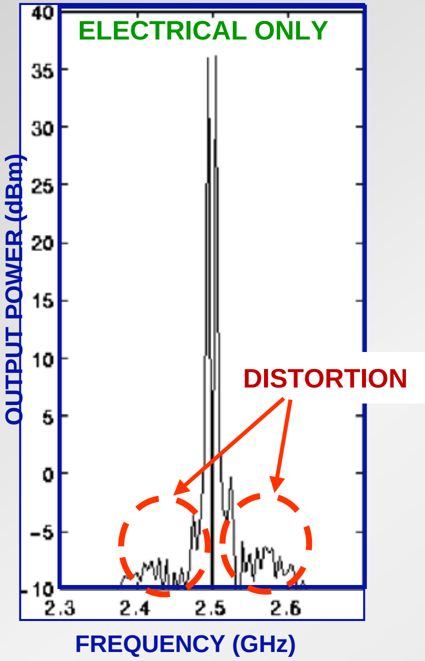
Gain varies with modulation of a signal.



Highest level of integrated global modeling of complex microwave subsystem, to date.

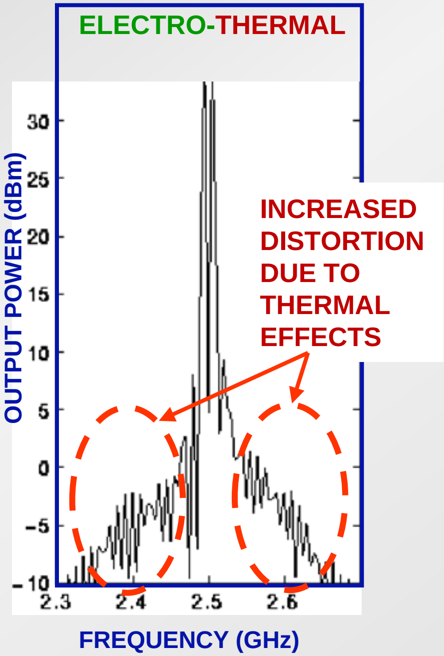
Illustrates impact of thermal effects on total System performance.

TWO TONE TEST



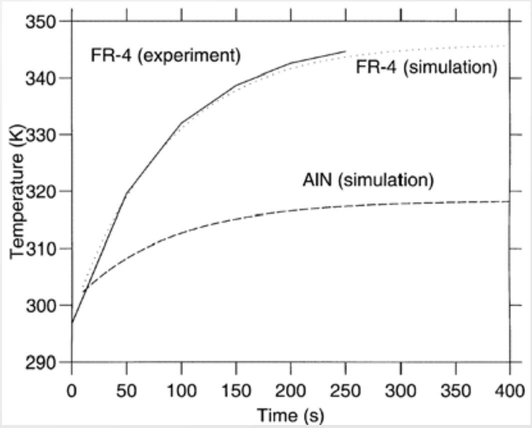
ELECTRICAL ONLY

DISTORTION



ELECTRO-THERMAL

INCREASED DISTORTION DUE TO THERMAL EFFECTS



MMIC Temperature Variation

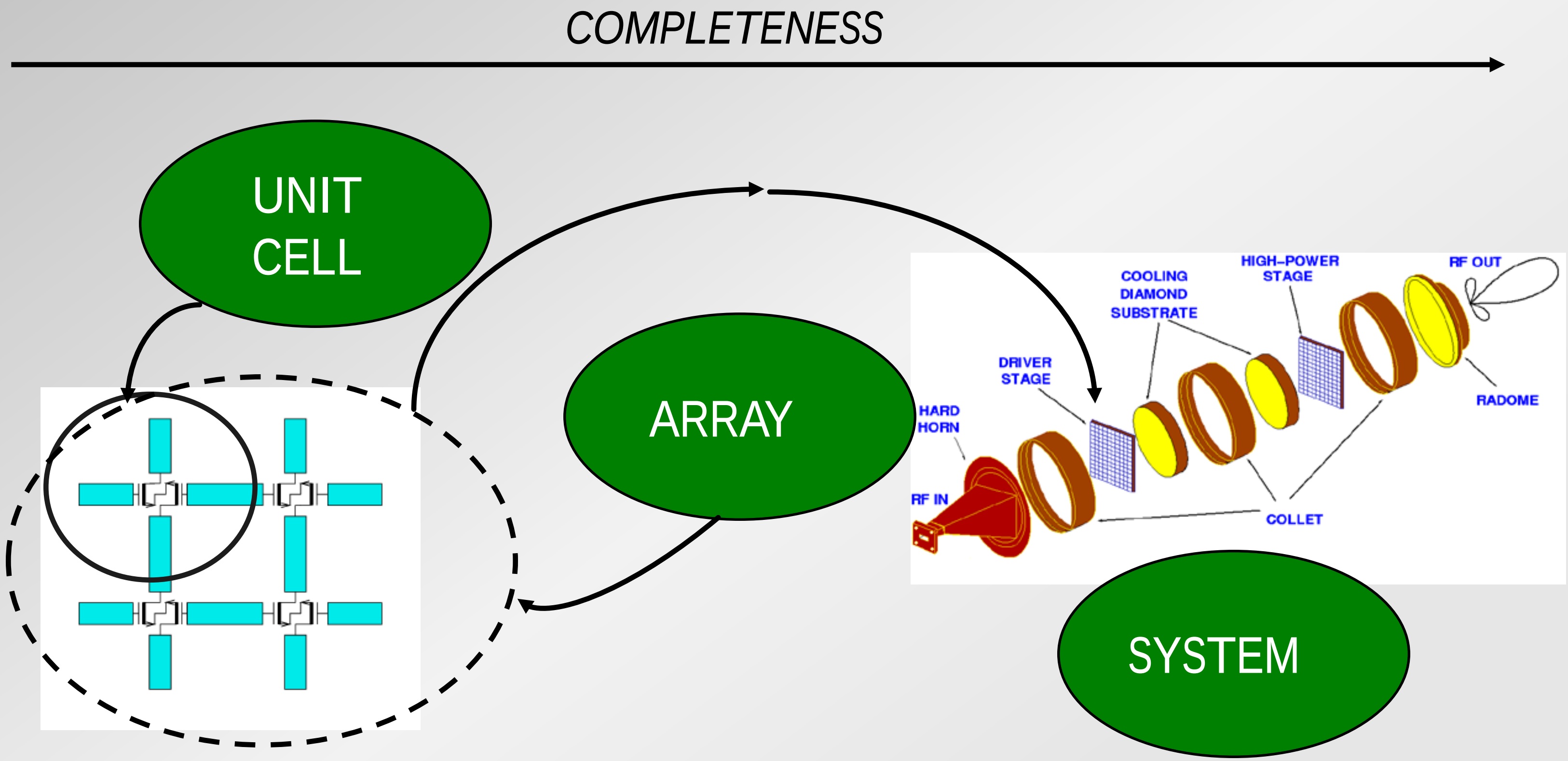
Variations in temperature due to
– turn-on transient (pulsed operation)
– modulation (variation of signal level)

For a Ka band MMIC typically there is a 4 dB drop in gain for a 30 K increase in temperature.

Electro-Thermal Simulation essential to accurate design.

Application: Modeling of a Quasi-Optical Power Combiner

Quasi-Optical Power Combining Amplifier



COMPLETENESS

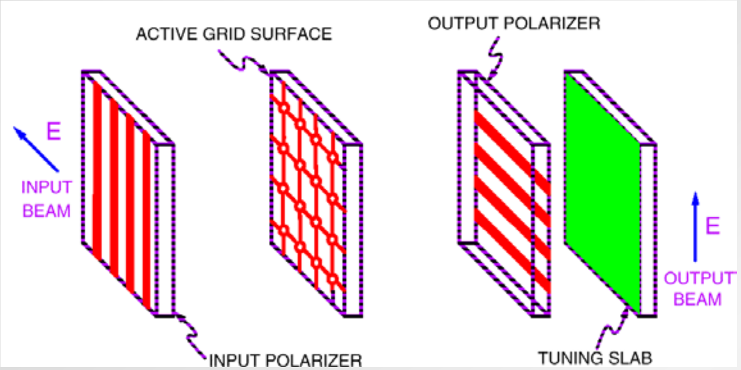
UNIT CELL

ARRAY

SYSTEM

Essential Problems in CAE of QO Systems

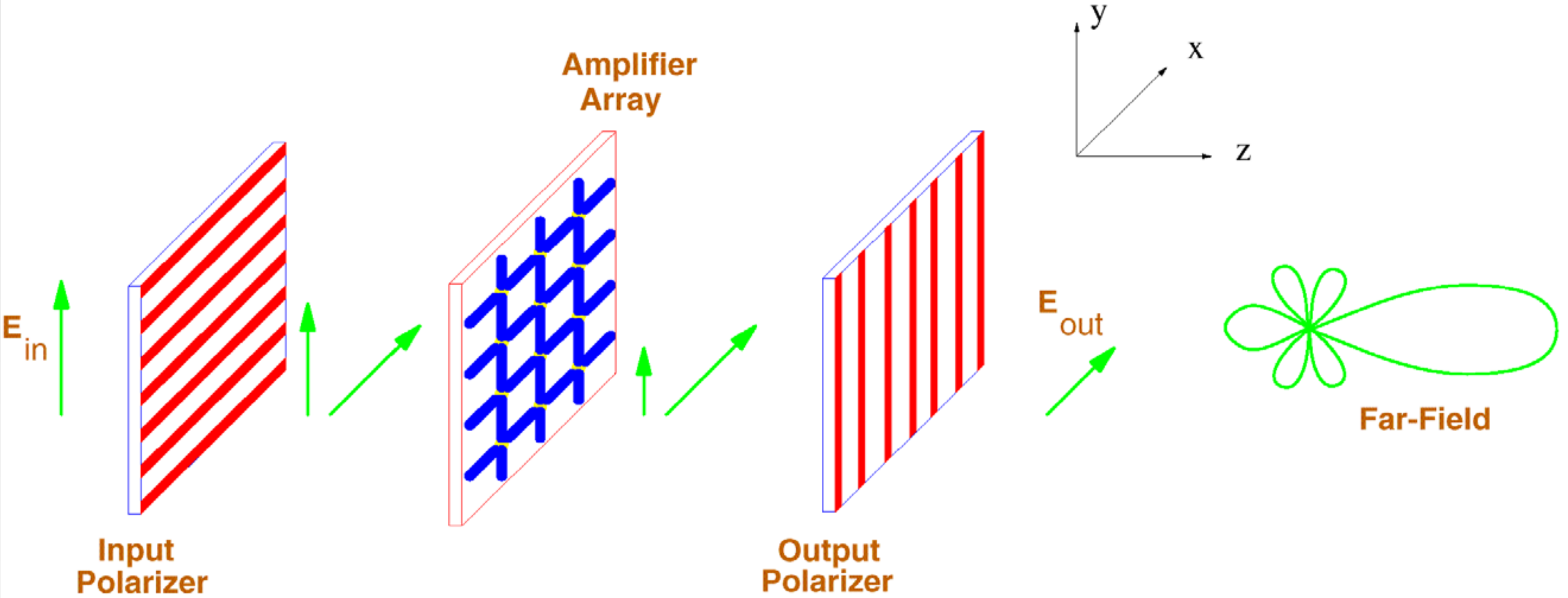
- *Generally There is Not a Common Reference Node*



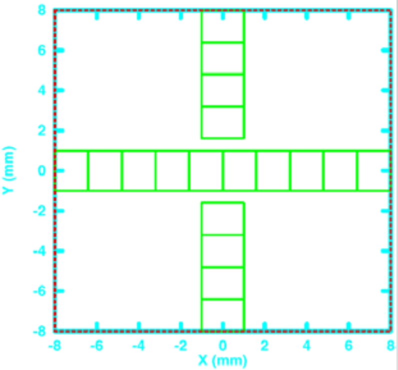
There is No Such Thing as a Node Voltage as Required in Current Microwave Circuit Simulators

- *Concerns Whenever Switching Between Domains*
- ***Time--Domain Frequency Domain Conversions: Aliasing etc.***
- *Electrically Large Distributed Structures*
- *Metrology (Model Verification)*
- *A Defined Metrology (Calibration/Measurement Procedure)*
- *Does Not Exist.*

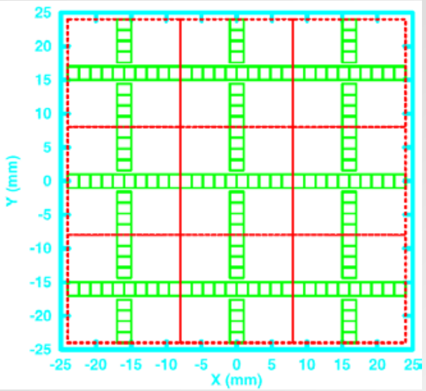
Grid Amplifier System



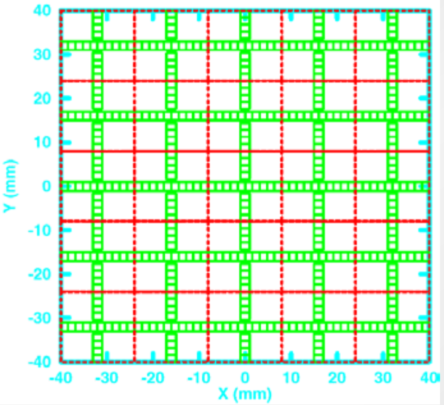
Near-Field Radiation



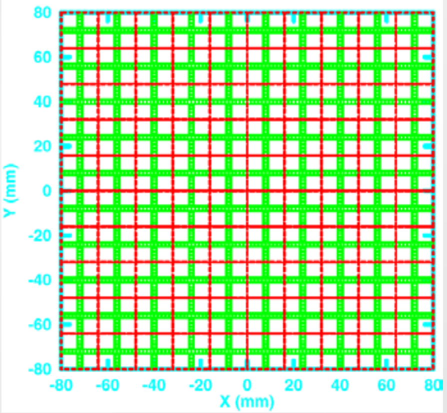
Unit Cell



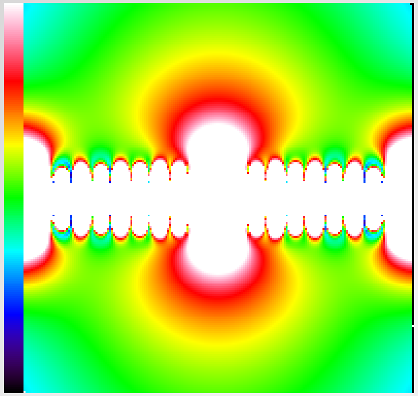
3x3 Grid

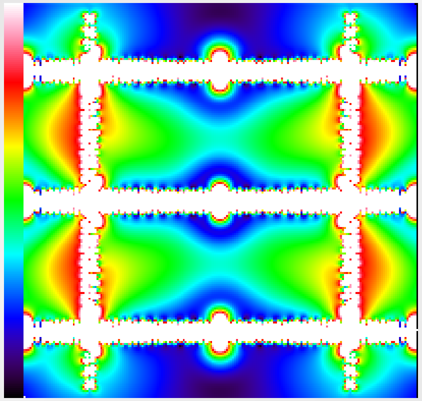


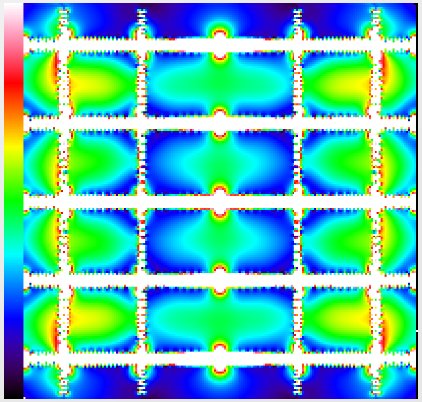
5x5 Grid

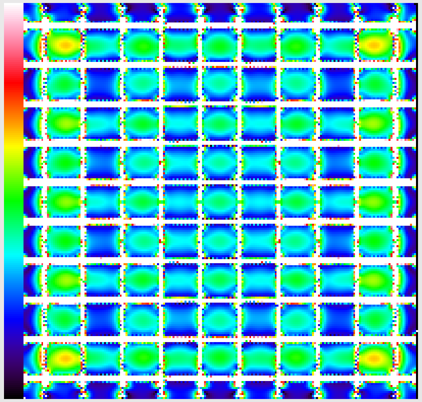


10x10 Grid



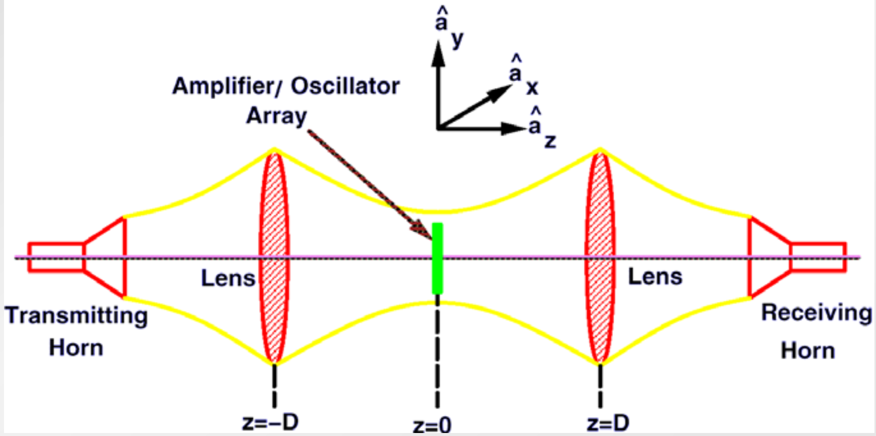






Electromagnetic Modeling of Quasi-Optical Systems

Interfacing Surfaces in Quasi-Optical Systems are Distributed Over Electrically Large Distances



3D Volume Discretization is Inefficient

2D Planar Discretization is Ideal

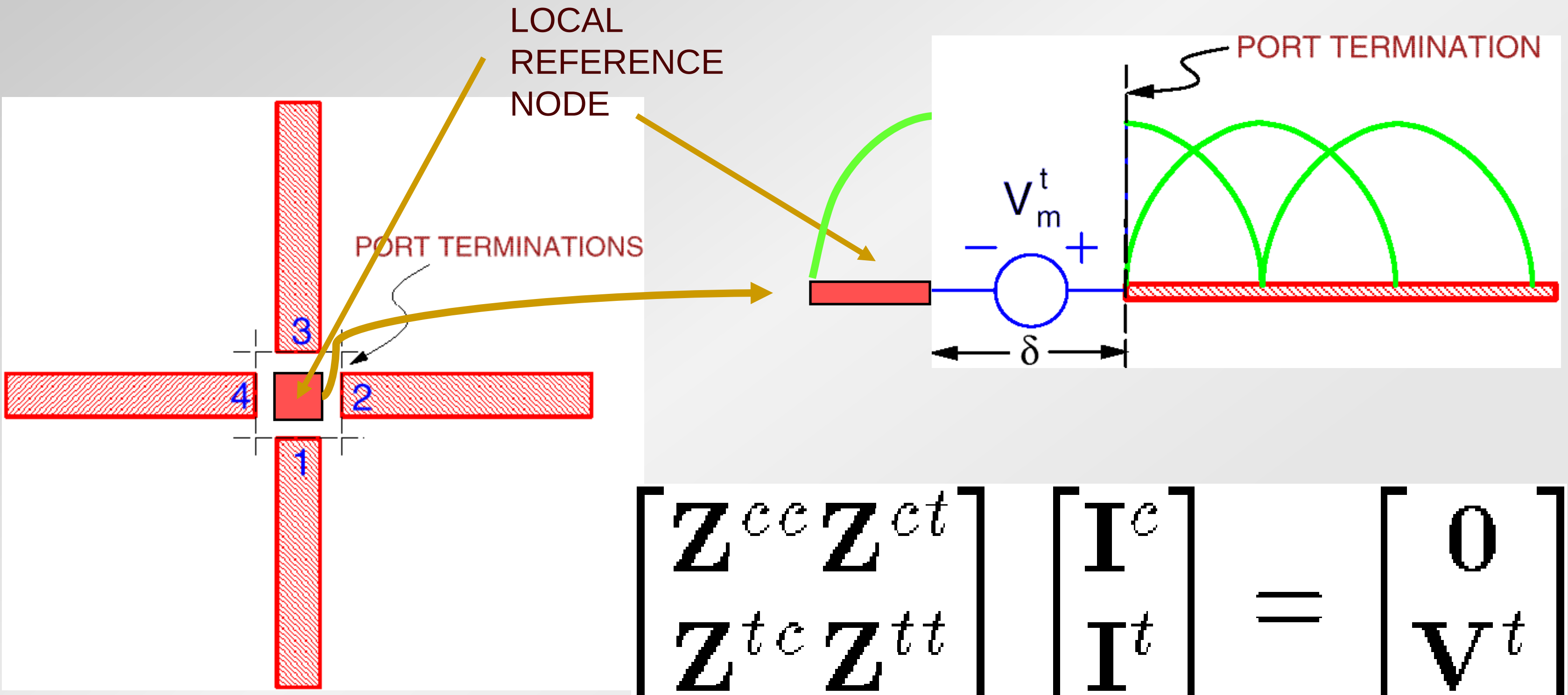
FEM and FDTD Methods Require 3D Volume Discretization
- Boundary Conditions Required on Volume Terminations
- Large Amounts of Memory and CPU Time Required

MoM Requires Only 2D Planar Discretization
- Green’s Functions Incorporate the Effects of Complete System
- Green’s Functions are Interchangeable for Modeling a Variety of Quasi-Optical System Configurations

Nodal Admittance Matrix Determination

Nodal Admittance Description Required in Microwave Circuit Simulators

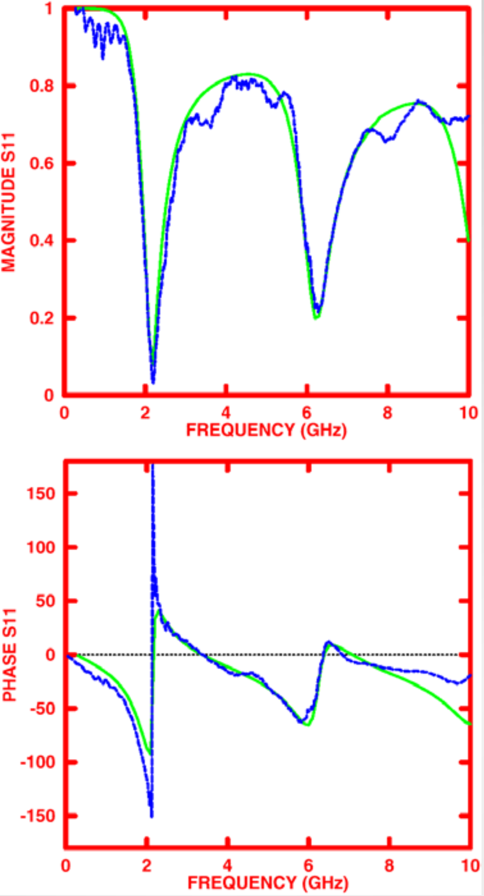
Process: Guess a node voltage and calculate node current.



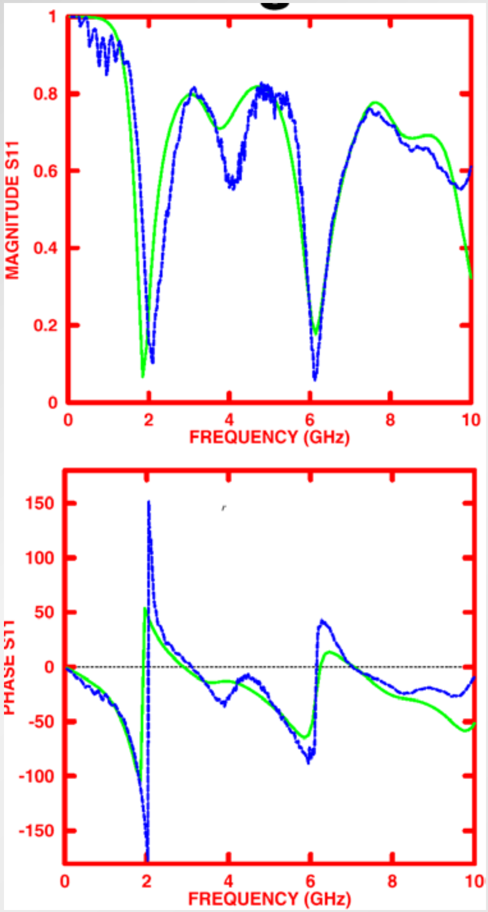
$$\begin{bmatrix} \mathbf{Z}^{cc} & \mathbf{Z}^{ct} \\ \mathbf{Z}^{tc} & \mathbf{Z}^{tt} \end{bmatrix} \begin{bmatrix} \mathbf{I}^{c} \\ \mathbf{I}^{t} \end{bmatrix} = \begin{bmatrix} \mathbf{0} \\ \mathbf{V}^{t} \end{bmatrix}$$

Input Reflection Coefficient

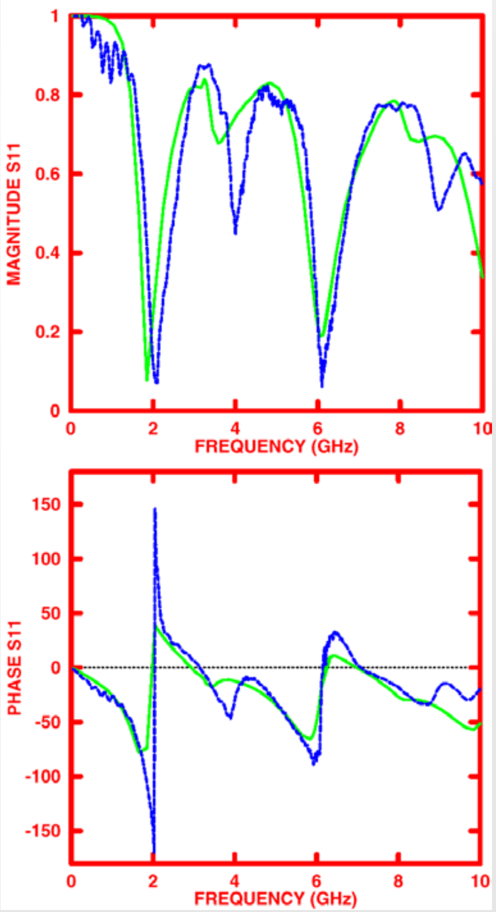
“unit cell”



3 X 3 grid



5 X 5 grid

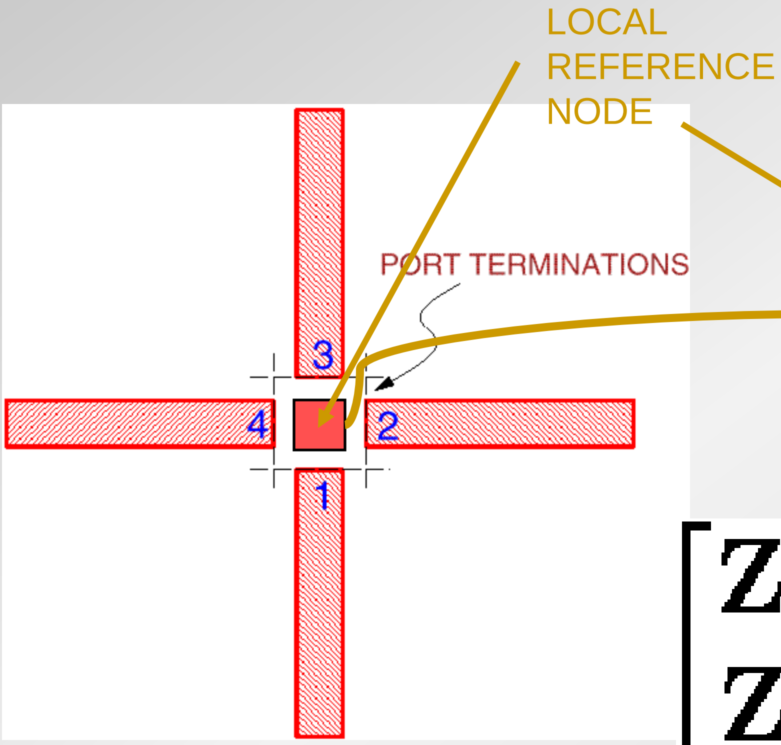


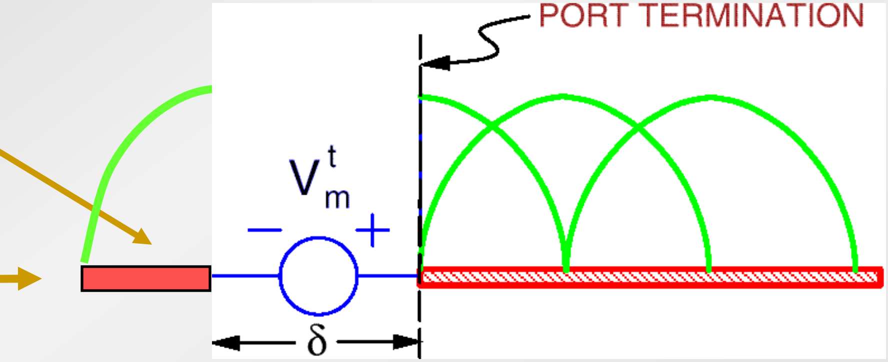
solid line: Circuit/MoM simulation dashed line: measurement

Nodal Admittance Matrix Determination

Nodal Admittance Description Required in Microwave Circuit Simulators

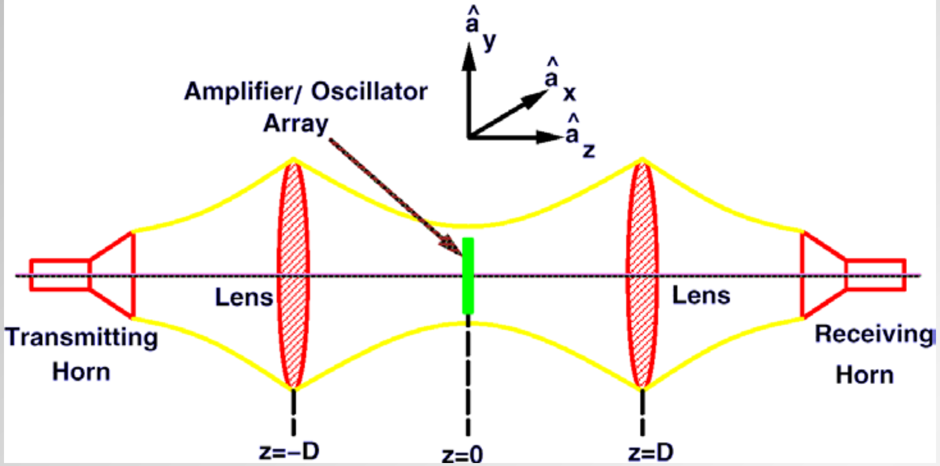
Process: Guess a node voltage and calculate node current.

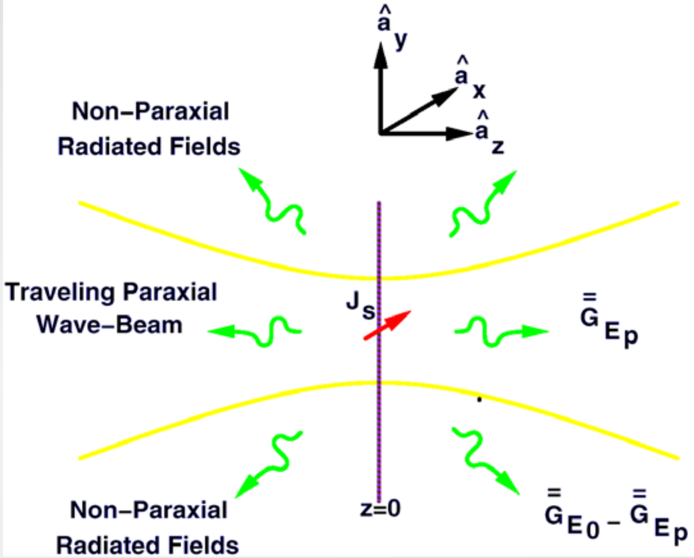




$$\begin{bmatrix} \mathbf{Z}^{cc} & \mathbf{Z}^{ct} \\ \mathbf{Z}^{tc} & \mathbf{Z}^{tt} \end{bmatrix} \begin{bmatrix} \mathbf{I}^{c} \\ \mathbf{I}^{t} \end{bmatrix} = \begin{bmatrix} \mathbf{0} \\ \mathbf{V}^{t} \end{bmatrix}$$

Development of a Quasi-Optical Green's Function





Green's Function Developed in Piece-wise Fashion

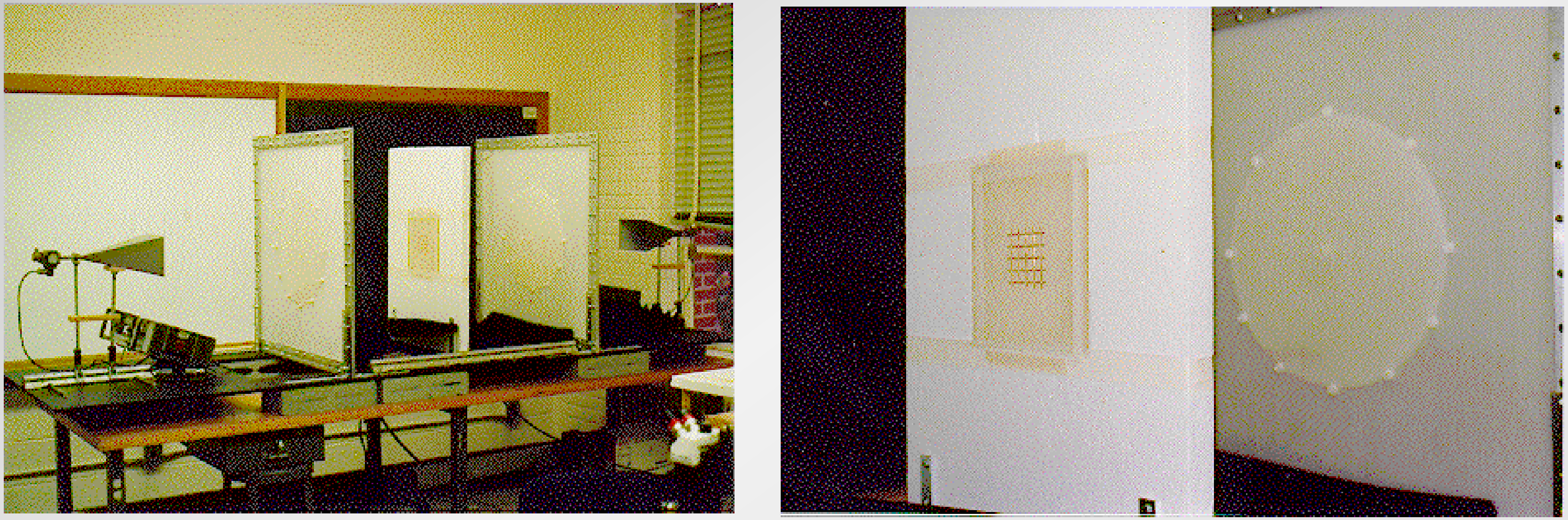
$$\overline{\overline{G}}_{E} = \overline{\overline{G}}_{Ef} + \overline{\overline{G}}_{EQO}$$

$\overline{\overline{G}}_{Ef} \Rightarrow$ free of any QO components

$\overline{\overline{G}}_{EQO} \Rightarrow$ **QO fields**

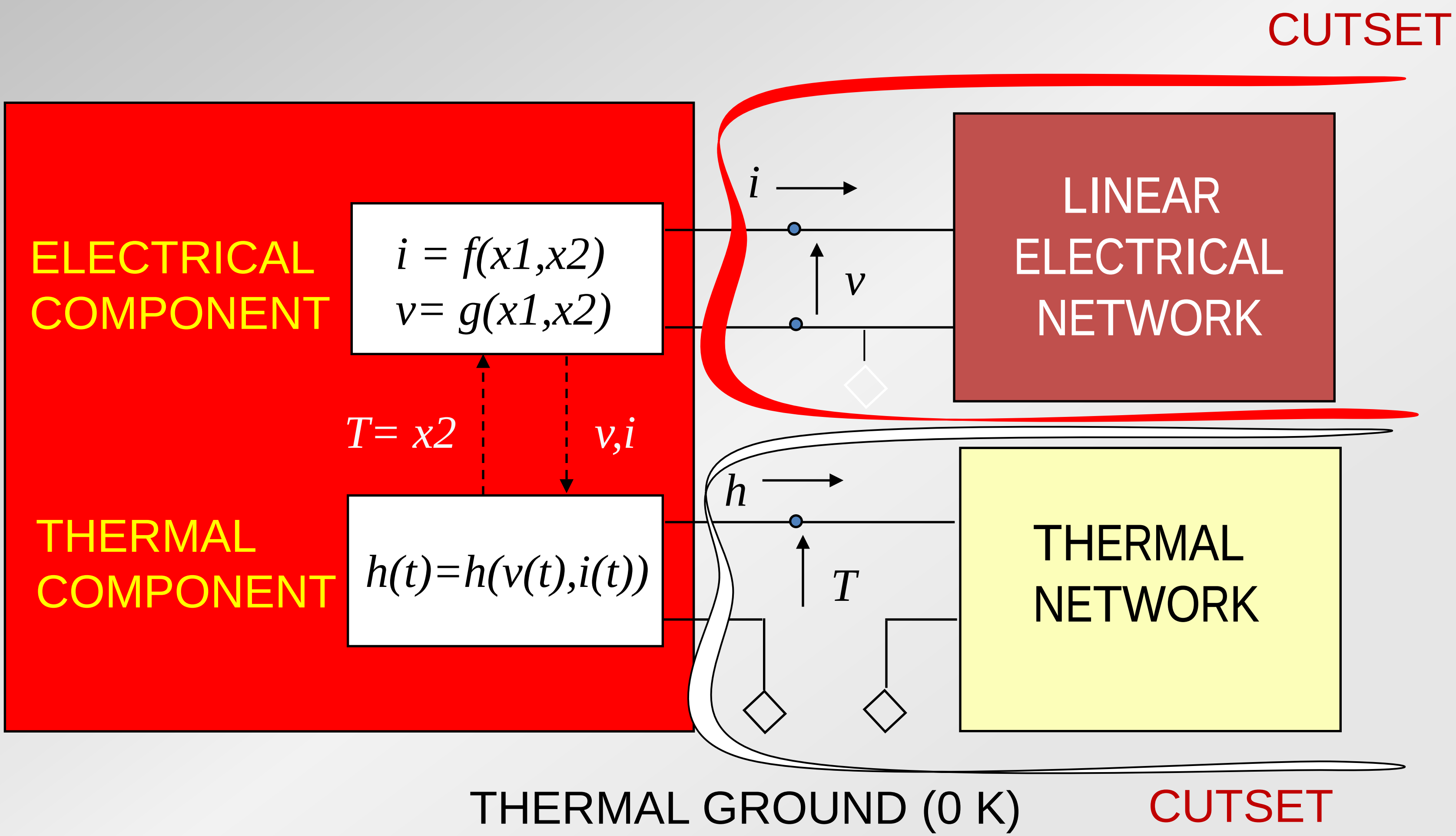
$\overline{\overline{G}}_{Em} \Rightarrow$ modal fields

Measurement Setup

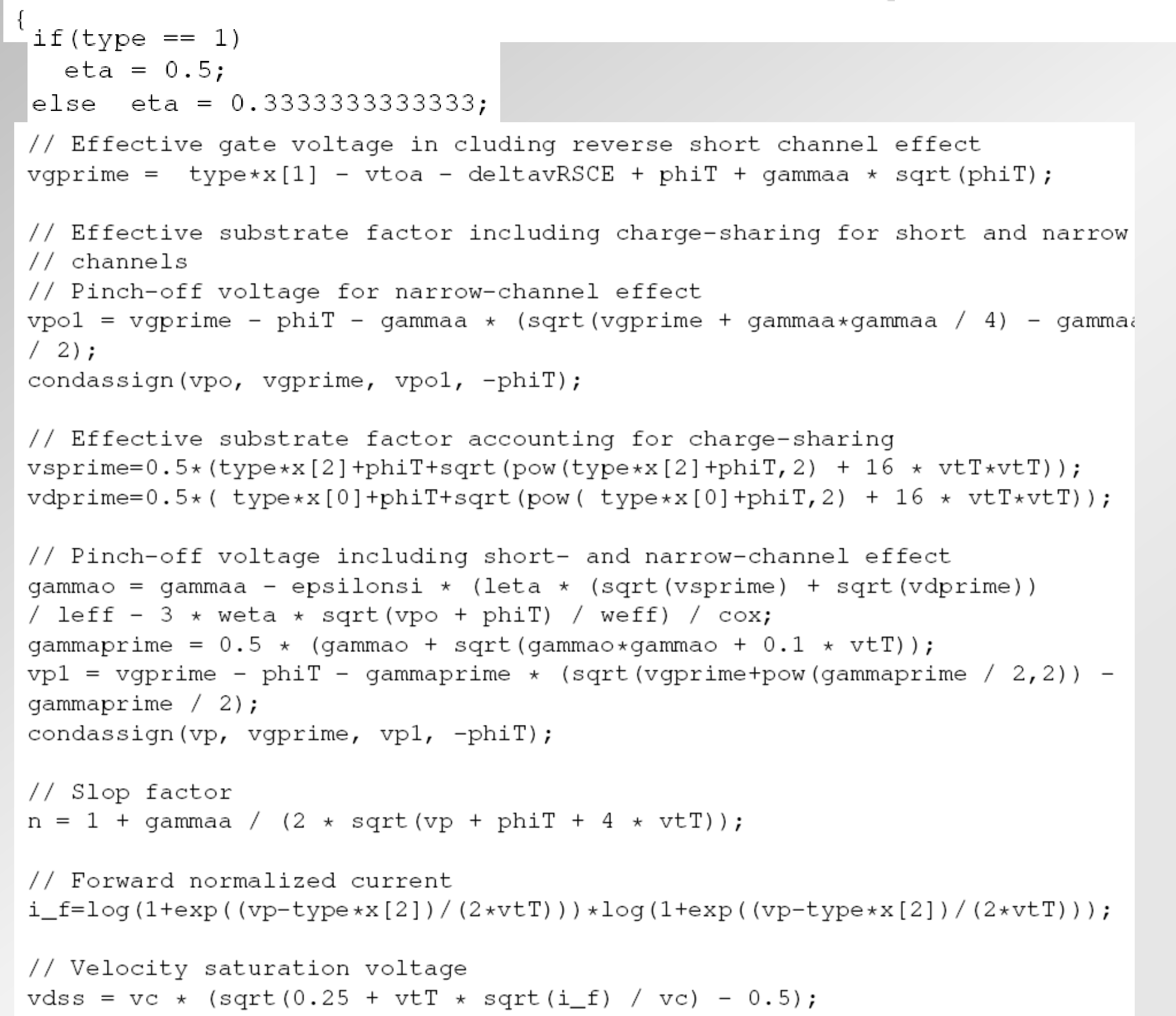


Transistor Model

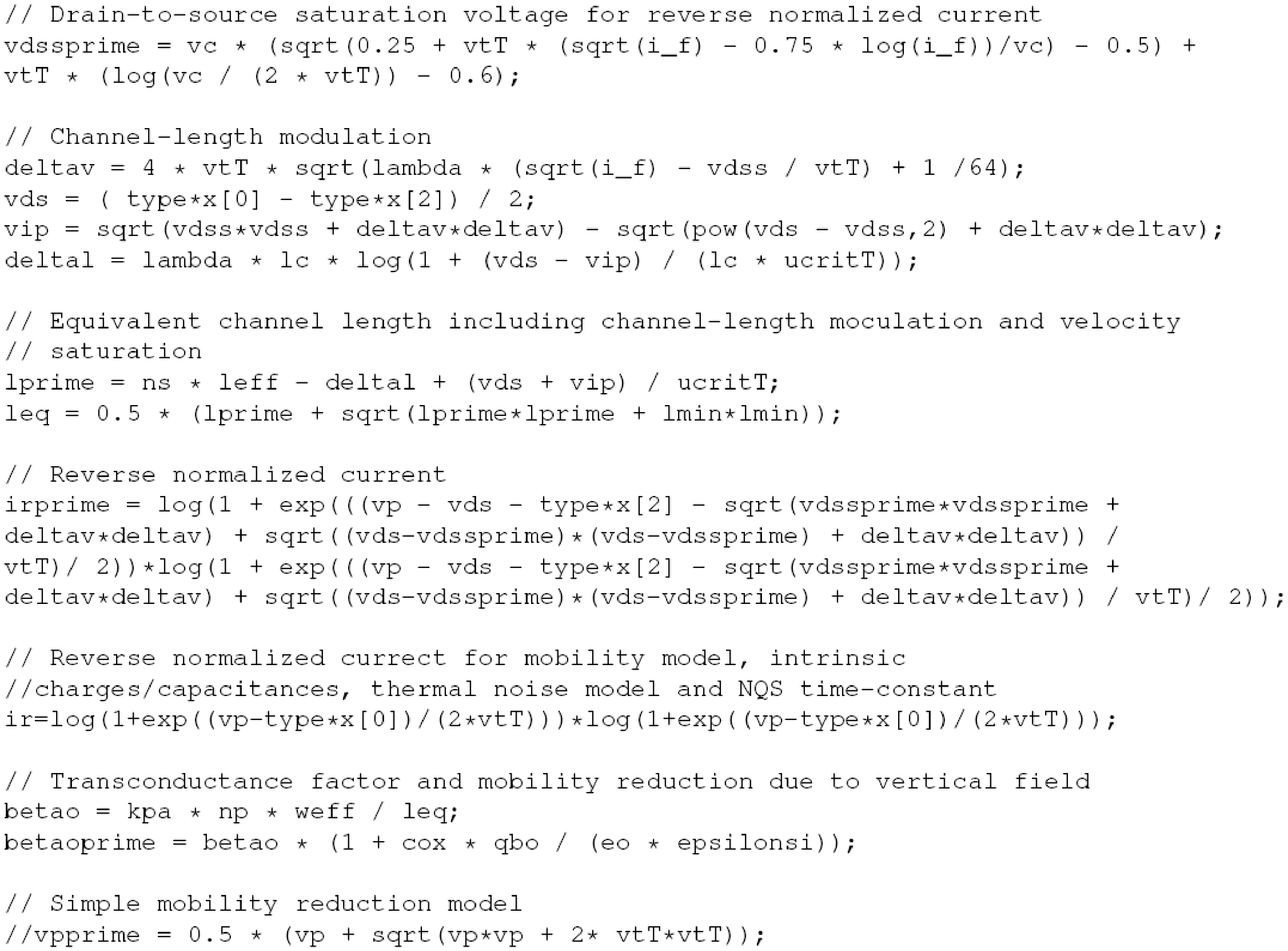
Nonlinear Electro-Thermal Element



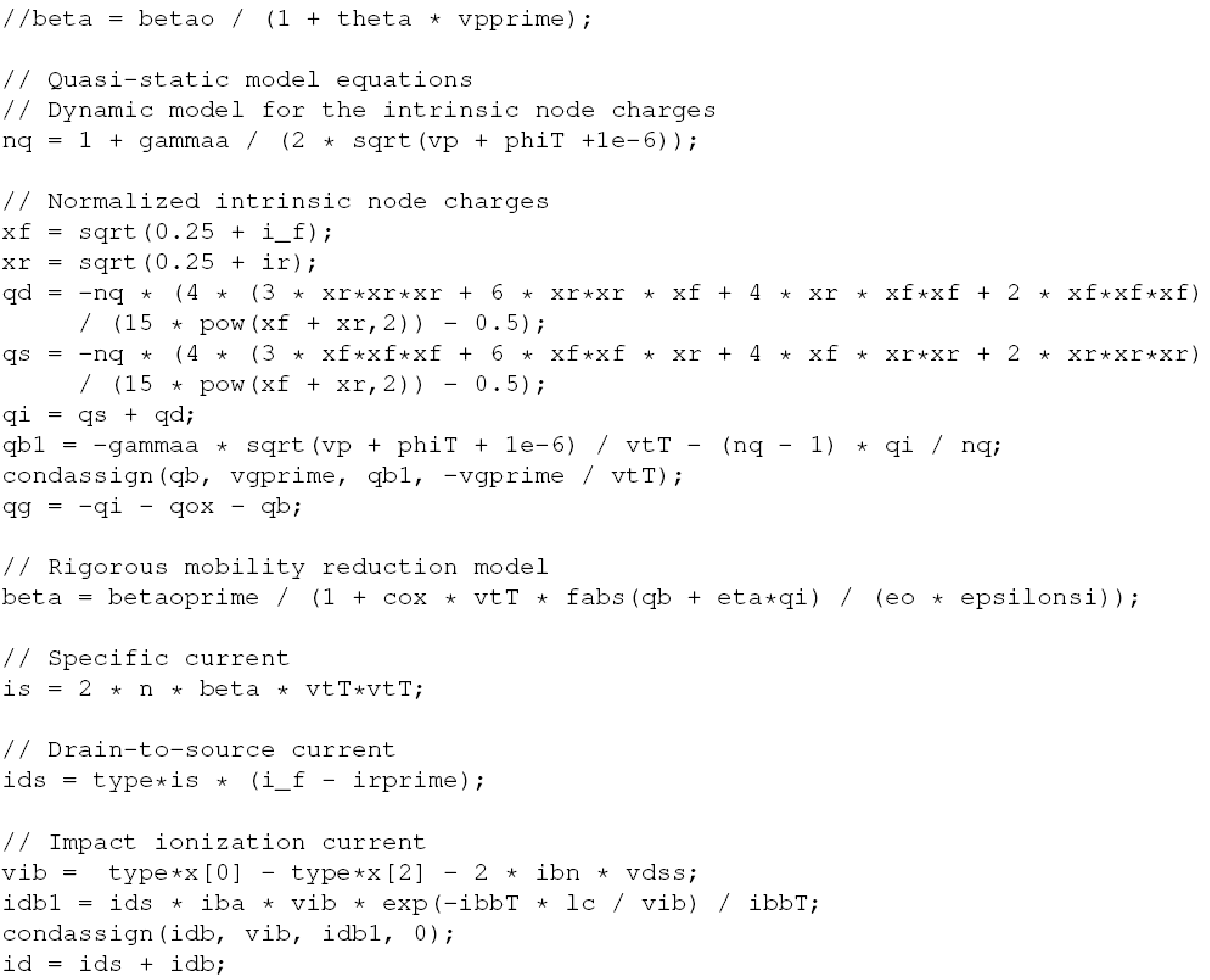
EKV Model (v2.6)



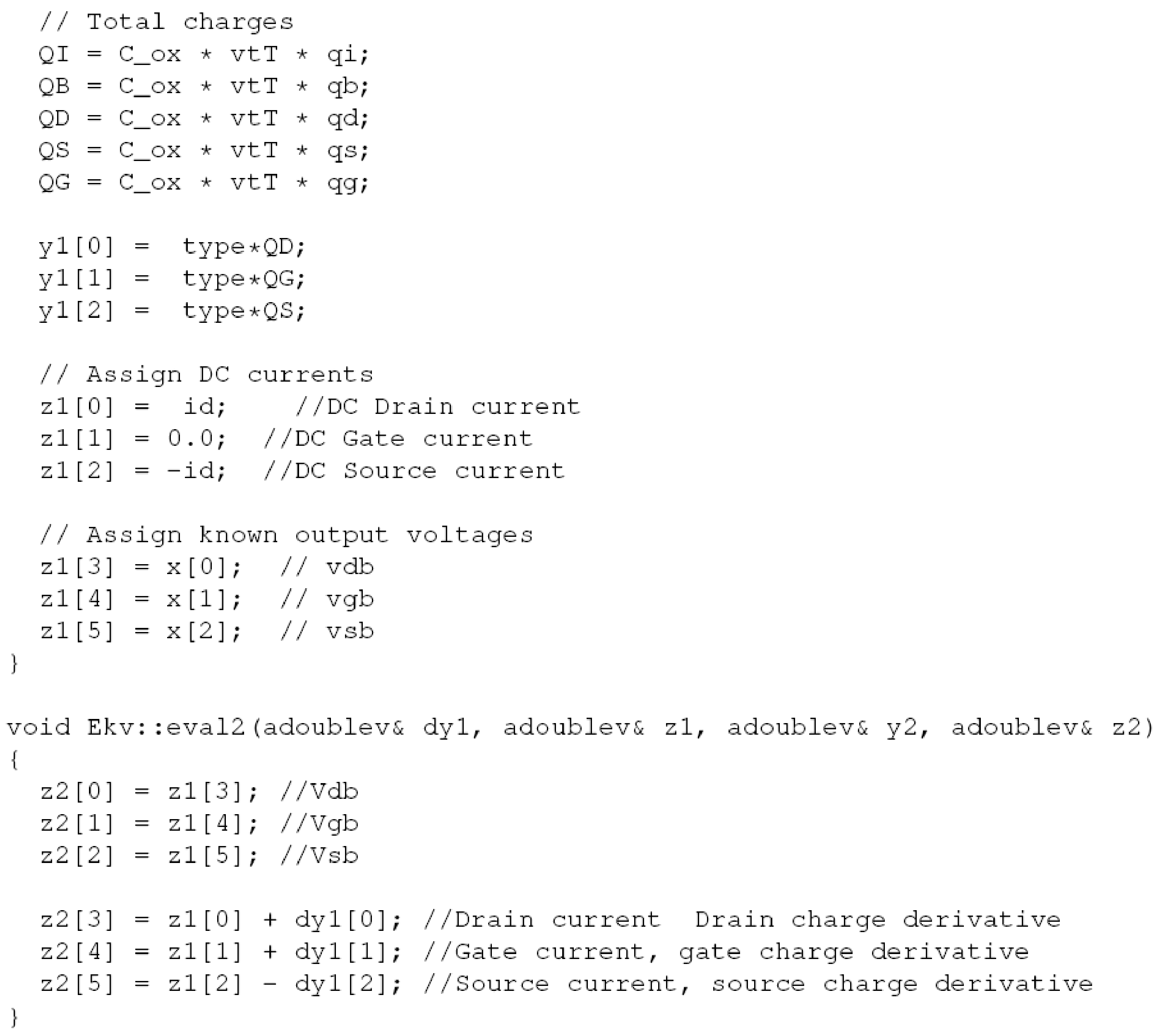
```
void Ekv::eval1(adoublev& x, adoublev& xt, adoublev& y1, adoublev& z1)
{
 if(type == 1)
   eta = 0.5;
 else  eta = 0.3333333333333;
// Effective gate voltage in cluding reverse short channel effect
vgprime =  type*x[1] - vtoa - deltavRSCE + phiT + gammaa * sqrt(phiT);

// Effective substrate factor including charge-sharing for short and narrow
// channels
// Pinch-off voltage for narrow-channel effect
vpo1 = vgprime - phiT - gammaa * (sqrt(vgprime + gammaa*gammaa / 4) - gammaa
/ 2);
condassign(vpo, vgprime, vpo1, -phiT);

// Effective substrate factor accounting for charge-sharing
vsprime=0.5*(type*x[2]+phiT+sqrt(pow(type*x[2]+phiT,2) + 16 * vtT*vtT));
vdprime=0.5*( type*x[0]+phiT+sqrt(pow( type*x[0]+phiT,2) + 16 * vtT*vtT));

// Pinch-off voltage including short- and narrow-channel effect
gammao = gammaa - epsilonsi * (leta * (sqrt(vsprime) + sqrt(vdprime))
/ leff - 3 * weta * sqrt(vpo + phiT) / weff) / cox;
gammaprime = 0.5 * (gammao + sqrt(gammao*gammao + 0.1 * vtT));
vp1 = vgprime - phiT - gammaprime * (sqrt(vgprime+pow(gammaprime / 2,2)) -
gammaprime / 2);
condassign(vp, vgprime, vp1, -phiT);

// Slop factor
n = 1 + gammaa / (2 * sqrt(vp + phiT + 4 * vtT));

// Forward normalized current
i_f=log(1+exp((vp-type*x[2])/(2*vtT)))*log(1+exp((vp-type*x[2])/(2*vtT)));

// Velocity saturation voltage
vdss = vc * (sqrt(0.25 + vtT * sqrt(i_f) / vc) - 0.5);
```



```
// Drain-to-source saturation voltage for reverse normalized current
vdssprime = vc * (sqrt(0.25 + vtT * (sqrt(i_f) - 0.75 * log(i_f))/vc) - 0.5) +
vtT * (log(vc / (2 * vtT)) - 0.6);

// Channel-length modulation
deltav = 4 * vtT * sqrt(lambda * (sqrt(i_f) - vdss / vtT) + 1 /64);
vds = ( type*x[0] - type*x[2]) / 2;
vip = sqrt(vdss*vdss + deltav*deltav) - sqrt(pow(vds - vdss,2) + deltav*deltav);
deltal = lambda * lc * log(1 + (vds - vip) / (lc * ucritT));

// Equivalent channel length including channel-length moculation and velocity
// saturation
lprime = ns * leff - deltal + (vds + vip) / ucritT;
leq = 0.5 * (lprime + sqrt(lprime*lprime + lmin*lmin));

// Reverse normalized current
irprime = log(1 + exp(((vp - vds - type*x[2] - sqrt(vdssprime*vdssprime +
deltav*deltav) + sqrt((vds-vdssprime)*(vds-vdssprime) + deltav*deltav)) /
vtT)/ 2))*log(1 + exp(((vp - vds - type*x[2] - sqrt(vdssprime*vdssprime +
deltav*deltav) + sqrt((vds-vdssprime)*(vds-vdssprime) + deltav*deltav)) / vtT)/ 2));

// Reverse normalized currect for mobility model, intrinsic
//charges/capacitances, thermal noise model and NQS time-constant
ir=log(1+exp((vp-type*x[0])/(2*vtT)))*log(1+exp((vp-type*x[0])/(2*vtT)));

// Transconductance factor and mobility reduction due to vertical field
betao = kpa * np * weff / leq;
betaoprime = betao * (1 + cox * qbo / (eo * epsilonsi));

// Simple mobility reduction model
//vpprime = 0.5 * (vp + sqrt(vp*vp + 2* vtT*vtT));
```

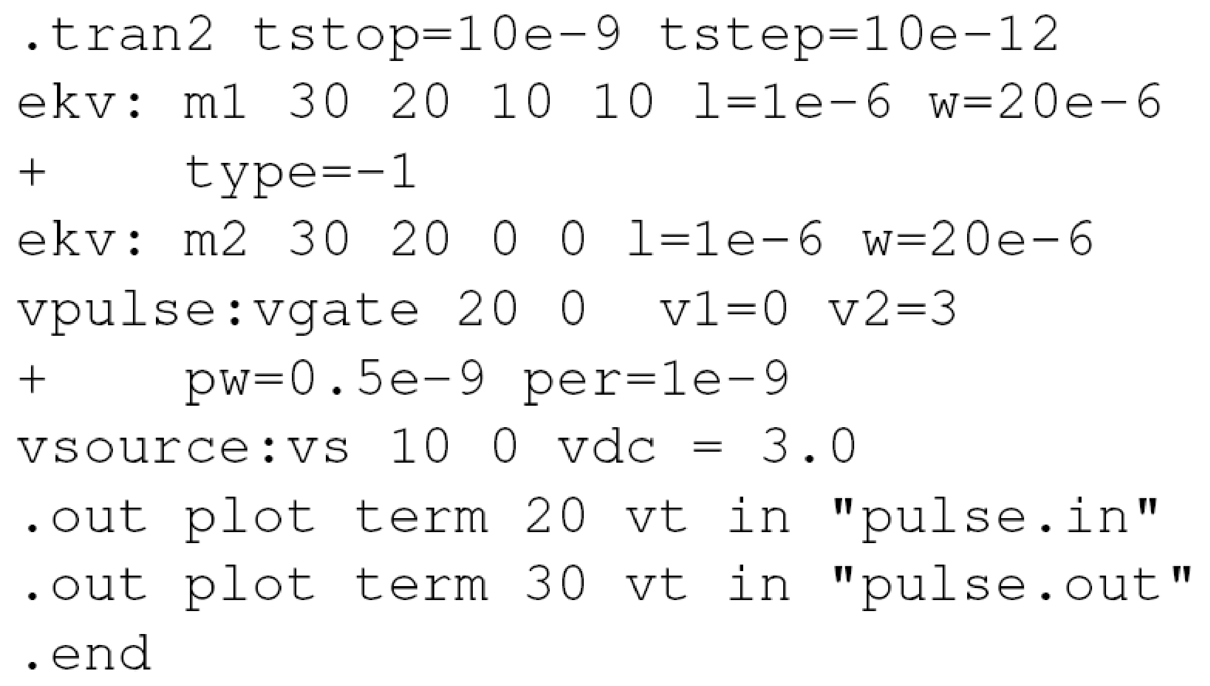


```
//beta = betao / (1 + theta * vpprime);

// Quasi-static model equations
// Dynamic model for the intrinsic node charges
nq = 1 + gammaa / (2 * sqrt(vp + phiT +1e-6));

// Normalized intrinsic node charges
xf = sqrt(0.25 + i_f);
xr = sqrt(0.25 + ir);
qd = -nq * (4 * (3 * xr*xr*xr + 6 * xr*xr * xf + 4 * xr * xf*xf + 2 * xf*xf*xf)
     / (15 * pow(xf + xr,2)) - 0.5);
qs = -nq * (4 * (3 * xf*xf*xf + 6 * xf*xf * xr + 4 * xf * xr*xr + 2 * xr*xr*xr)
     / (15 * pow(xf + xr,2)) - 0.5);
qi = qs + qd;
qb1 = -gammaa * sqrt(vp + phiT + 1e-6) / vtT - (nq - 1) * qi / nq;
condassign(qb, vgprime, qb1, -vgprime / vtT);
qg = -qi - qox - qb;

// Rigorous mobility reduction model
beta = betaoprime / (1 + cox * vtT * fabs(qb + eta*qi) / (eo * epsilonsi));

// Specific current
is = 2 * n * beta * vtT*vtT;

// Drain-to-source current
ids = type*is * (i_f - irprime);

// Impact ionization current
vib =  type*x[0] - type*x[2] - 2 * ibn * vdss;
idb1 = ids * iba * vib * exp(-ibbT * lc / vib) / ibbT;
condassign(idb, vib, idb1, 0);
id = ids + idb;
```



```
  // Total charges
  QI = C_ox * vtT * qi;
  QB = C_ox * vtT * qb;
  QD = C_ox * vtT * qd;
  QS = C_ox * vtT * qs;
  QG = C_ox * vtT * qg;

  y1[0] =  type*QD;
  y1[1] =  type*QG;
  y1[2] =  type*QS;

  // Assign DC currents
  z1[0] =  id;    //DC Drain current
  z1[1] = 0.0;  //DC Gate current
  z1[2] = -id;  //DC Source current

  // Assign known output voltages
  z1[3] = x[0];  // vdb
  z1[4] = x[1];  // vgb
  z1[5] = x[2];  // vsb
}

void Ekv::eval2(adoublev& dy1, adoublev& z1, adoublev& y2, adoublev& z2)
{
  z2[0] = z1[3]; //Vdb
  z2[1] = z1[4]; //Vgb
  z2[2] = z1[5]; //Vsb

  z2[3] = z1[0] + dy1[0]; //Drain current  Drain charge derivative
  z2[4] = z1[1] + dy1[1]; //Gate current, gate charge derivative
  z2[5] = z1[2] - dy1[2]; //Source current, source charge derivative
}
```

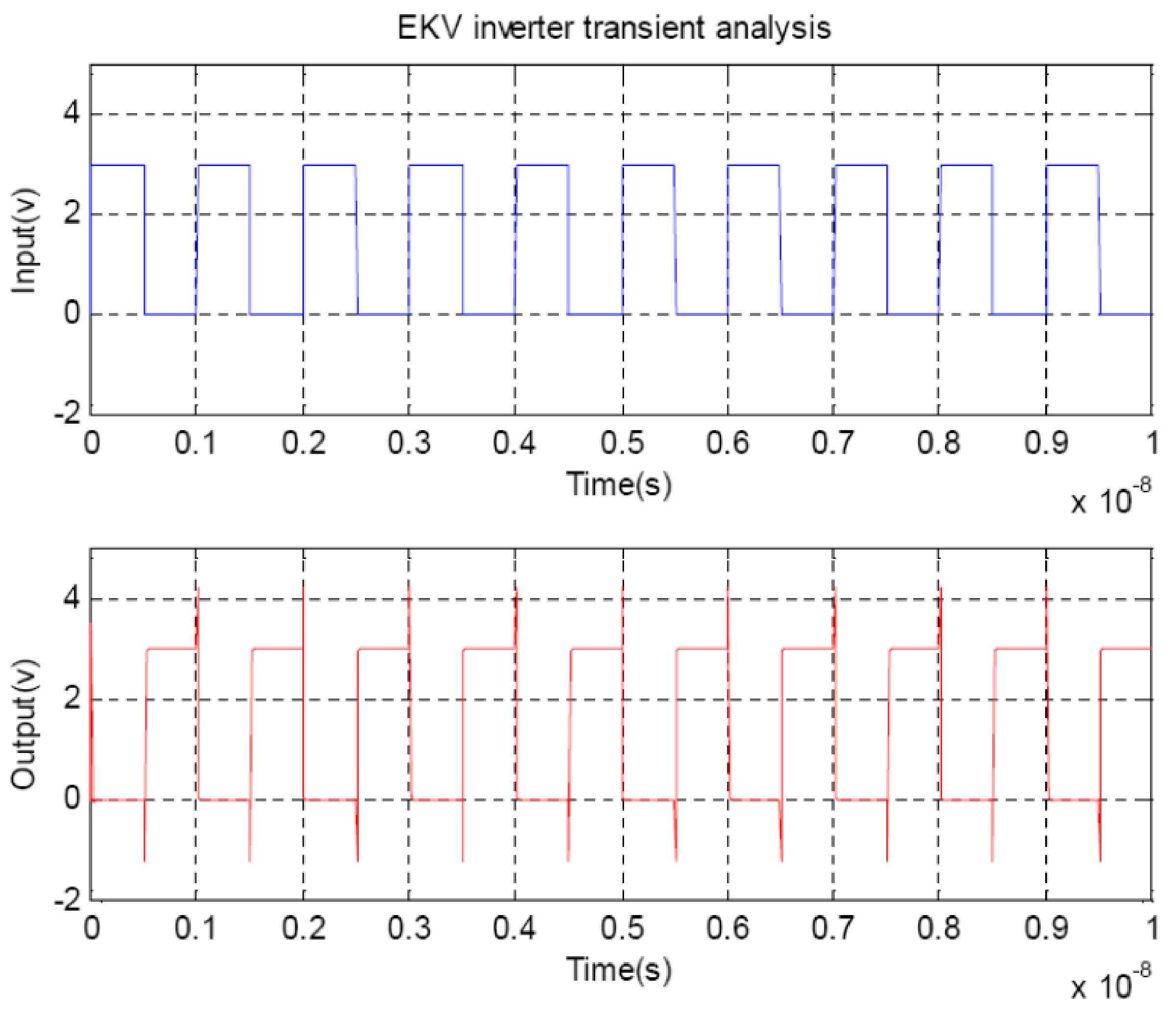
Inverter in fREEDA netlist



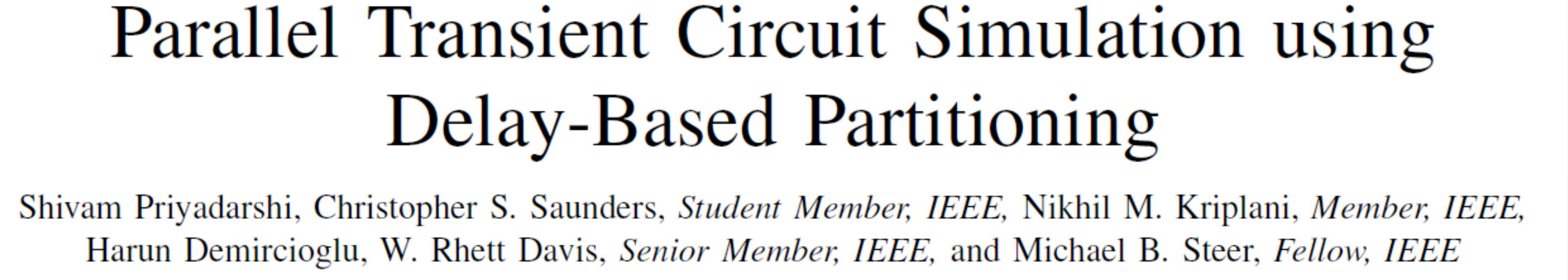
```
.tran2 tstop=10e-9 tstep=10e-12
ekv: m1 30 20 10 10 l=1e-6 w=20e-6
+    type=-1
ekv: m2 30 20 0 0 l=1e-6 w=20e-6
vpulse:vgate 20 0  v1=0 v2=3
+    pw=0.5e-9 per=1e-9
vsource:vs 10 0 vdc = 3.0
.out plot term 20 vt in "pulse.in"
.out plot term 30 vt in "pulse.out"
.end
```

Also read SPICE netlist (can be mixed with fREEDA native netlist.)

EKV 2.6 Model

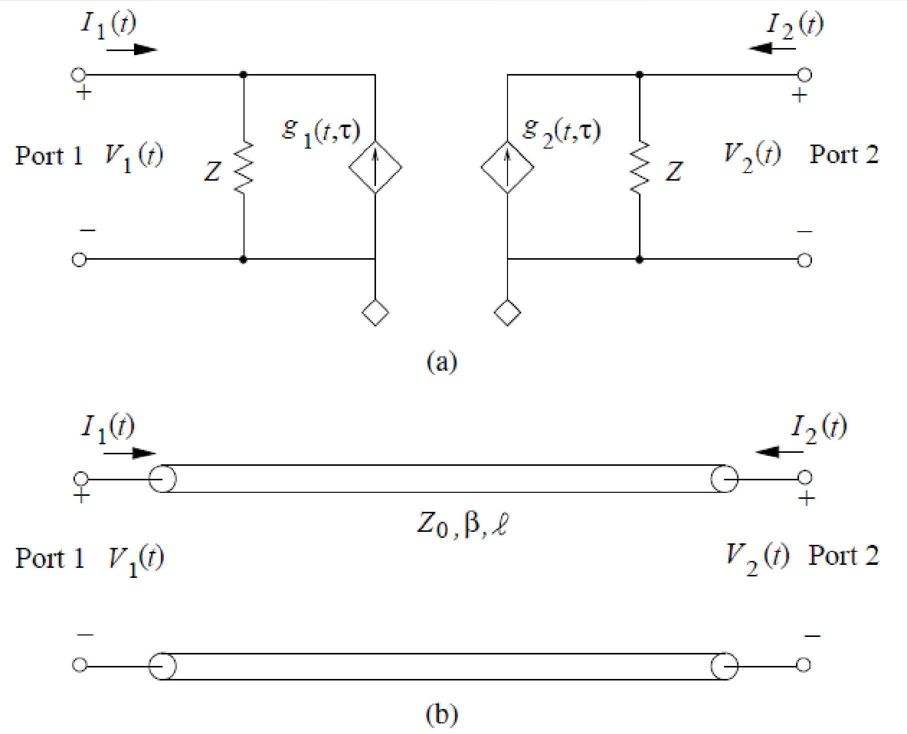

EKV inverter transient analysis
Input(v)
4
2
0
-2
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Time(s)
x 10-8
Output(v)
4
2
0
-2
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Time(s)
x 10-8

Parallelization

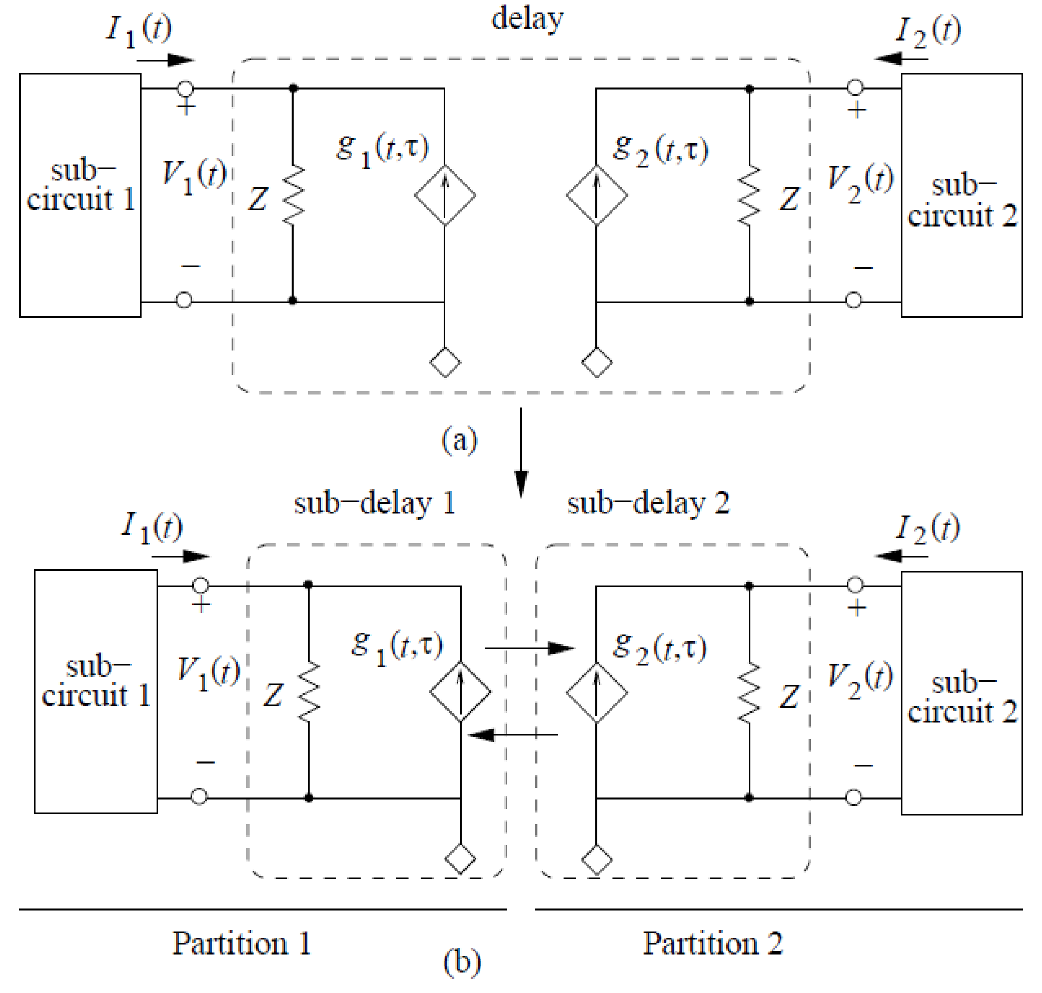


Parallel Transient Circuit Simulation using Delay-Based Partitioning

Shivam Priyadarshi, Christopher S. Saunders, *Student Member, IEEE,* Nikhil M. Kriplani, *Member, IEEE,*
Harun Demircioglu, W. Rhett Davis, *Senior Member, IEEE,* and Michael B. Steer, *Fellow, IEEE*

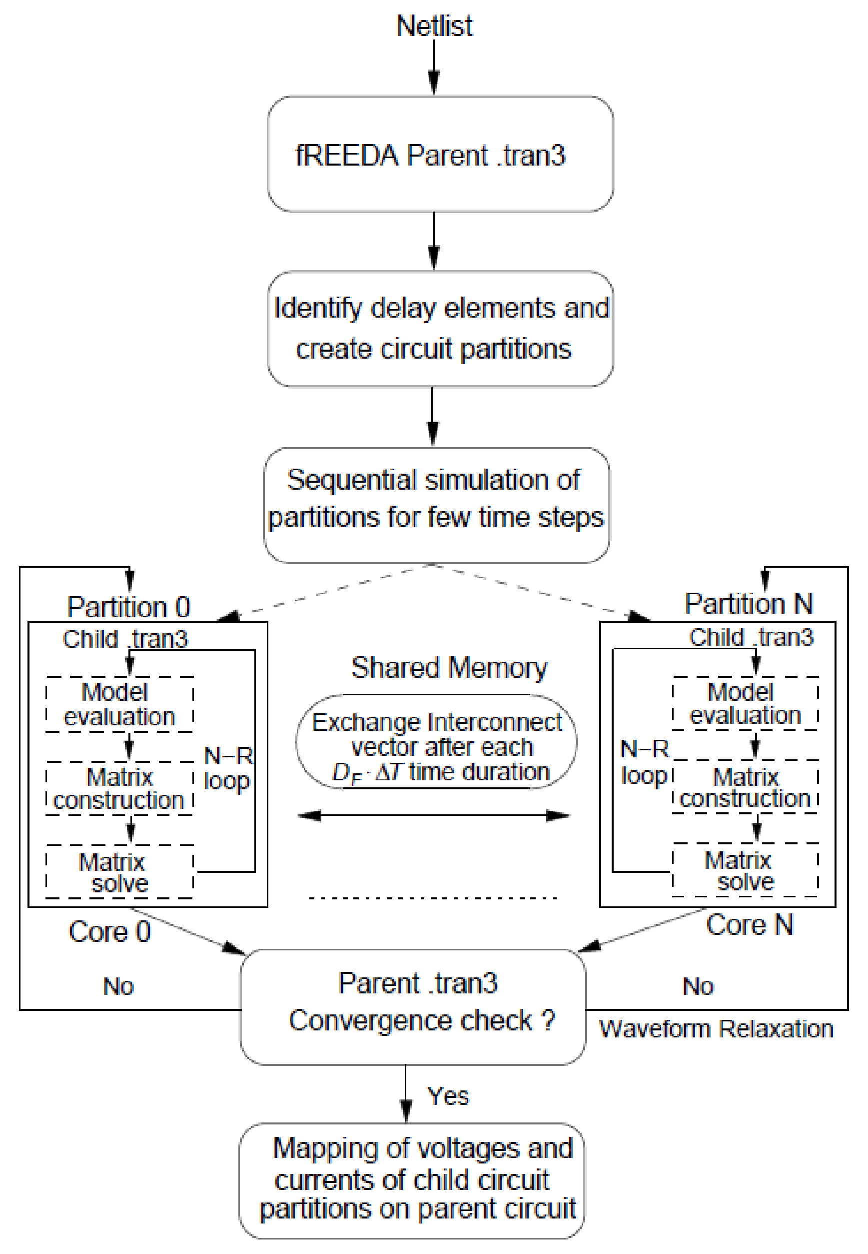


Splitting Delay Element



Splitting one delay element, (a), into two sub-delay elements, (b), showing the delay element with two local reference terminals.

Flow



Netlist

fREEDA Parent .tran3

Identify delay elements and create circuit partitions

Sequential simulation of partitions for few time steps

Partition 0

Child .tran3

Model evaluation

Matrix construction

Matrix solve

N−R loop

Core 0

No

Shared Memory

Exchange Interconnect vector after each $D_F \cdot \Delta T$ time duration

Partition N

Child .tran3

Model evaluation

Matrix construction

Matrix solve

N−R loop

Core N

No

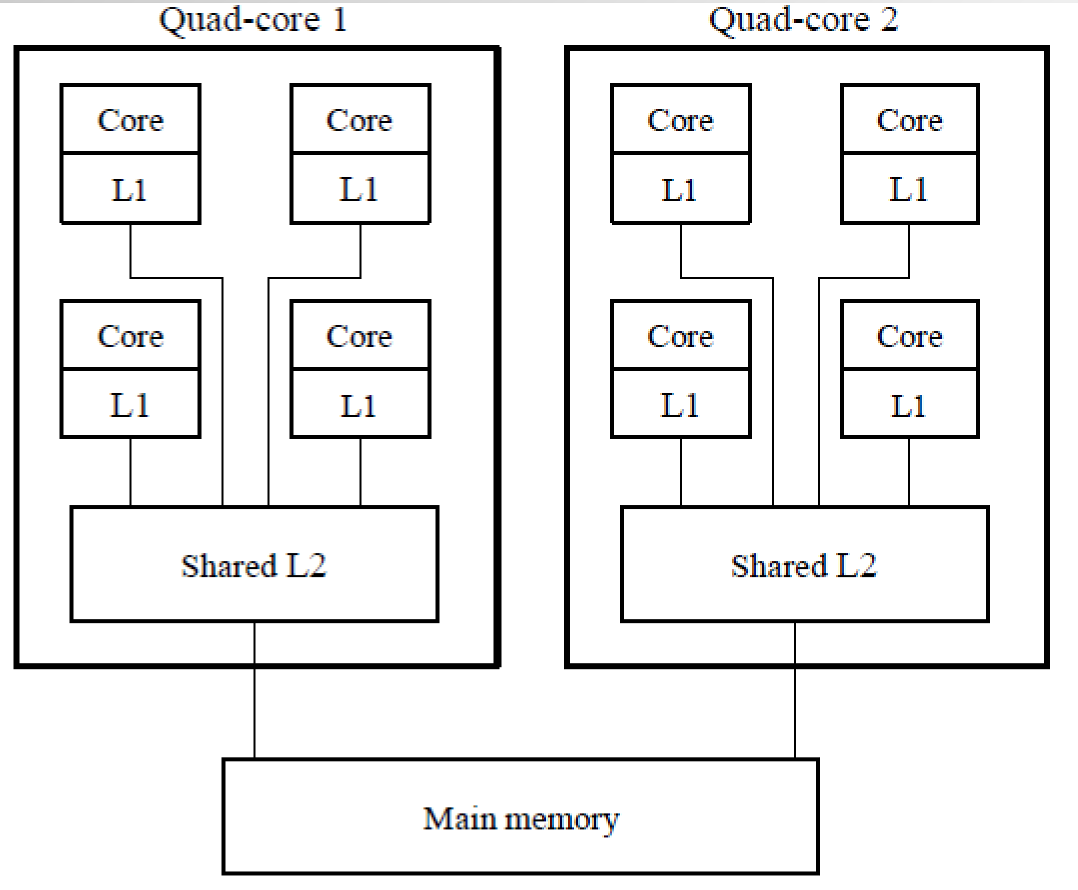
Parent .tran3 Convergence check ?

Waveform Relaxation

Yes

Mapping of voltages and currents of child circuit partitions on parent circuit

Multi-Processor Implementation



Multiprocessor Implementation

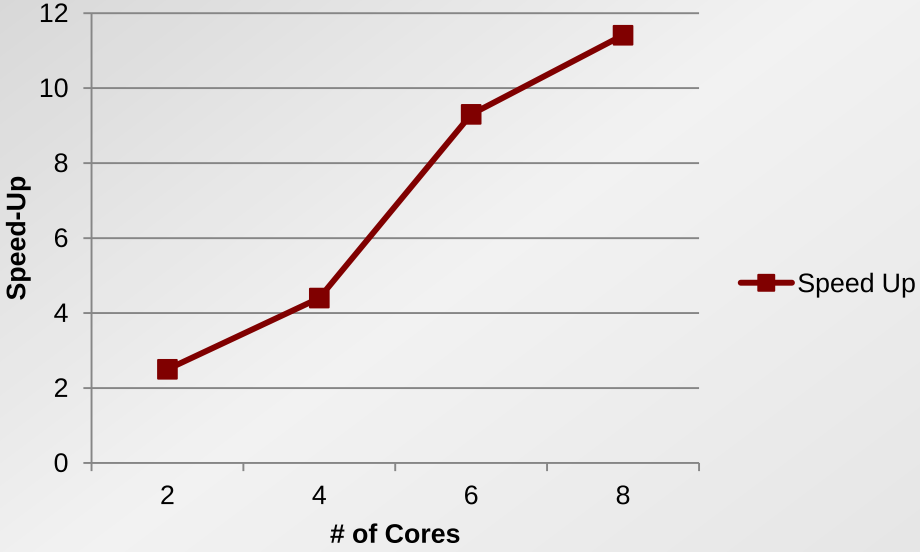
fREEDA Parallelization

Divider Circuit

Chain of 12 Dividers

Number of Non Linear State Variable (ns) : 1238

Number of Linear Element (nm): 229



On a single core most time 68% is in model evaluation. Matrix solve is 11% of the simulation time.

Circuit is partitioned at Delay Elements

Super Linear Speed Up

Load factors (on 4 core) (3-3-3-3)

Load factors (on 6 core) (2-2-2-2-2-2)

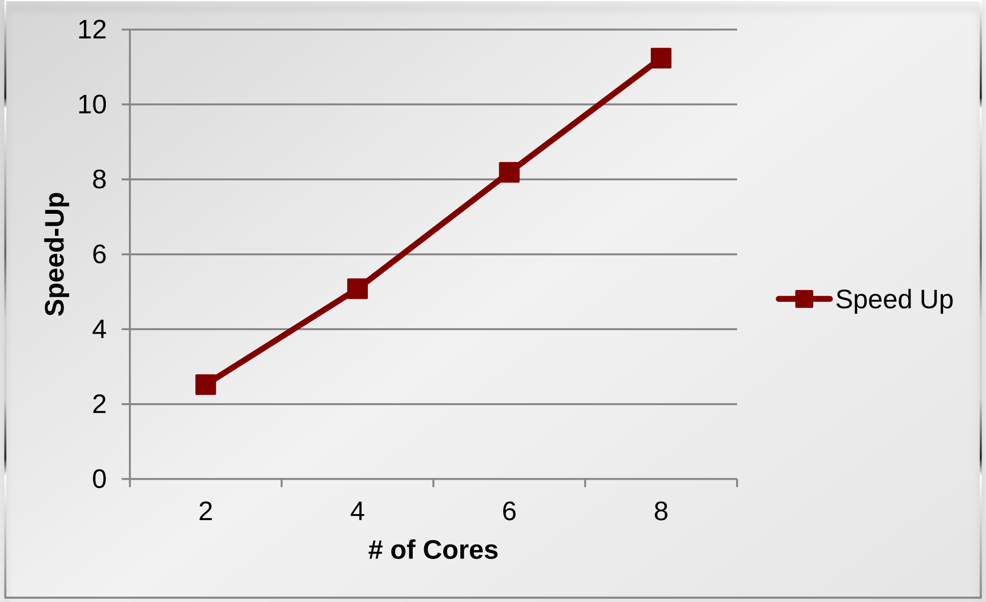
Load factors (on 8 core) (2-2-2-2-1-1-1-1)

fREEDA Parallelization

20-bit Adder

Number of Non Linear State Variable (ns) : 2174

Number of Linear Element (nm): 465

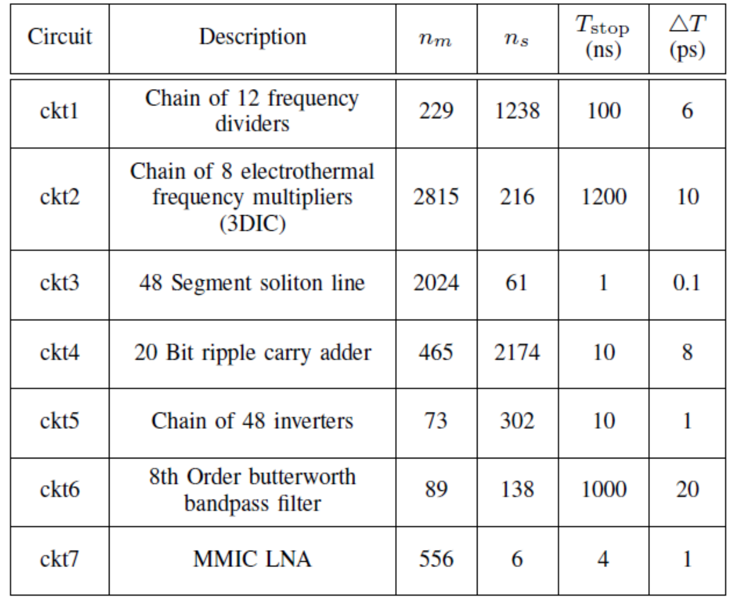


On a single core 54.8% of the time is in model evaluation. Matrix solve is 0.85% of the simulation time.

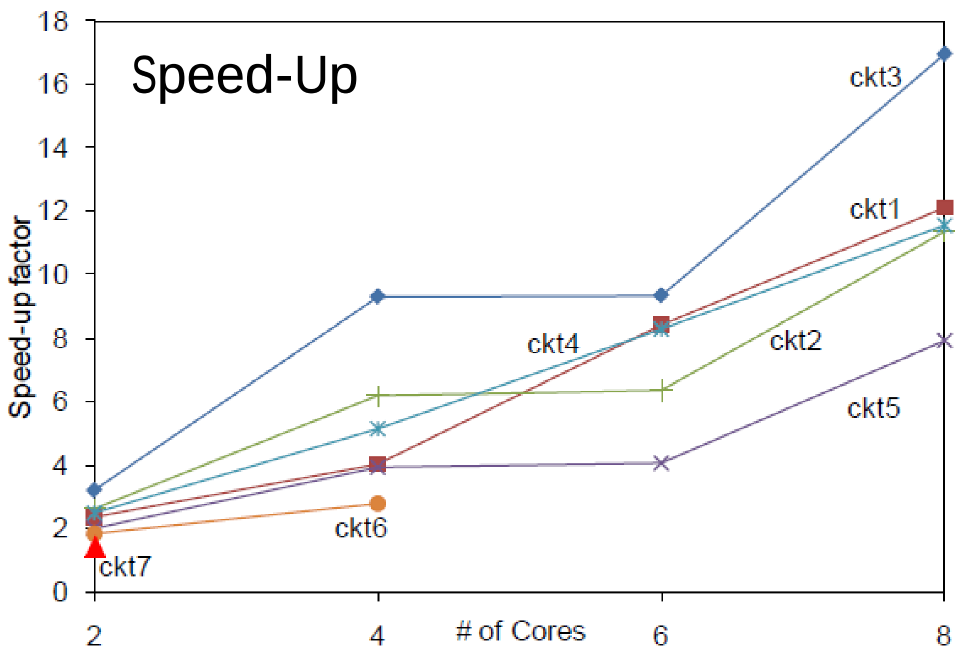
Circuit is partitioned at Delay Elements

Super Linear Speed Up

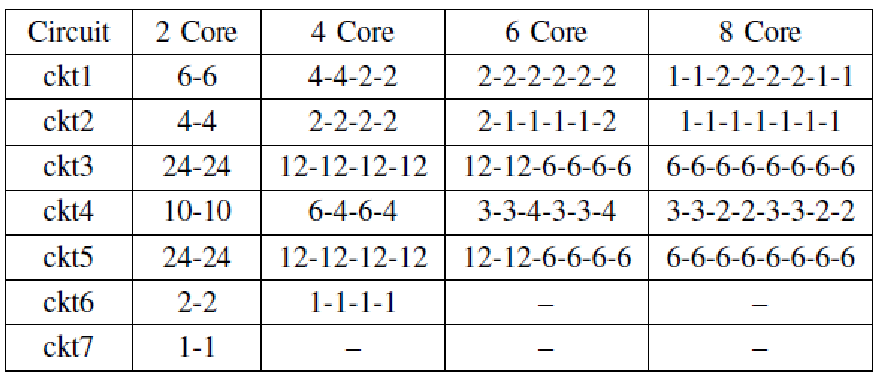
Speed-Up



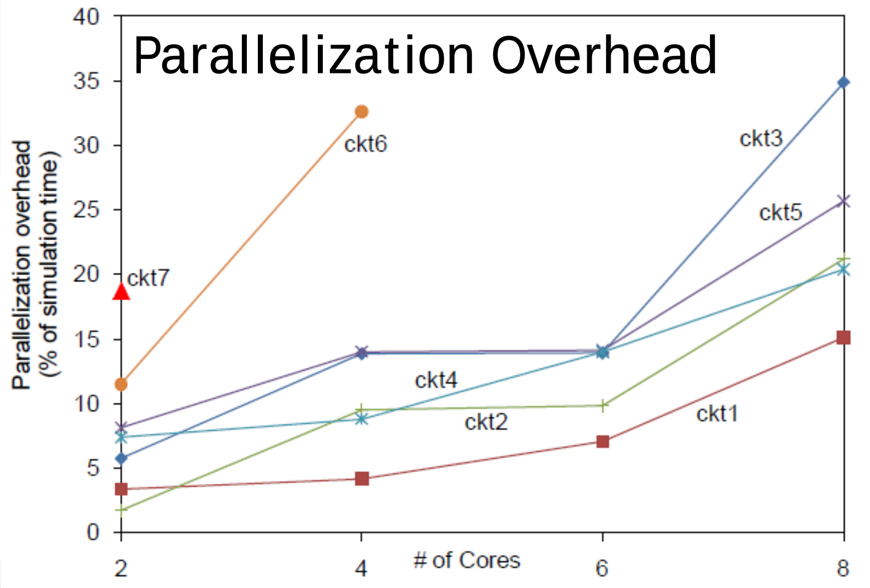
Circuit	Description	n_m	n_s	T_{stop} (ns)	$\triangle T$ (ps)
ckt1	Chain of 12 frequency dividers	229	1238	100	6
ckt2	Chain of 8 electrothermal frequency multipliers (3DIC)	2815	216	1200	10
ckt3	48 Segment soliton line	2024	61	1	0.1
ckt4	20 Bit ripple carry adder	465	2174	10	8
ckt5	Chain of 48 inverters	73	302	10	1
ckt6	8th Order butterworth bandpass filter	89	138	1000	20
ckt7	MMIC LNA	556	6	4	1



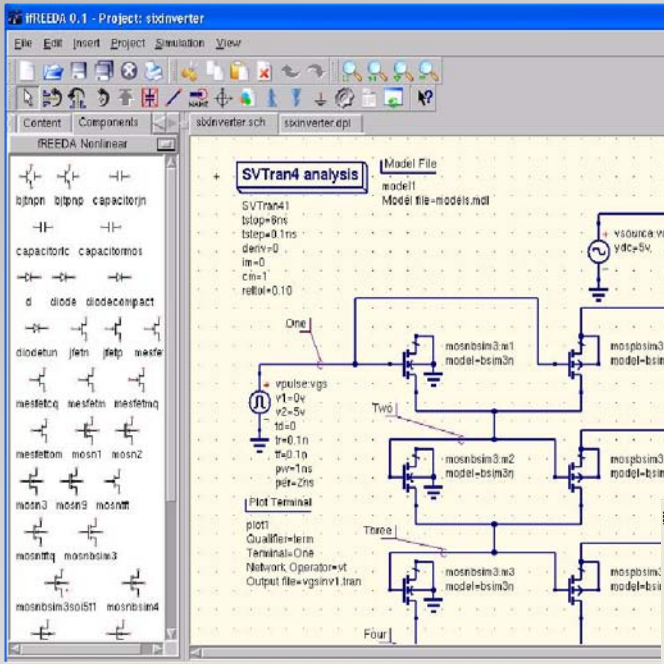
WORKLOAD DISTRIBUTION ACROSS THE CORES



Circuit	2 Core	4 Core	6 Core	8 Core
ckt1	6-6	4-4-2-2	2-2-2-2-2-2	1-1-2-2-2-2-1-1
ckt2	4-4	2-2-2-2	2-1-1-1-1-2	1-1-1-1-1-1-1-1
ckt3	24-24	12-12-12-12	12-12-6-6-6-6	6-6-6-6-6-6-6-6
ckt4	10-10	6-4-6-4	3-3-4-3-3-4	3-3-2-2-3-3-2-2
ckt5	24-24	12-12-12-12	12-12-6-6-6-6	6-6-6-6-6-6-6-6
ckt6	2-2	1-1-1-1	–	–
ckt7	1-1	–	–	–



fREEDA and REMCOM’s xFDTD



SVTran4 analysis
SVTran41
tstop=8ns
tstep=0.1ns
deriv=0
im=0
cm=1
reltol=0.10

Model File
model1
Model file=models.mdl

vsource:vdd
vdc=5V

vpulse:vgs
v1=0v
v2=5v
td=0
tr=0.1n
tf=0.1n
pw=1ns
per=2ns

mosnbsim3:m1
model=bsim3n

mospbsim3:m1
model=bsim3p

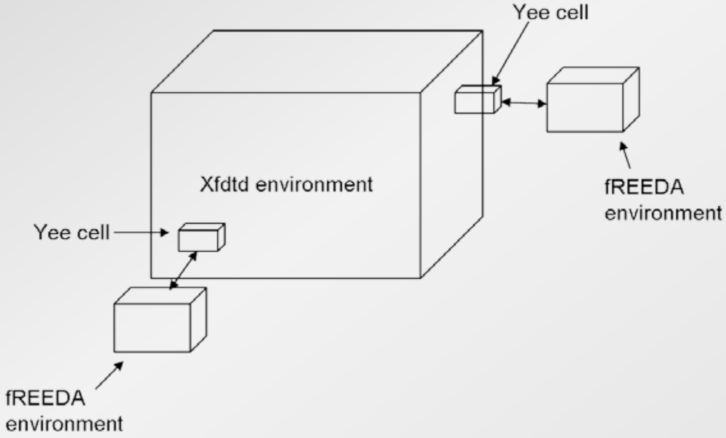
mosnbsim3:m2
model=bsim3n

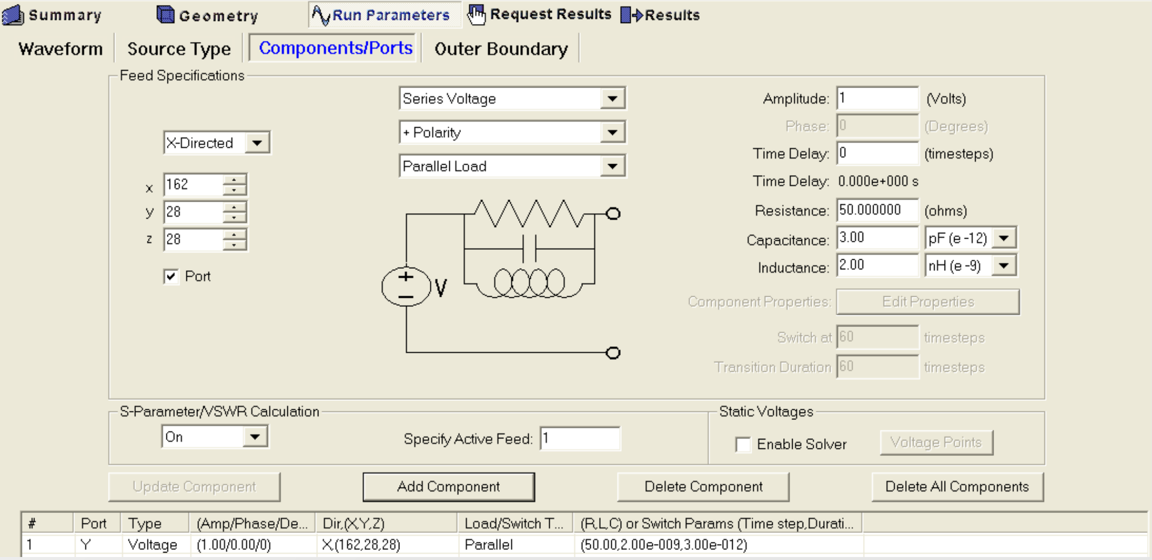
mospbsim3:m2
model=bsim3p

mosnbsim3:m3
model=bsim3n

Plot Terminal
plot1
Qualifier=term
Terminal=One
Network Operator=vt
Output file=vgsinv1.tran

Plot Terminal
plot2
Qualifier=term
Terminal=Two
Network Operator=vt
Output file=vdsinv2.out





Feed Specifications

X-Directed

x 162

y 28

z 28

☑ Port

Series Voltage

+ Polarity

Parallel Load

Amplitude: 1 (Volts)

Phase: 0 (Degrees)

Time Delay: 0 (timesteps)

Time Delay: 0.000e+000 s

Resistance: 50.000000 (ohms)

Capacitance: 3.00 pF (e -12)

Inductance: 2.00 nH (e -9)

Component Properties:

Switch at 60 timesteps

Transition Duration 60 timesteps

S-Parameter/VSWR Calculation

On

Specify Active Feed: 1

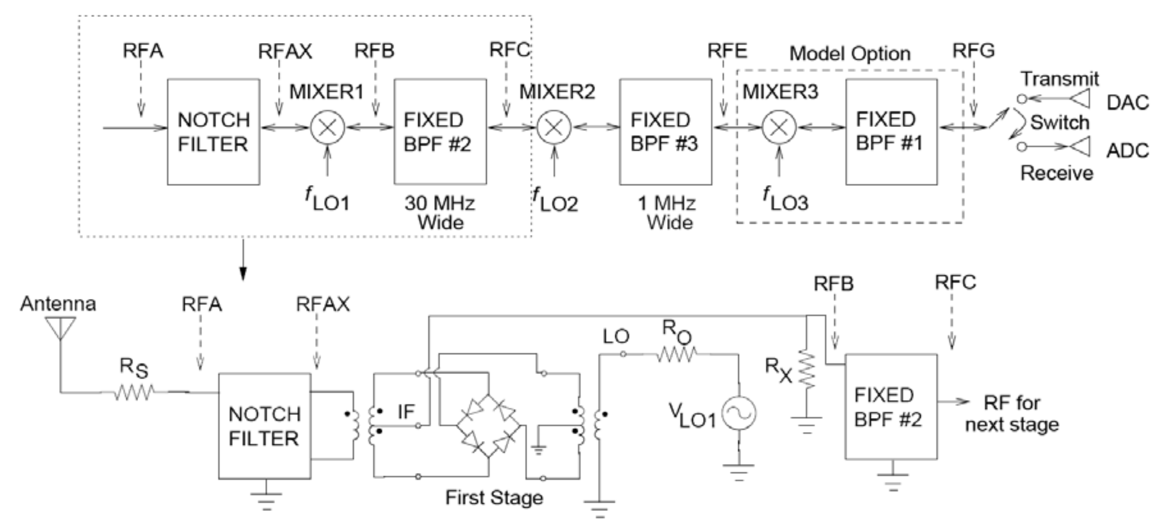
Static Voltages

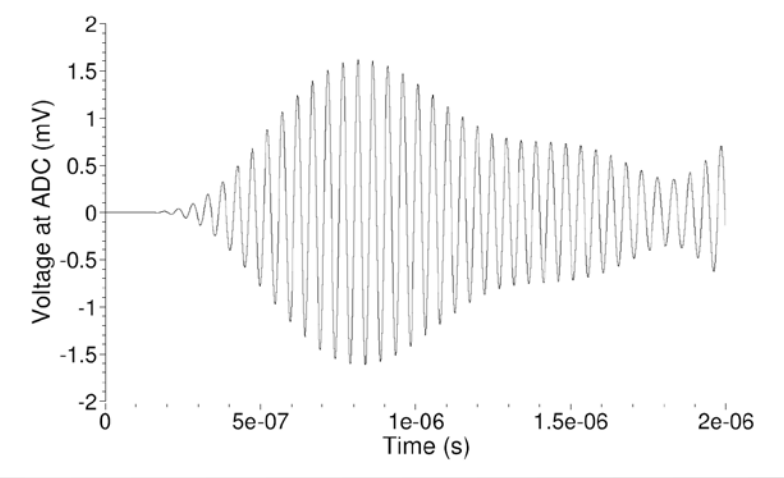
☐ Enable Solver

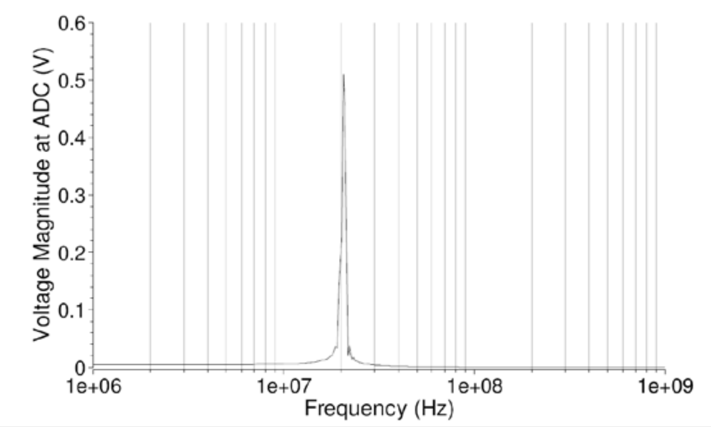
#	Port	Type	(Amp/Phase/De...	Dir.(X,Y,Z)	Load/Switch T...	(R,L,C) or Switch Params (Time step,Durati...
1	Y	Voltage	(1.00/0.00/0)	X,(162,28,28)	Parallel	(50.00,2.00e-009,3.00e-012)

fREEDA GUI is iFREEDA

Based on QUCS Schematic Capture and Display Front-End (GPL license)


RFA
RFAX
RFB
RFC
RFE
Model Option
RFG
NOTCH FILTER
MIXER1
FIXED BPF #2
MIXER2
FIXED BPF #3
MIXER3
FIXED BPF #1
Transmit
DAC
Switch
ADC
Receive
f_{LO1}
30 MHz Wide
f_{LO2}
1 MHz Wide
f_{LO3}
Antenna
RFA
RFAX
RFB
RFC
R_S
NOTCH FILTER
IF
LO
R_O
R_X
V_{LO1}
FIXED BPF #2
RF for next stage
First Stage


Voltage at ADC (mV)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
0
5e-07
1e-06
1.5e-06
2e-06
Time (s)


Voltage Magnitude at ADC (V)
0.6
0.5
0.4
0.3
0.2
0.1
0
1e+06
1e+07
1e+08
1e+09
Frequency (Hz)

Distributions

- fREEDA 2
  - Current on-line distribution
  - Circa November 2010
  - Mostly GPL/LGPL licensed
- fREEDA 3
  - Current in-house version
  - Mostly BSD Licensed
    - Some Trilinos packages currently LGPL to be transferred to BSD
  - Compiles cross-platform (Mac, Windows, Unix)
  - Conversion from spice netlist (-like) to XML
  - To Do:
    - Update GUI (iFREEDA)
    - Spice to freeda3 translator
    - Documentation
    - Commercialization
  - Kernal and standard library will be open source
    - Comemrcialization:
      - Model libraries
      - Specialized analyses.

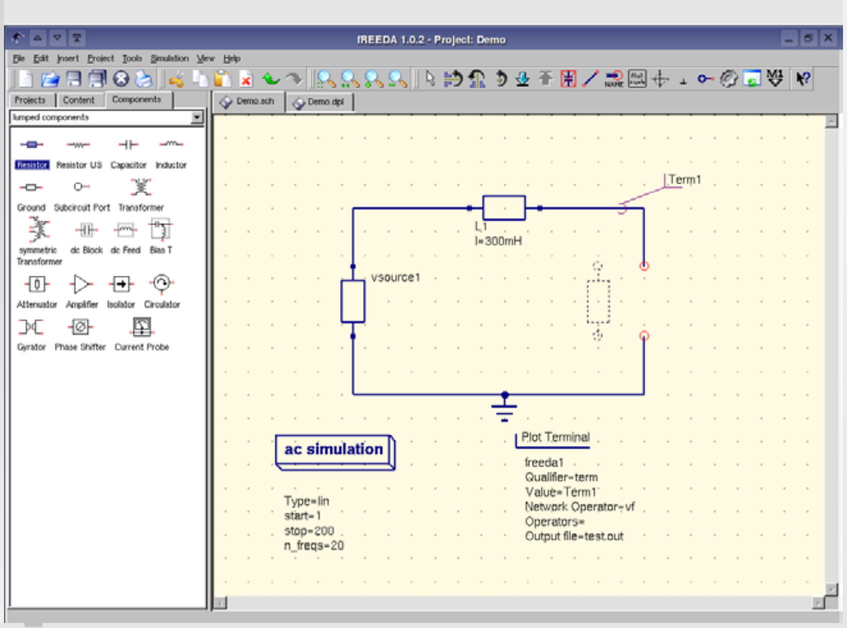
fREEDA

[Similar to](http://qucs.sourceforge.net)

[Quite Universal Circuit Simulator](http://qucs.sourceforge.net)

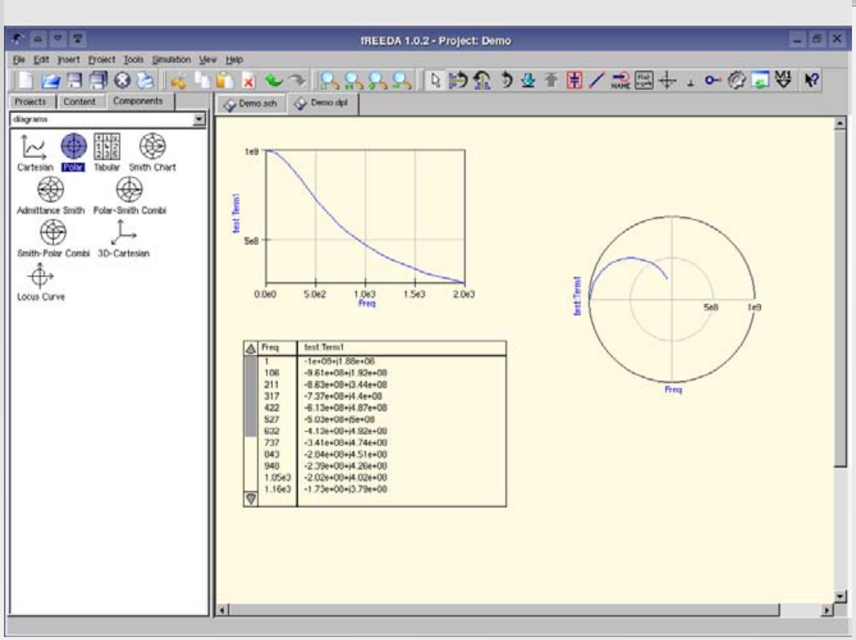
Developers
Michael Margraf *<michael.margraf@alumni.tu-berlin.de>*
owner of the project, GUI programmer
http://qucs.sourceforge.net

Based on the QT graphics package:
http://www.trolltech.com

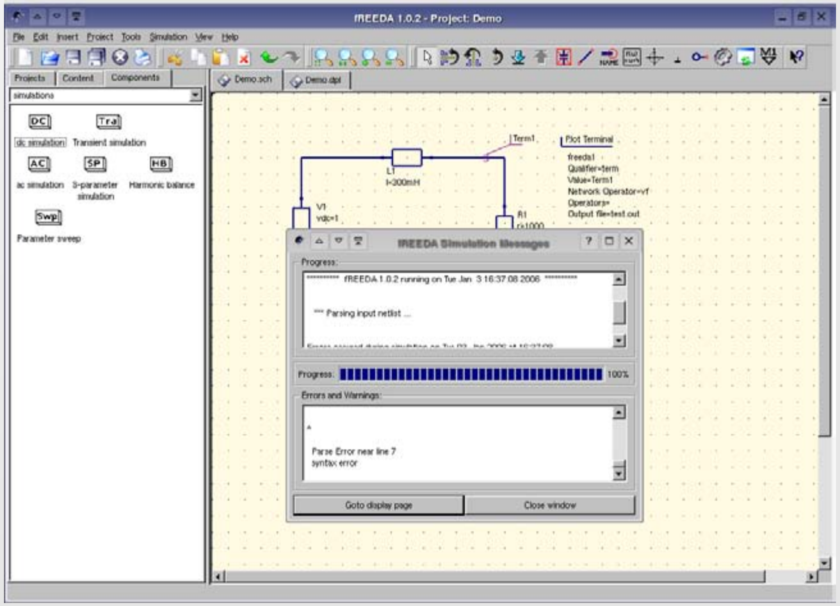


Type=lin
start=1
stop=200
n_freqs=20

freeda1
Qualifier=term
Value=Term1
Network Operator=vf
Operators=
Output file=test.out



Freq	test.Term1
1	-1e+09+j1.88e+08
106	-9.61e+08+j1.92e+08
211	-8.63e+08+j3.44e+08
317	-7.37e+08+j4.4e+08
422	-6.13e+08+j4.87e+08
527	-5.03e+08+j5e+08
632	-4.13e+08+j4.92e+08
737	-3.41e+08+j4.74e+08
843	-2.84e+08+j4.51e+08
948	-2.39e+08+j4.26e+08
1.05e3	-2.02e+08+j4.02e+08
1.16e3	-1.73e+08+j3.79e+08



freeda1
Qualifier=term
Value=Term1
Network Operator=vf
Operators=
Output file=test.out

Progress:

```
********** fREEDA 1.0.2 running on Tue Jan  3 16:37:08 2006 **********

 *** Parsing input netlist ...
```

Progress: 100%

Errors and Warnings:

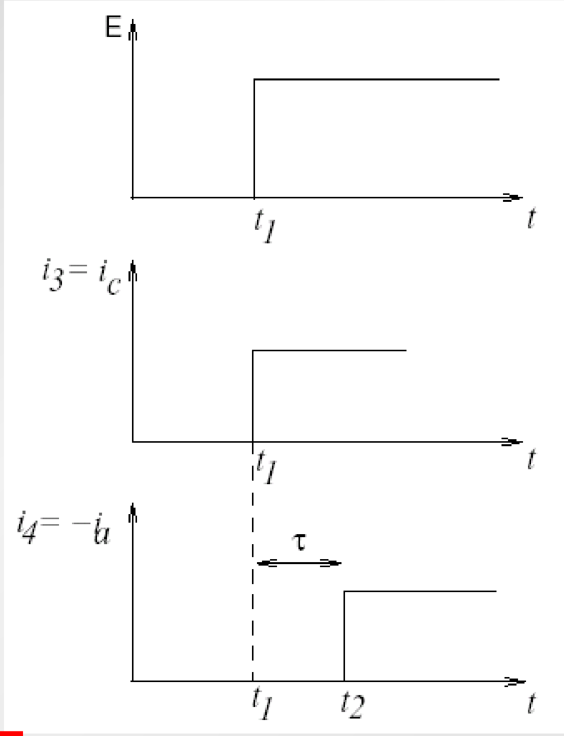
```
^

 Parse Error near line 7
 syntax error
```

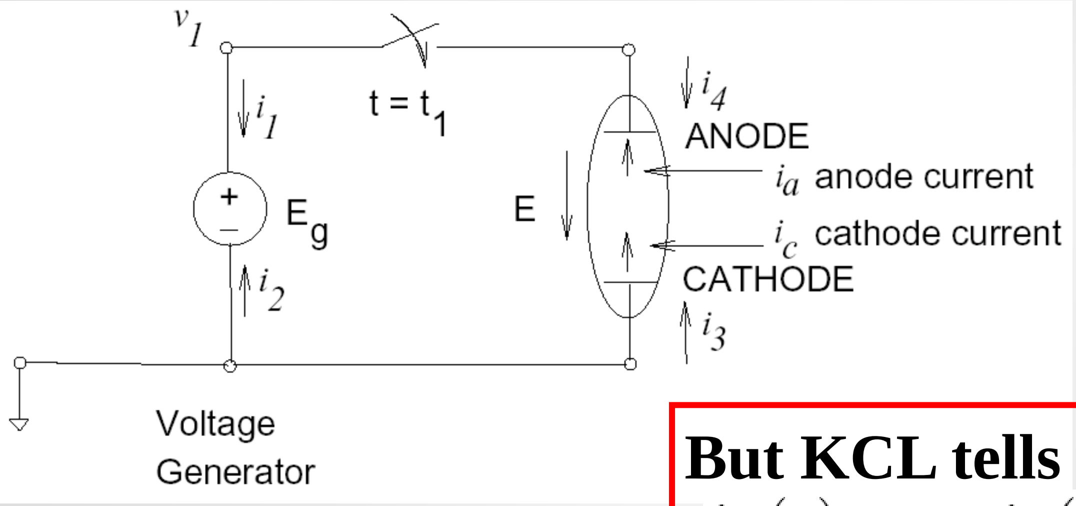
fREEDA Commercialization

- ***Open Source / Open Licensing***
  - ***BSD License (Open to companies to do what they want)***
- ***Parallel Simulator***
  - ***Two Commercialization Efforts under way***

Modeling Challenge: Non KCL

Two Terminal Element with Delay →





But KCL tells us

$$i_4(t) = -i_3(t)$$

↓

$$i_4(t) = -i_3(t - \tau)$$

We do not know how to handle some important aspects of the real world in a circuit simulator!

SIMULATOR TECHNOLOGY IMPOSES A LIMIT ON WHAT CAN BE MODELED

CIRCUITS ARE AN ABSTRACTION

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Summary