Overview IMST

Rüdiger Follmann

Profile

Deutscher Akkreditierungs Rat
DAR
TTI-P-G 158

RegTP
Regulierungsbehörde für Telekommunikation und Post
Zert-QM Zertifikat-Nr.: 0598
ISO 9001

legal GmbH (Ltd.)

founded September 1992

area Research + Development

- → ComTech solutions
- → RF Sensor
- → MultiMedia
- → EMC-techniques
- → Wireless technologies

IMST is industry's center of competence

IMST

Headquarters

10.000 sqm	site area
4.500 sqm	overall space
1.500 sqm	laboratories
300 sqm	hybrid technologies

Organisation IMST

Prof. Dr. Ingo Wolff

Dr. Peter Waldow

- **Marketing**
- **Technology Transfer**
- **MultiMedia & Layout**
- **Quality Assurance**
- **Controlling**
- **EDV-Administration**
- **Central Services**

G. Seidel

Systems

Dr. Matthias Rittweger

Circuits

Dr. M. Geissler

Antennas & EM

J. J. Borkes

Test Centre

→> 100 Researchers 11 Administration
→ 19 PhDs 20 Students, e.t.c
→ 79 Engineers

Products and services

Services

- → System Design
- → Circuit & Antenna Design
- → Integrated Circuit Design
- → Active & Passive Device Modeling
- → RF & Antenna Measurements
- → Channel Sounder Measurements
- → EMC - Tests
- → Mobile Phone Tests
- → Technical Consulting and seminars

Products

- → COPLAN Coplanar Design Library
  Add-On to Agilent EEsof's ADS
- → EMPIRE™ Advanced 3D EM Simulation Software
- → TOPAS State-of-the-art HEMT, MESFET, LDMOS models and Parameter Extraction
- → **MultiLib™** Design Library for LTCC/PCB multi-layered circuits
  Add-On to Agilent EEsof's ADS

Measurements, models and extractions

Rüdiger Follmann

Contents

- → Models
- → Linear part
- → Nonlinear part
- → Current measurements
- → S-parameter measurements
- → Power measurements
- → Noise
- → Verification

Ways of modeling

→**Physical models**: Particle models or semiconductor equations

→**Table based models**: Bias dependentS-parameters are saved in a table

→**Mathematical models**: Transfer behavior is described by mathematical functions

→**Equivalent circuits**: Physical behavior is emulated by lumped elements

Ways of modeling

Linear models

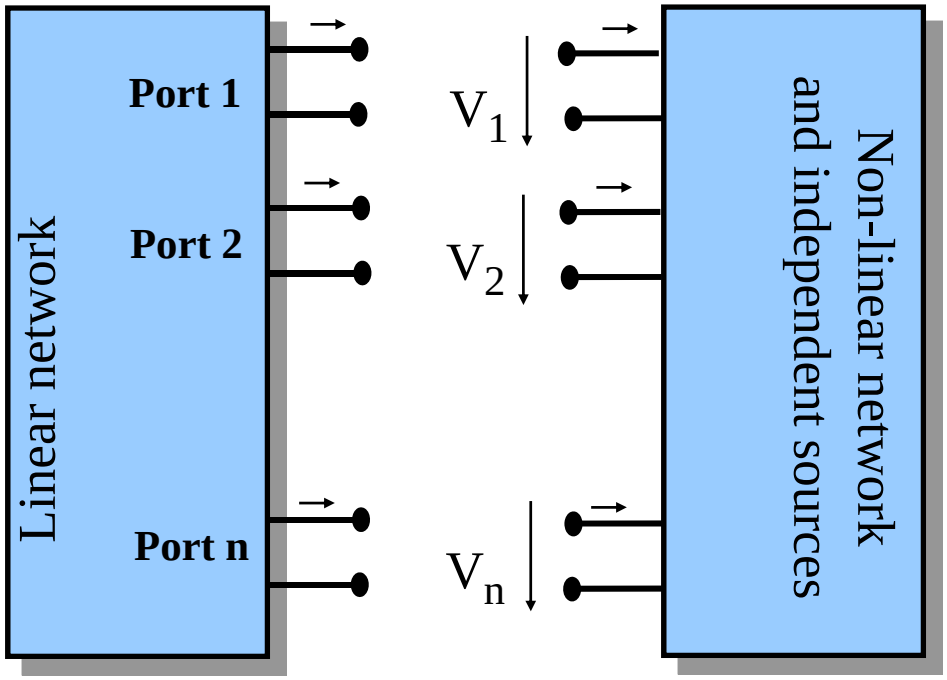
→Description of DC behavior

→Description of RF behavior, e.g. in dependence of bias point. Only small signal amplitudes close to bias point are allowed

Non-linear models

→Large signal amplitudes and change of bias point (Harmonic balance).

Harmonic balance



Only linear elements

Only non-linear elements

HB is a hybrid between time- and frequency domain calculations.
Non-linear part is calculated In time domain, linearer part in frequency domain

Voltages and currents at each port are balanced, until they are equal for both part of network.

DC measurements

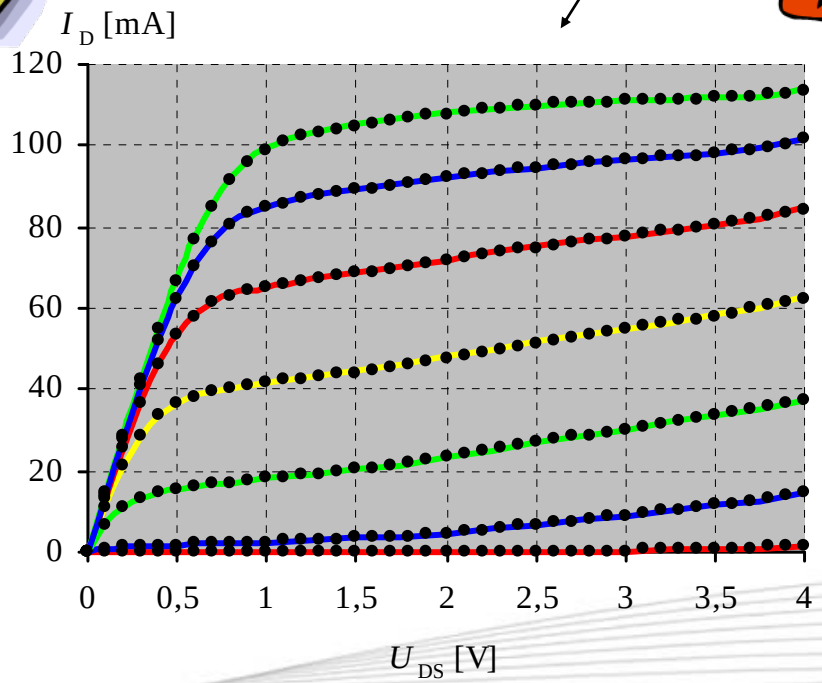
Port 1
Input

Port 2
Output

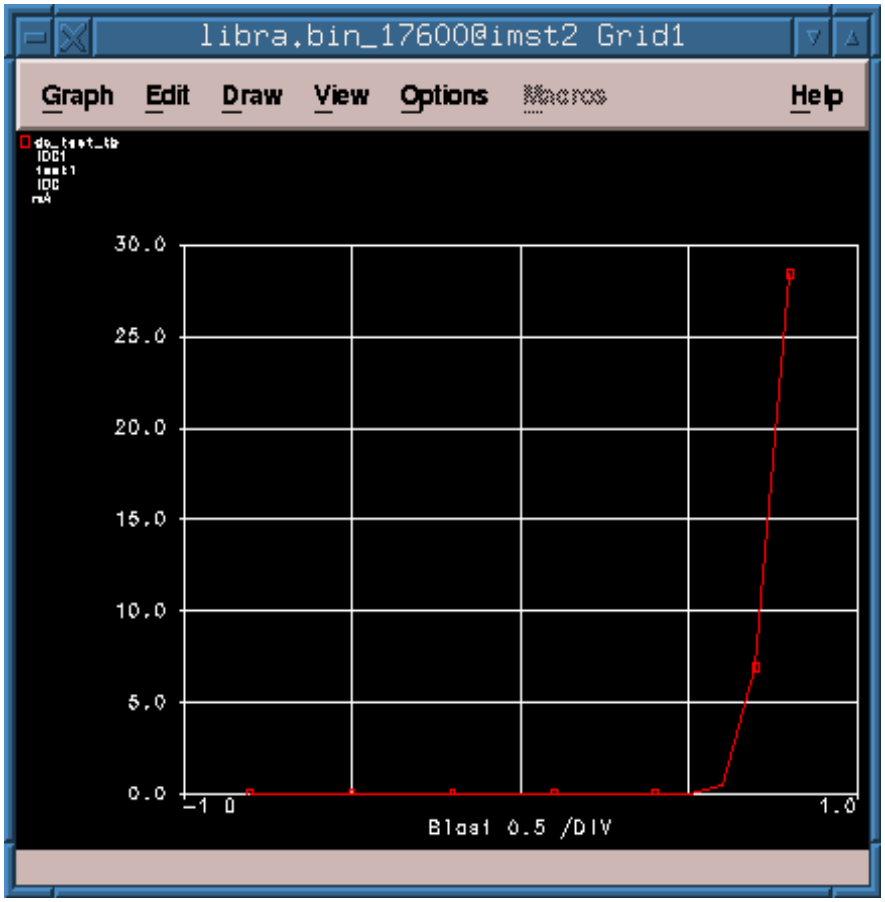
V_{GS}

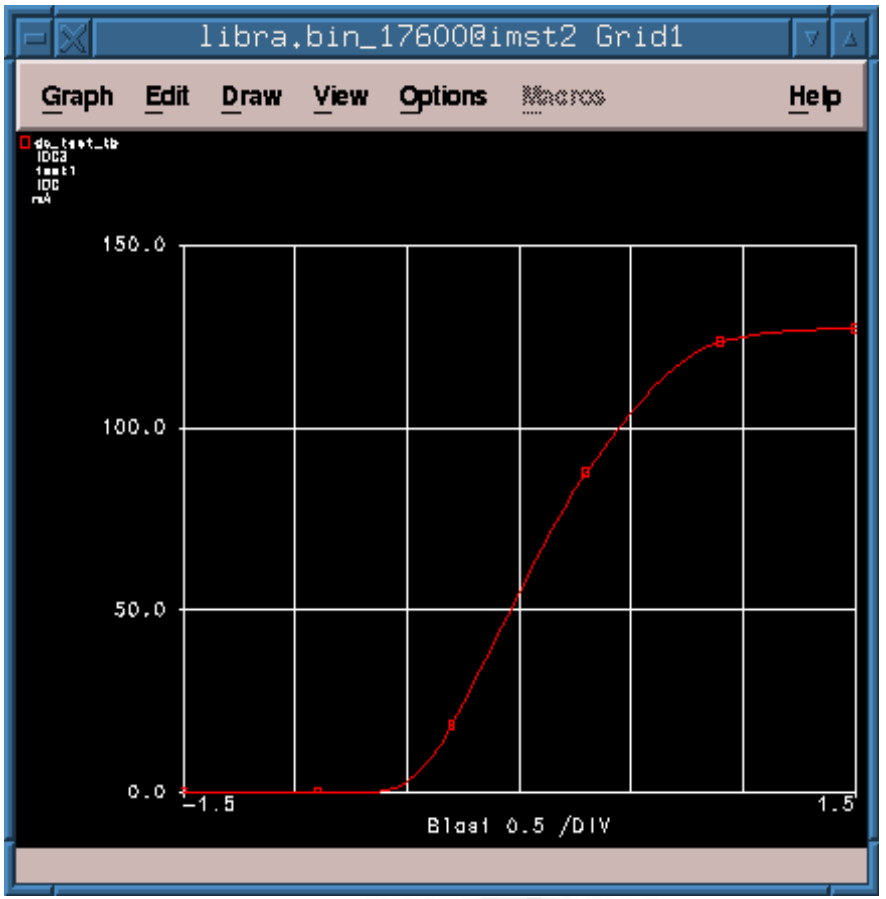
V_{DS}

DC IV-curves

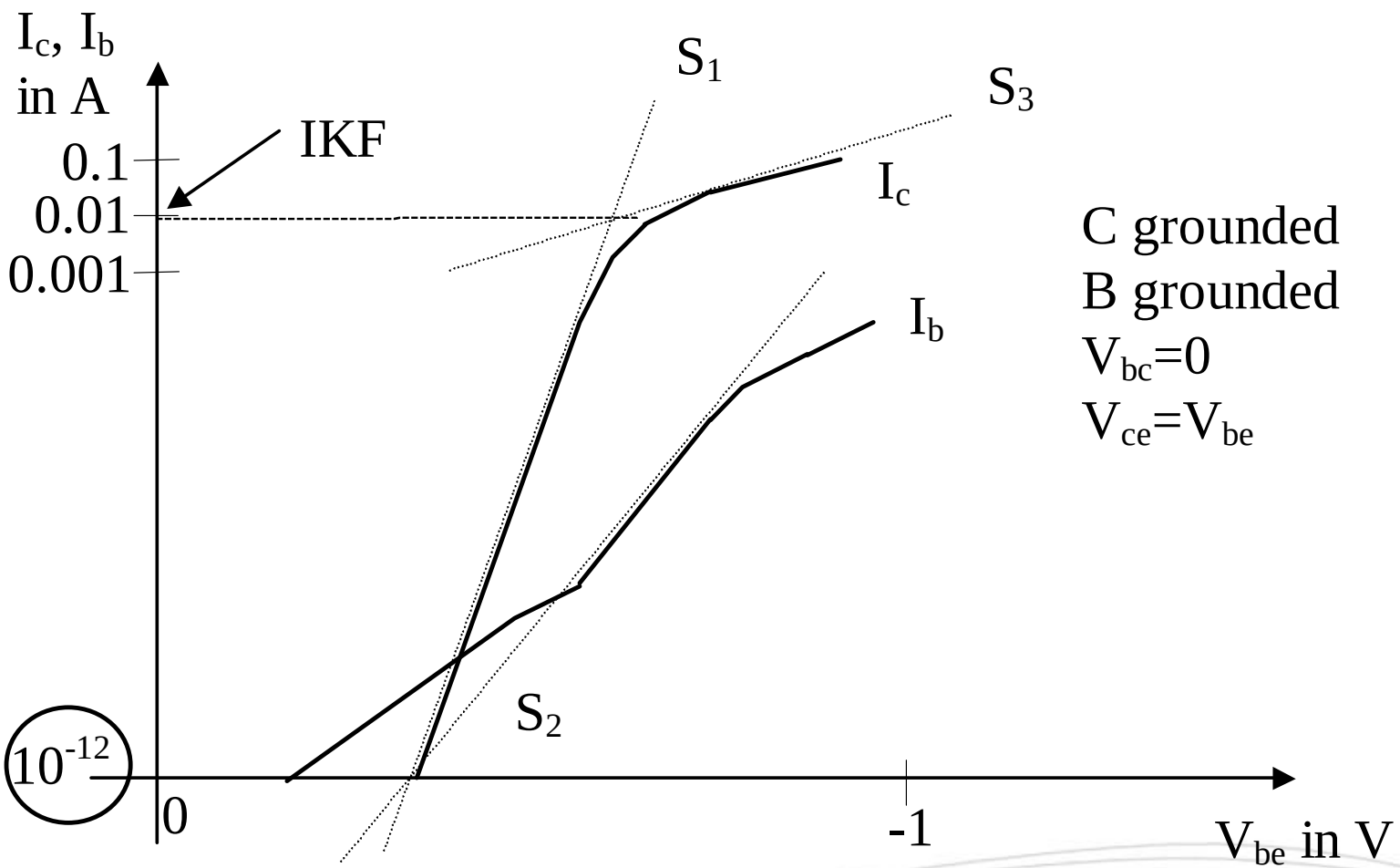


Transistor transfer curves



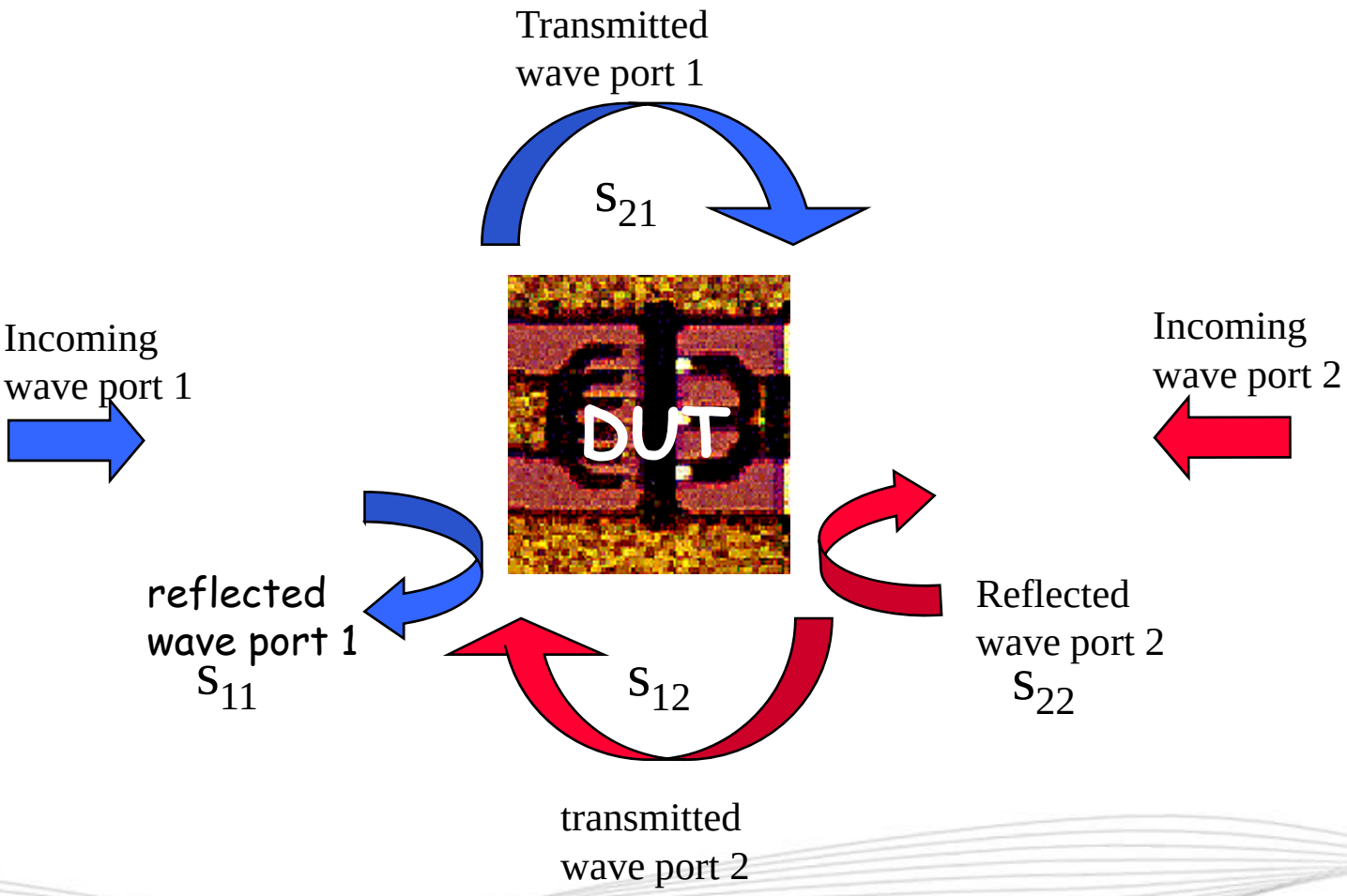


Gummel-Plots



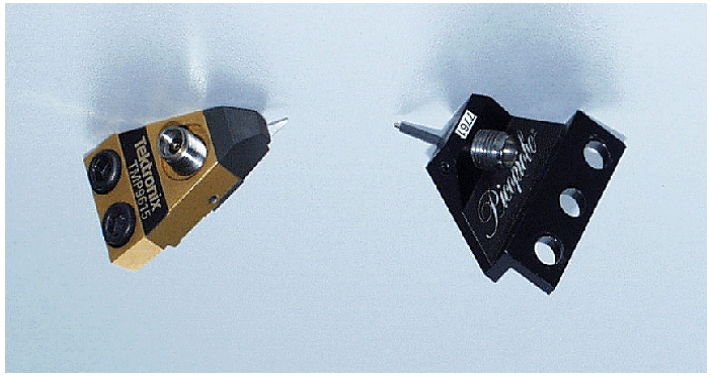
RF measurements

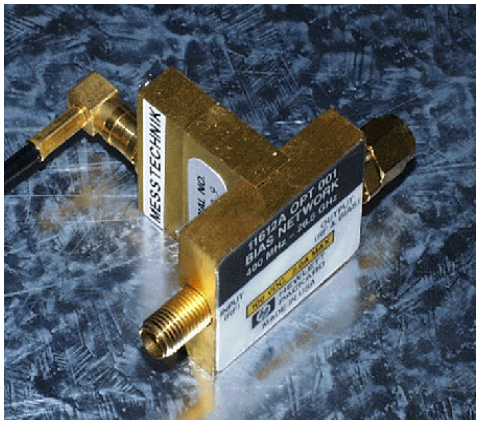
S-parameter measurements



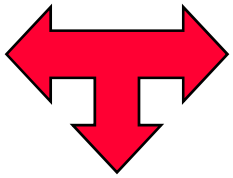
RF measurements

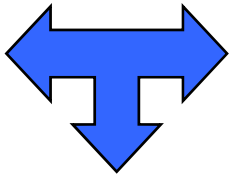
S-parameter measurements





Port 1





Port 2

V_{GS}

V_{DS}

Qualification

→Pinch-off of transistor device

→Enhancement or depletion mode

→Slope and IV curves

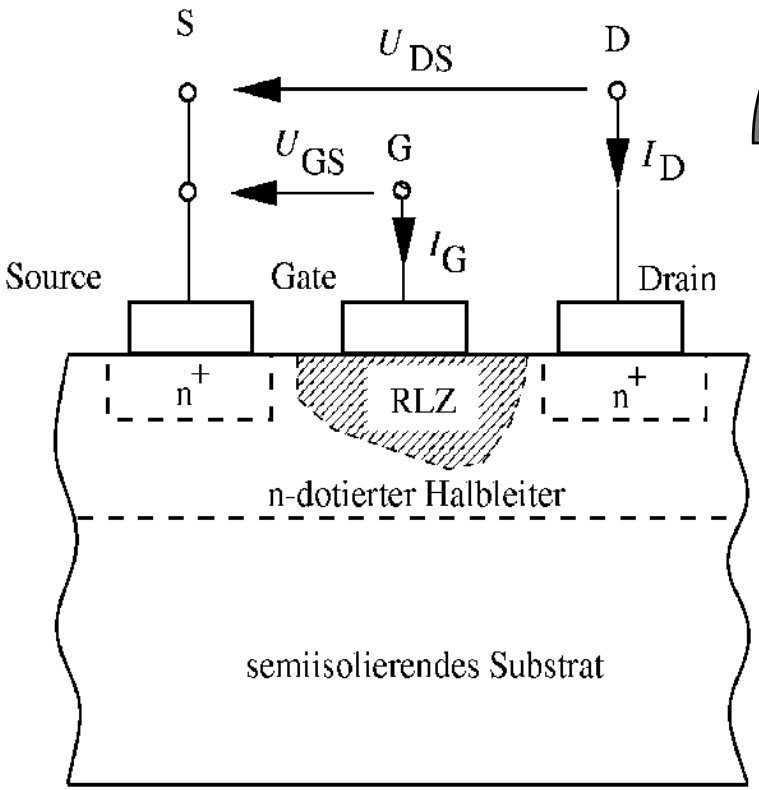
→Gate diode current

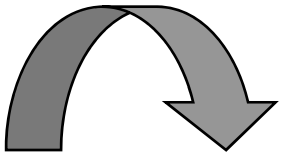
→amplification s_{21} and attenuation

→Compression behavior

→Other s-parameters < 0 dB

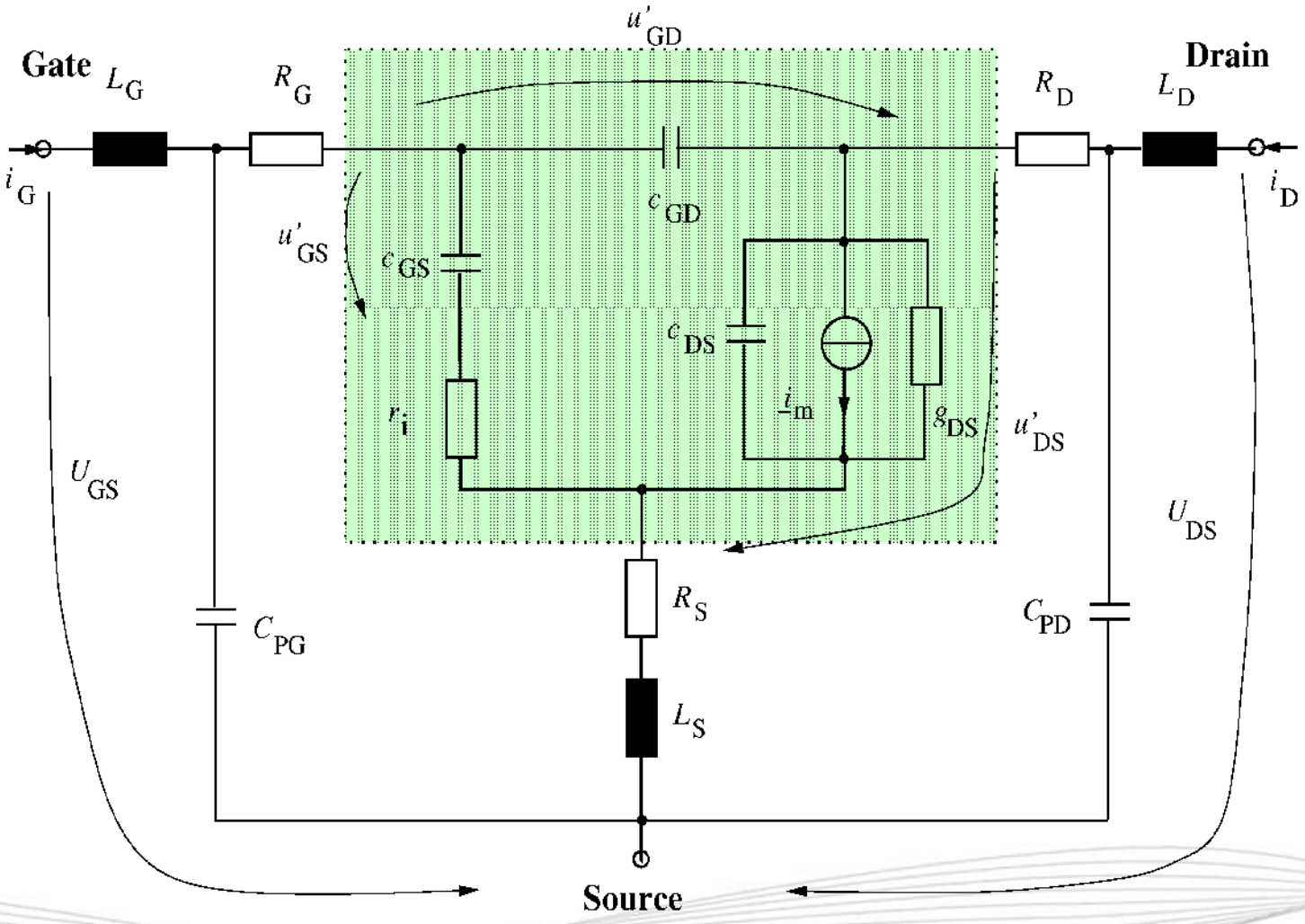
Composition FET und equivalent circuit



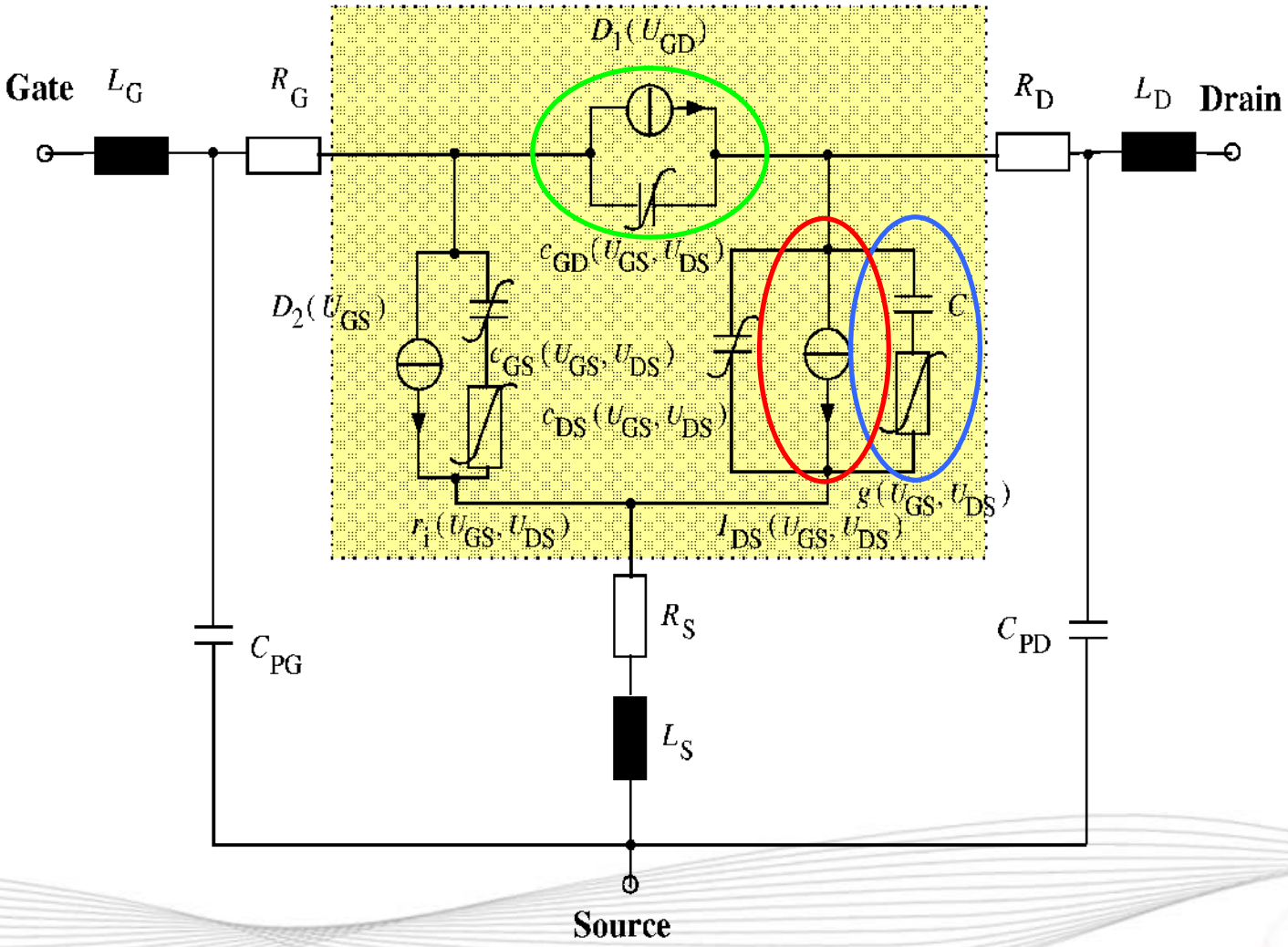


Das Bild kann nicht angezeigt werden. Dieser Computer verfügt möglicherweise über zu wenig Arbeitsspeicher, um das Bild zu öffnen, oder das Bild ist beschädigt. Starten Sie den Computer neu, und öffnen Sie dann erneut die Datei. Wenn weiterhin das rote x angezeigt wird, müssen Sie das Bild möglicherweise löschen und dann erneut einfügen.

Small signal equivalent circuit



Enhanced small signal equivalent circuit

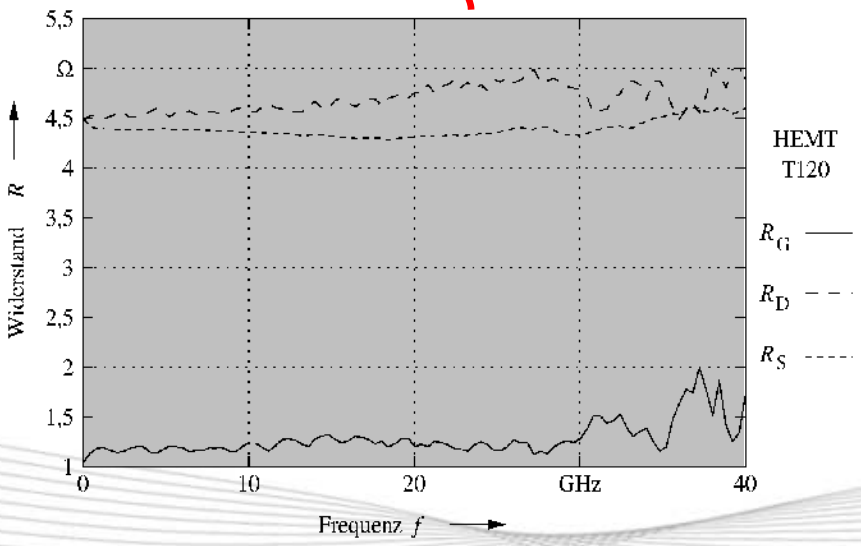


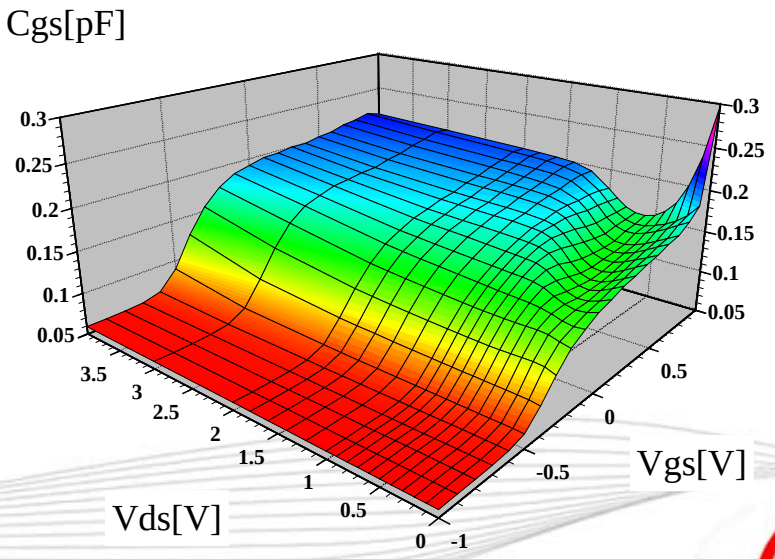
Parameter extraction

S-Parameter IV curves → Extrinsic elements → Intrinsic elements →

$$R_S = \mathrm{Re}\{\underline{z}_{12}\}$$

$$c_{GS}(V_{GS},V_{DS}) = \sum_{f=f_1}^{f_2} \frac{1}{\omega}\left(\mathrm{Im}\{\underline{y}_{11}(V_{GS},V_{DS})\} + \mathrm{Im}\{\underline{y}_{12}(V_{GS},V_{DS})\}\right)/(n_{f2} - n_{f1})$$



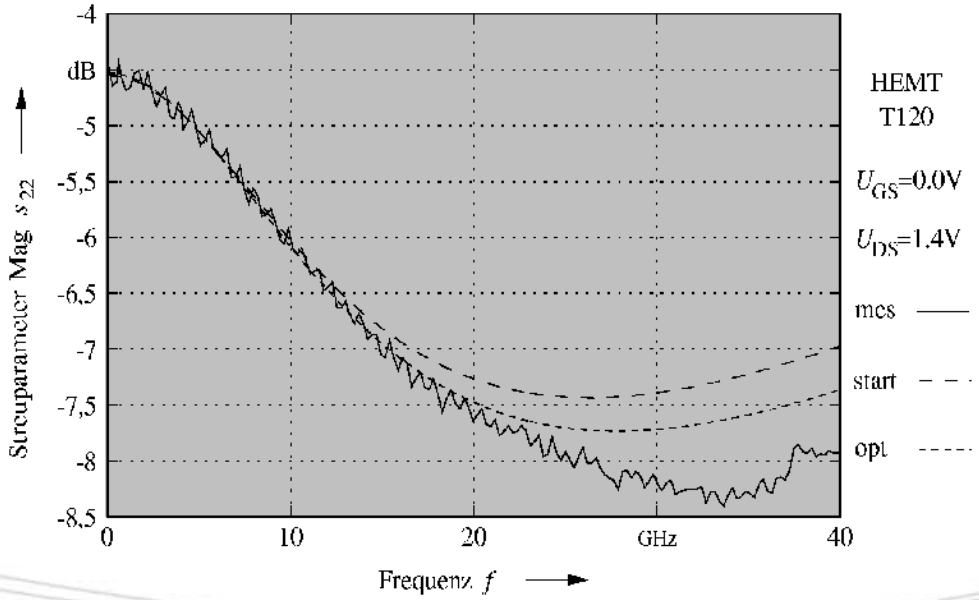


Parameter extraction

Optimization of intrinsic elements

Calcualtion of conductance g

De-embedding of voltages



$$V'_{GS} = V_{GS} - I_{DS} R_S$$

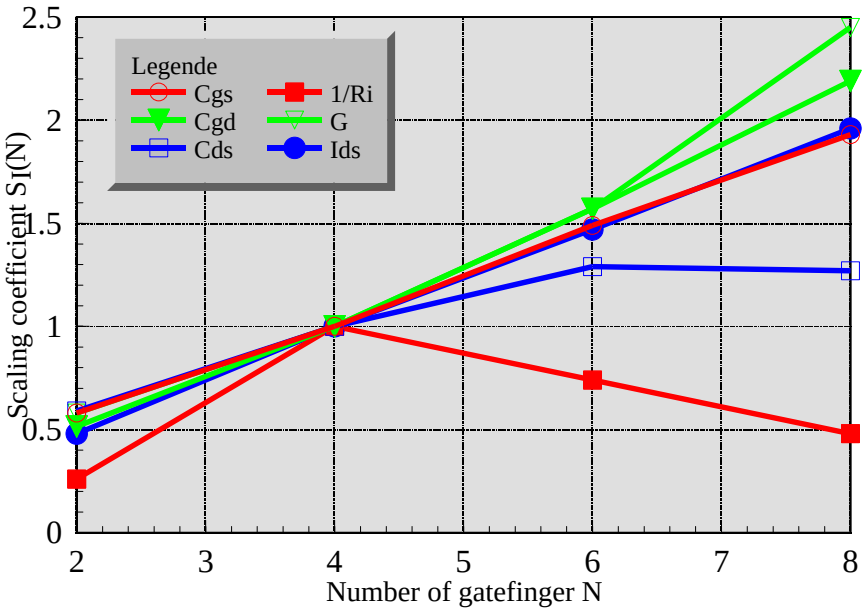
$$V'_{DS} = V_{DS} - I_{DS} \left(R_D + R_S \right)$$

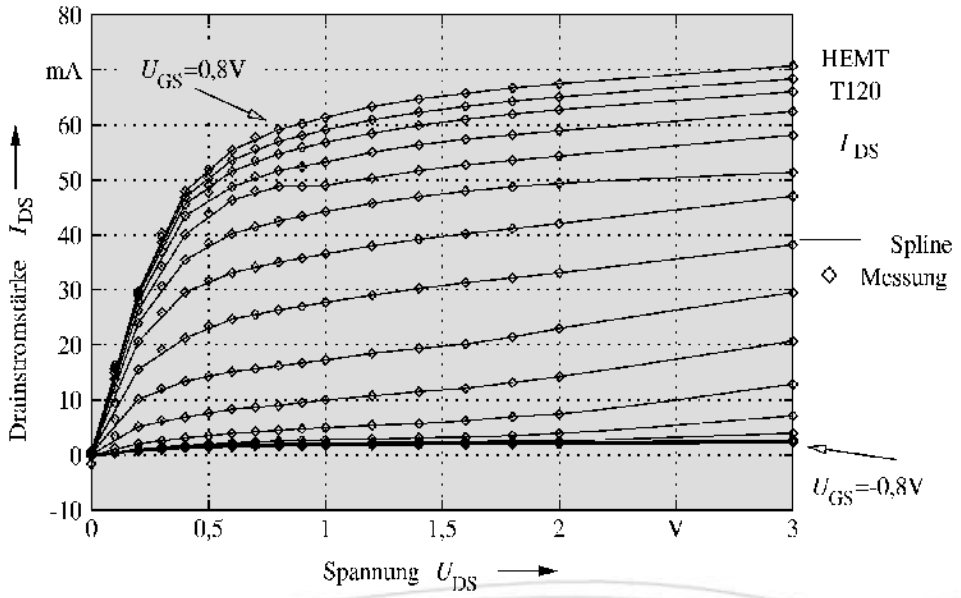
Parameterextraktion

Calculation of scaling and noise parameters

Description of intrinsic elements

Store the Simulation file



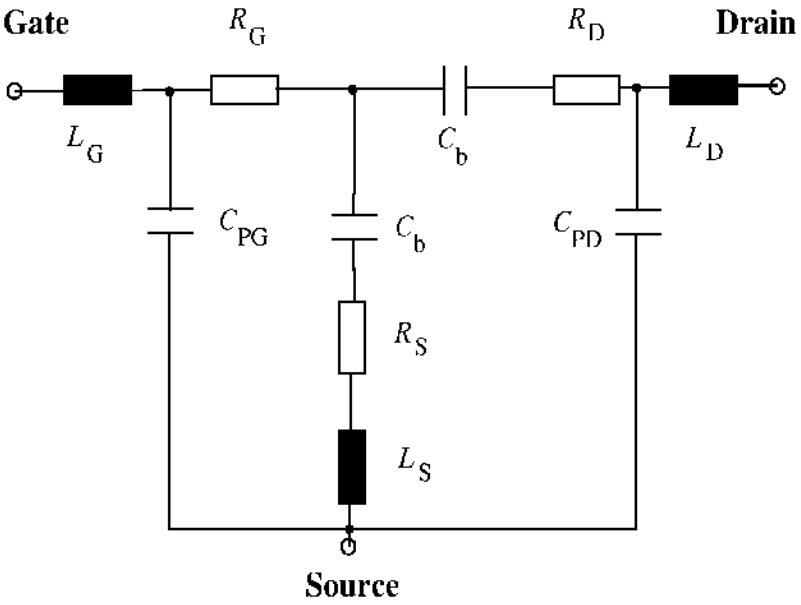


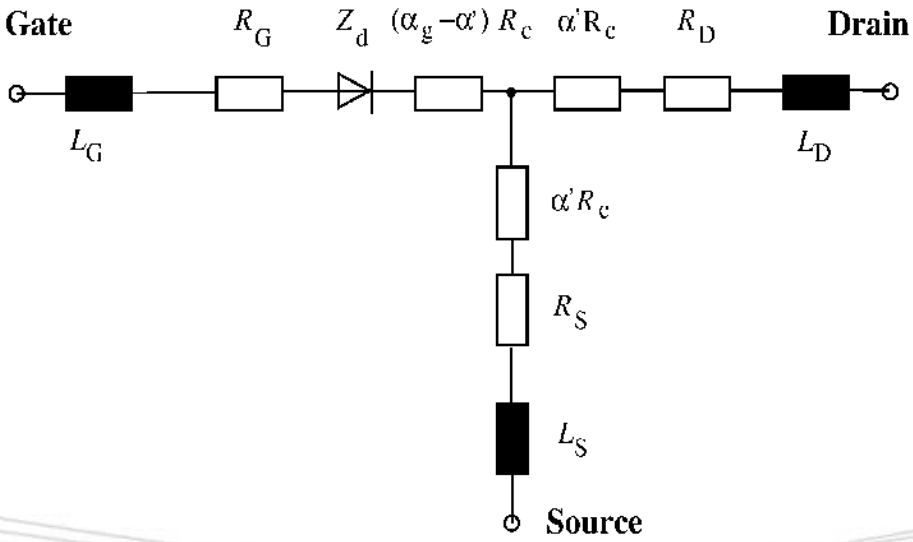
Extraction of extrinsic elements

Extraction of capacitances

$$V_{GS} < V_p$$

$$V_{DS} = 0\,\mathrm{V}$$





Extraction of inductances and resistors

$$V_{GS} > 0\,\mathrm{V}$$

$$V_{DS} = 0\,\mathrm{V}$$

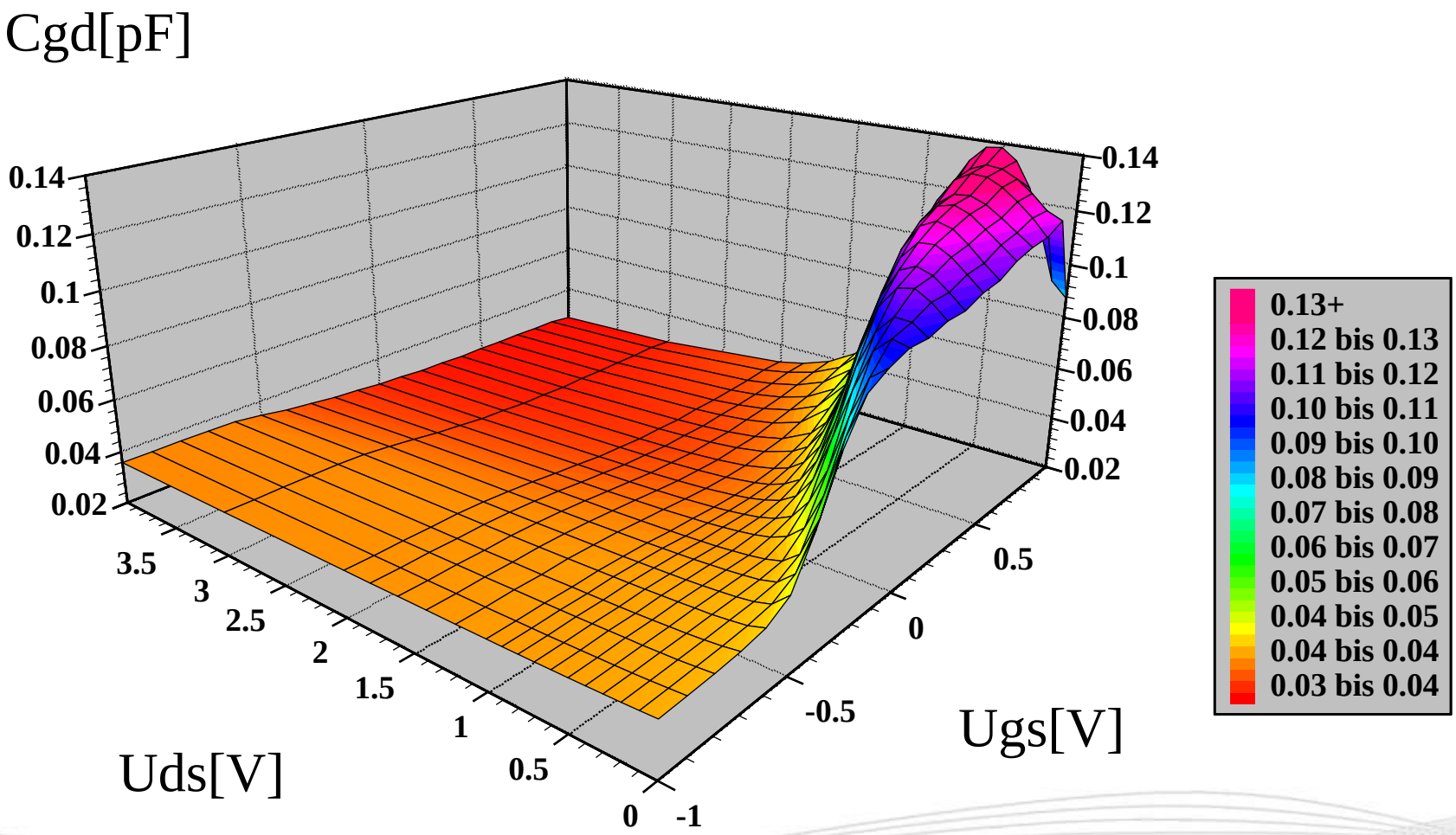
Extraction of intrinsic elements

$$\underline{S} \rightarrow \underline{Z} \rightarrow \begin{pmatrix} \underline{z}_{11} - j\omega L_G & \underline{z}_{12} \\ \underline{z}_{21} & \underline{z}_{22} - j\omega L_D \end{pmatrix}$$

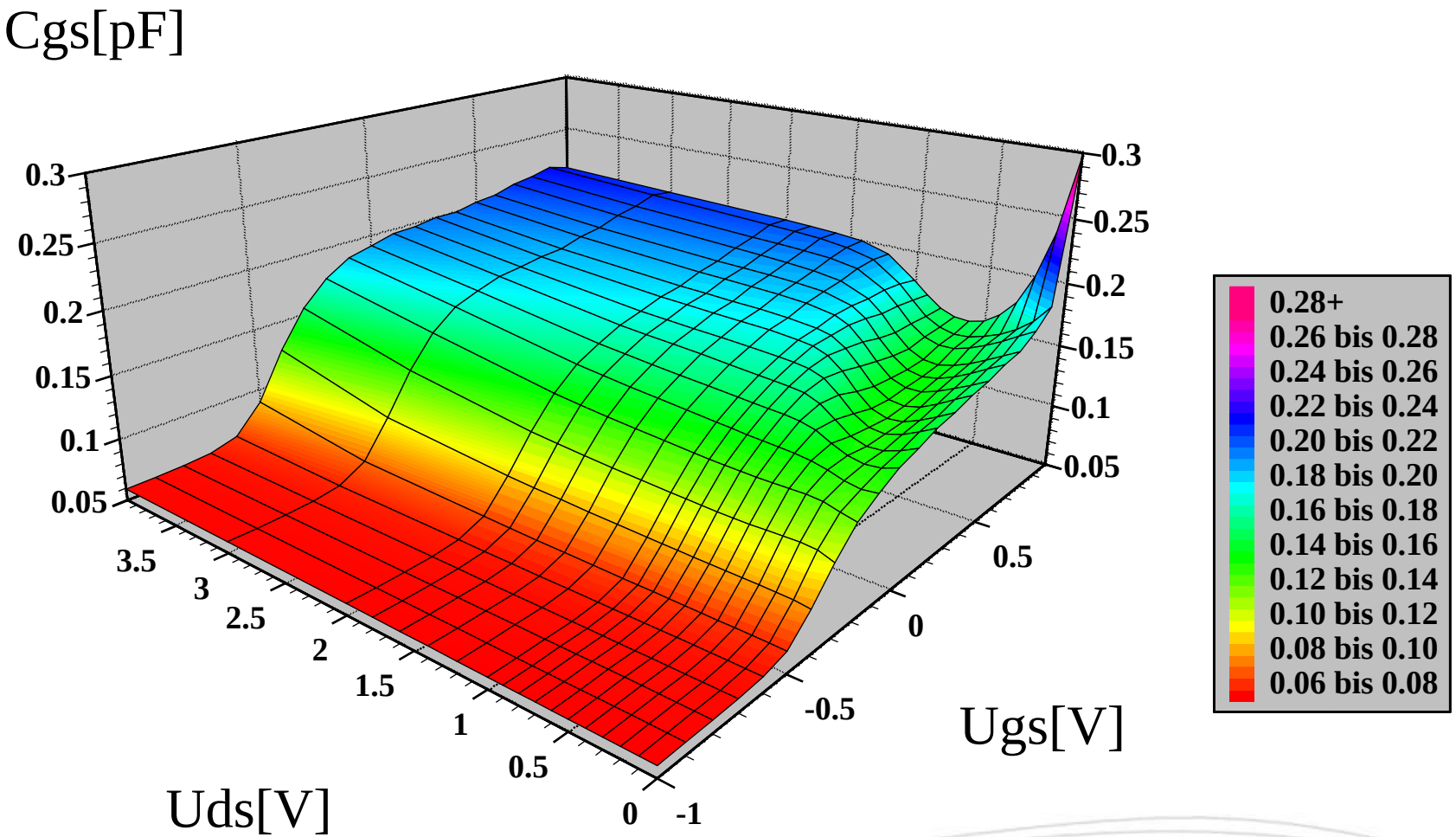
$$\underline{Z} \rightarrow \underline{Y} \rightarrow \begin{pmatrix} \underline{y}_{11} - j\omega C_{PG} & \underline{y}_{12} \\ \underline{y}_{21} & \underline{y}_{22} - j\omega C_{PD} \end{pmatrix}$$

$$\underline{Y} \rightarrow \underline{Z} \rightarrow \begin{pmatrix} \underline{z}_{11} - R_S - R_G - j\omega L_S & \underline{z}_{12} - R_S - j\omega L_S \\ \underline{z}_{21} - R_S - j\omega L_S & \underline{z}_{22} - R_S - R_D - j\omega L_S \end{pmatrix}$$

Extraction of intrinsic elements

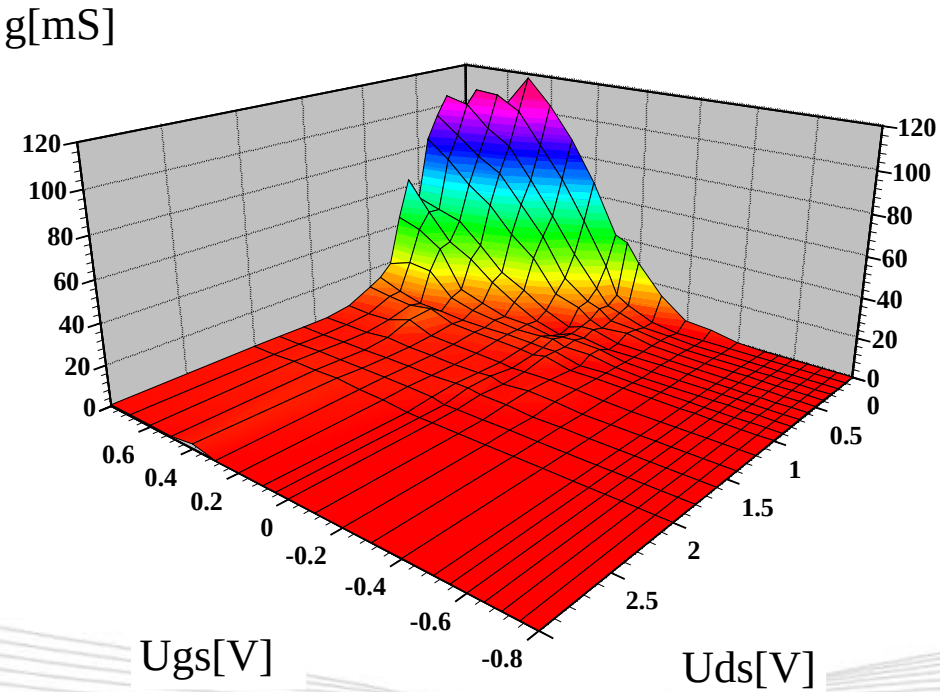


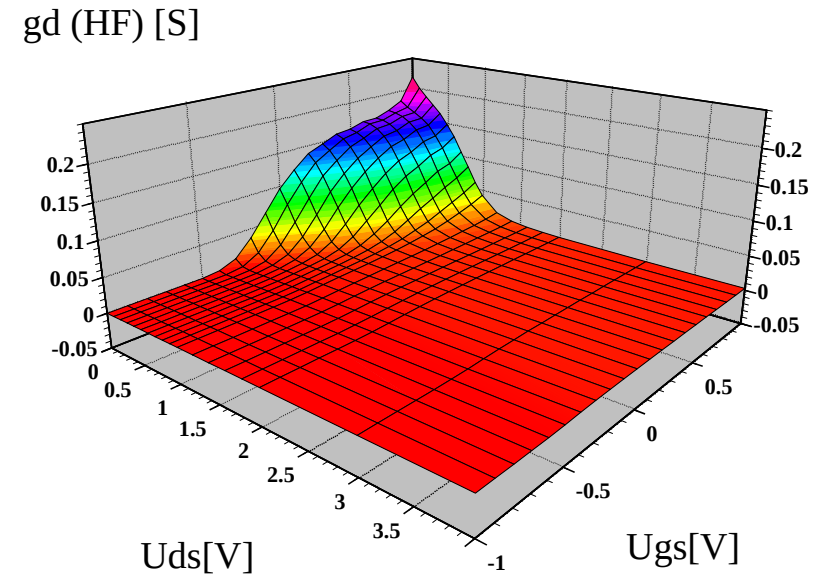
Extraction of intrinsic elements

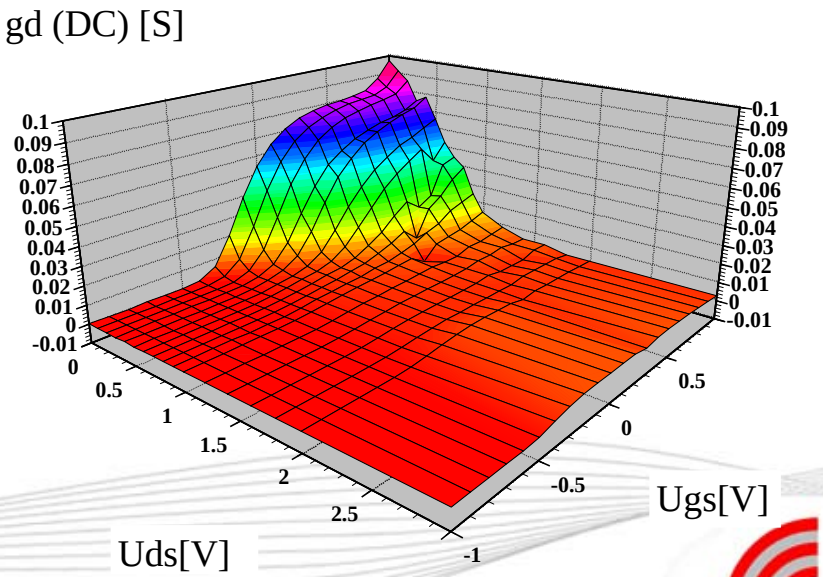


Calculation of output conductance

Extraction of output conductance *g* using optimizing process

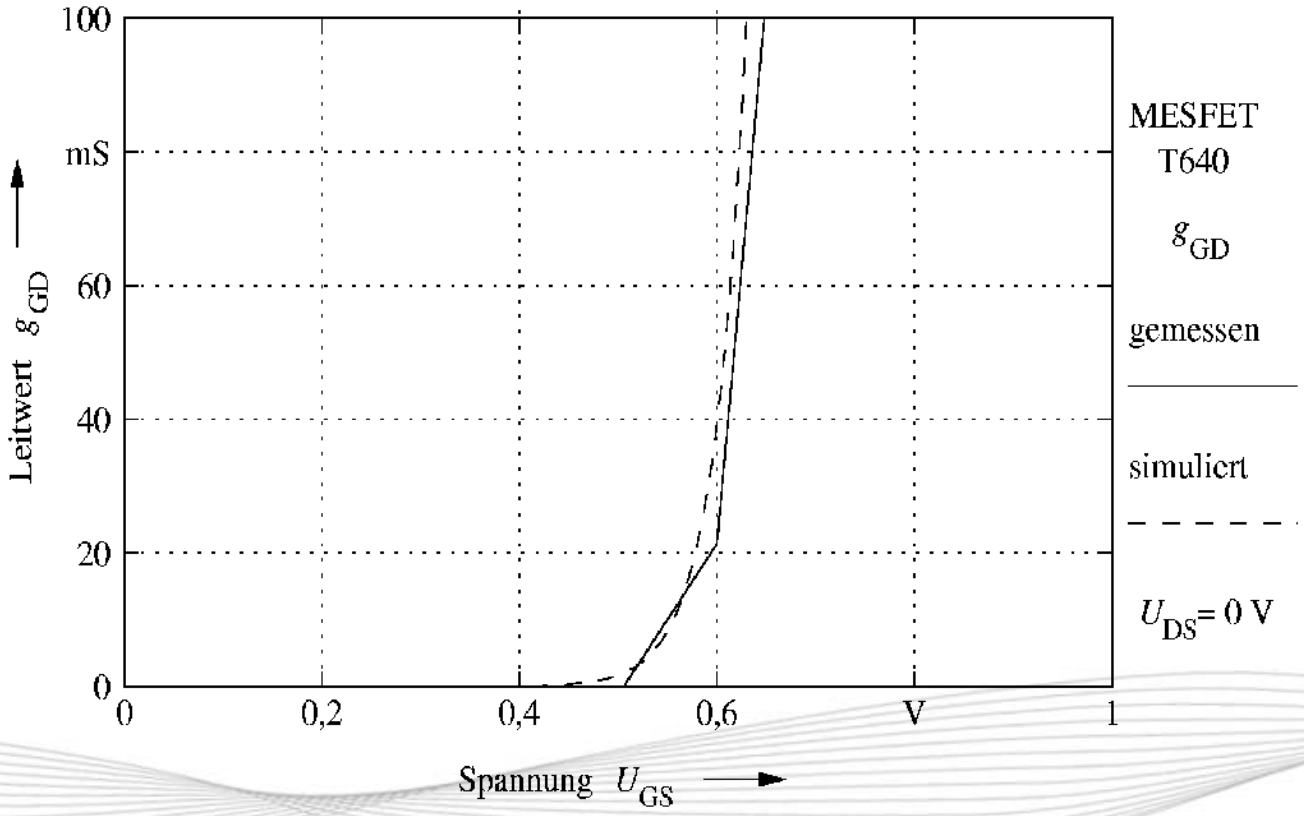






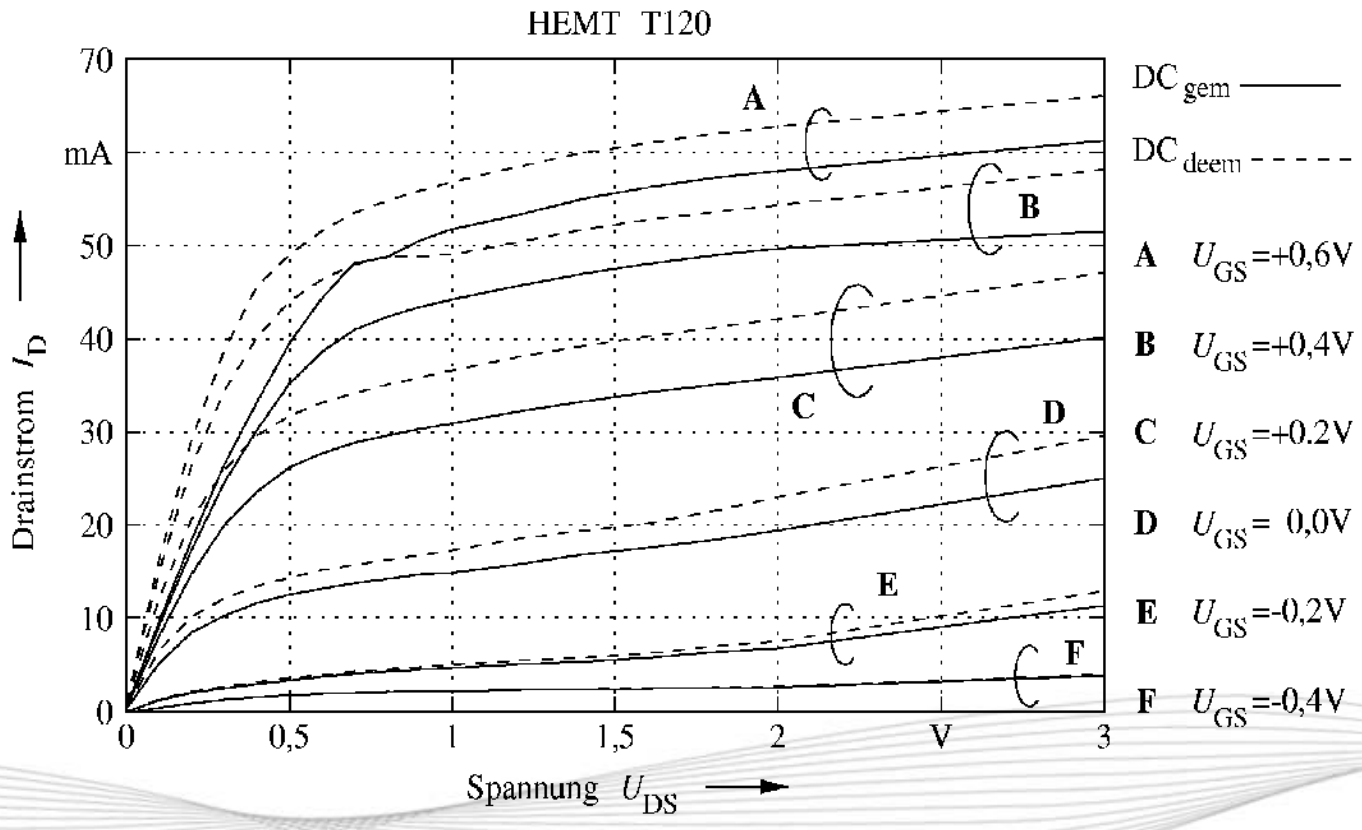
Extraction of Is and n

$$\mathrm{Re}\{\underline{y}_{12}\} = -\frac{\mathrm{d}I_{\mathrm{d1}}}{\mathrm{d}U_{\mathrm{GD}}} = -\frac{I_{\mathrm{S}}}{nU_{\mathrm{t}}}\exp\left(\frac{U_{\mathrm{GD}}}{nU_{\mathrm{t}}}\right)$$



Outer and inner voltages

$$V'_{GS} = V_{GS} - I_{DS} R_S$$
$$V'_{DS} = V_{DS} - I_{DS} \left(R_D + R_S \right)$$



Description of intrinsic elements

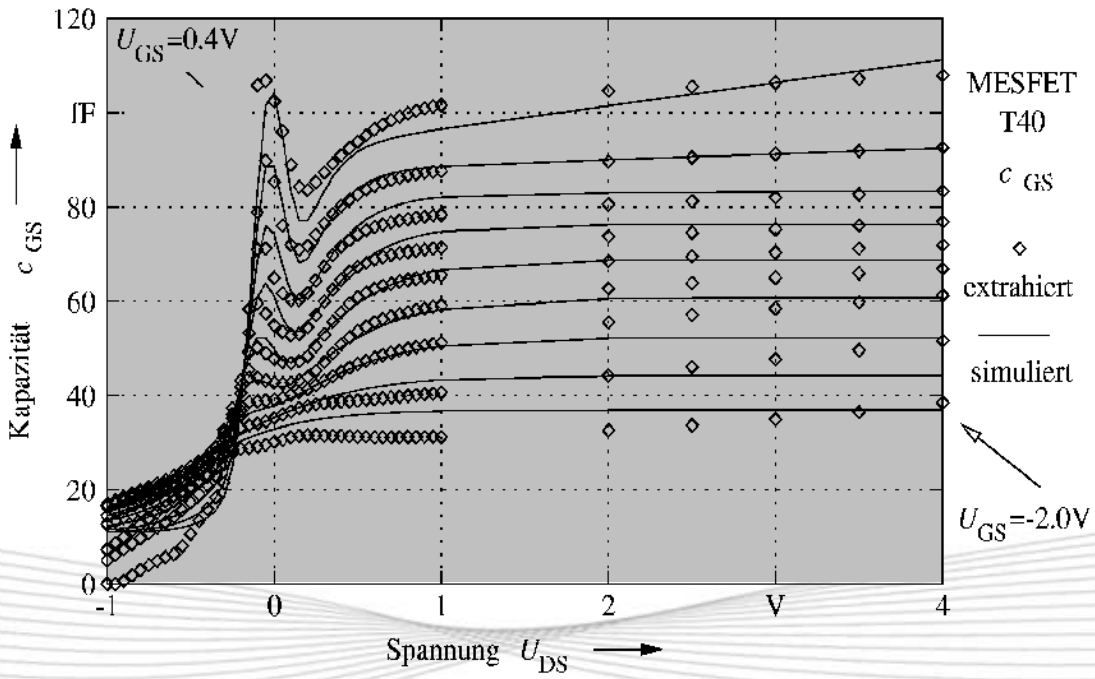
$$c_{\mathrm{GS}} = \begin{cases} k_{\mathrm{h}} + k_{\mathrm{g}} U_{\mathrm{DS}} + x_{20} & U_{\mathrm{DS}} > 0 \\ k_{\mathrm{h}} + x_{20} & \text{sonst} \end{cases}$$

$$k_a = \begin{cases} x_0 (U_{\mathrm{GS}} - x_1)^2 & U_{\mathrm{GS}} \geq x_1 \\ 0 & \text{sonst} \end{cases}$$

$$k_{\mathrm{b}} = x_2 \left(\tanh\left(x_3 \left(U_{GS} - x_{17} \right) \right) + 1 \right)$$

$$k_{\mathrm{h}} = k_a \left(\exp\left(k_b \left(U_{DS} - k_c \right)^2 \right) \right) + k_d \left(\tanh\left(k_e \left(U_{DS} - k_f \right) \right) + 1 \right)$$

$$k_{\mathrm{c}} = x_4 \exp\left(x_5 \left(U_{\mathrm{GS}} - x_6 \right)^2 \right)$$



$$k_{\mathrm{d}} = x_7 \left(\tanh\left(x_{21} \left(U_{\mathrm{GS}} - x_8 \right) \right) + 1 \right)$$

$$k_{\mathrm{e}} = x_9 \left(U_{\mathrm{GS}} - x_{10} \right)^2 + x_{11}$$

$$k_{\mathrm{f}} = x_{12} \exp\left(x_{13} \left(U_{\mathrm{GS}} - x_{14} \right)^2 \right) + x_{18}$$

$$k_{\mathrm{g}} = x_{15} \exp\left(x_{16} \left(U_{\mathrm{GS}} - x_{19} \right)^2 \right)$$

Large signal simulation

$$Q_1(u_1) = \int_{u_{10}}^{u_1} c(\tilde{u}_1)\,\mathrm{d}\tilde{u}_1$$

$$\Delta Q = \oint_{\partial\Omega} c(\tilde{u}_1)\,\mathrm{d}\tilde{u}_1 = 0$$

$$Q_2(u_1,u_2) = \int_{u_{10}}^{u_1} c(\tilde{u}_1,u_2)\,\mathrm{d}\tilde{u}_1 + Q_1'(u_2)$$

Defined charge cycle

Trans elements

$$C(u_1,u_2) = \sum_{i=0}^{n} c_i(u_1)\,T_i(u_2)$$

Complete gate current

$$i_\mathrm{G} = i_\mathrm{GS} + i_\mathrm{GD}$$

$$u_\mathrm{GS} = U_\mathrm{GS} + u_\mathrm{GS\sim} \Rightarrow \frac{\mathrm{d}u_\mathrm{GS}}{\mathrm{d}t} = \frac{\mathrm{d}u_\mathrm{GS\sim}}{\mathrm{d}t}$$

GS-part of gate current

$$i_\mathrm{GS} = \frac{\mathrm{d}Q_\mathrm{GS}}{\mathrm{d}t} = C'_\mathrm{GS}(u_\mathrm{GS},u_\mathrm{DS})\frac{\mathrm{d}u_\mathrm{GS}}{\mathrm{d}t}$$

Large signal simulation

$$i_{GS} = C'_{GS}\left(U_{GS} + u_{GS\sim}, U_{DS} + u_{DS}\right)\frac{\mathrm{d}u_{GS\sim}}{\mathrm{d}t}$$

Taylor-series

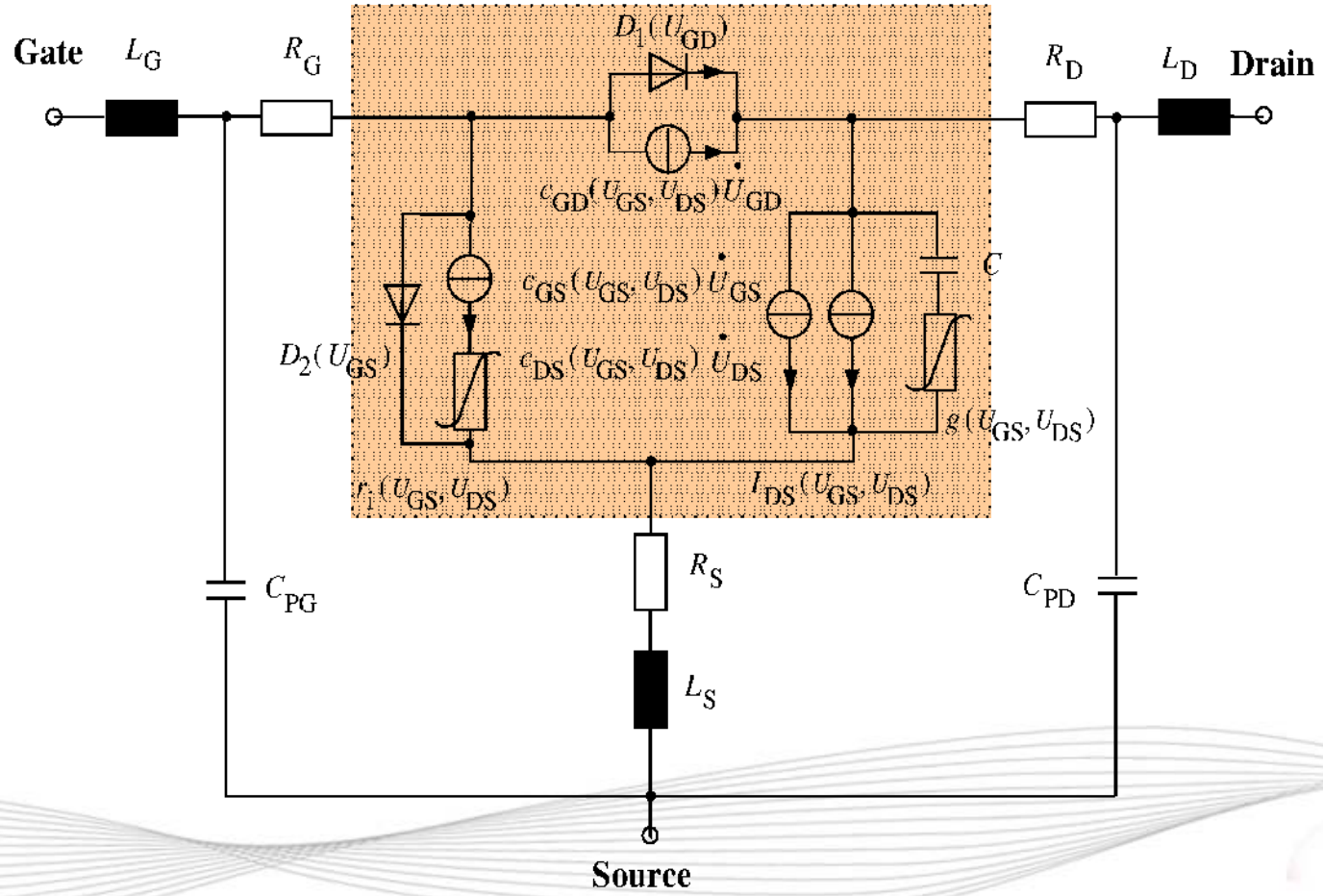
$$C'_{GS}\left(U_{GS} + u_{GS\sim}, U_{DS} + u_{DS\sim}\right) = C'_{GS}\left(U_{GS}, U_{DS}\right) + \left.\frac{\partial C'_{GS}\left(u_{GS}, u_{DS}\right)}{\partial u_{GS}}\right|_{\substack{u_{GS}=U_{GS} \\ u_{DS}=U_{DS}}} u_{GS\sim} + \left.\frac{\partial C'_{GS}\left(u_{GS}, u_{DS}\right)}{\partial u_{DS}}\right|_{\substack{u_{GS}=U_{GS} \\ u_{DS}=U_{DS}}} u_{DS\sim} + \ldots$$

GS-part of gate current

$$i_{GS} = c_{GS}\left(U_{GS}, U_{DS}\right)\frac{\mathrm{d}u_{GS}}{\mathrm{d}t}$$

Large signal simulation

$$i_G = \frac{dQ(u_{GS}, u_{DS})}{dt} = \frac{\partial Q(u_{GS}, u_{GD})}{\partial u_{GS}} \frac{du_{GS}}{dt} + \frac{\partial Q(u_{GS}, u_{GD})}{\partial u_{GD}} \frac{du_{GD}}{dt}$$



Large signal simulation

Due to designation of 2 voltages of Vgs, Vds and Vgd, the third voltage is always defined!

Case 1: Gate charge is known

$$Q_G = a u_{GS}^2 + b u_{GS} u_{DS} + a u_{DS}^2$$

$$i_G = \frac{dQ(u_{GS}, u_{DS})}{dt} = \frac{\partial Q_G(u_{GS}, u_{GD})}{\partial u_{GS}} \frac{du_{GS}}{dt} + \frac{\partial Q_G(u_{GS}, u_{GD})}{\partial u_{GD}} \frac{du_{GD}}{dt}$$

$$u_{DS} = f \cos(\omega t) \qquad u_{GS} = e \sin(\omega t)$$

$$i_G = \omega\left(A \sin(2\omega t) + B \cos(2\omega t)\right) \qquad A = ae^2 - cf^2 \qquad B = bef$$

Pure capacitive gate current, no DC part

Large signal simulation

Case 2: The capacitances are known

$$c_{DS}(u_{GS},u_{DS}) = \left.\frac{\partial Q_G}{\mathrm{d}u_{DS}}\right|_{u_{GS}=\text{const.}} = bu_{GS} + 2cu_{DS}$$

$$c_{GS}(u_{GS},u_{DS}) = \left.\frac{\partial Q_G}{\mathrm{d}u_{GS}}\right|_{u_{DS}=\text{const.}} = 2au_{GS} + bu_{DS}$$

$$i_{GS} = \omega\left(C + D\sin(2\omega t) + C\cos(2\omega t)\right) \qquad C = 0{,}5bef \qquad D = ae^2$$

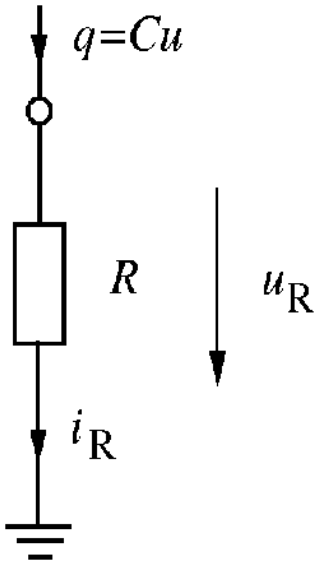
$$i_{GD} = \omega\left(-C + E\sin(2\omega t) + C\cos(2\omega t)\right) \qquad E = -cf^2$$

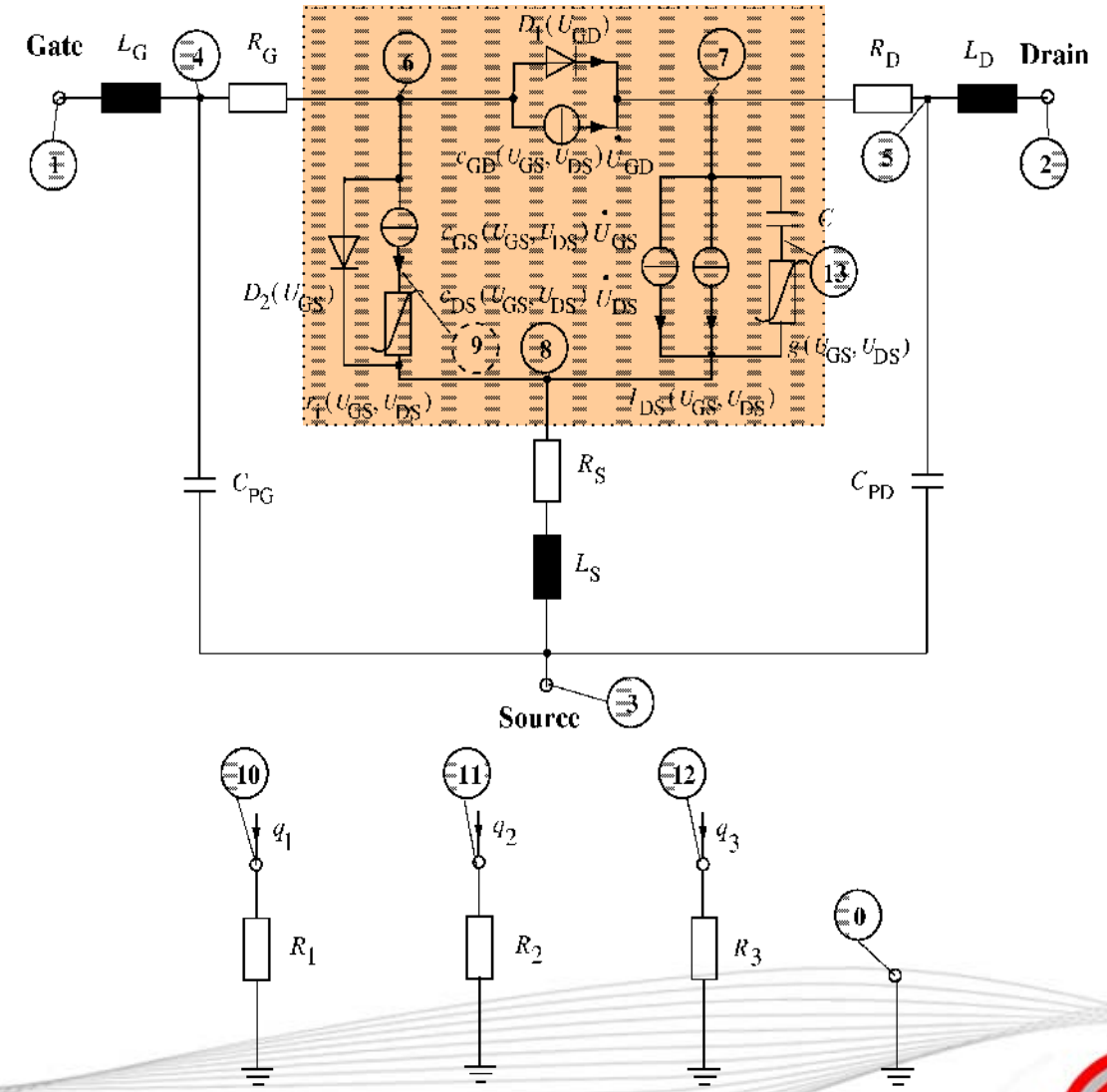
DC current parts, which compensate each other

Large signal simulation

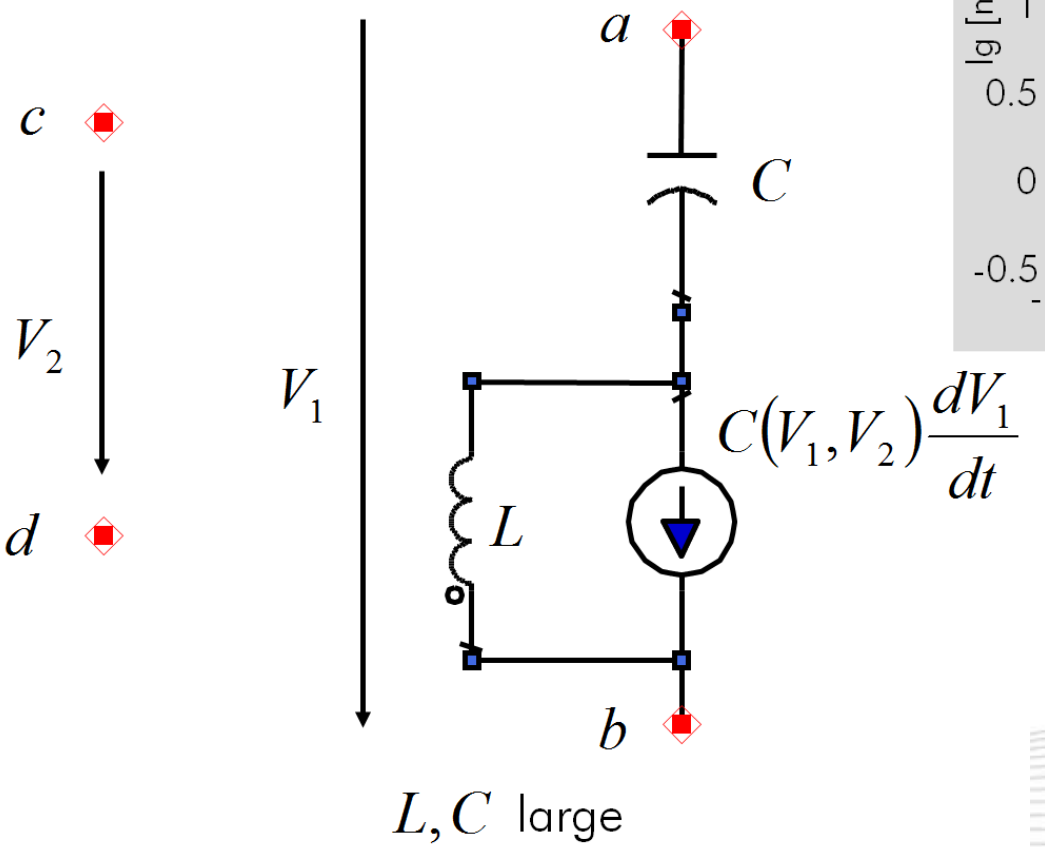
$$i_R = \dot{q} = C \cdot \dot{V}$$

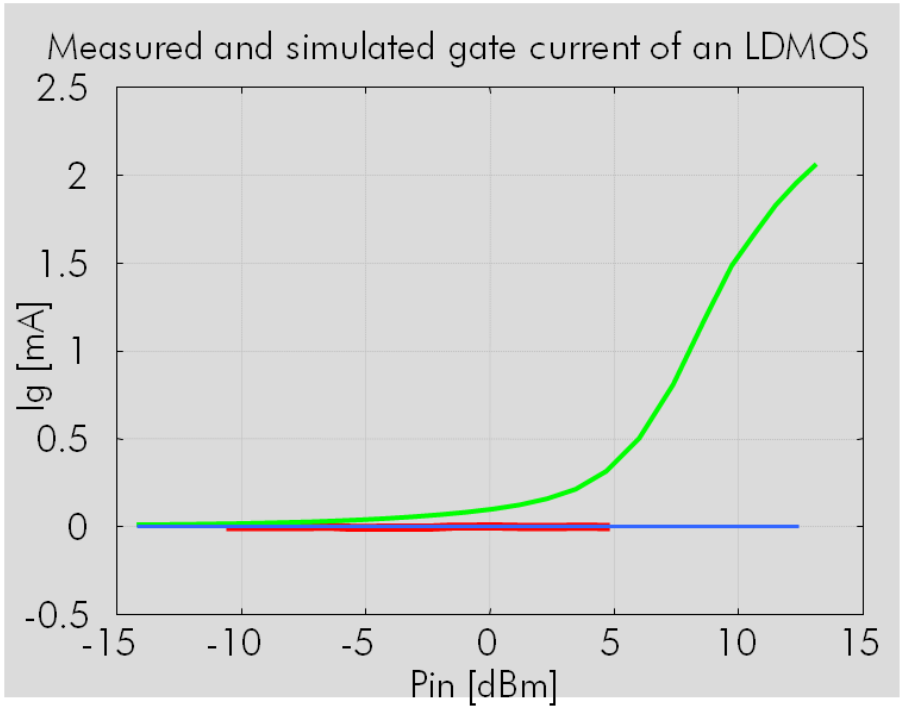
$$V_R = i_R R = CR \cdot \dot{V}$$





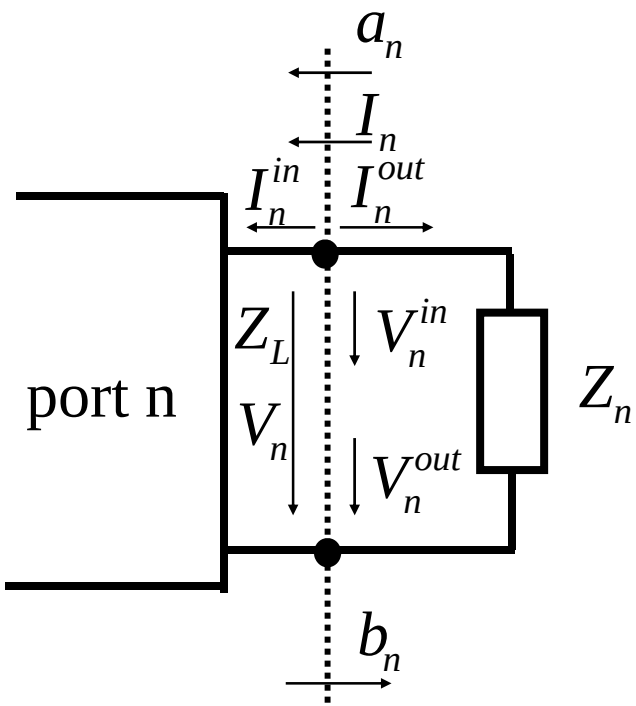
Example





Consistent implementation

Calculation of S-parameters using currents and voltages



Waves in an out of port n

$$a_n = \frac{V_n^{in}}{\sqrt{Z_{Ln}}} = I_n^{in}\sqrt{Z_{Ln}} \qquad b_n = \frac{V_n^{out}}{\sqrt{Z_{Ln}}} = I_n^{out}\sqrt{Z_{Ln}}$$

Voltages and currents on the line

$$u_n = \frac{V_n}{\sqrt{Z_{Ln}}} = \frac{V_n^{in} + V_n^{out}}{\sqrt{Z_{Ln}}} = a_n + b_n$$

$$i_n = I_n\sqrt{Z_{Ln}} = \left(I_n^{in} - I_n^{out}\right)\sqrt{Z_{Ln}} = a_n - b_n$$

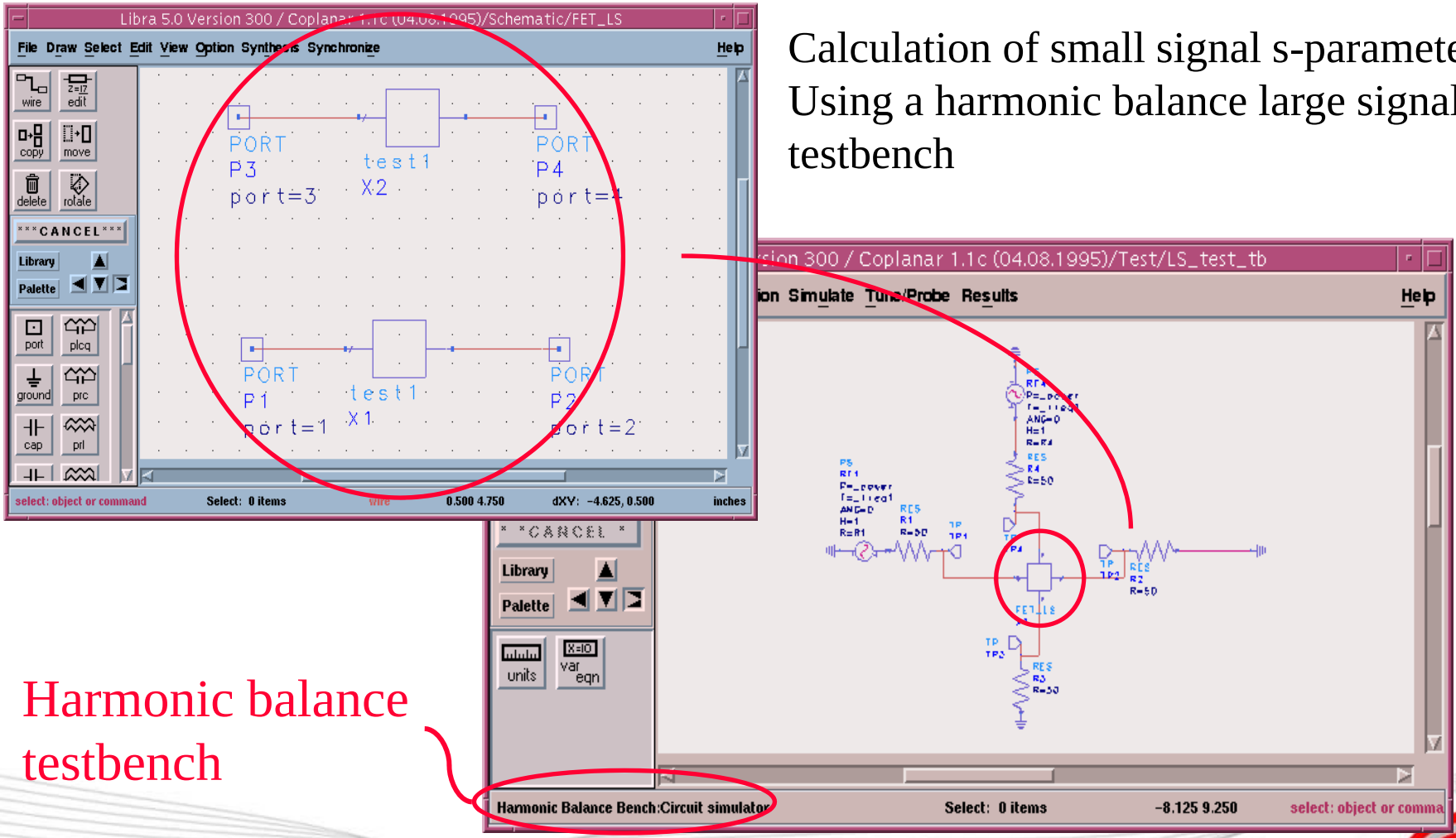
$$\Rightarrow \quad a_n = \frac{1}{2}(u_n + i_n) \qquad b_n = \frac{1}{2}(u_n - i_n) \quad \Rightarrow \quad \|b\| = \|s\| \cdot \|a\|$$

S-Matrix

Example

$$s_{11} = \left.\frac{b_1}{a_1}\right|_{a_{2=0}} \qquad s_{11,dB} = 20 \cdot \log\frac{u_1 - i_1}{u_1 + i_1}$$

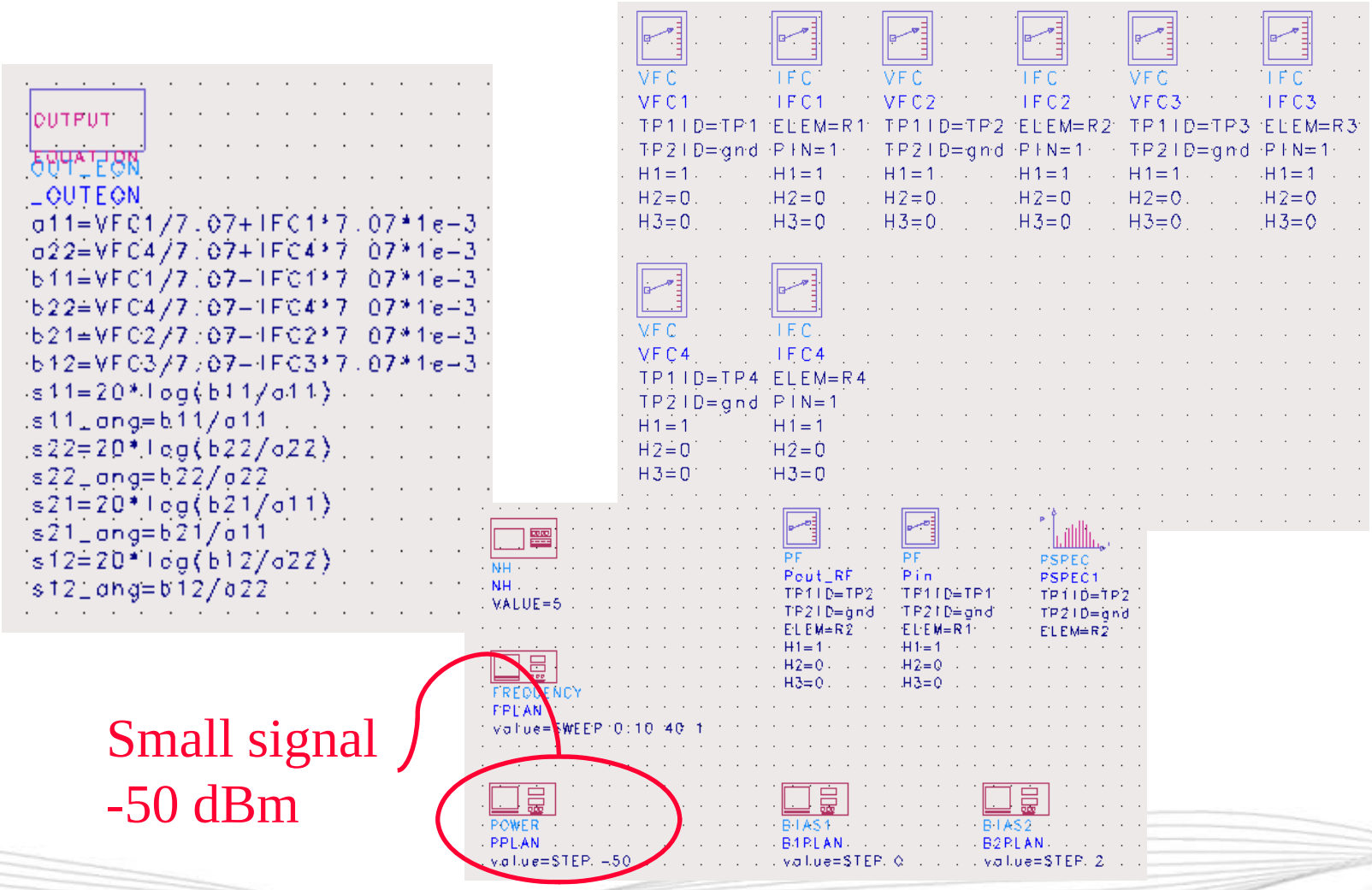
Consistent implementation



Calculation of small signal s-parameters Using a harmonic balance large signal testbench

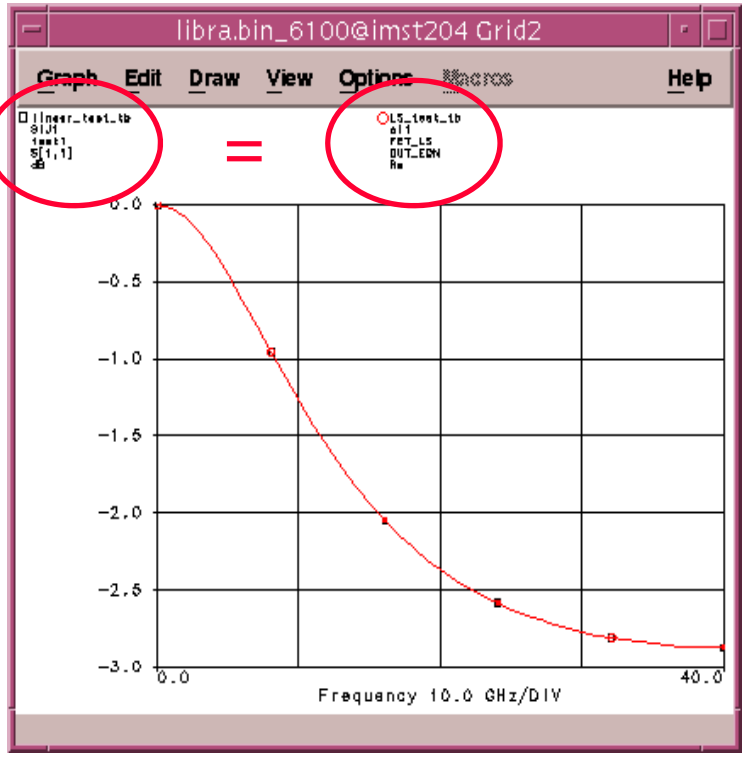
Harmonic balance testbench

Consistent implementation

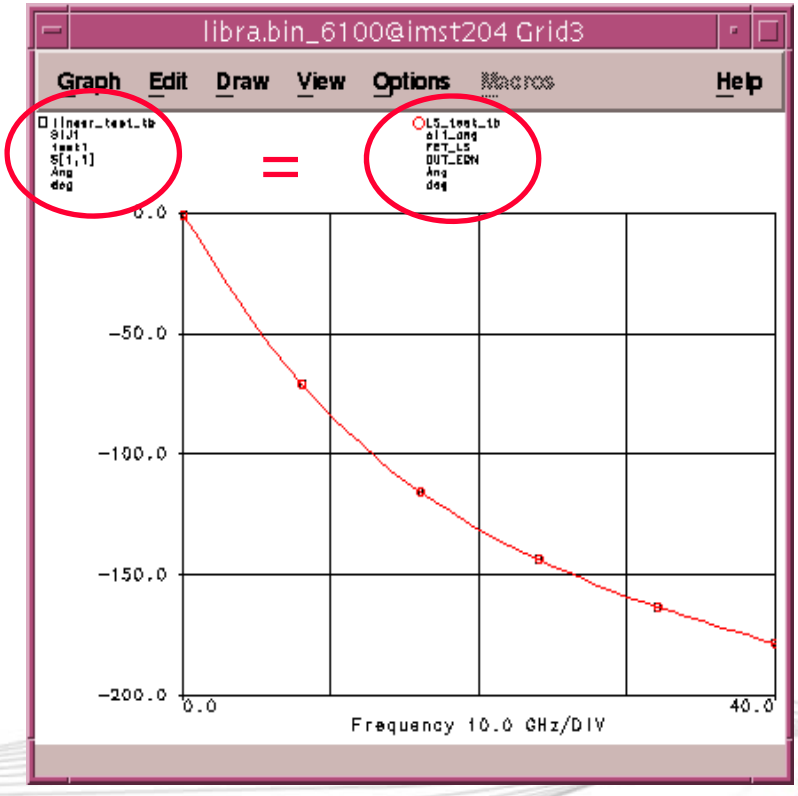


Small signal
-50 dBm

Consistent implementation



Phase(s_{11}), simulated using Small signal and HB testbench for very low input power (-50 dBm)

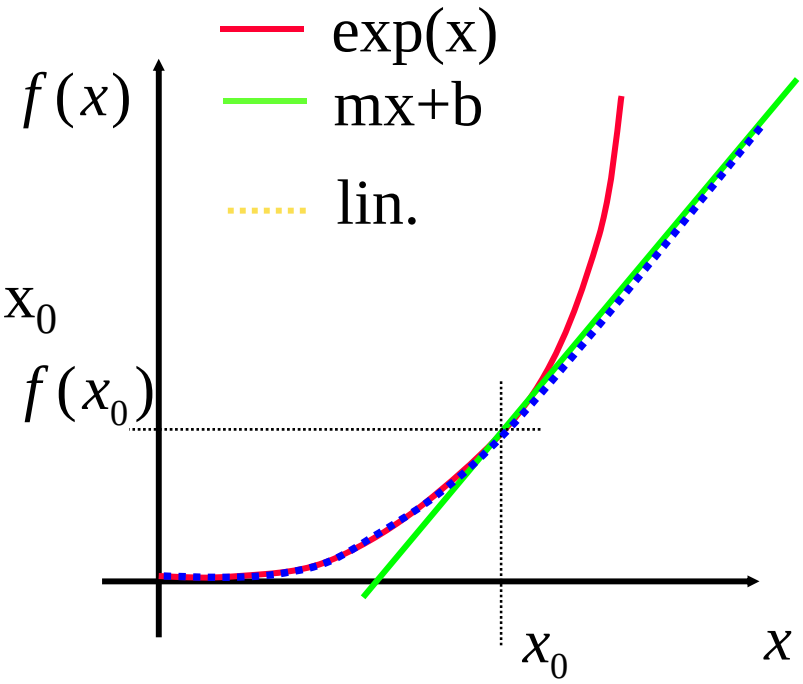


Mag(s_{11}), simulated using Small signal and HB testbench for very low input power (-50 dBm)

Needful things

Linearize exp functions

$$f(x)=\begin{cases}\exp(x) & x \le x_0 \\ mx+b & x > x_0\end{cases}$$



Function must be continuous at x_0

$$f_1(x_0) = f_2(x_0) \qquad \left.\frac{df_1}{dx}\right|_{x_0} = \left.\frac{df_2}{dx}\right|_{x_0}$$

$$\Rightarrow \quad \exp(x_0) = mx_0 + b$$

$$m = \exp(x_0)$$

$$\Rightarrow \quad b = \exp(x_0)(1-x_0) \Rightarrow f_2(x) = \exp(x_0)(x+1-x_0)$$

Noise sources

Thermal noise

$$\left\langle i_{th}^2 \right\rangle = \frac{4kT_0}{R}\Delta f$$

Popcorn (burst)-noise

$$\left\langle i_{burst}^2 \right\rangle = KB\frac{I_D^{CF}}{1+\left(\frac{f}{f_{CF}}\right)^2}\Delta f$$

Shot-noise

$$\left\langle i_{shot}^2 \right\rangle = 2qI_D\Delta f$$

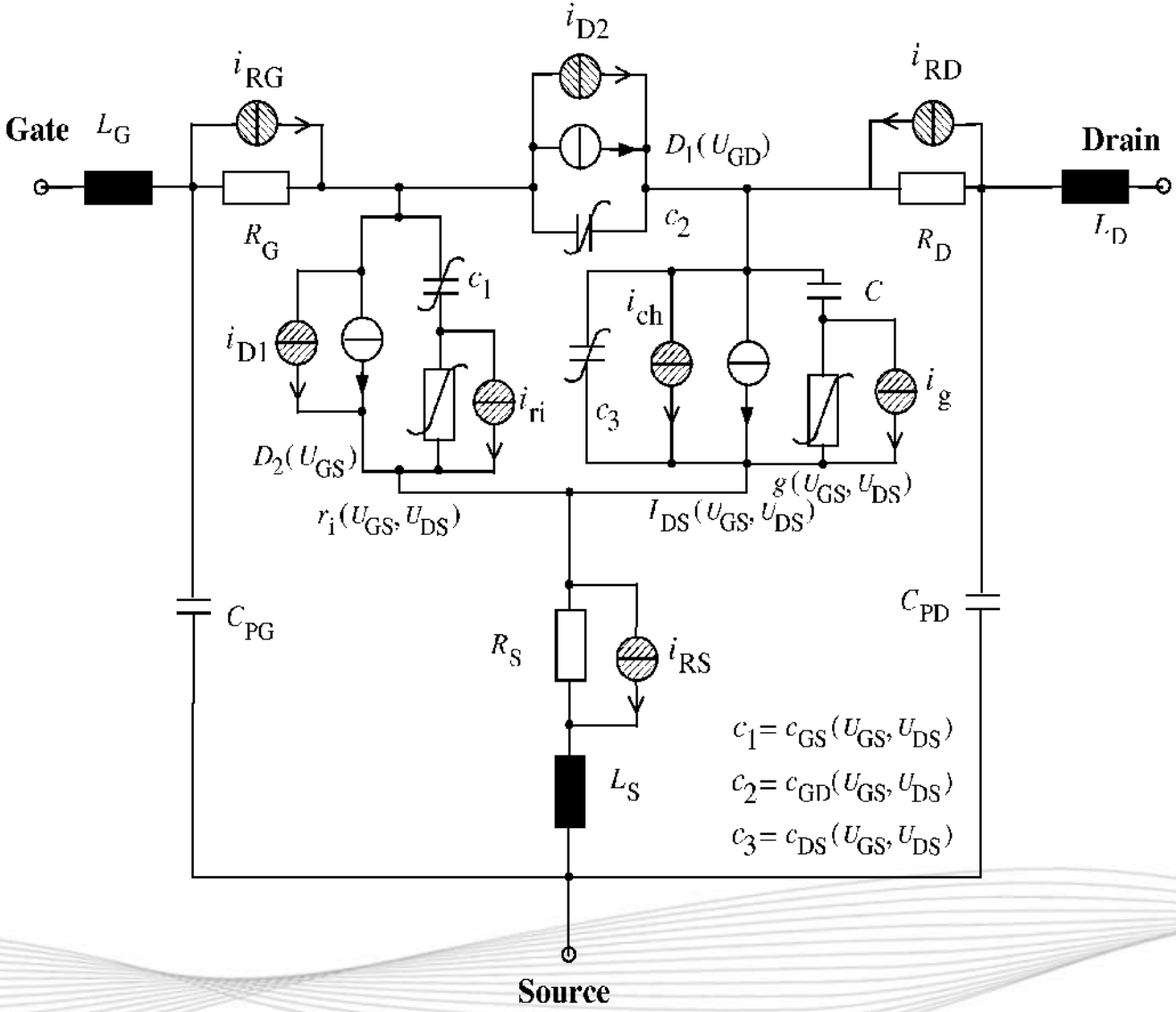
1/f (flicker)-noise

$$\left\langle i_{1/f}^2 \right\rangle = KF\frac{I_D^{AF}}{f^{FFE}}\Delta f$$

Channel noise

$$\left\langle i_c^2 \right\rangle = \frac{8kTg_m}{3}\Delta f$$

Noise equivalent ciruit

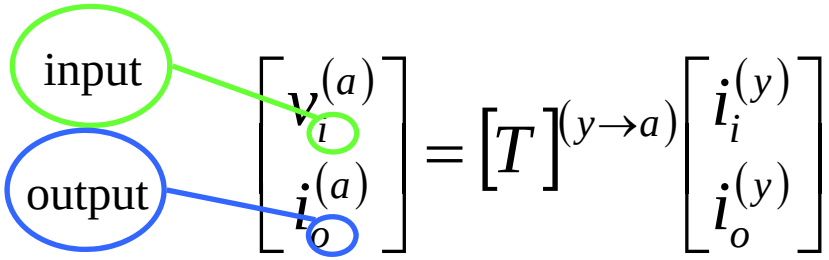


Noisy 2-ports

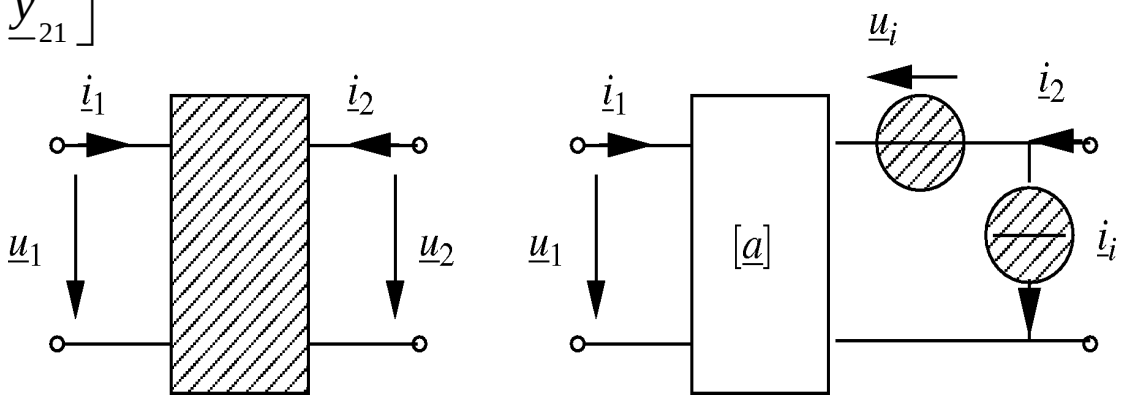
Transformation matrix

$$[T]^{(y\to a)} = \begin{bmatrix} 0 & -\dfrac{1}{\underline{y}_{21}} \\ 1 & -\dfrac{\underline{y}_{11}}{\underline{y}_{21}} \end{bmatrix}$$

Noise matrix



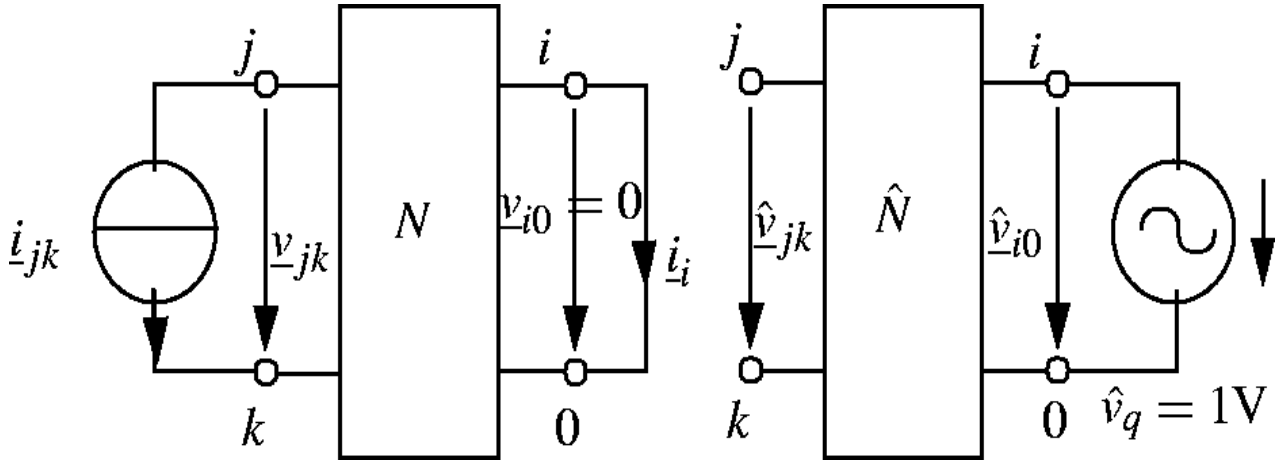
Transformation of noise sources.



Correlation matrix, calculation of noise power

$$[\underline{C}]^{(a)} = \frac{1}{4kT\Delta f}\left(\begin{bmatrix} \underline{v}_i \\ \underline{i}_i \end{bmatrix}\begin{bmatrix} \underline{v}_i^* & \underline{i}_i^* \end{bmatrix}\right)$$

Separation of noise sources



Calculation of transformation fucntion

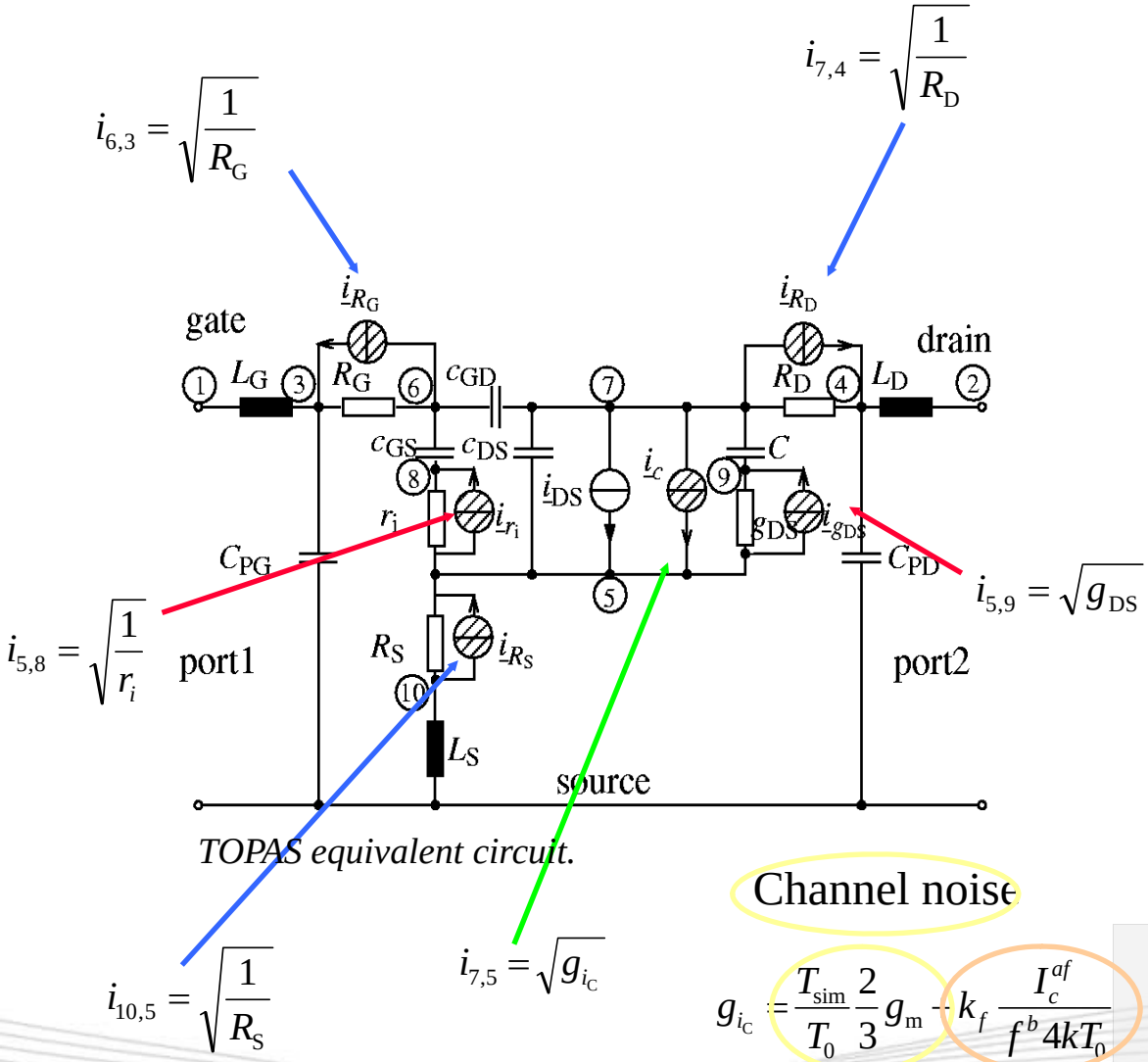
Network N **Adjoint network**

Y-Matrix **transposed Y-Matrix**

Current transforming function

$$\alpha_{i,jk} = \frac{i_i}{i_{jk}} = -\frac{\hat{v}_{jk}}{\hat{v}_q}$$

FET example



TOPAS equivalent circuit.

Noise current matrix

$$[i_N] = \sqrt{4kT\Delta f} \cdot$$

$$\begin{pmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & i_{5,8} & i_{5,9} & 0 \\
0 & 0 & i_{6,3} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & i_{7,4} & i_{7,5} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & i_{10,5} & 0 & 0 & 0 & 0 & 0
\end{pmatrix}$$

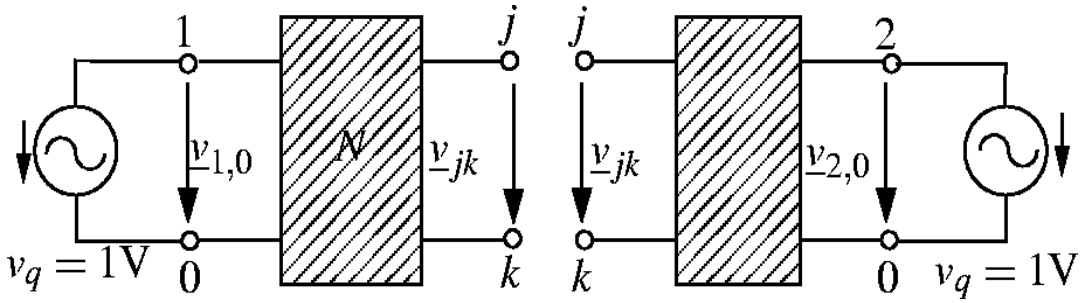
Channel noise

$$g_{i_C} = \frac{T_{sim}}{T_0}\frac{2}{3}g_m + k_f \frac{I_c^{af}}{f^b 4kT_0}$$

1/f-noise

Tellegen Thoerem

Y-Matrix → Z-Matrix → Y_{2x2}-Matrix → $[\underline{y}_T] = [\underline{y}]^T$



Tellegen Theorem for noisy n-ports

Adjoined network for calculation of transformation function

$$i_{Q_1} = v_q \cdot \underline{y}_{T,2\times2_{1,1}} \quad \text{and} \quad i_{Q_2} = v_q \cdot \underline{y}_{T,2\times2_{2,2}}$$

Tellegen Theorem

$$\begin{bmatrix} i_{Q1} \\ \vdots \\ i_{Q10} \end{bmatrix} = \begin{bmatrix} y_{T1,1} & \cdots & y_{T1,10} \\ \vdots & \ddots & \vdots \\ y_{T10,1} & \cdots & y_{T10,10} \end{bmatrix} \begin{bmatrix} v_1 \\ \vdots \\ v_{10} \end{bmatrix}$$

Solving the equation system for the voltagesusing the Gaussian algorithm

Voltage transformation factor

One single noise source
at Eingang, one at output

$$[T]^{(y \to a)} = \begin{bmatrix} 0 & -\dfrac{1}{\underline{y}_{2\times 2_{21}}} \\ 1 & -\dfrac{\underline{y}_{2\times 2_{11}}}{\underline{y}_{2\times 2_{21}}} \end{bmatrix}$$

1 current source,
1 voltage source
at output

Correlation matrix

$$F = 1 - \frac{T_{sim}}{T_o} \frac{\left|\underline{y}_G\right|^2 C_{11}^{(a)} + C_{22}^{(a)} + 2\Re\left\{\underline{y}_G \underline{C}_{12}^{a}\right\}}{g_G}$$

$$R_n = \frac{T_{sim}}{T_0} C_{11}^{a}$$

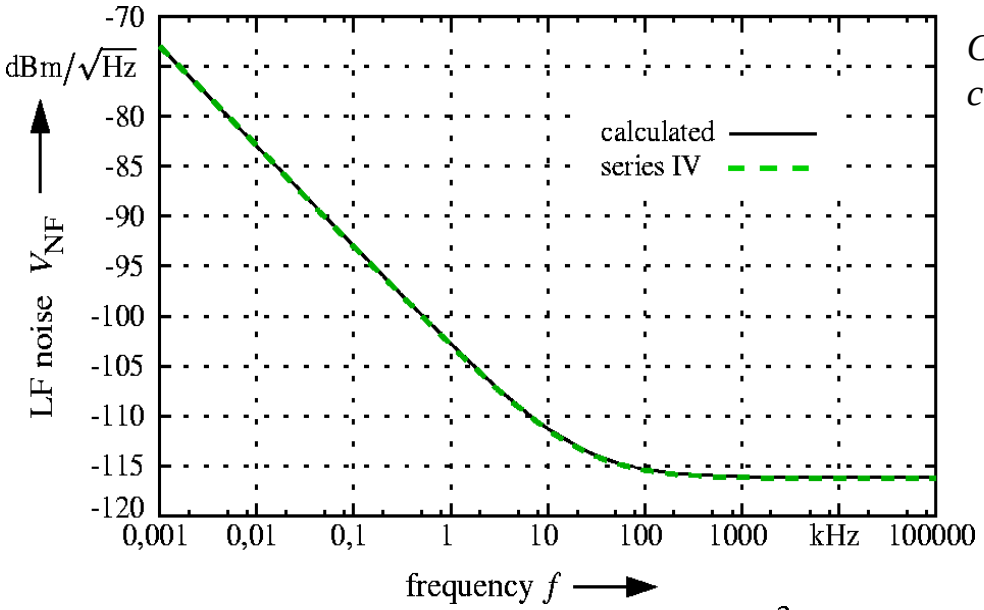
Korrelationsmatrix

$$\left[\underline{C}\right]^{(a)} = \left[T\right]^{(y\to a)} \left[\underline{C}\right]^{(y)} \left[T\right]^{(y\to a)^+}$$

$$V_{NF}\left[\mathrm{dBm}/\sqrt{\mathrm{Hz}}\right] = 20\log\left(\sqrt{\frac{T_{sim}}{T_0} \cdot i_0 i_0^* \frac{50\Omega}{50\Omega\Re\left(\underline{y}_{2\times 2_{22}}\right)+1}} \cdot 1000\right)$$

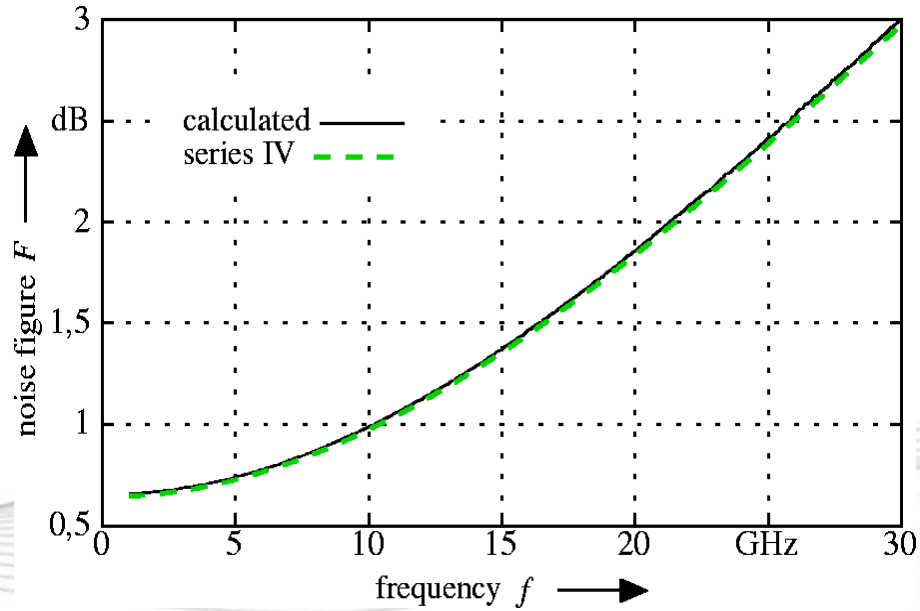
$$\Gamma_{G_{opt}} = \frac{1 - \underline{y}_{G_{opt}} Z_0}{1 + \underline{y}_{G_{opt}} Z_0}$$

Verifications

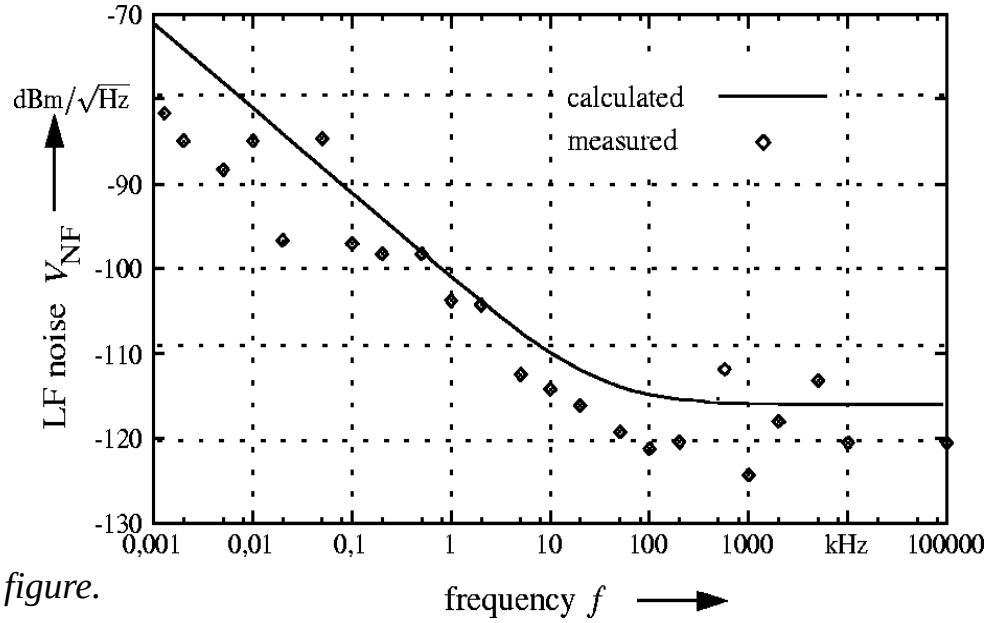


Calculation of 1/f noise..Simulation in comparison to calcualtion using the porposed algorithm.

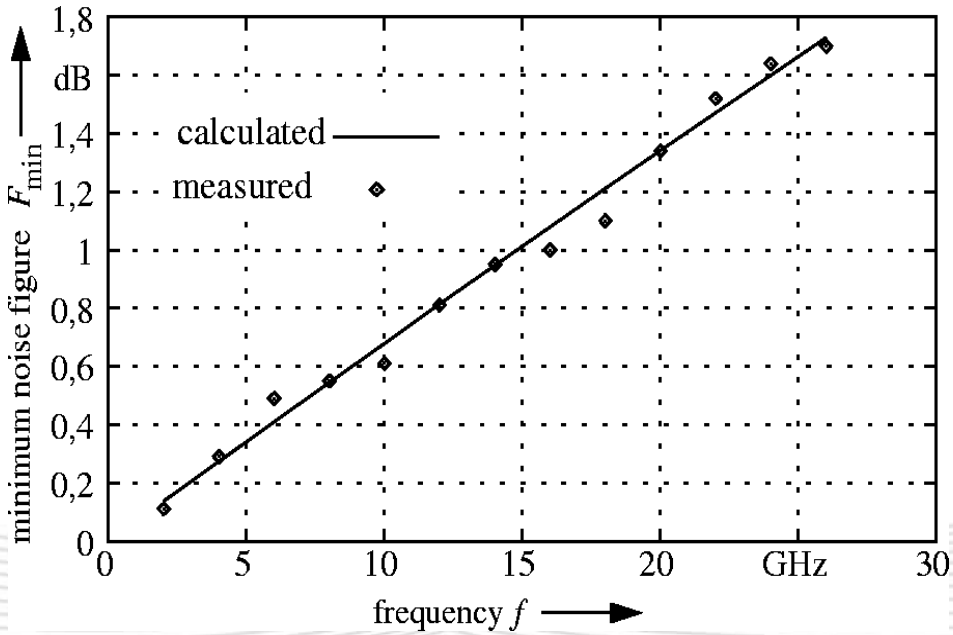
Calcualtion of noise figure NF. Comparison of simulation and calculation.



Verifications

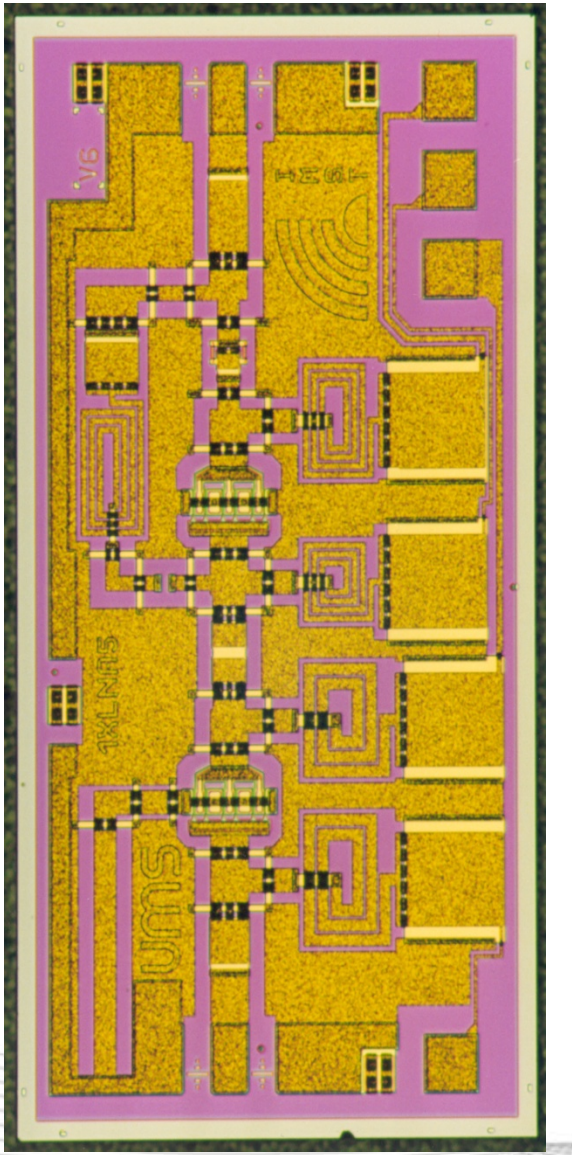


Simulation and measurement of 1/noise.

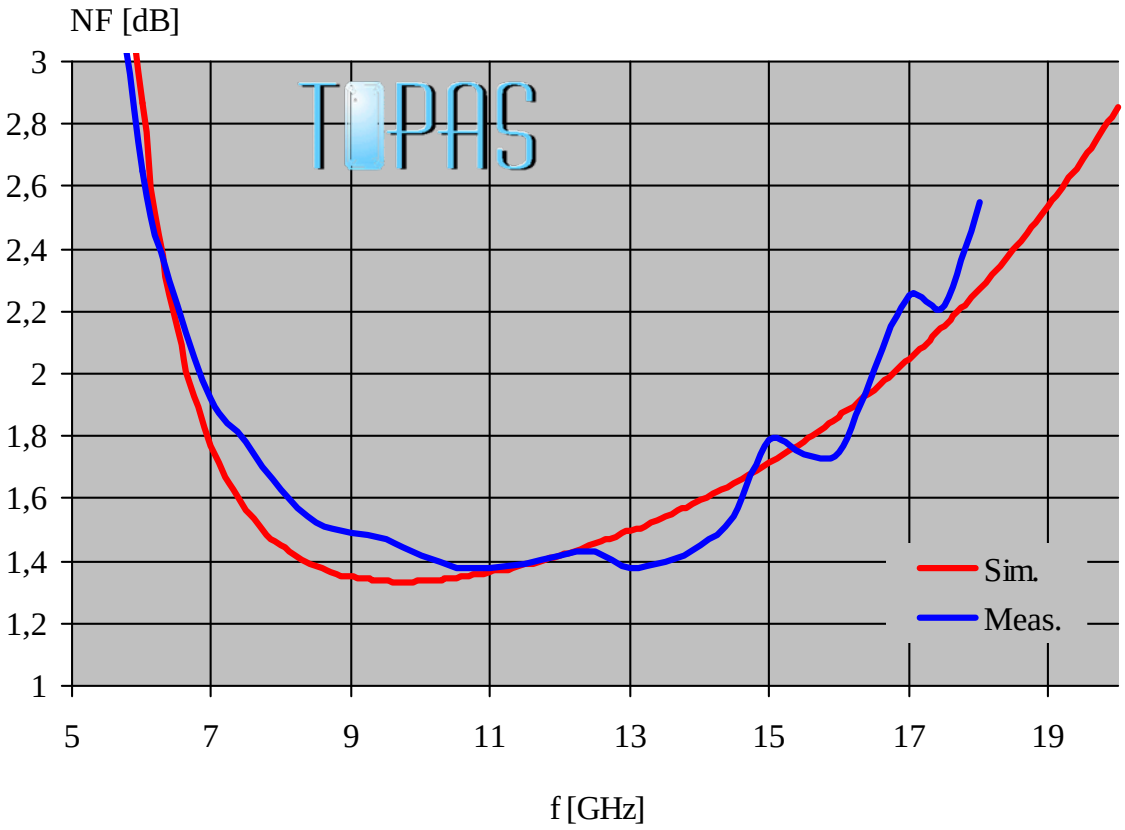


Simulation and measurement of minimum noise figure.

Verifications



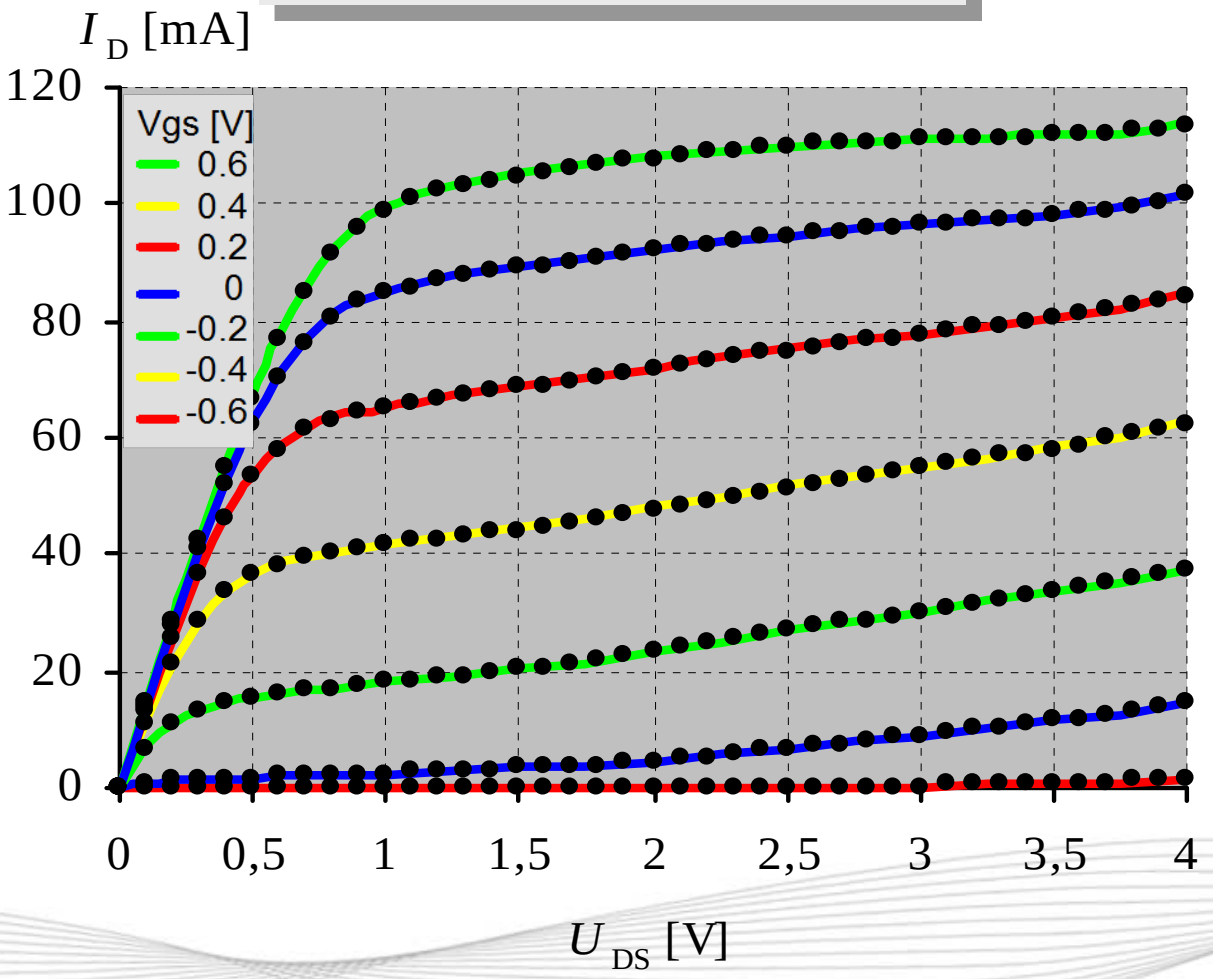
Realized LNA



Minimum noise figure, simulation versus measurement.

Verfications

UMS 4x50 μm
HEMT

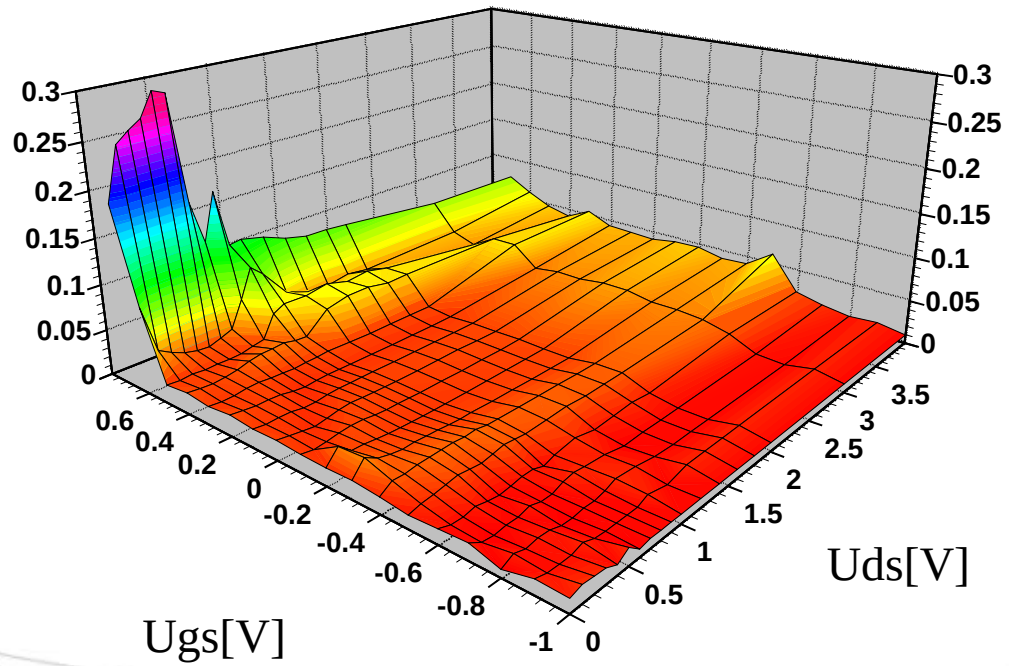


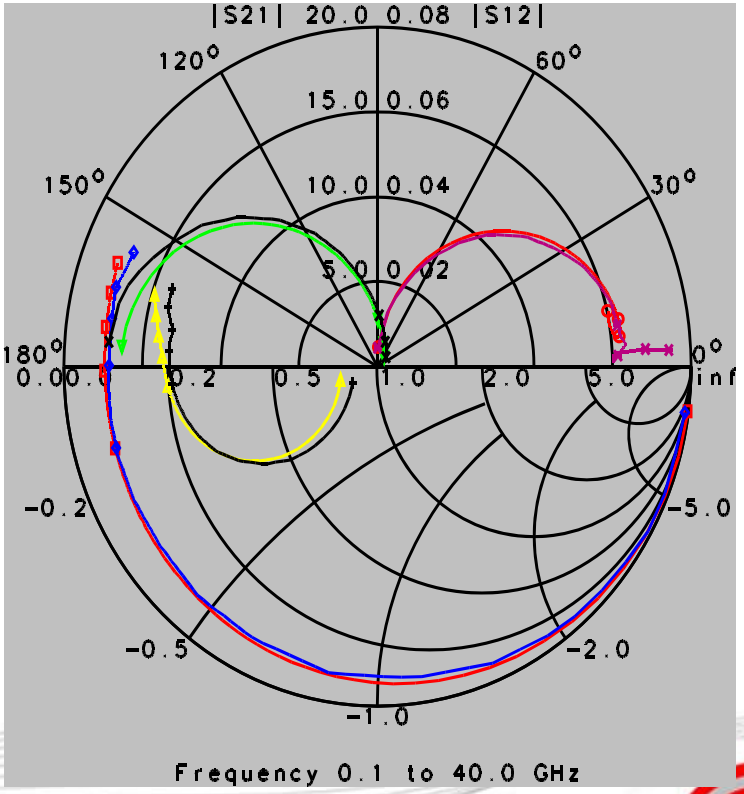
Verifications

Deviations
6x20 µm HEMT

4x50µm ⇗ 8x75µm
V_{GS} = 0 V, V_{DS} = 2 V

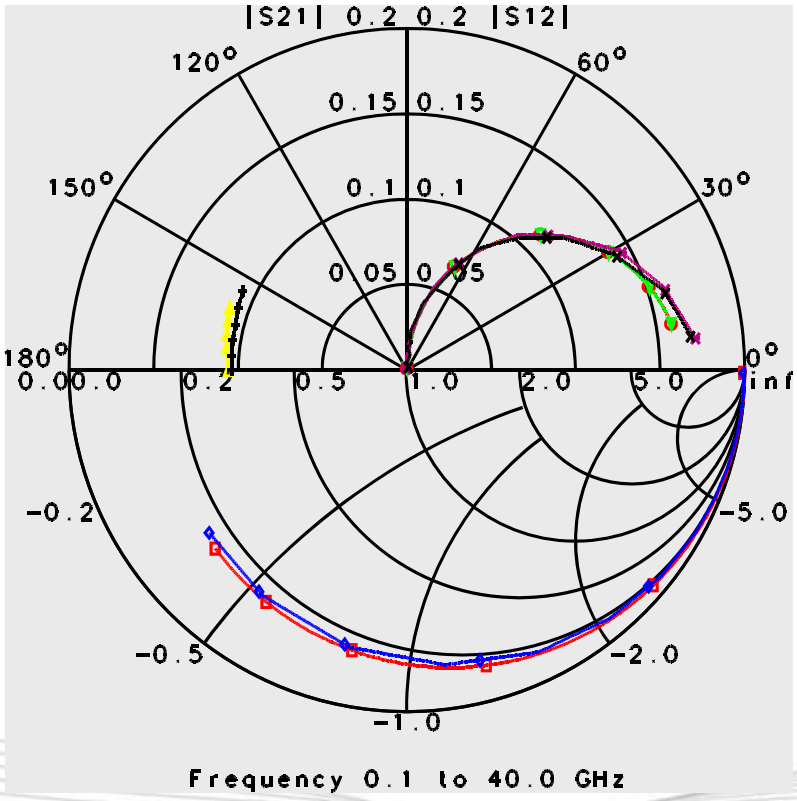
Fehler



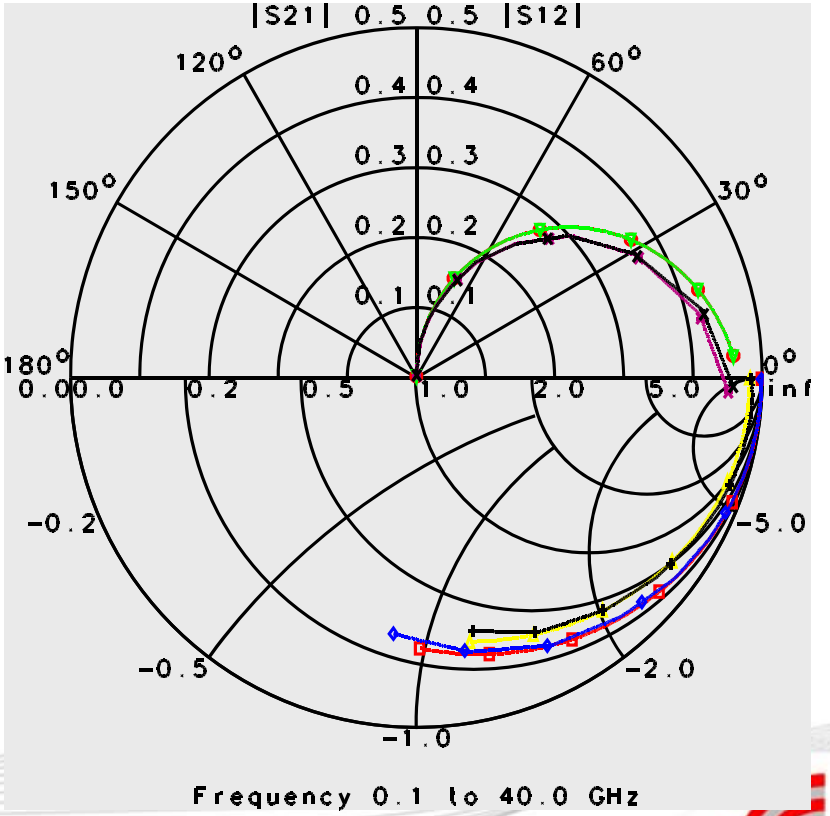


Verifications

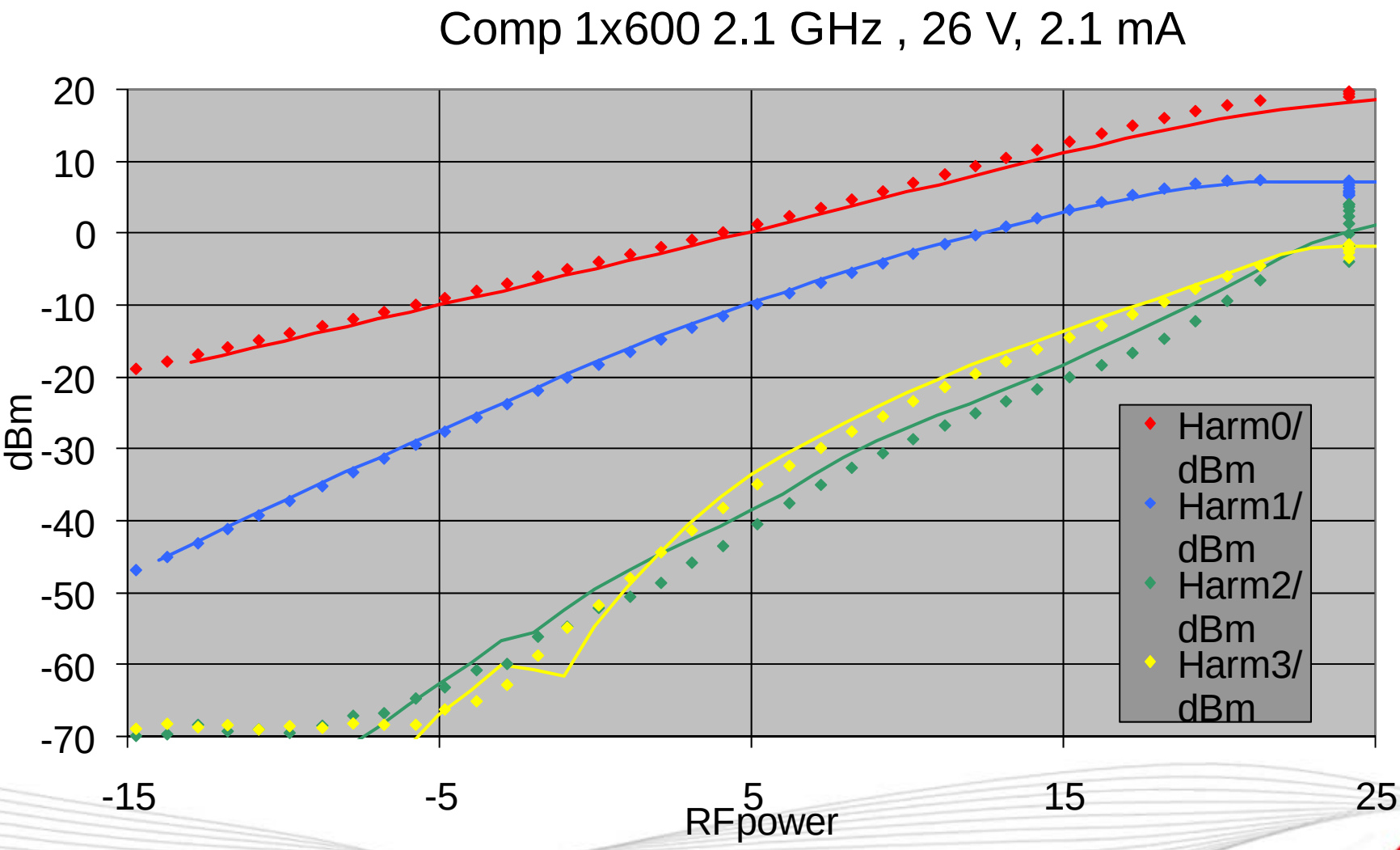
4x50 µm ⇗ 2x40 µm
$V_{GS} = 0$ V, $V_{DS} = 0$ V



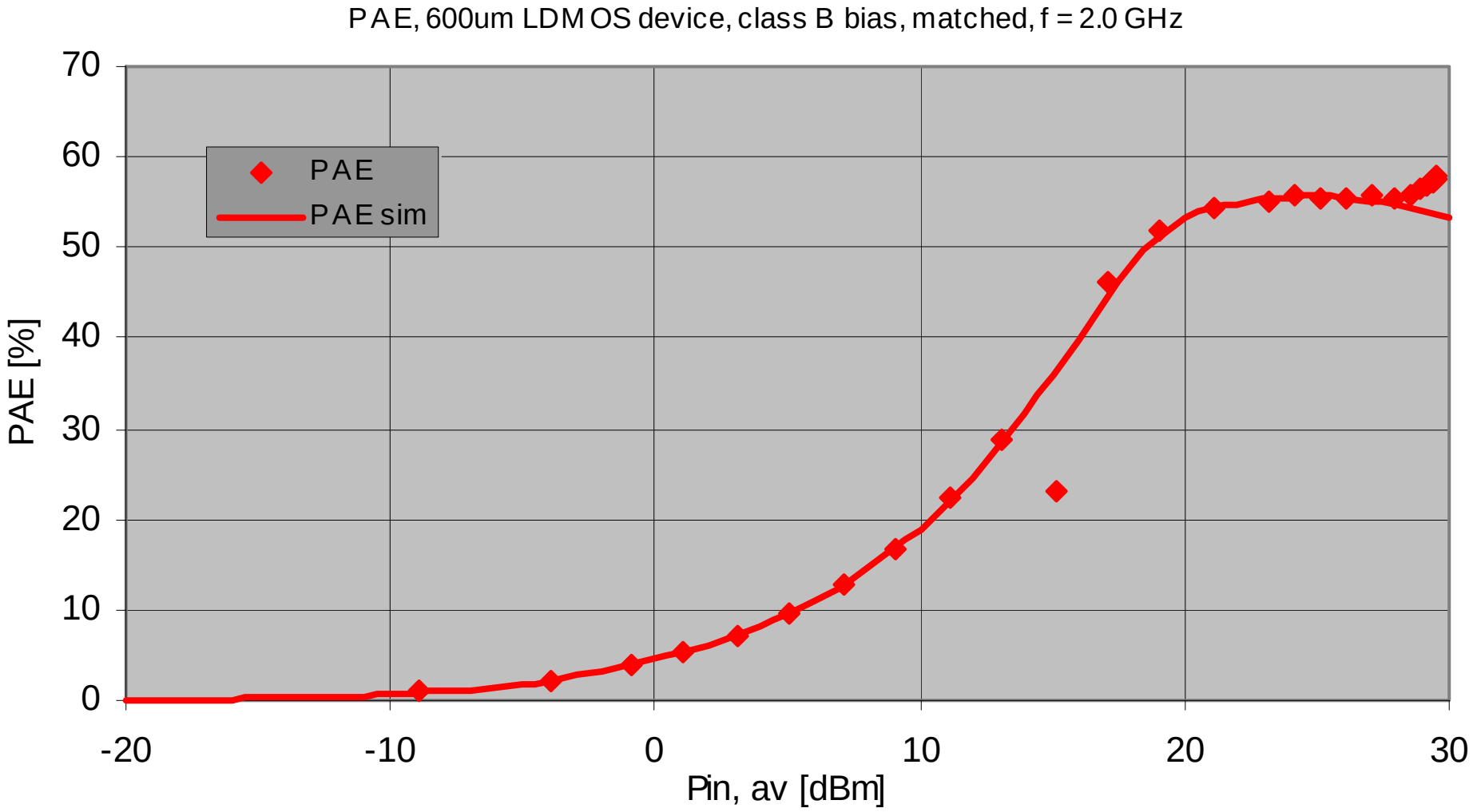
4x50 µm ⇗ 2x40 µm
$V_{GS} = -0.8$ V, $V_{DS} = 2$ V



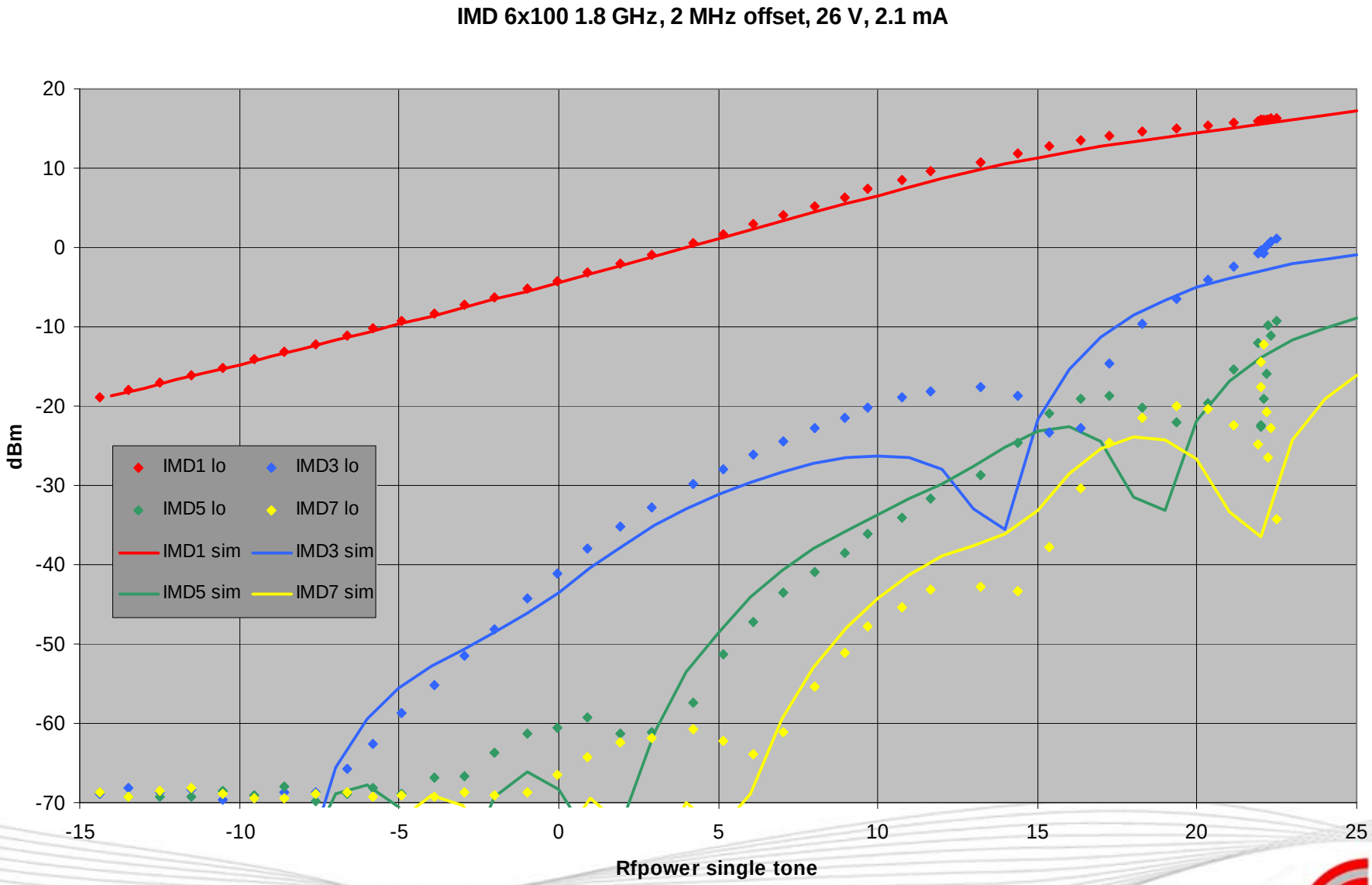
Verifications



Verifications

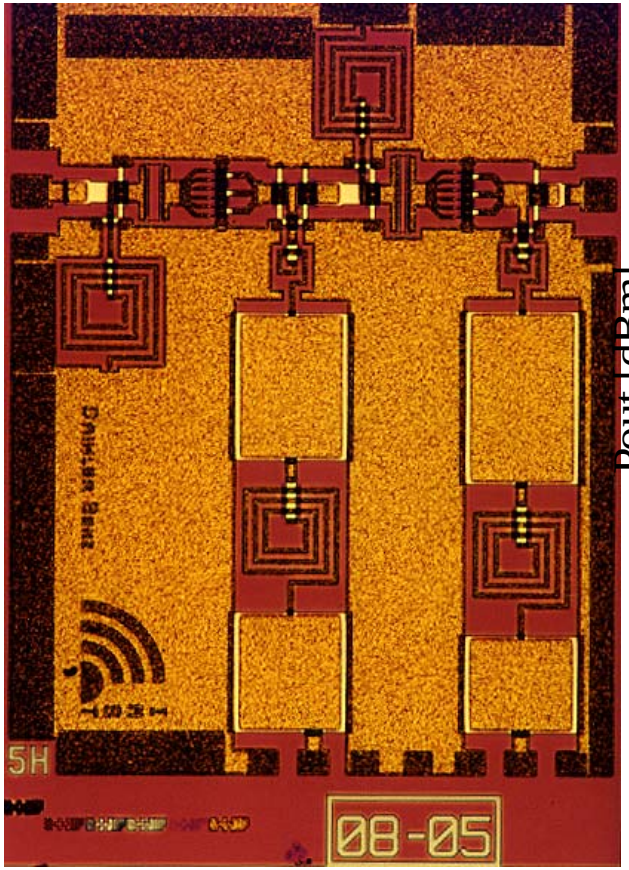


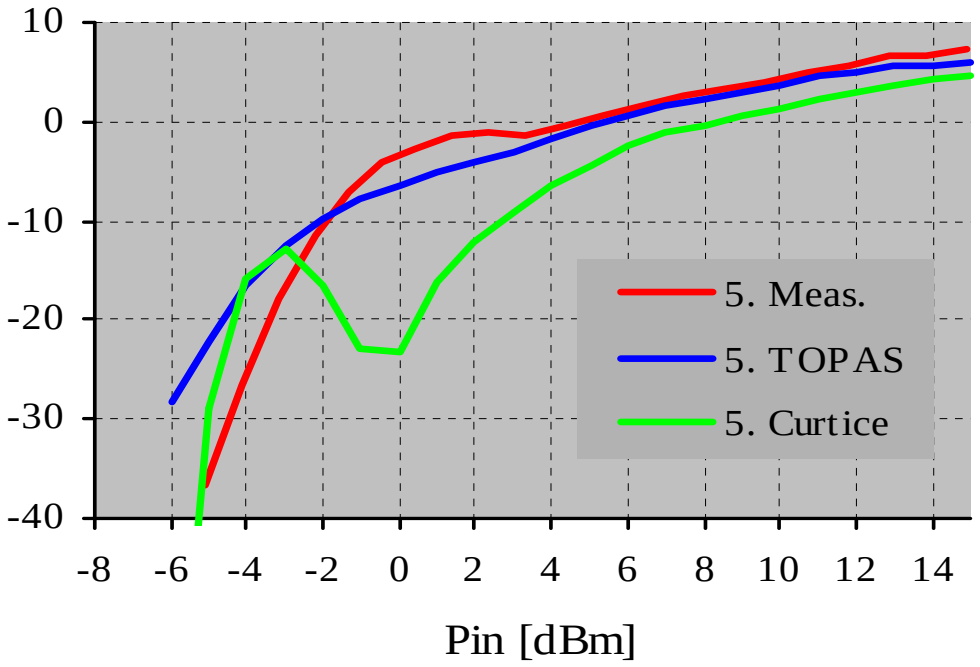
Verifications



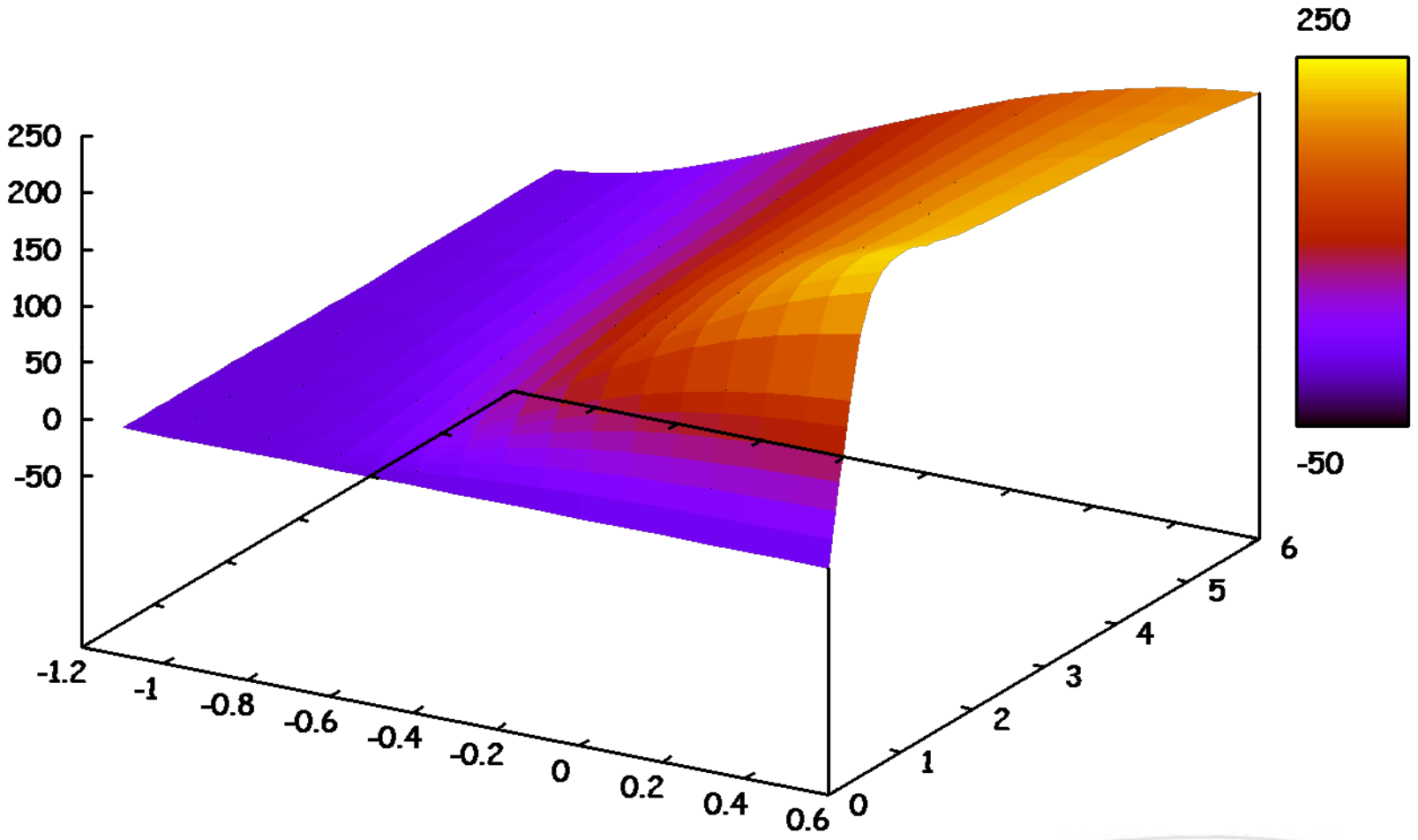
Verifications

Times 5 multiplier

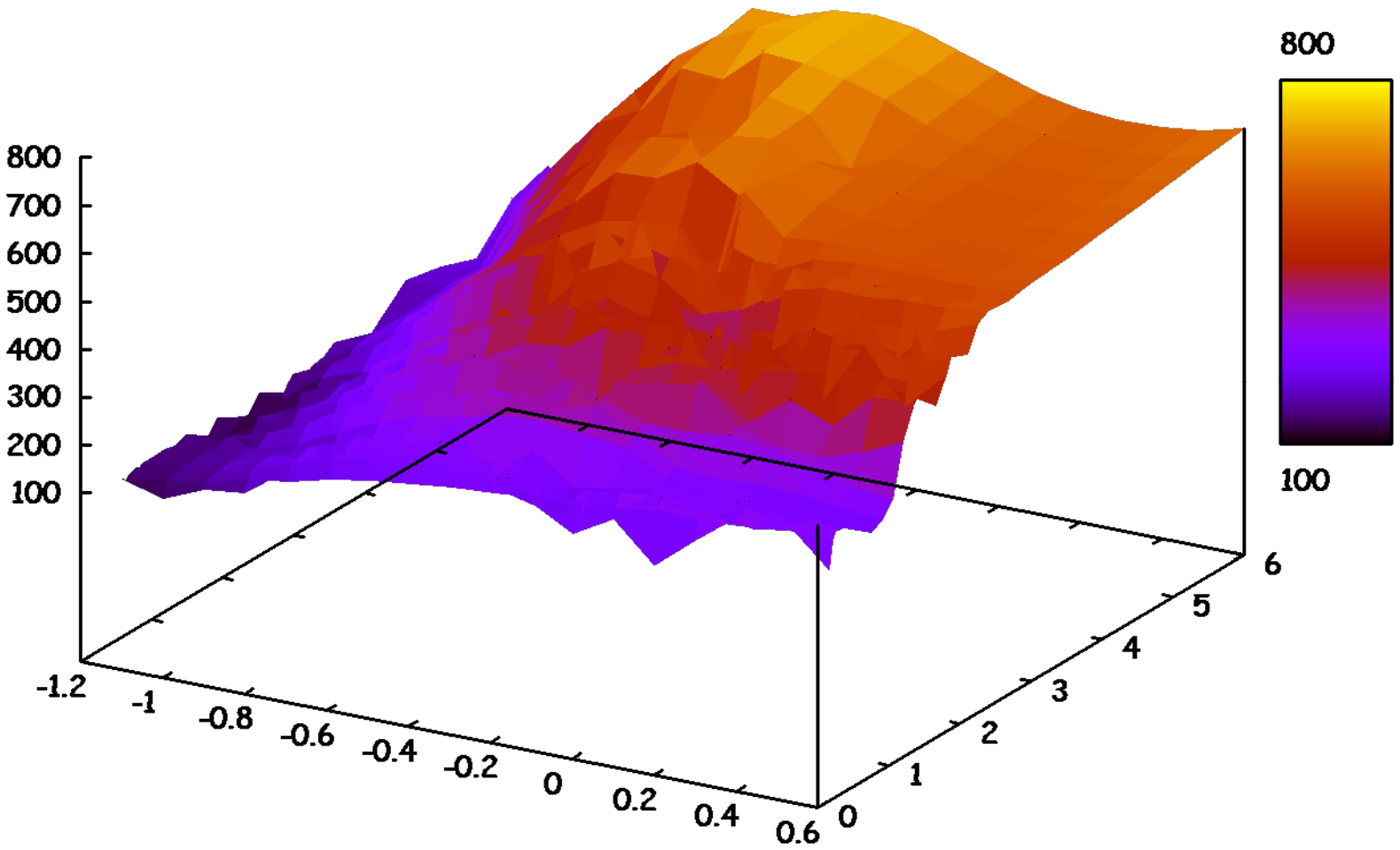




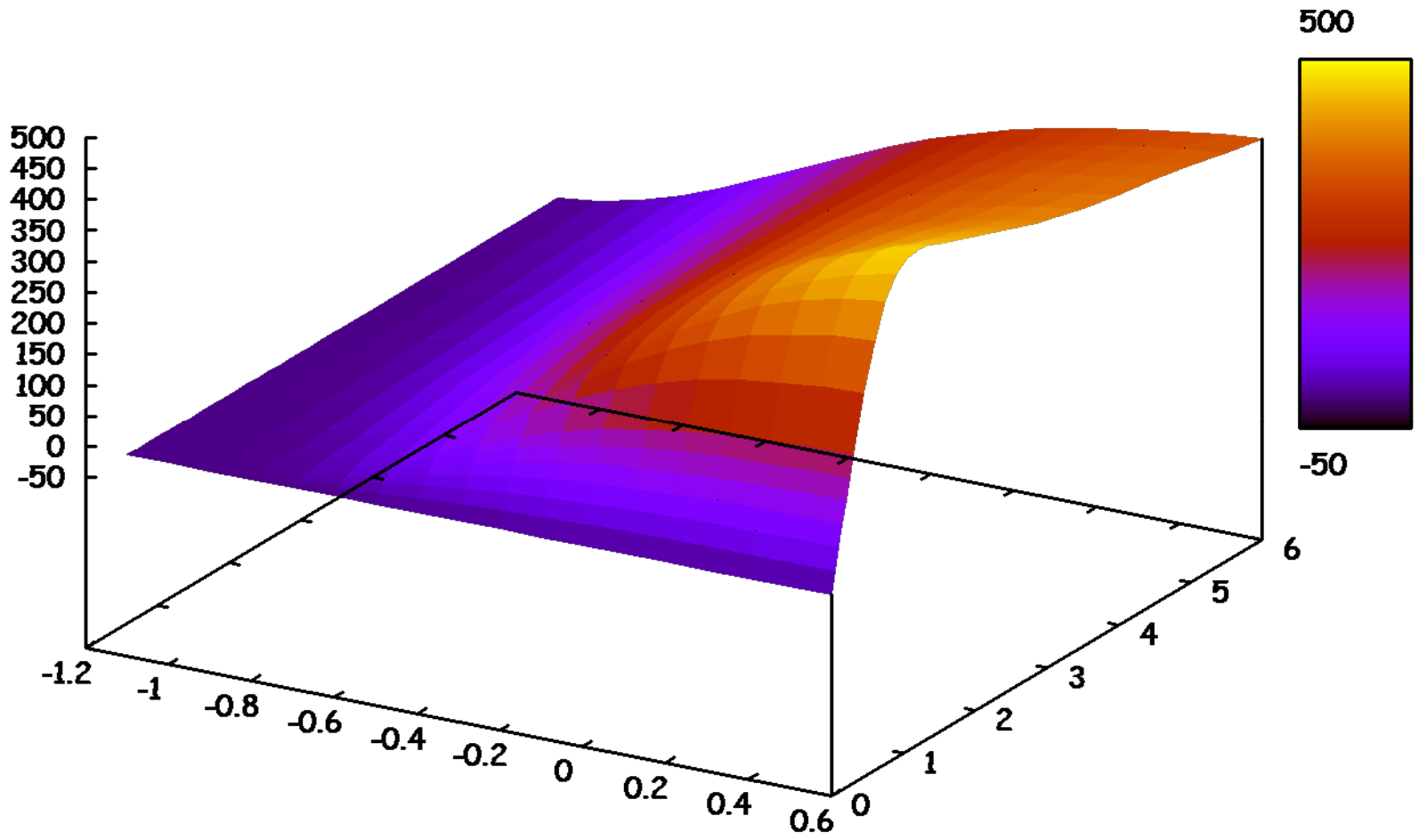
Oscillations



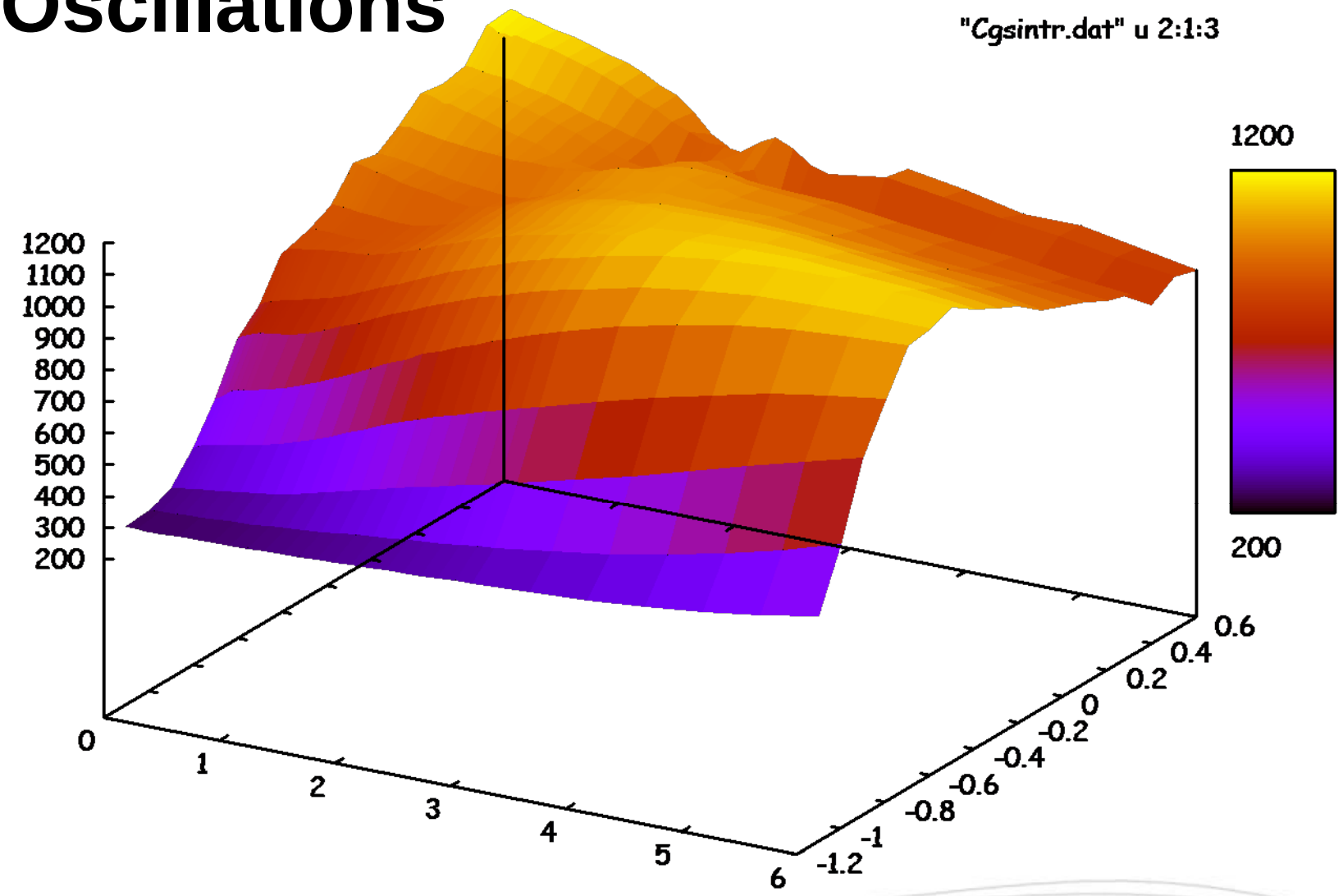
Oscillations



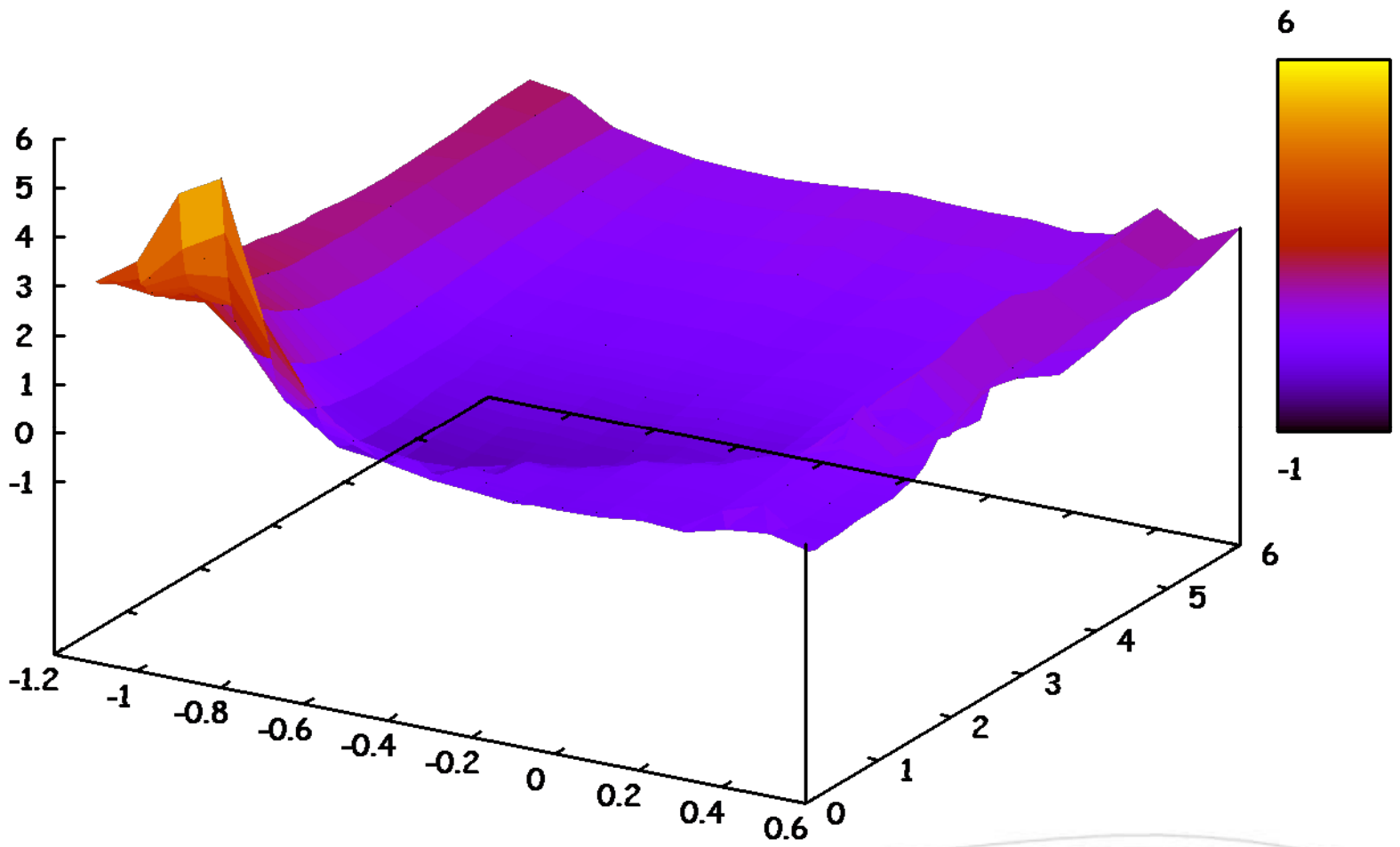
Oscillations



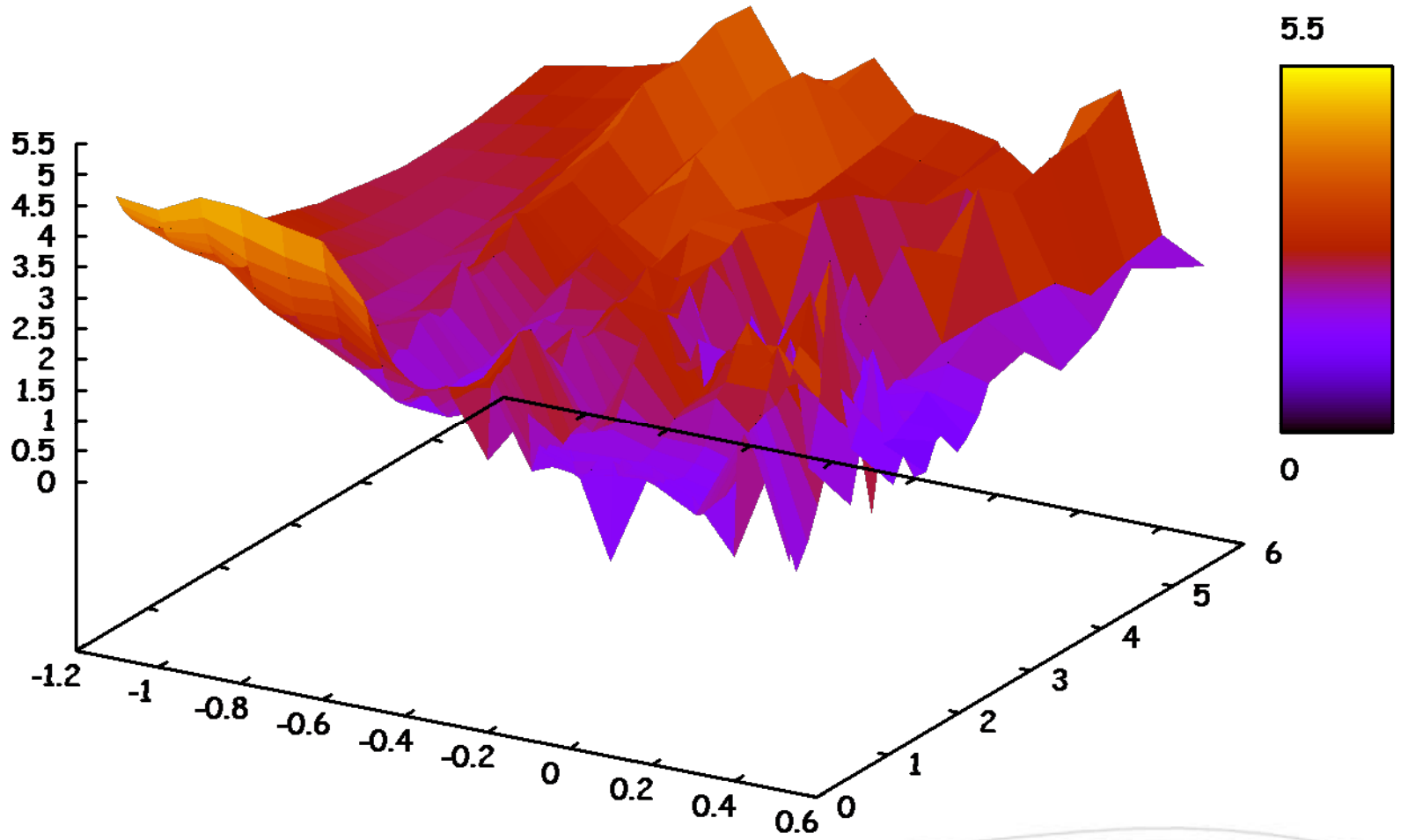
Oscillations



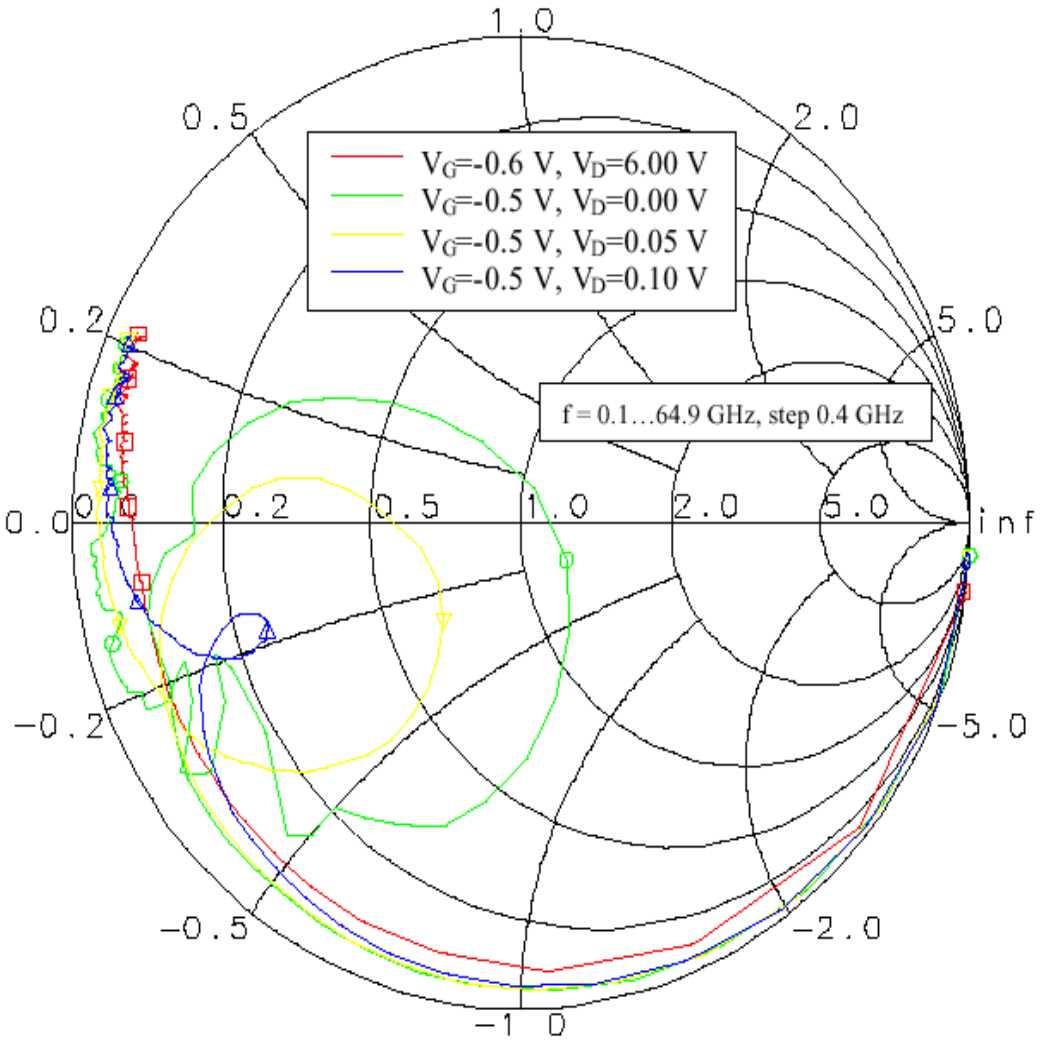
Oscillations



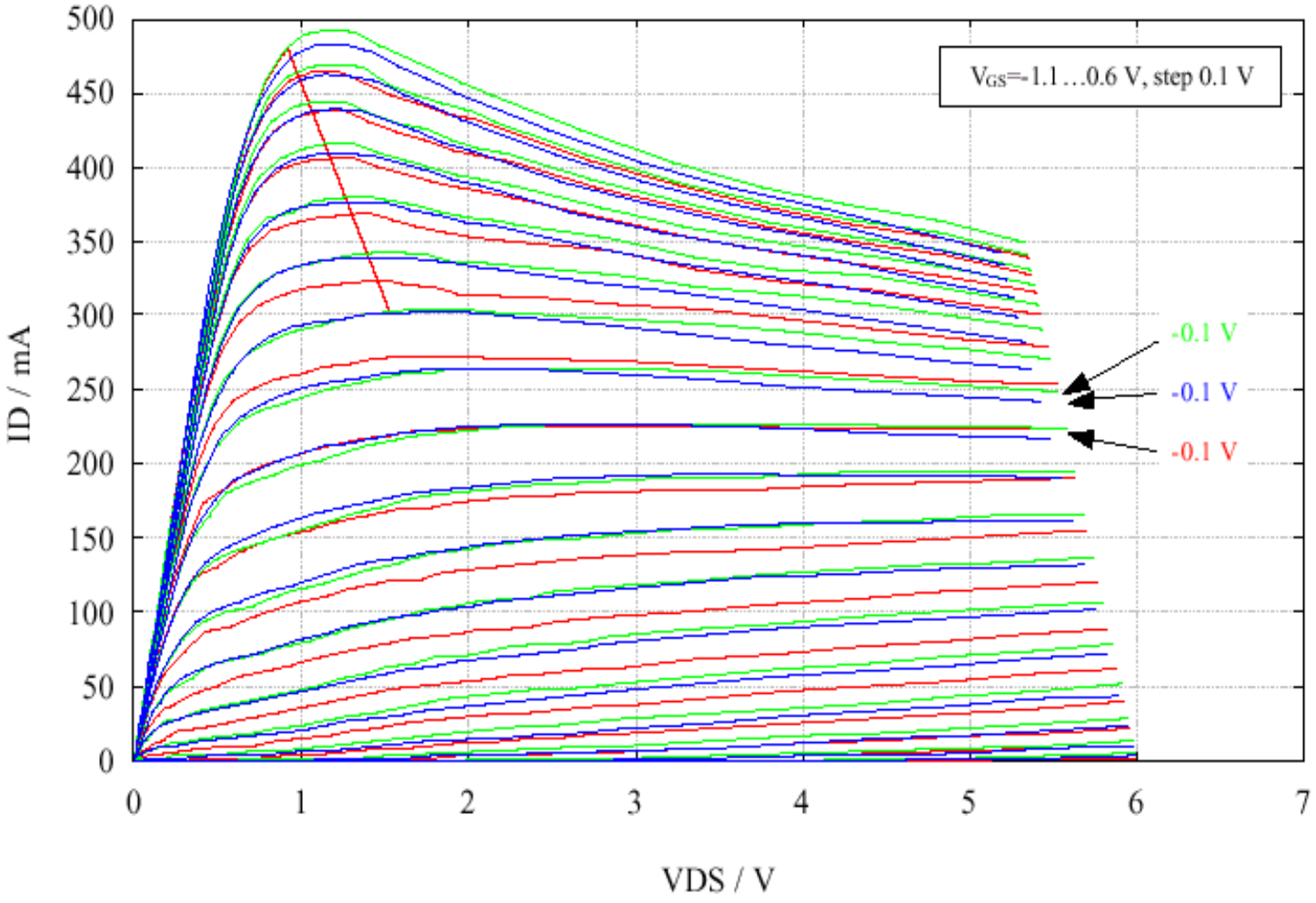
Oscillations



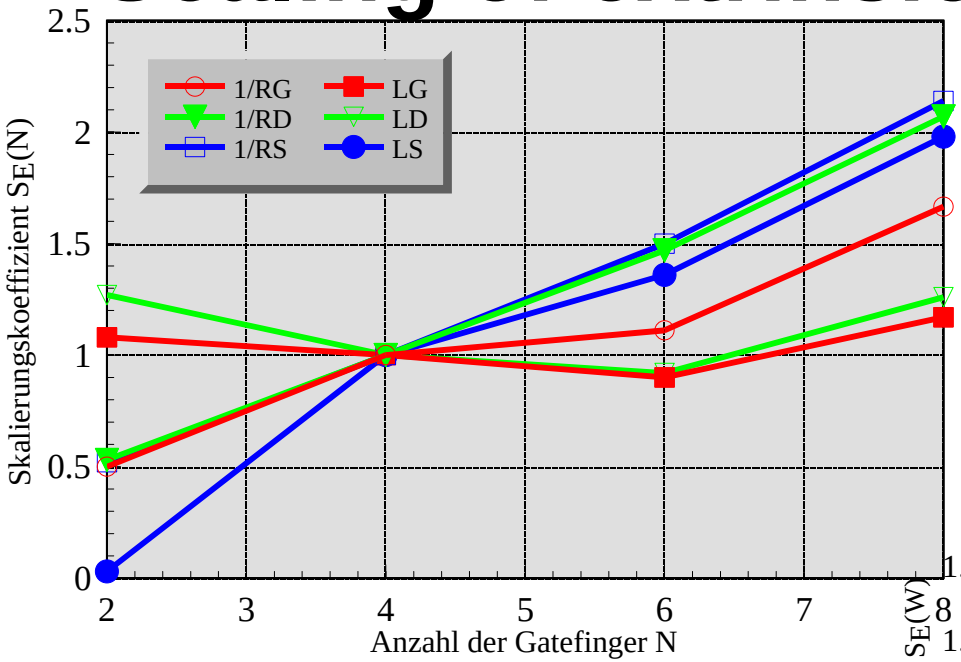
Switching problems



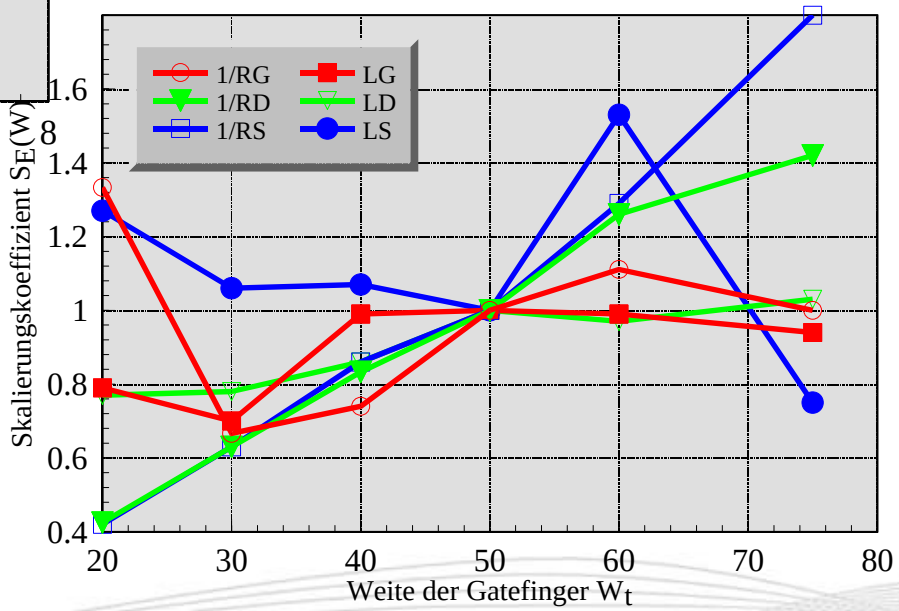
Burn-in effects



Scaling of extrinsic elements



Variation of gate finger width



Variation of gate finger number

Scaling of extrinsic elements

$$S_E(N) = a_{EN} \cdot N + b_{EN}$$

$$S_E(W_t) = a_{EW} \cdot W_t + b_{EW}$$

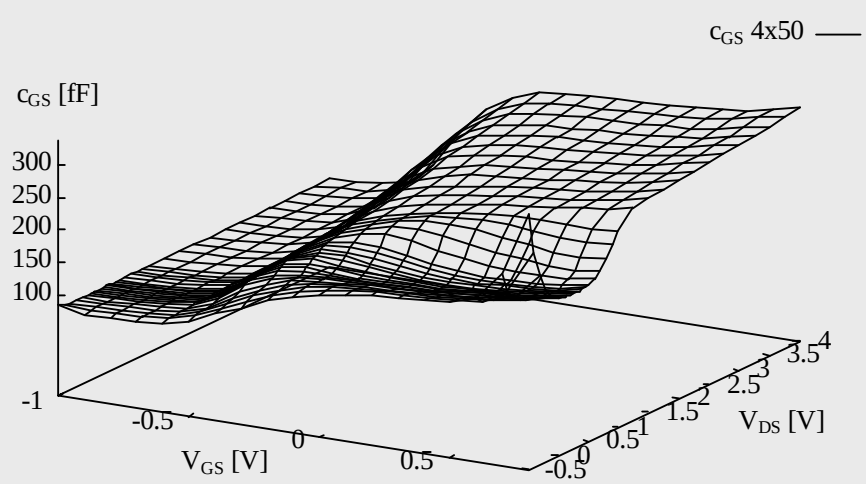
$$S_E(N, W_t) = S_E(N) \cdot S_E(W_t)$$

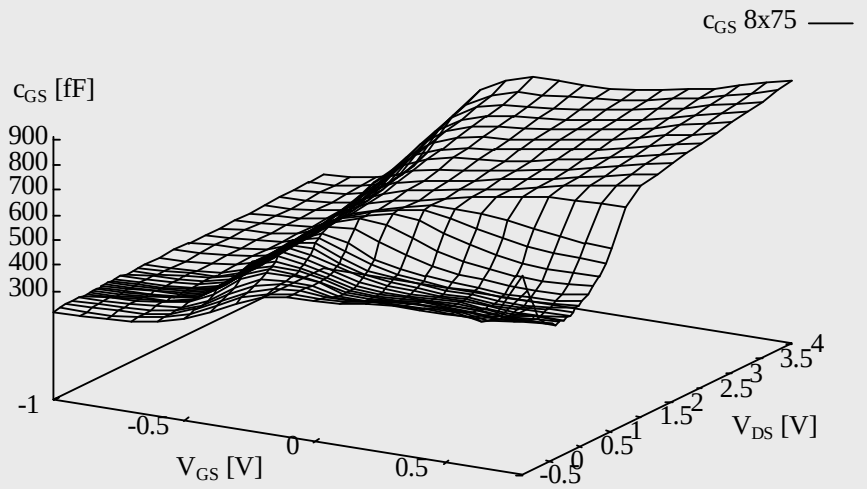
$S_E(N)$	$S_E(W)$	a_{EN}	b_{EN}	a_{EW}	b_{EW}
GG	GG	0.18	0.17	0.0	0.98
GD	GD	0.25	0.0	0.019	0.076
GS	GS	0.27	-0.04	0.024	-0.11
1/LG	LG	0.0	0.993	0.004	0.713
1/LD	LD	0.0	0.895	0.005	0.67
LS	1/LS	0.31	-0.46	0.006	0.68

Scaling of intrinsic elements

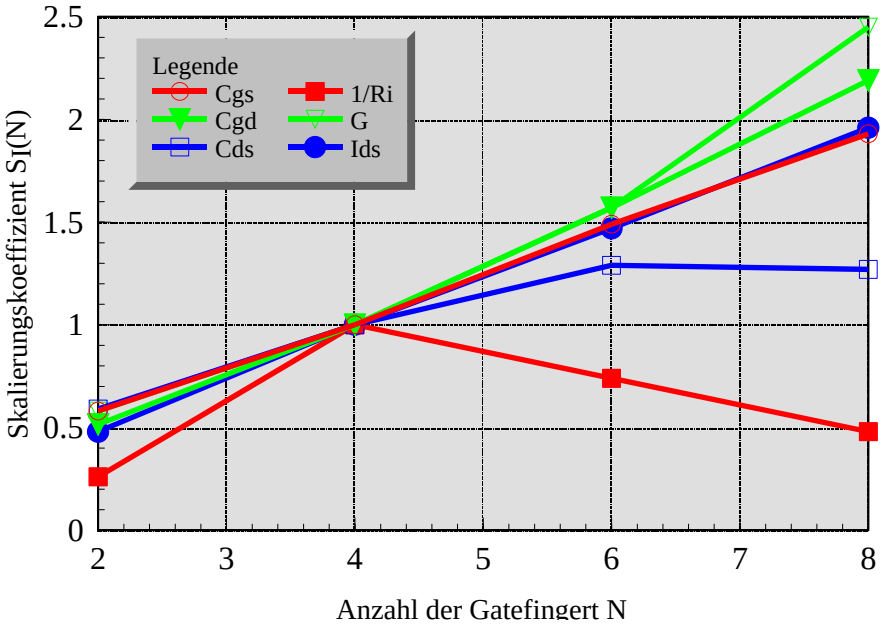
$$c_{old} = \frac{8x75\mu m}{4x50\mu m} = 3$$

$$c = \frac{\sum_{V_{gs},V_{ds}} \frac{G_x(V_{GS},V_{DS})}{G_{ref}(V_{GS},V_{DS})}}{n_{V_{GS},V_{DS}}}$$



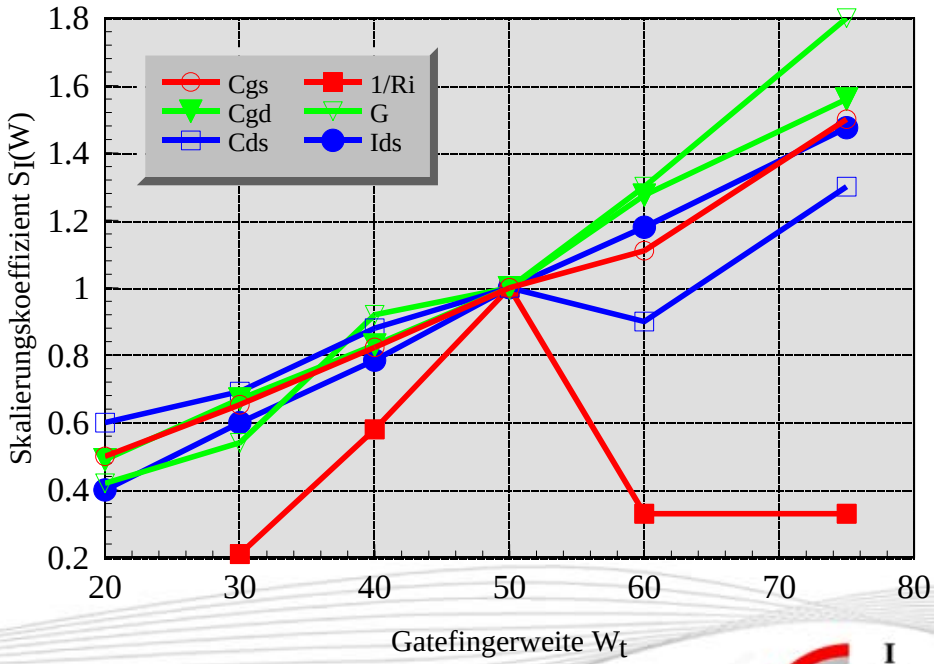


Scaling of intrinsic elements



Variation of
gate finger number

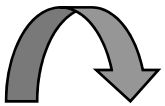
Variation of
gate finger width



Scaling of intrinsic elements

$$S_I(N) = a_{IN} \cdot N + b_{IN}$$

$$S_I(W) = a_{IWt} \cdot W + b_{IWt}$$



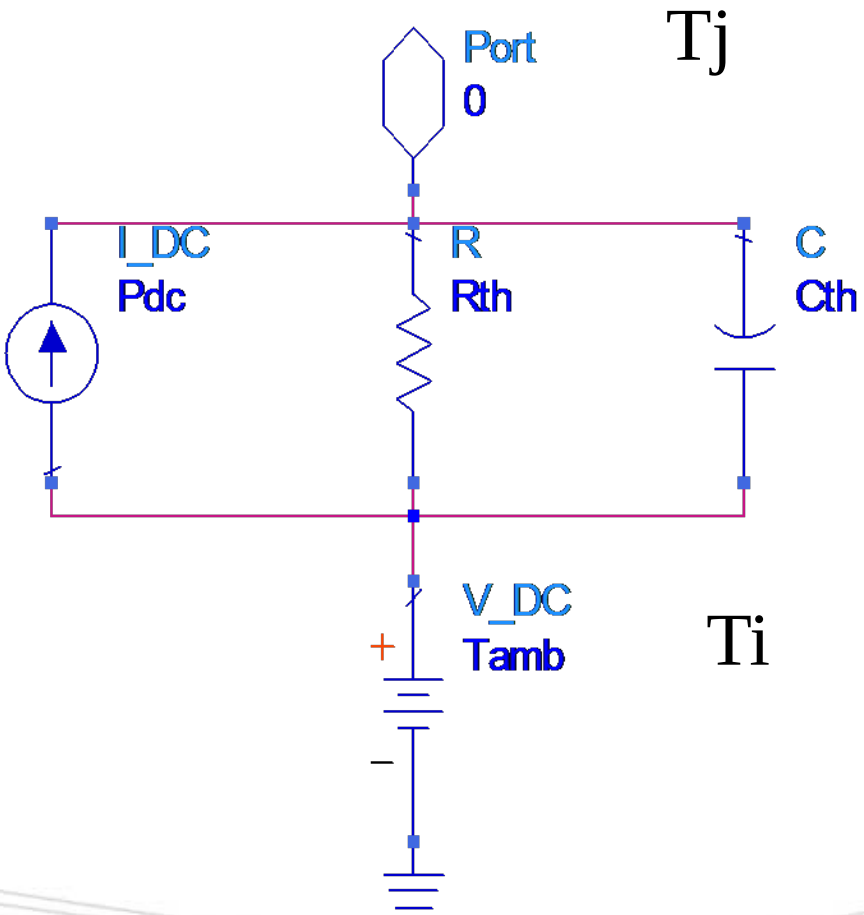
$$S_I(N,W) = S_I(N) \cdot S_I(W)$$

$S_I(N)$	$S_I(W)$	a_{IN}	b_{IN}	a_{IW}	b_{IW}
Cgs	Cgs	0.22	0.116	0.018	0.129
Cgd	Cgd	0.28	-0.08	0.019	0.077
Cds	Cds	0.12	0.459	0.011	0.371
Gi	Gi	0.02	0.52	-0.06	3.878
G	G	0.31	-0.14	0.025	-0.15
Id	Id	0.25	0.0	0.02	0.01

$$c_{new} = S_I(N = 4 \rightarrow N = 8) \cdot S_I(W_t = 50 \rightarrow W_t = 75)$$

$$1.93 \cdot 1.49 = 2.88$$

Thermal model



$$C_{TH}\frac{d\Delta T}{dt} = P - \frac{\Delta T}{R_{TH}}$$

$$P = I_D V_{DS}$$

$$I_D = \frac{V_{Rd1} - V_{Rd2}}{R_D\left(V_{GS}, V_{DS}\right)}$$

4D spline interpolation

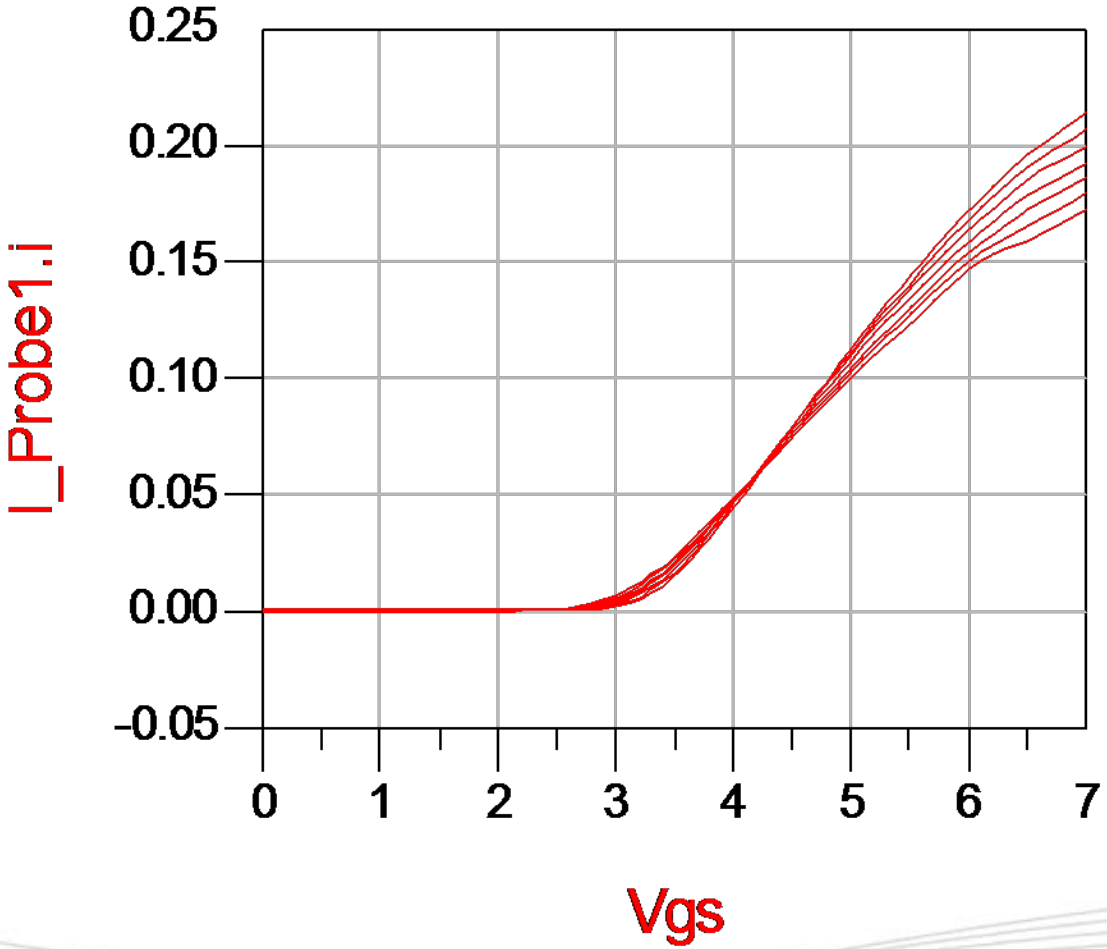
- Accurate description of $I_D(V_{GS}, V_{DS}, Tjunc)$

$$f(\vec{x}) = \sum_{i=0}^{3}\sum_{j=0}^{3}\sum_{k=0}^{3} a_{ijk} x_1^i x_2^j x_3^k$$

- 64 unknown values, 8 points at same time

$$f, \frac{\partial f}{\partial x_i}, \left.\frac{\partial^2 f}{\partial x_i \partial x_j}\right|_{i \neq j}, \frac{\partial^3 f}{\partial x_1 \partial x_2 \partial x_3}$$

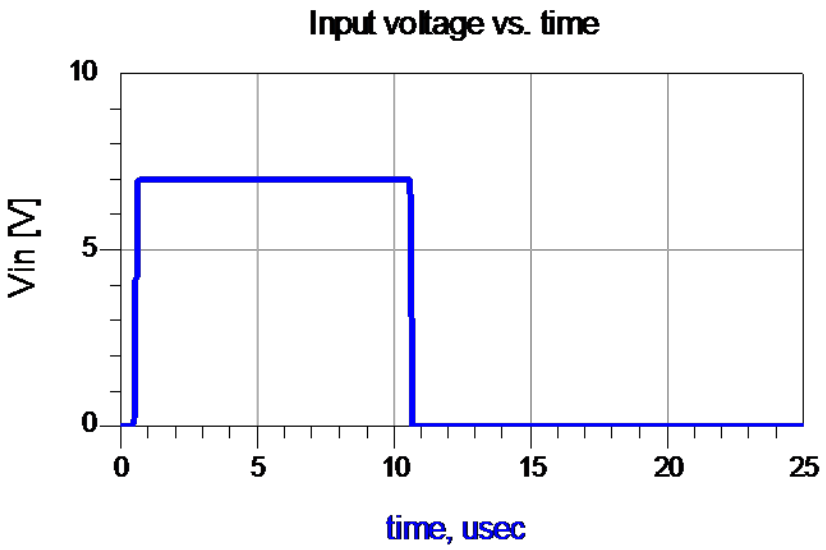
DC verification (LDMOS example)

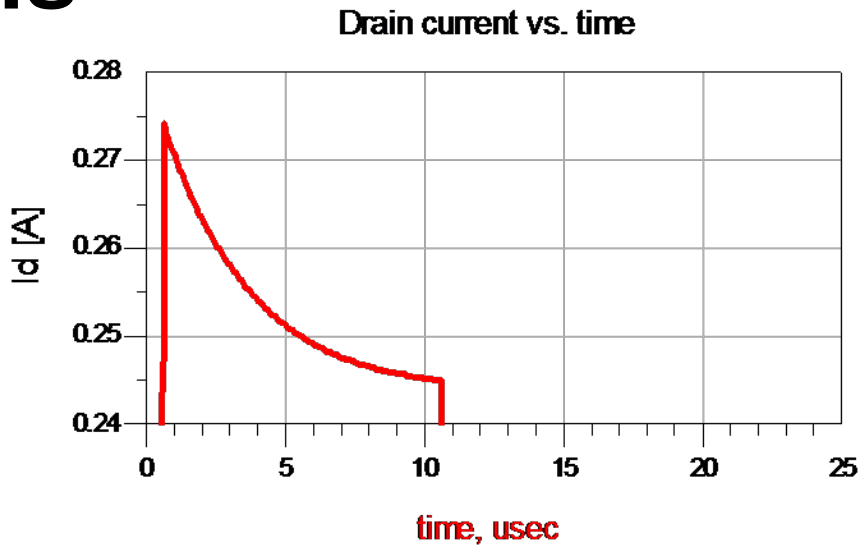


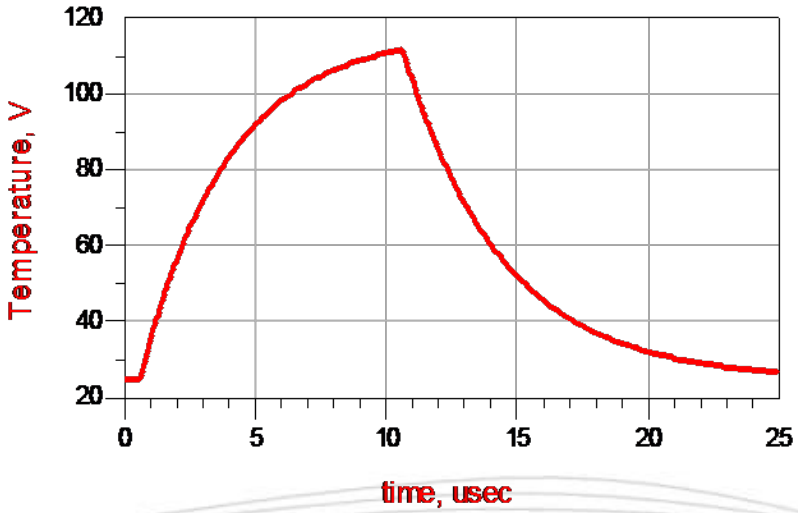
→Intersection in one point

7x100 µm device

Transient analysis







Rth/Cth extraction

→Compare pulsed and CW currents at different temperatures

$$R_{TH} = \frac{T - T_{amb}}{V_{DS} I_{DS}}$$

→Cth: Monitor current versus time

Thank you for you attention

→ Any questions?

Model implementation into ADS

Rüdiger Follmann

Contents

→PN-diode, equivalent circuit and equations

→Linear part

→Non-linear part

→Linearized part

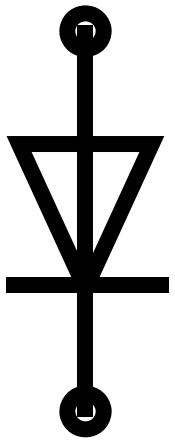
→Noise

→Interface

→Consistent implementation

PN diode

Implementation of a pn-diode model into Agilents ADS



How to start?

A non-linear model consists of the parts

→Equivalent circuit and associated equations

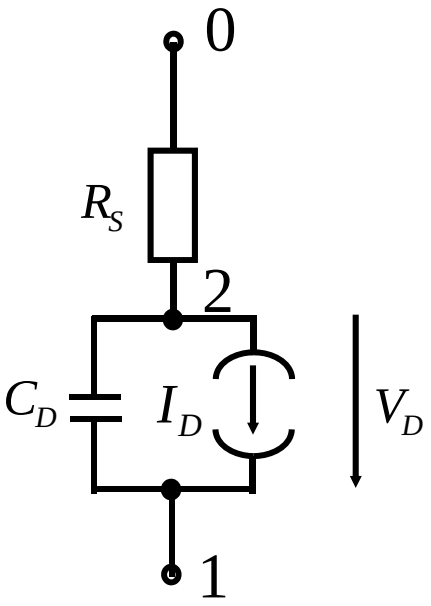
→Linear part containing linear elements

→Same with non-linear part

→Bias point dependent linearized part (Jacobian matrix)

→Bias dependent noise part

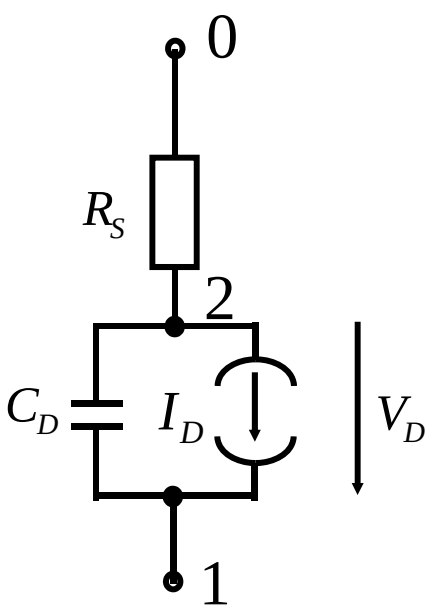
ADS specific things



→All nodes are numbered

→Outer nodes get smallest numbers

Equivalent circuit and equations



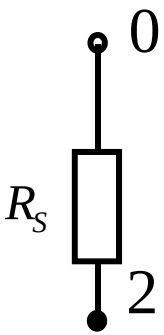
$$I_D(V_D) = I_S\left(e^{\frac{V_D}{V_{te}}} - 1\right) + 10^{-12}\,\frac{\mathrm{A}}{\mathrm{V}}\,V_D$$

$$\frac{dI_D}{dV_D} = \frac{I_S e^{\frac{V_D}{V_{te}}}}{V_{te}} + 10^{-12}\,\frac{\mathrm{A}}{\mathrm{V}}$$

$$C_D(V_D) = TT\frac{dI_D}{dV_D} + CJ0\left(1 - \frac{V_D}{VJ}\right)^{-M}$$

$$Q_D(V_D) = \int_0^{V_D} C_D(\tilde{V}_D)\,d\tilde{V}_D = TT \cdot I_D + \frac{VJ \cdot CJ0}{1-M}\left(1 - \left(1 - \frac{V_D}{VJ}\right)^{1-M}\right)$$

Linear part



R_S is the only linear element between nodes 0-2

Admittances here

nodes

Y-matrix

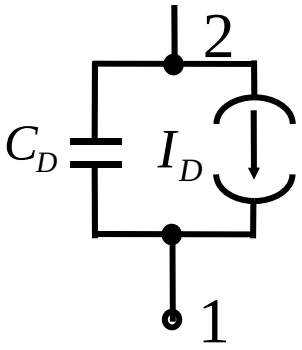
```
COMPLEX y;

 y.real = 1/Rs; y.imag = 0.0;
 status = add_y_branch(userInst, 0, 2,
y);
```


Non-linear part

→Number all nodes in order to get the voltages

→Start with outer nodes

→Use code calculates charges at each node and non-linear currents out of each node



I_D and C_D are non-linear elements between nodes 1-2

Linearized part

→Calculation of partial derivatives for non-linear elements with respect to the nodes to get capacitances and conductances for Jacobian matrix

→The linearized part does not influence the final harmonic balance solution

→The linearized part influences the convergence speed

Noise

→ Noise part contains the bias dependent correlation parameters - normalized to $4KT_0$

→ This part is only needed for noise analysis

Possible noise sources:

Thermal noise $\left\langle i_{th}^2 \right\rangle = \frac{4kT_0}{R}\Delta f$

Shot noise $\left\langle i_{shot}^2 \right\rangle = 2qI_D\Delta f$

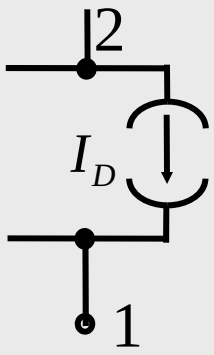
1/f noise $\left\langle i_{1/f}^2 \right\rangle = KF\frac{I_D^{AF}}{f^{FFE}}\Delta f$

Burst or popcorn noise

$$\left\langle i_{burst}^2 \right\rangle = KB\frac{I_D^{CF}}{1+\left(\frac{f}{f_{CF}}\right)^2}\Delta f$$

Non-linear part

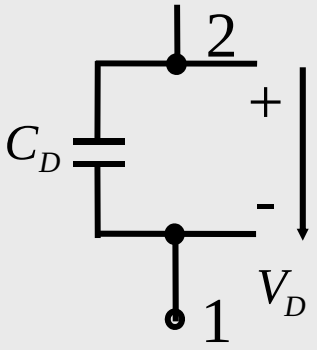
Calculation of node currents and charges



Node 1: $i_1 = -I_D$

Node 2: $i_2 = +I_D$

Current from node:+, to node:-



$V_D = V_2 - V_1$

Node 1: $q_1 = -Q_D$

Node 2: $q_2 = +Q_D$

Node i q

```
status =   add_nl_iq(userInst, 1, -id, -qd) &&
           add_nl_iq(userInst, 2, +id, +qd);
```


Jacobian matrix

$$\frac{\partial I_1}{\partial V_1} = -1 \cdot \left(-\frac{dI_D}{dV_D} \right) = \frac{dI_D}{dV_D} \qquad \frac{\partial I_1}{\partial V_2} = -\frac{dI_D}{dV_D}$$

$$\frac{\partial I_2}{\partial V_1} = -\frac{dI_D}{dV_D} \qquad \frac{\partial I_2}{\partial V_2} = \frac{dI_D}{dV_D}$$

Real part

$$\frac{\partial Q_1}{\partial V_1} = C_D \qquad \frac{\partial Q_1}{\partial V_2} = -C_D$$

$$\frac{\partial Q_2}{\partial V_1} = -C_D \qquad \frac{\partial Q_2}{\partial V_2} = C_D$$

Imaginary part

partial derivatives g c + -

$V_D = V_2 - V_1$

```
status =    add_nl_gc(userInst, 1, 1, +gd, +cd) &&
            add_nl_gc(userInst, 1, 2, -gd, -cd) &&
            add_nl_gc(userInst, 2, 1, -gd, -cd) &&
            add_nl_gc(userInst, 2, 2, +gd, +cd);
```


Noise

```
COMPLEX thermal, dNoise;

thermal.imag = dNoise.imag = 0.0;

thermal.real = 1.0/Rs*DEV_TEMP/NOISE_REF_TEMP;

dNoise.real = 2 * CHARGE * id;

dNoise.real = kf * pow(id, AF)*pow(omega/TWOPI, -FFE);

dNoise.real /= FOUR_K_T0;

status =      add_n_branch(userInst, 0, 2, thermal) &&
              add_n_branch(userInst, 1, 2, dNoise);
```

Thermal noise

Shot noise

1/f noise

Attention: All noise currents are normalized to $4KT_0$

Interface

nonlin_ele.h

```
// name      numPars     params     compute_y     post_analysis      senior Info
//      numExtNodes     pre_analysis     compute_n     devDef      tranDef

{"PNDIODE",  0,  size(PNDIODE),  PNDIODE,  NULL,  NULL,  NULL, NULL,
NULL, NULL, NULL}
```

nonlin_def.h

```
static UserNonLinDef PNDIODE =
{
  0,                /* numIntNodes   */
  NULL,             /* analyze_lin() */
  sdiode_nl,        /* analyze_nl()  */
  sdiode_ac,        /* analyze_ac()  */
  NULL,             /* modelDef      */
  NULL              /* analyze_ac_n  */
};
```


Interface

nonlin_typ.h

```
PNDIODE[] =
{ /* P-N junction diode */
        {"AREA",     REAL_data},
        {"IS",       REAL_data},
        {"RS",       REAL_data},
        {"N",        REAL_data},
        {"TT",       REAL_data},
        ...
}
```

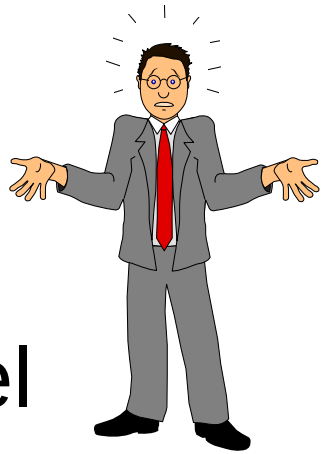
nonlin_fun.h

```
* NON-LINEAR PN-DIODE MODEL */
EXTERN_FUNCTION( extern boolean  pndiode_lin, (UserInstDef *userInst, double omega));
EXTERN_FUNCTION( extern boolean  pndiode_nl,  (UserInstDef *userInst, double *vPin));
EXTERN_FUNCTION( extern boolean  pndiode_ac,  (UserInstDef *userInst, double *vPin, double omega));
EXTERN_FUNCTION( extern boolean  pndiode_ac_n,(UserInstDef *userInst, double *vPin, double omega));
```


Interface

→AEL programming language is the GUI for the simulator

Summary



→Different parts of a non-linear model

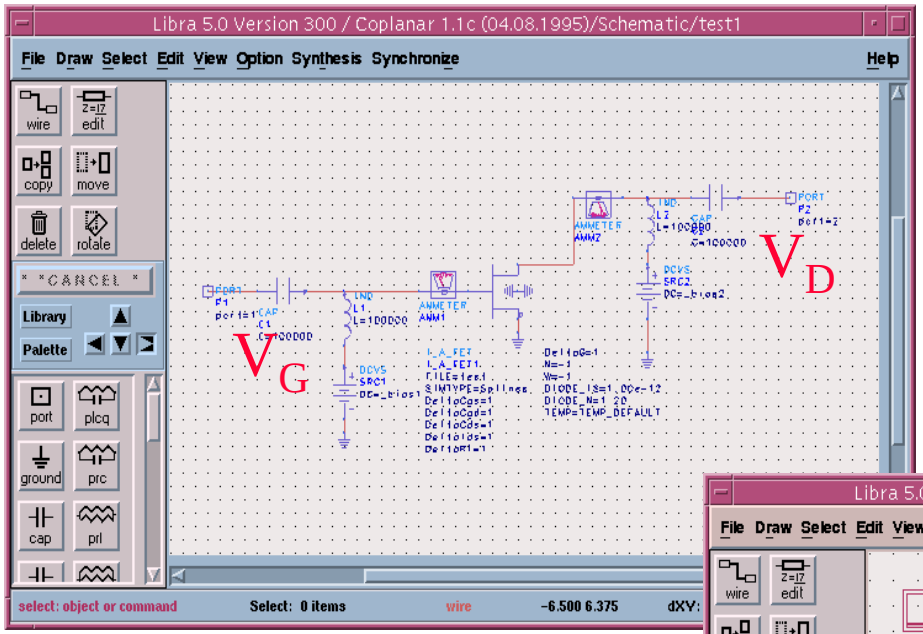
→Nonlinear equations and their derivatives

→Implementation into circuit simulation software

→Noise sources

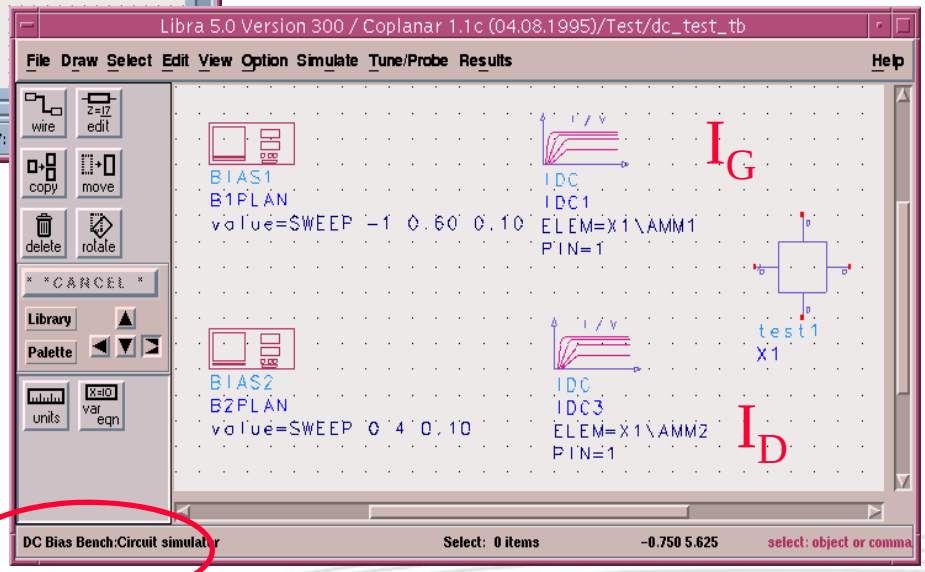
→Jacobian matrix

DC tests



All tests are shown for a transistor device. The are valid for diode devices as well.

Perform a DC analysis first!

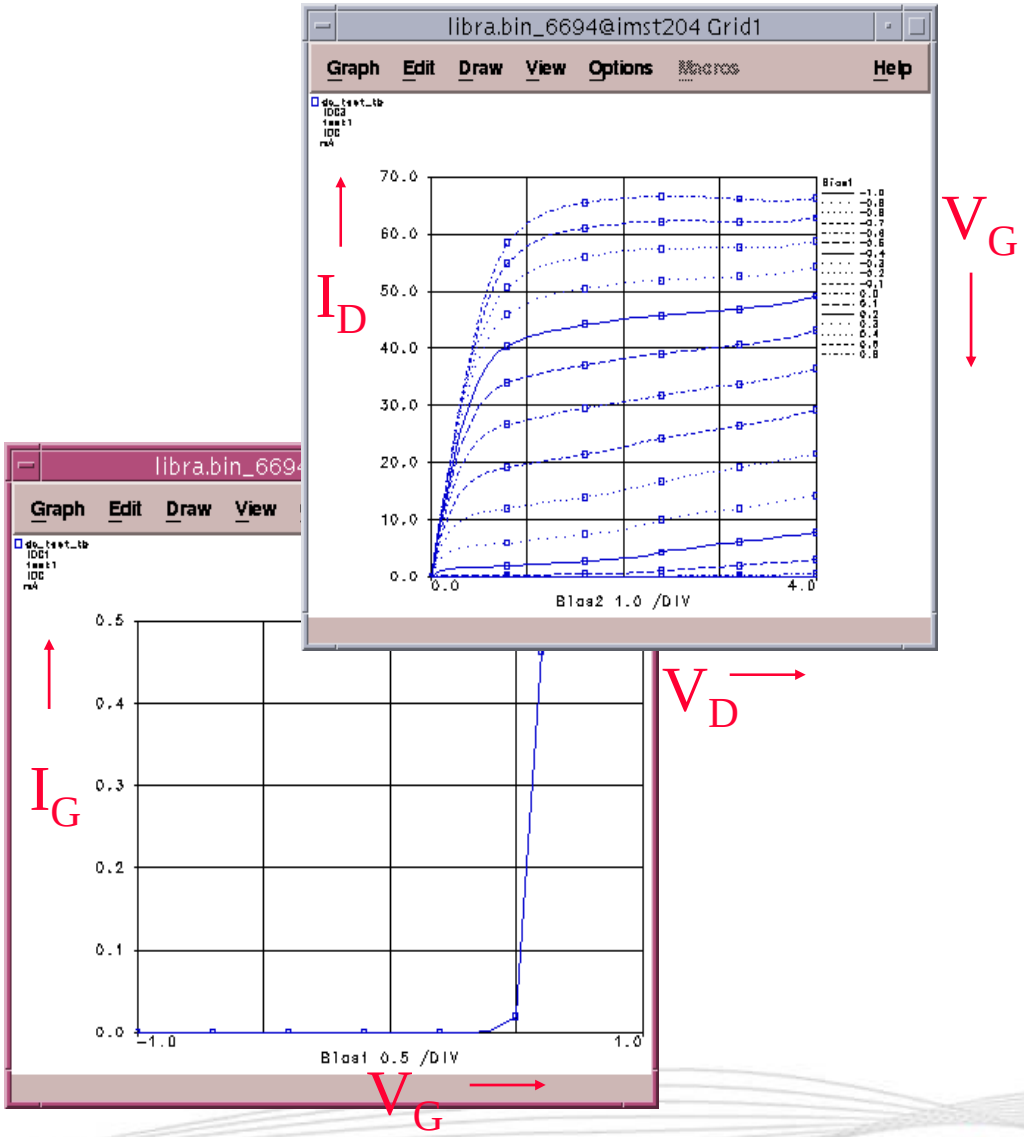


Only currents are calculated

DC testbench

DC tests

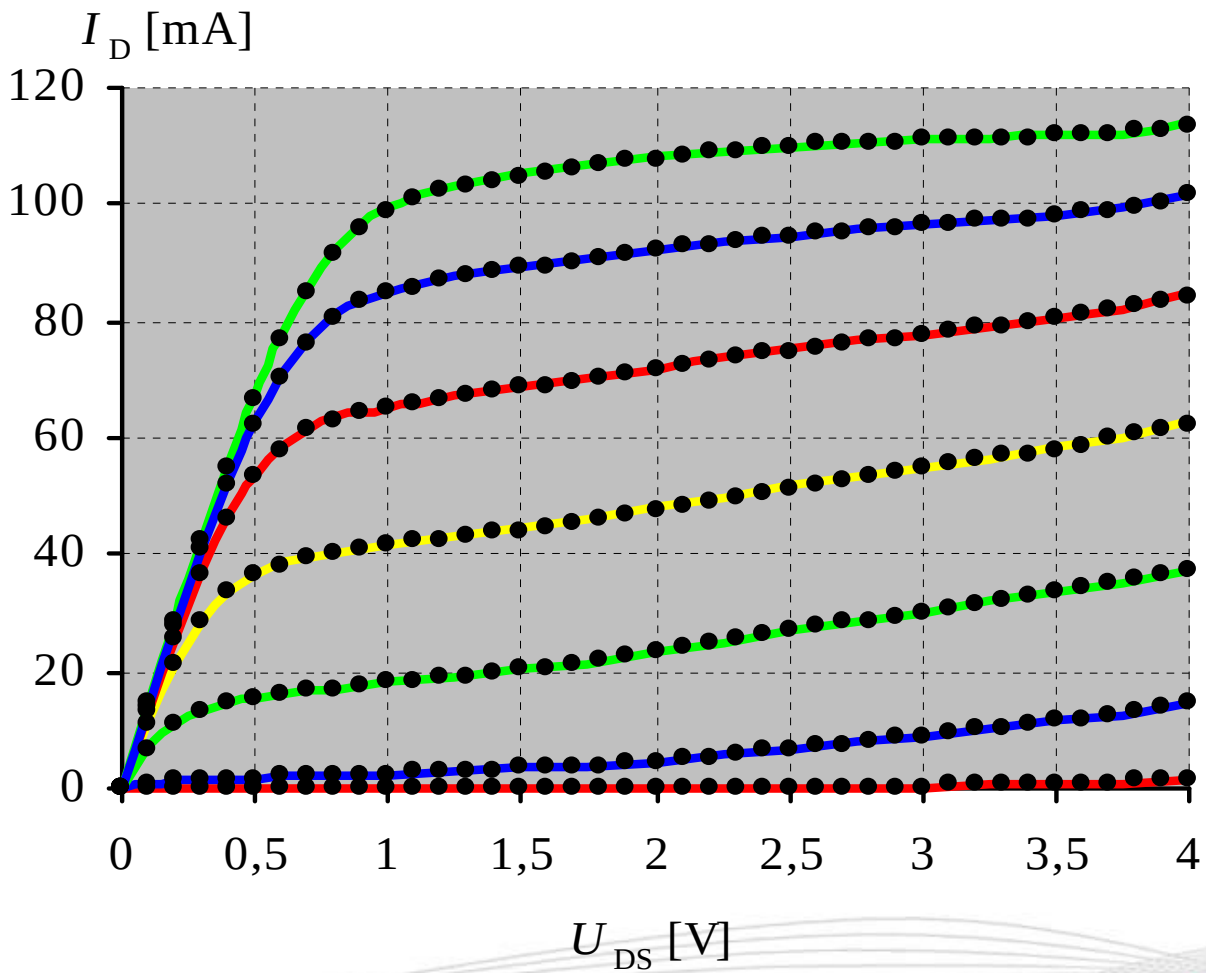
- → IV output curves OK?
- → IV input curves OK?
- → Curves typical for element?
- → Show measurements similar behaviour?



DC tests

T4x50µm HEMT, simulation vs. measurements

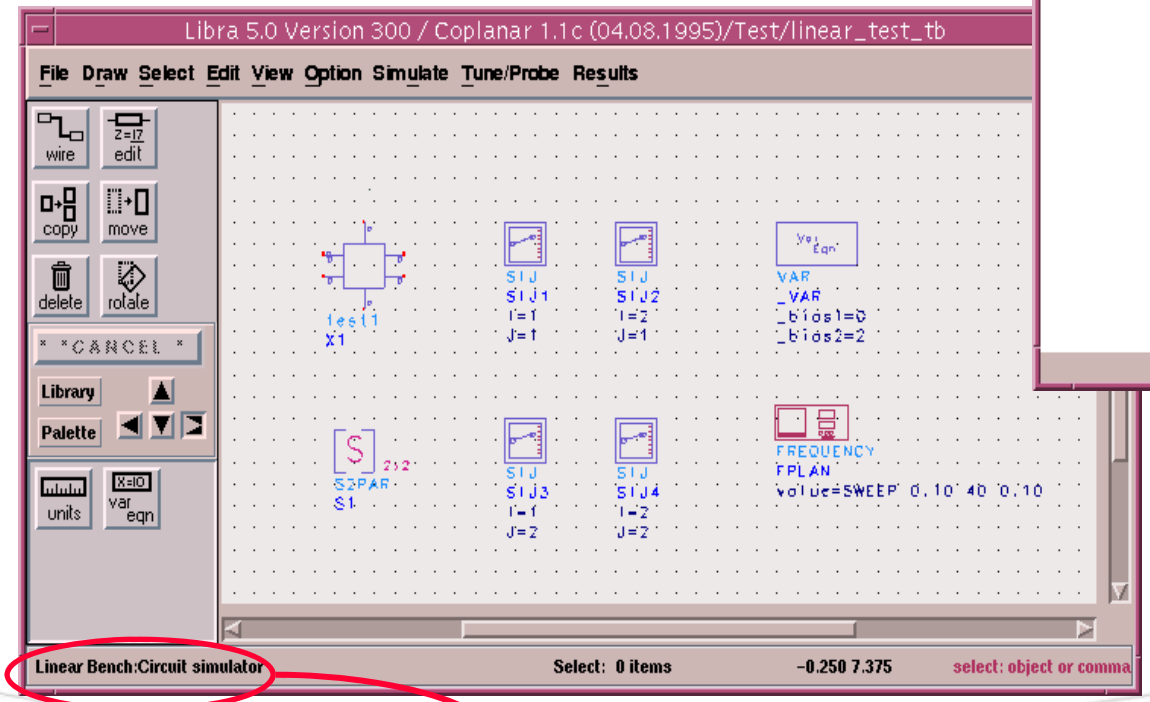
Show simulation and measurements similar behaviour?



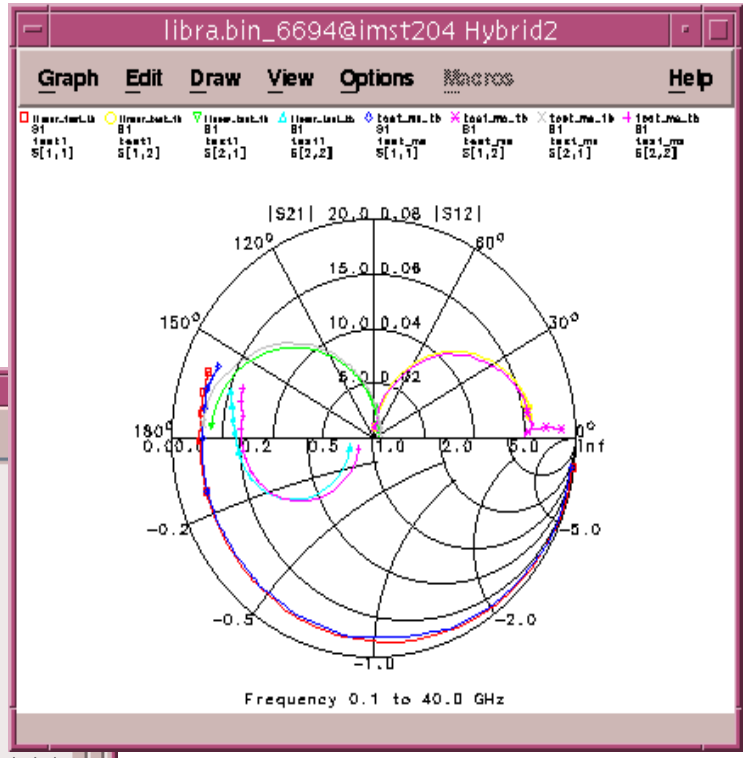
RF Tests

Are measured and simulated S-parameters similar ?

Transistor: Gain, pinch-off S-parameters OK?



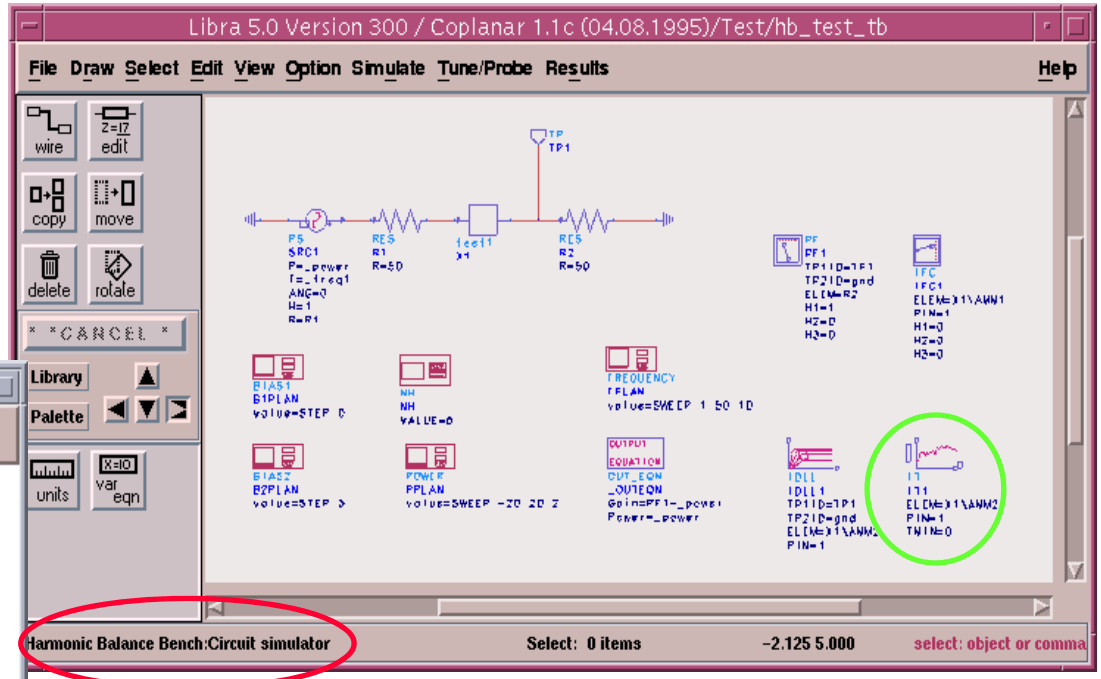
Lineares testbench

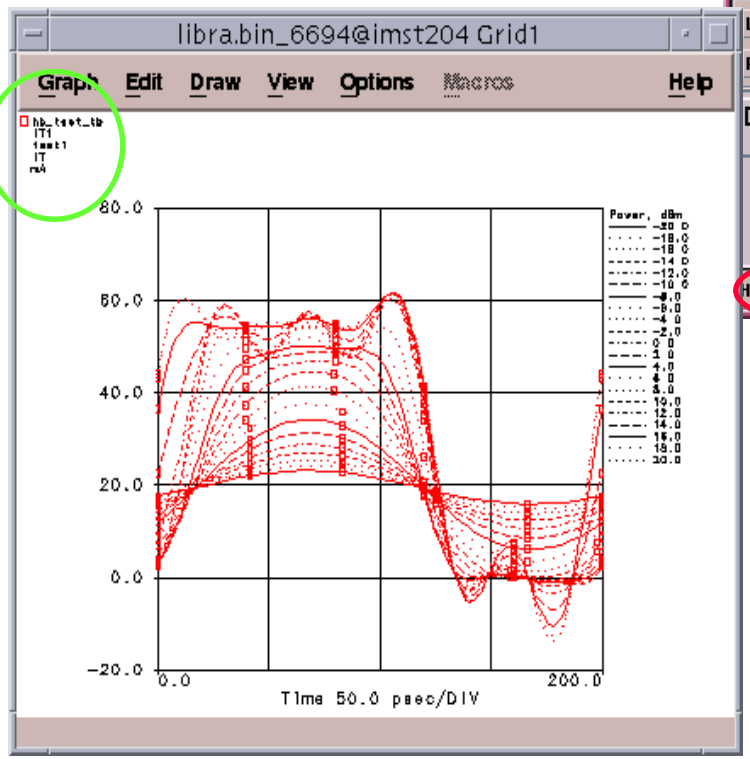


Diode: Forward and reverse S-parameters OK?

HB tests

Simulate a power sweep

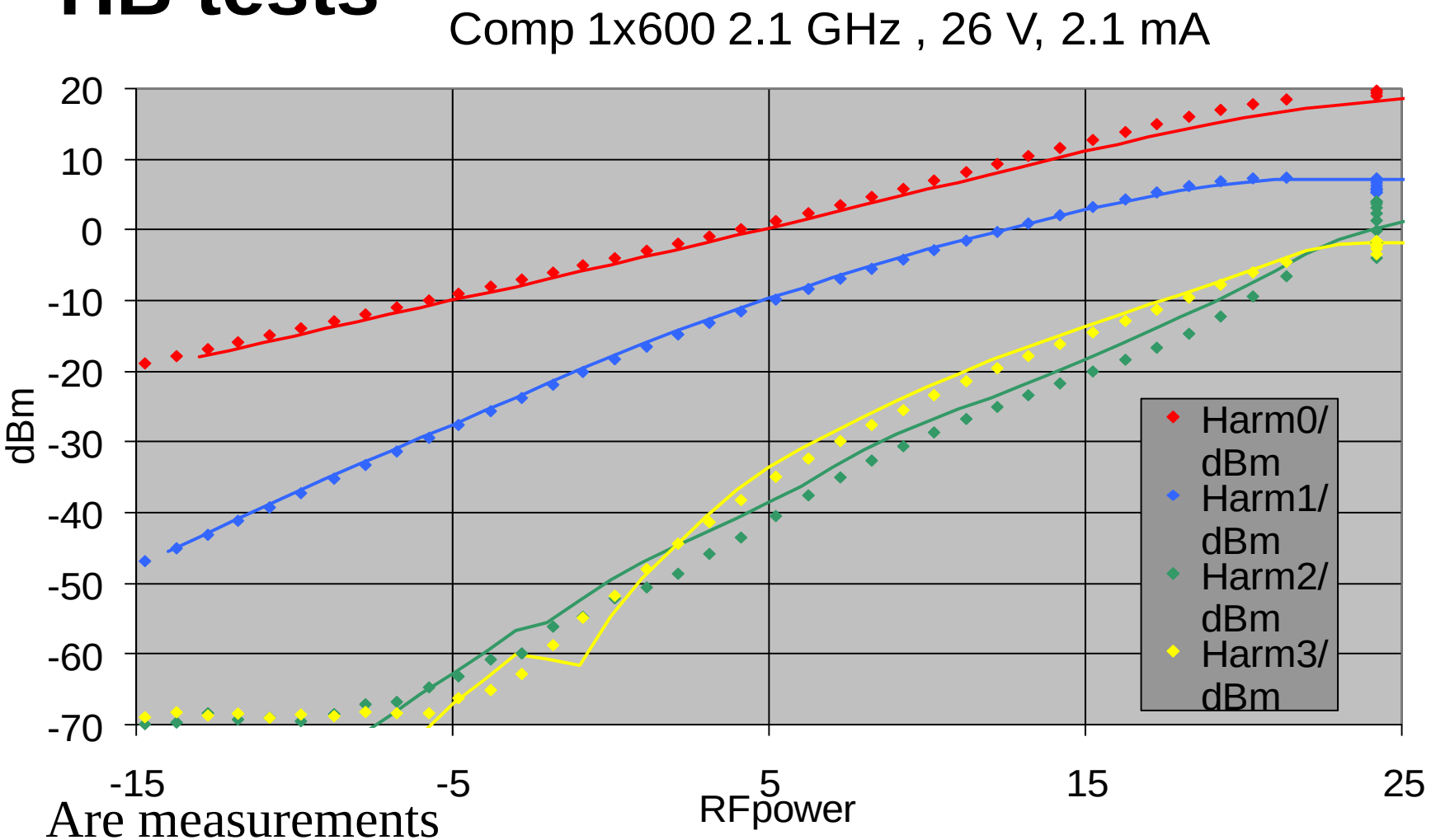




Harmonic Balance testbech

Is the behaviour as expected?
Are the nonlinearities dominant for high input power

HB tests

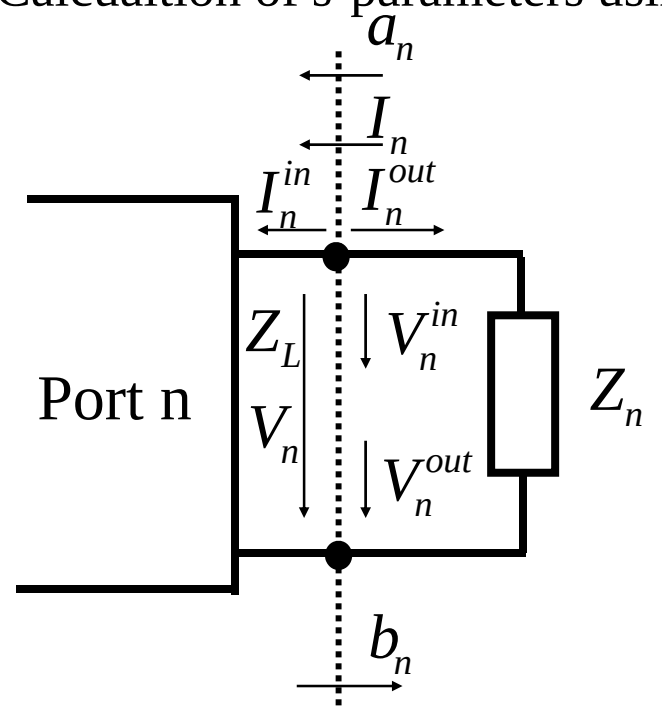


Are measurements and simulations similar ?

How good is the quality of the model ?

Consistent implementation

Calcualtion of s-parameters using voltage and current definition



Waves in und out of port n

$$a_n = \frac{V_n^{in}}{\sqrt{Z_{Ln}}} = I_n^{in}\sqrt{Z_{Ln}}$$

$$b_n = \frac{V_n^{out}}{\sqrt{Z_{Ln}}} = I_n^{out}\sqrt{Z_{Ln}}$$

Currents and voltages

$$u_n = \frac{V_n}{\sqrt{Z_{Ln}}} = \frac{V_n^{in} + V_n^{out}}{\sqrt{Z_{Ln}}} = a_n + b_n$$

$$i_n = I_n\sqrt{Z_{Ln}} = \left(I_n^{in} - I_n^{out}\right)\sqrt{Z_{Ln}} = a_n - b_n$$

$$\Rightarrow \quad a_n = \frac{1}{2}(u_n + i_n), \quad b_n = \frac{1}{2}(u_n - i_n) \quad \Rightarrow$$

S matrix

$$\|b\| = \|s\| \cdot \|a\|$$

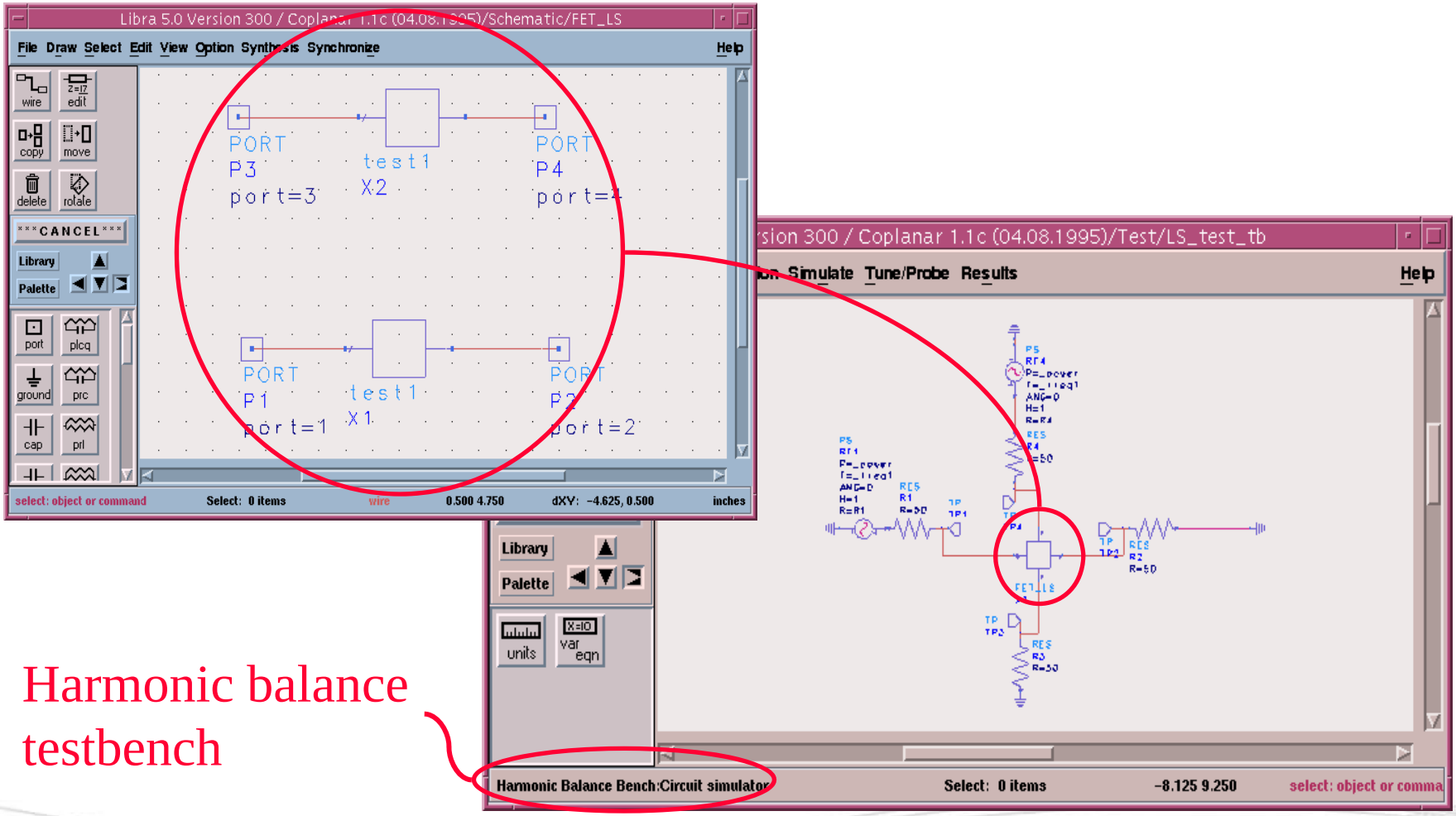
Example

$$s_{11} = \left.\frac{b_1}{a_1}\right|_{a_{2=0}}$$

$$s_{11,dB} = 20 \cdot \log\frac{u_1 - i_1}{u_1 + i_1}$$

Consistent implementation

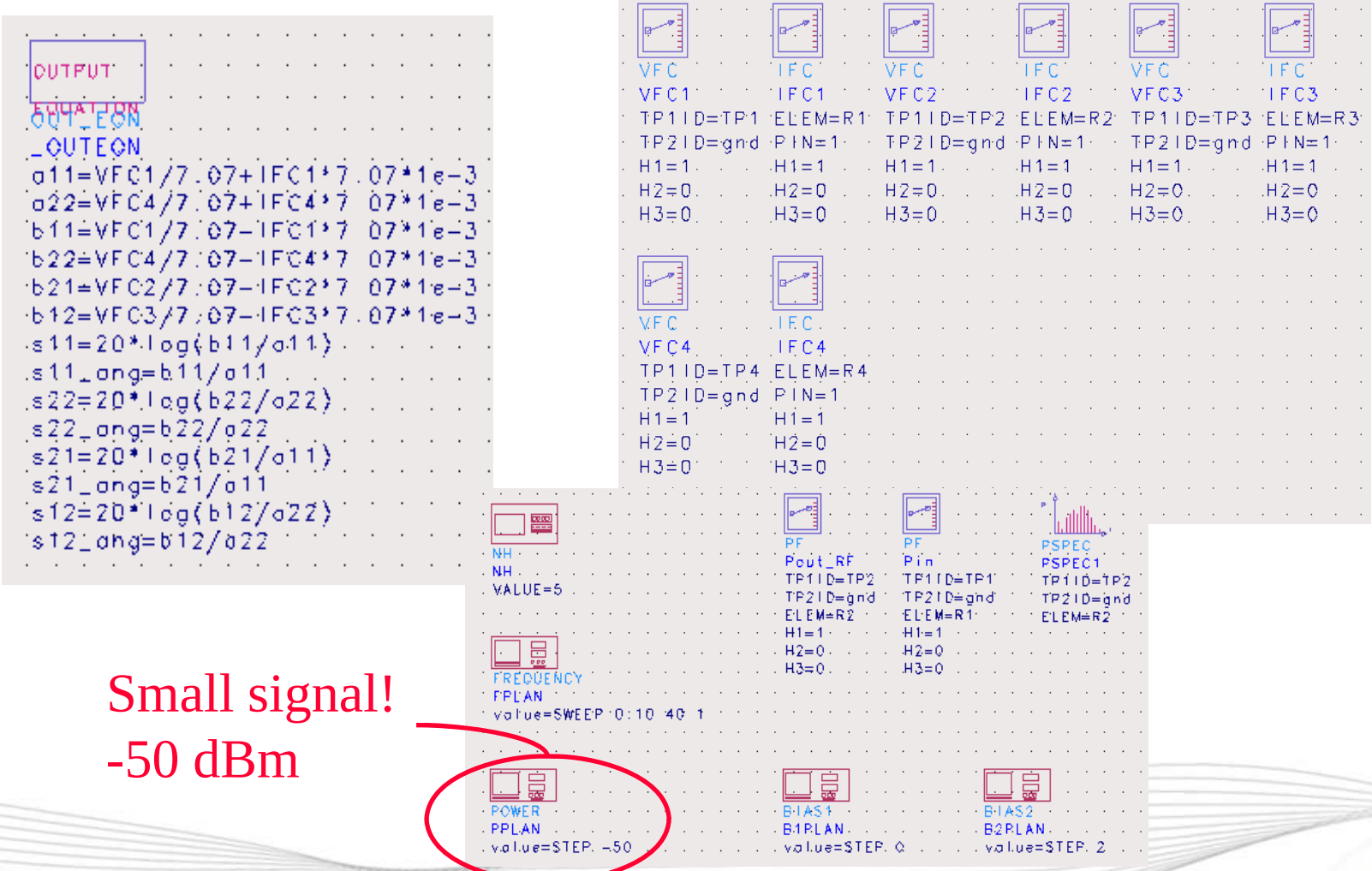
Calculation of small signal S-parameters using a large signal test bench



Harmonic balance testbench

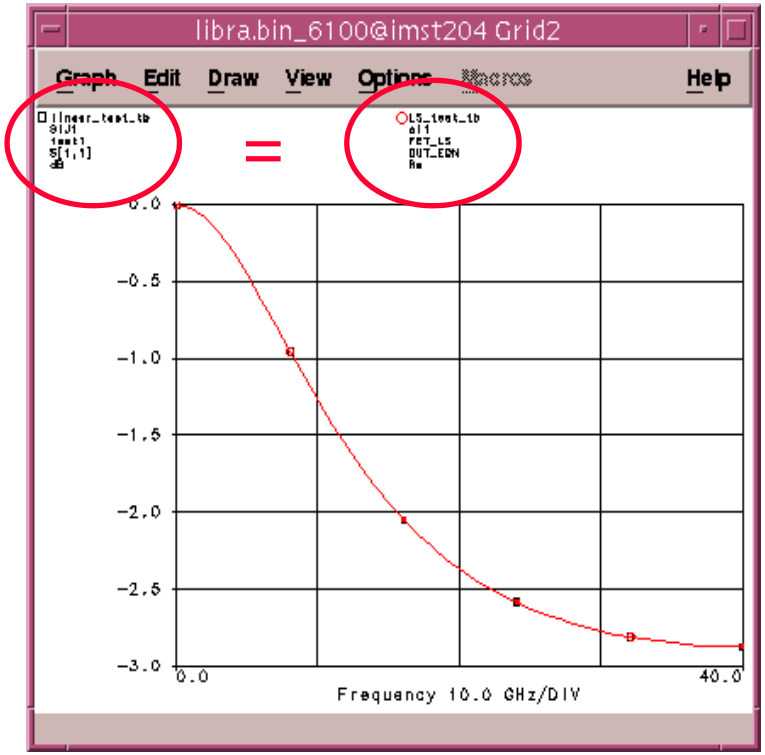
Consistent implementation

Calculation of small signal s-parameters using a large signal testbench



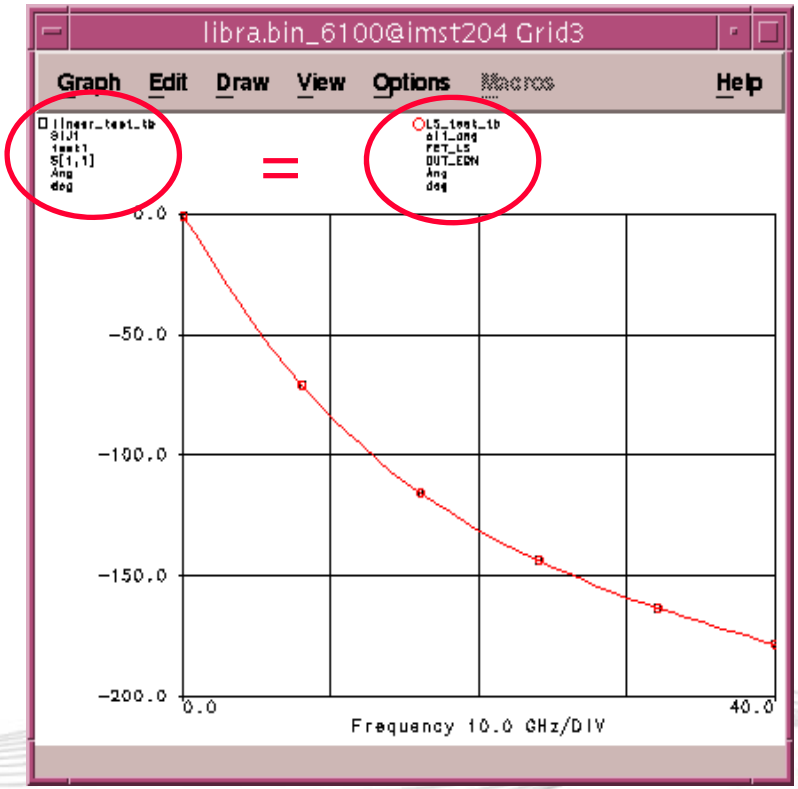
Small signal!
-50 dBm

Consistent implementation



Mag(s_{11}), simulated using Small signal and large signal testbench for very low input power (-50 dBm)

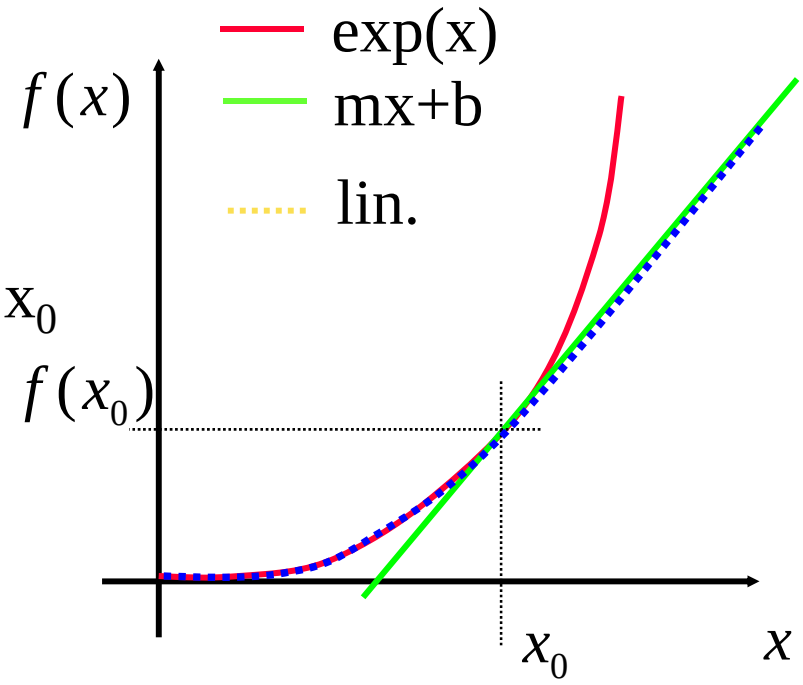
Phase(s_{11}), simulated using Small signal and large signal testbench for very low input power (-50 dBm)



Needful things

Linearize exp() function for better conversion and avoid errors such as numerical overflows

$$f(x)=\begin{cases}\exp(x) & x \le x_0 \\ mx+b & x > x_0\end{cases}$$



Function must be continuous at x_0

$$f_1(x_0) = f_2(x_0) \qquad \left.\frac{df_1}{dx}\right|_{x_0} = \left.\frac{df_2}{dx}\right|_{x_0}$$

$$\Rightarrow \quad \exp(x_0) = mx_0 + b$$

$$m = \exp(x_0)$$

$$\Rightarrow \quad b = \exp(x_0)(1 - x_0) \Rightarrow \quad f_2(x) = \exp(x_0)(x + 1 - x_0)$$

Summary

→Perform different tests (DC, RF, harmonic balance)

→Typical results for a FET

→Calcualtion of small signal s-parameters using a large signal testbench

→Linearization of functions

Foundries, MMICs, systems

Rüdiger Follmann

Content

→ MMIC foundries

→ Designs and trends

→ Examples

MMIC foundries

Foundries

IMST is a UMS certified design house

Memberships

MOSIS

GaAs in principal

→ 3,4 and 6 inch production

→ Target markets: High power and linearity, low noise, broad band

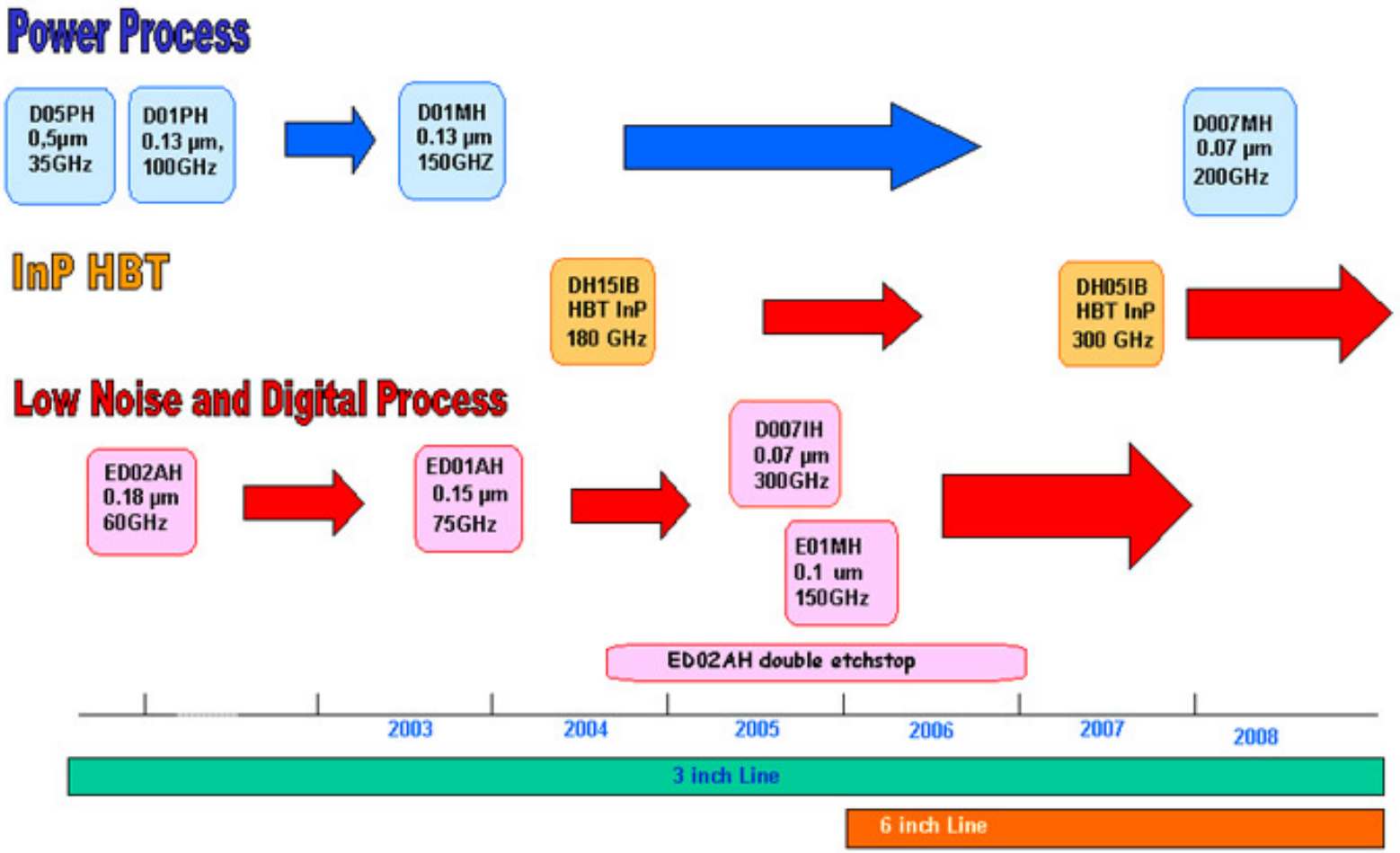
→ Specials available (e.g. E/D mode or HBT and pHEMT on same wafer)

→ Frequencies up to 100 GHz

→ Radiation hard

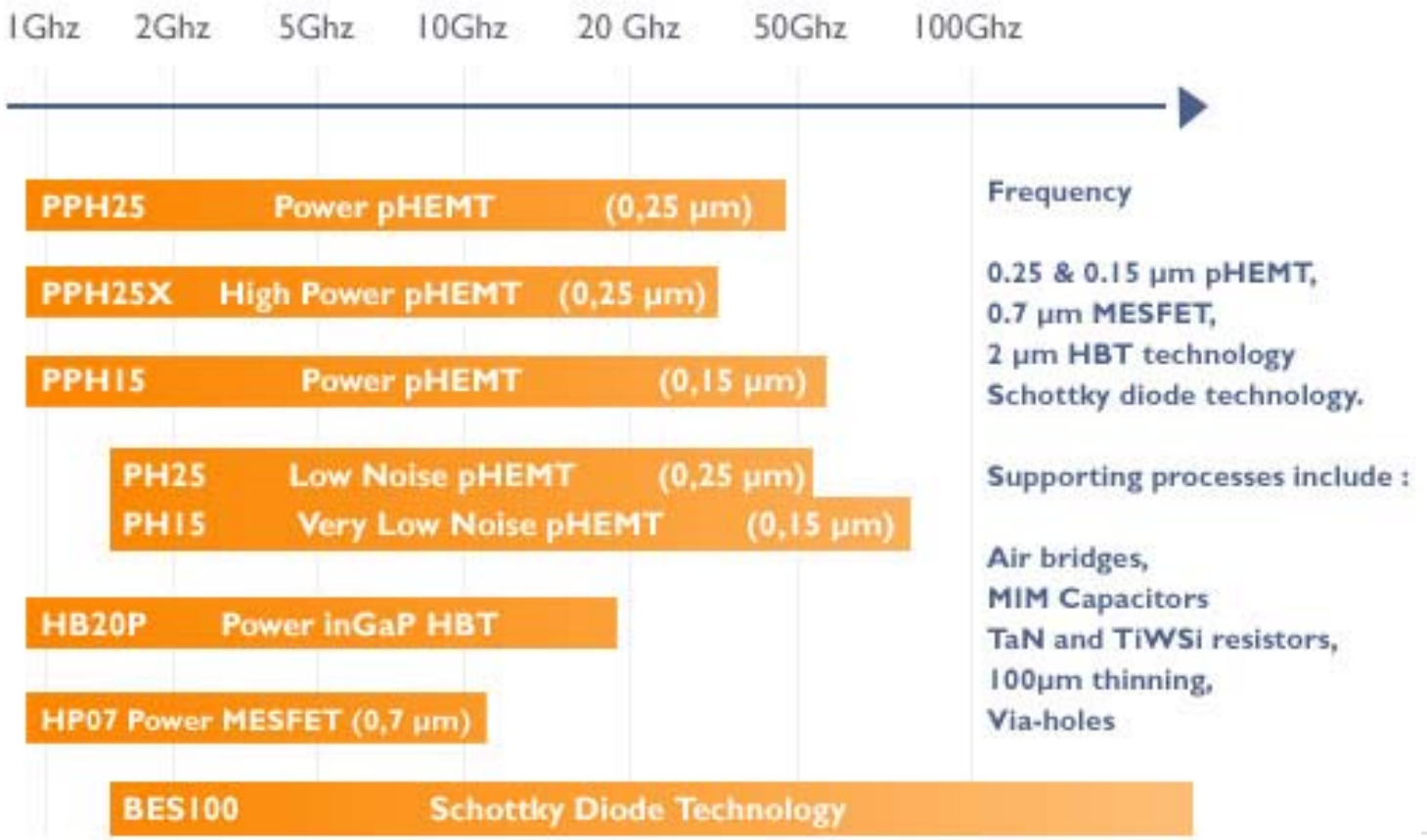
GaAs foundries

→ OMMIC, France



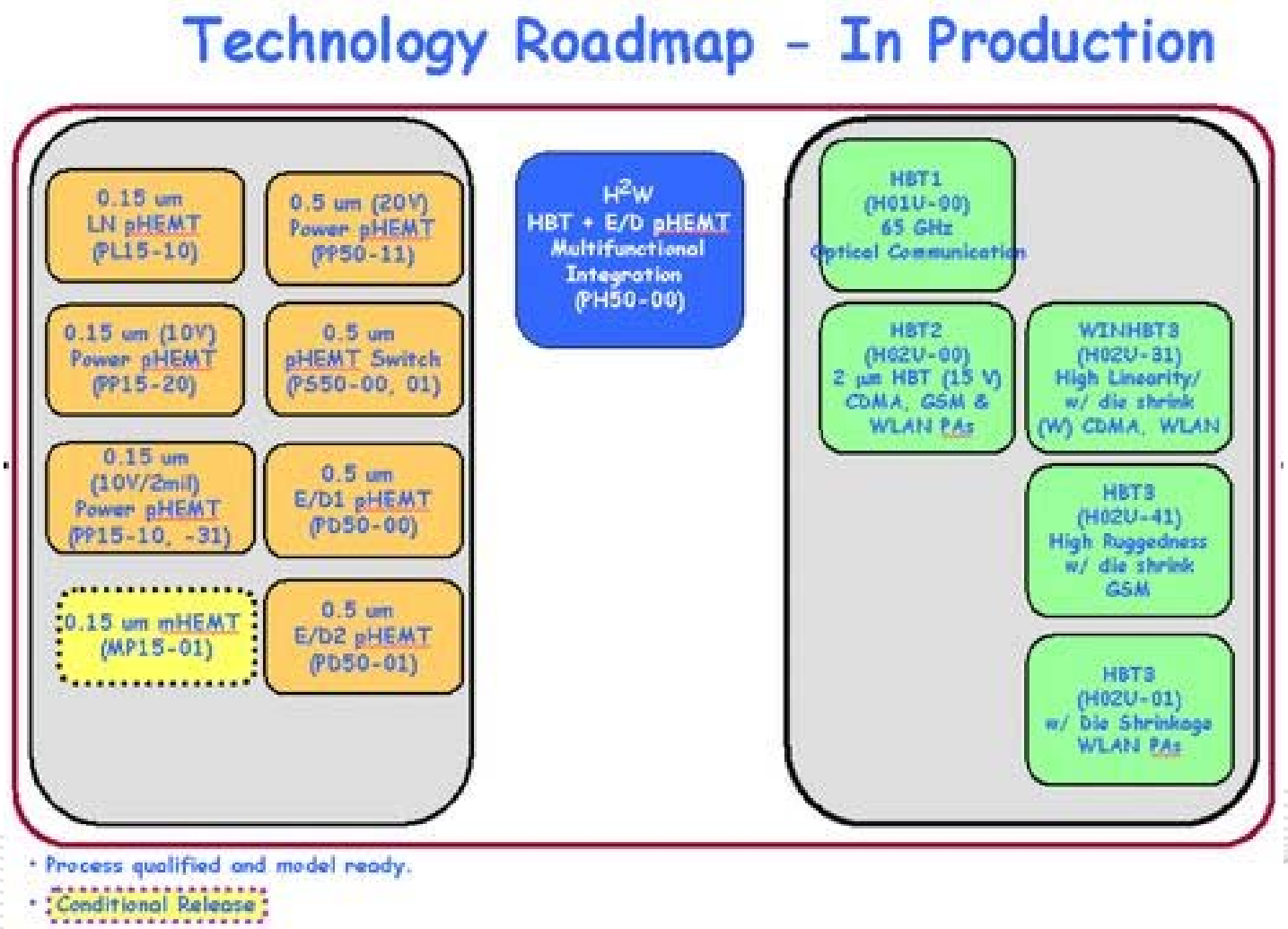
GaAs foundries

→ UMS, France (+ USA)



WIN, Taiwan

→ WIN, Taiwan



GaN

→ 4 inch to 6 inch wafers

→ Several foundries (TriQuint, UMS, Cree, Sandia and others)

→ Very high power possible

→ Defense market, radar, telecommunication

→ Single transistor devices available, very first MMICs launched (IMS 2008, Cree)

→ „Reliability“ problems

→ Frequencies up to 20 GHz and higher (100 GHz)

State-of-the-art

→ HRL examples

GaN HFET MMIC Power Amplifiers

GaN POWER AMPLIFIERS						
Part Number	Function	Frequency (GHz)	Gain (dB)	P1dB (dBm)	Psat (dBm)	Application Note
PA3C-76	High Power Amplifier	71-76	15	24	26	X
PA3C-86	High Power Amplifier	81-86	13	24	26	X
PA3C-96	High Power Amplifier	91-96	12	23.5	25.5	X

http://www.hrl.com/media/gan/gan.html

http://kiss.caltech.edu/mmic2008/presentations/micovic.pdf

Si(Ge)

→ 8 inch production

→ Combination of CMOS logic, ECL and BiCMOS

→ Frequencies up to 100 GHz

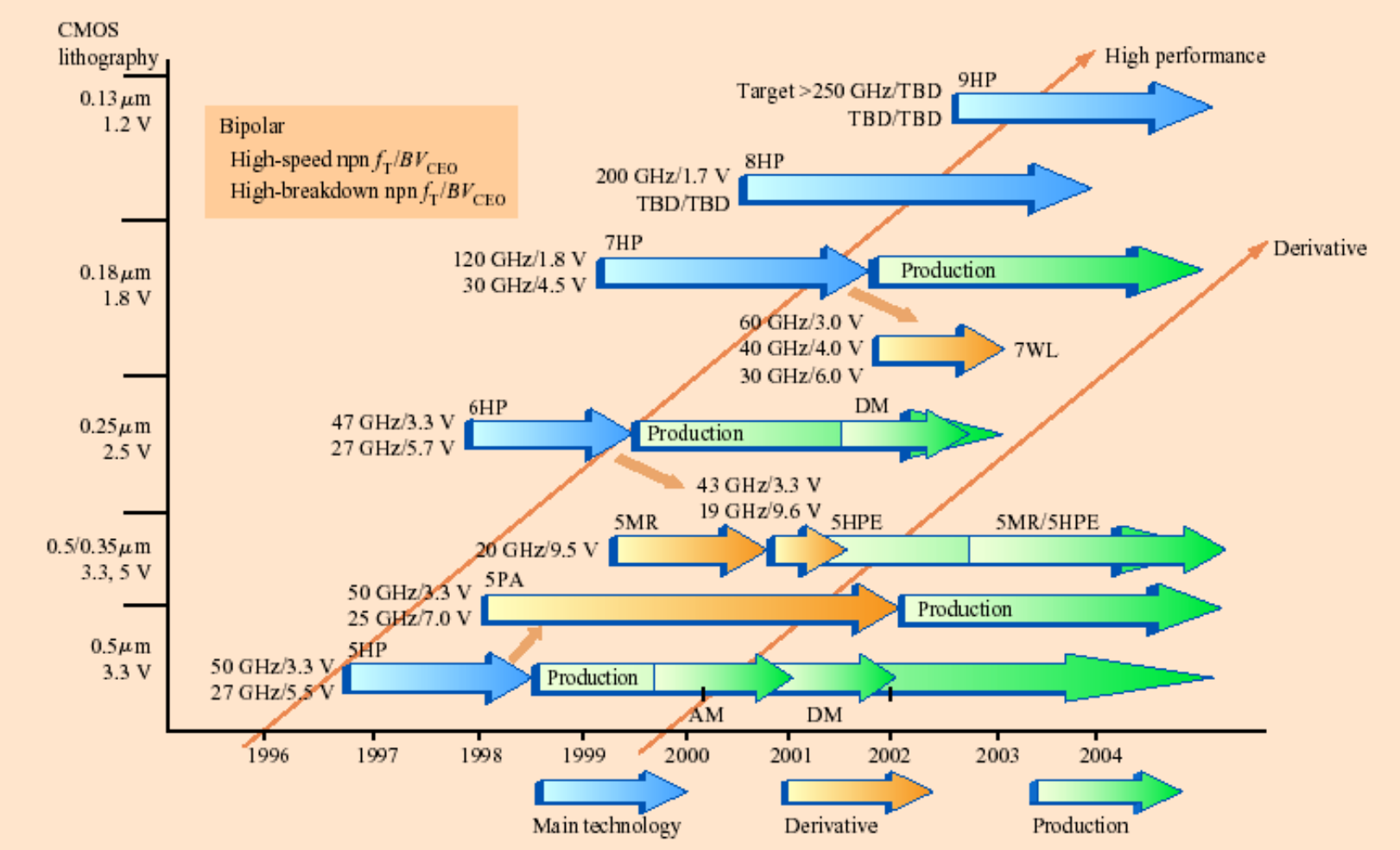
→ Complete transceiver chips possible (e.g. 60 GHz)

→ Well known foundries e.g. IBM (8HP)

→ Si LDMOS for high power

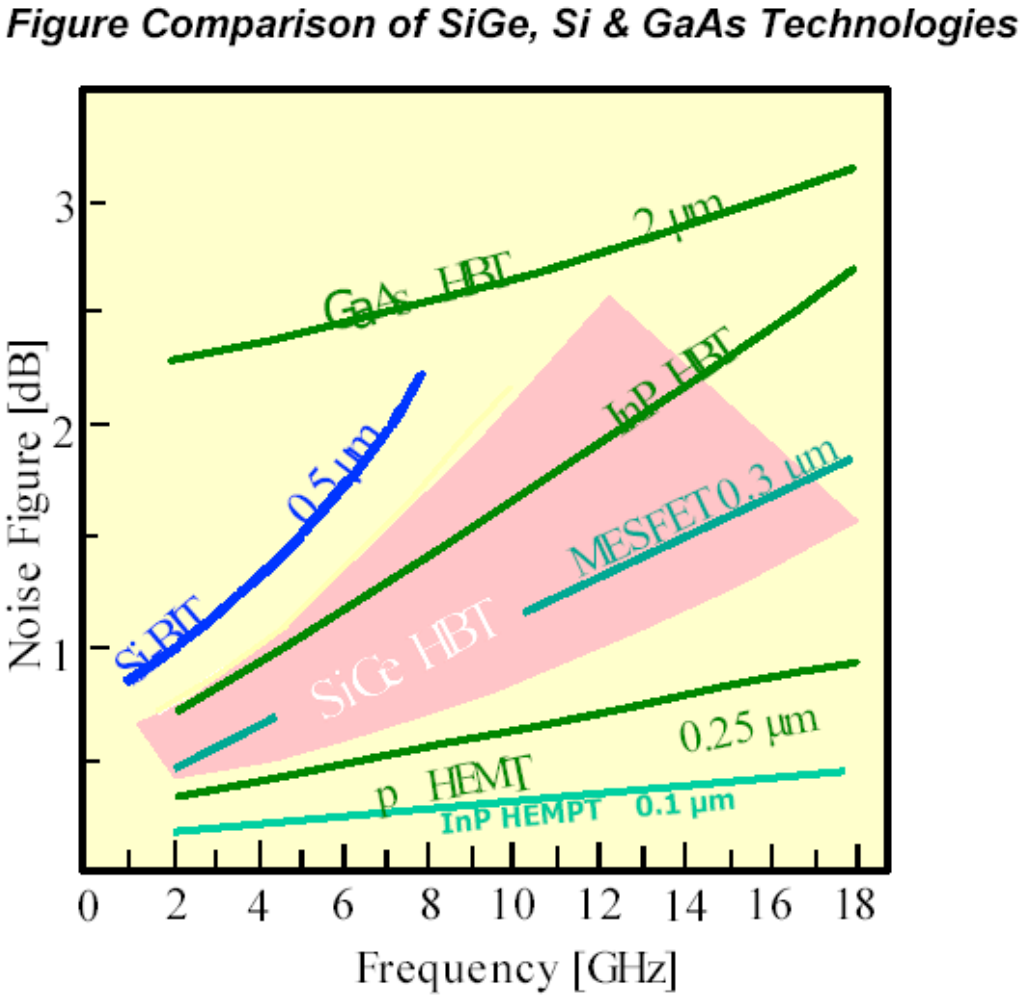
SiGe

→ IBM roadmap



Trade-offs

→ Noise figure

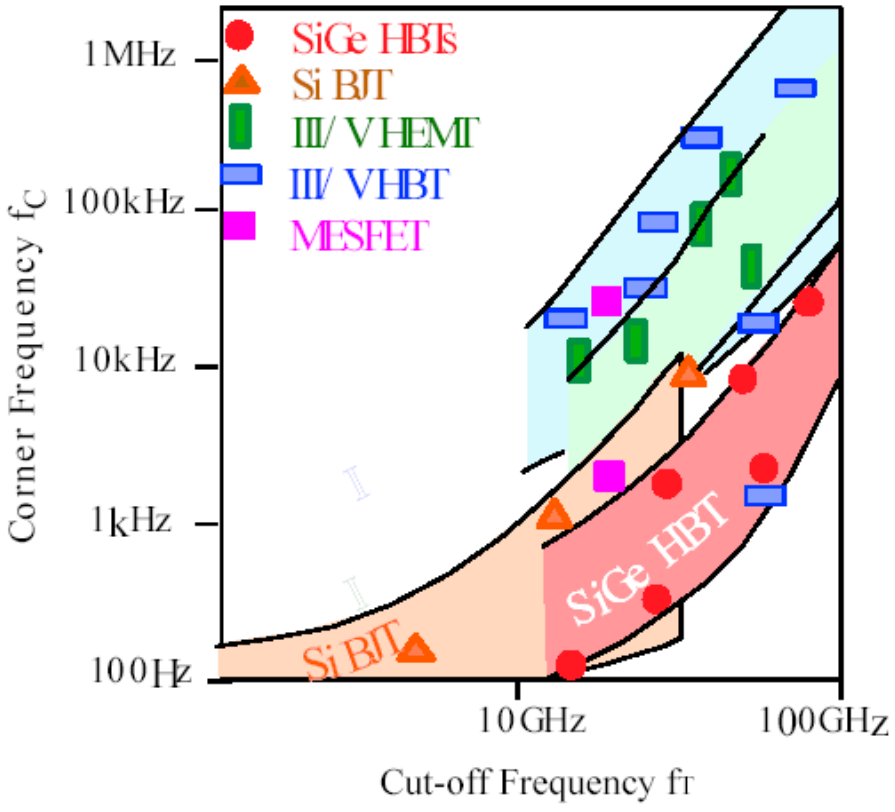


http://www.sirenza.com/pdfs/semiconductor%20technology.pdf

Trade-offs

→ 1/f noise

Low Frequency Phase Noise of SiGe, Si & GaAs Technologies



Trade-offs

→ Costs

Item	GaAs		SiGe		Units
	FET	HBT	HBT	BiCMOS	
Feature Size	0.5	2.0	0.5	0.5	µm
Starting Material	200	600	200	200	$
Mask steps	12	14	28	32	
Photo cost	1200	1400	2800	3200	$
Raw cost	1400	2000	3000	3400	$
Wafer Diameter	100	100	200	200	mm
Yield	80	70	95	95	%
Cost/mm^2	0.22	0.36	0.10	0.11	$/mm^2

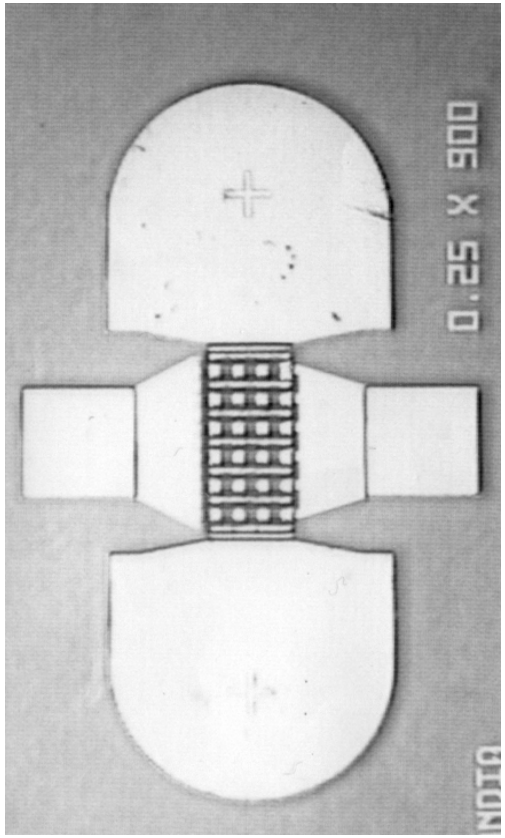
Trade-offs

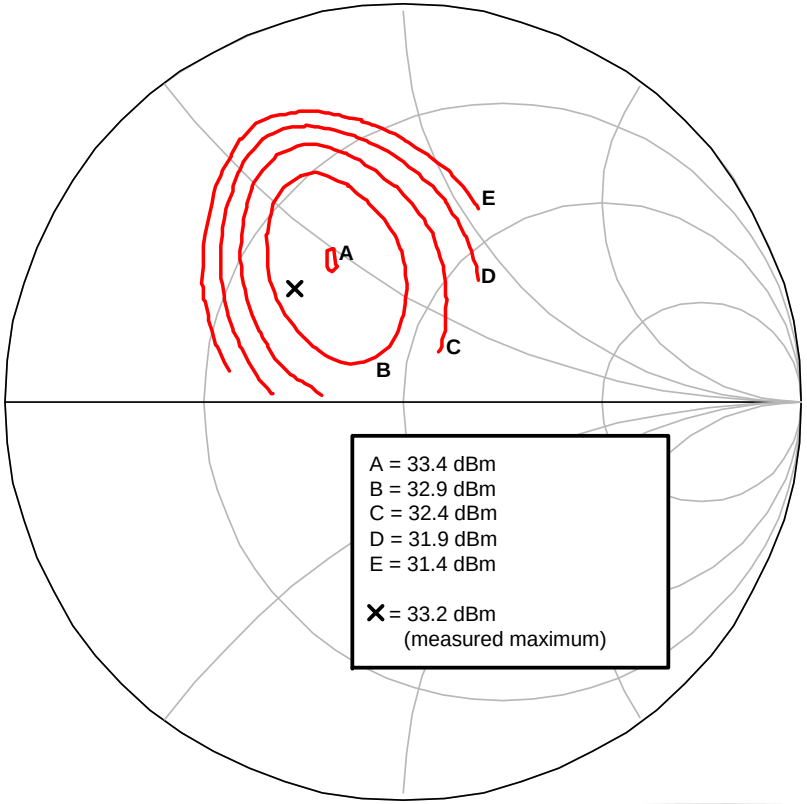
→ Power and linearity

Technology	Price/Watt	Power Density	Supply Voltage	Linearity	Frequency	PAE
Si BJT	Low Cost	Medium	26 V	Poor	<2 GHz	Low
SiGe BJT	Low Cost	Medium	<20 V	Good	>2 GHz	High
Si LDMOS	Low Cost	Low	26 V	Very Good	<3 GHz	Medium
GaAs MESFET	Competitive	Medium	12 V	Good	>2 GHz	Medium
GaAs pHEMT	Medium	Medium	8 V to 12 V	Very Good	>2 GHz	High
GaAs HBT	Competitive	High	8 V to 26 V	Good	>2 GHz	High
SiC MESFET	Competitive	Very High	48 V	Good	>4 GHz	Medium
GaN HEMT	N/A	Very High	48 V	Promising	>12 GHz	High

GaN devices

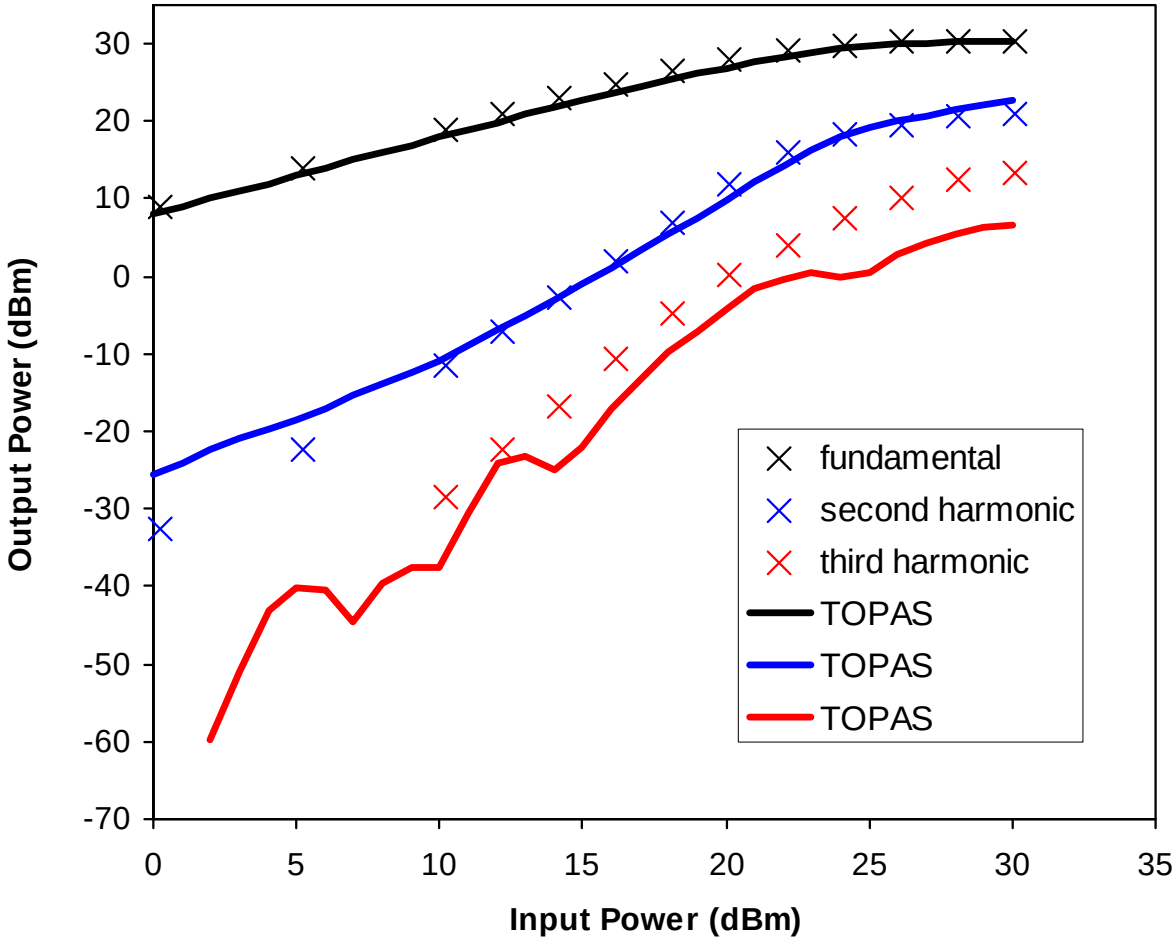
→ Non-linear model and measurement





GaN devices

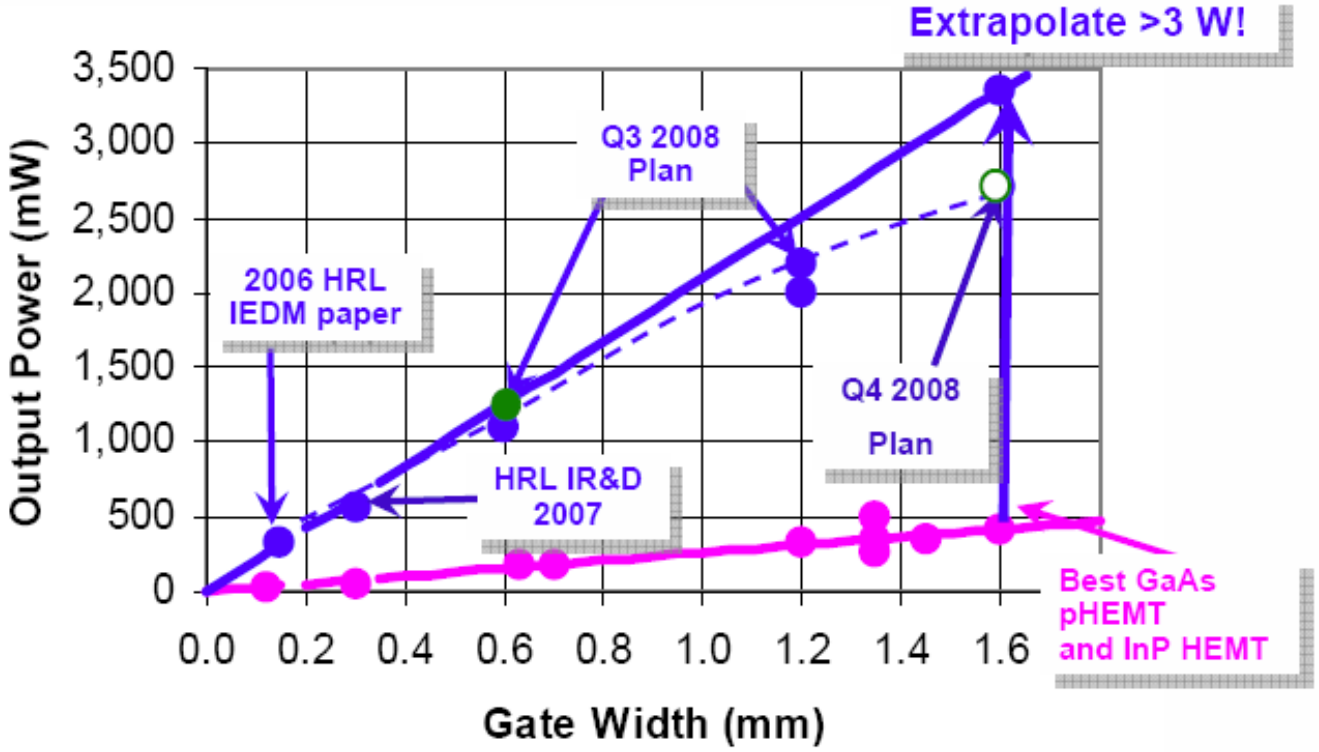
→ Model verification



GaN mmwave power

HRL LABORATORIES

HRL W-band GaN Roadmap



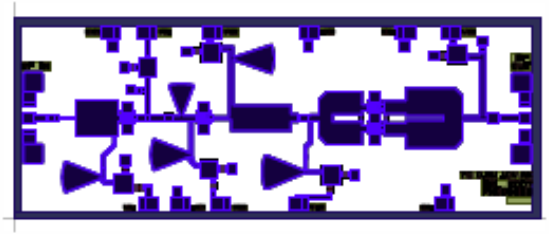
Disruptive W-band GaN Power MMICs

8X higher power density than mmW GaAs pHEMT

GaN mmwave PA

HRL LABORATORIES

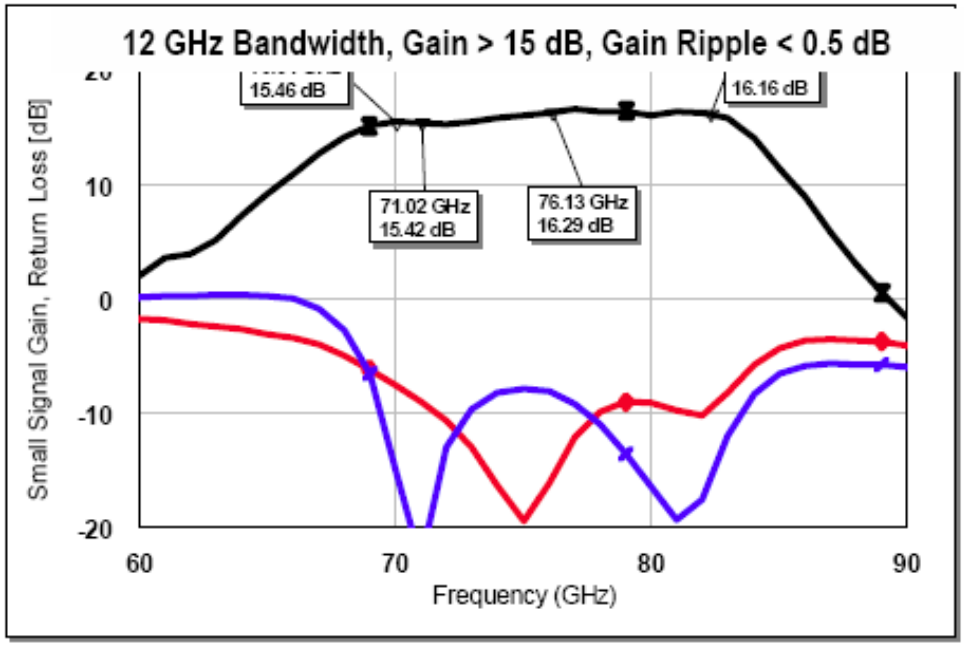
500 mW 70 GHz GaN MMIC PA



70 GHz MMIC Chip Layout
Size 3.4 mm x 1.3 mm

Operating Voltage = 15 V

Measured Gain > 15 dB



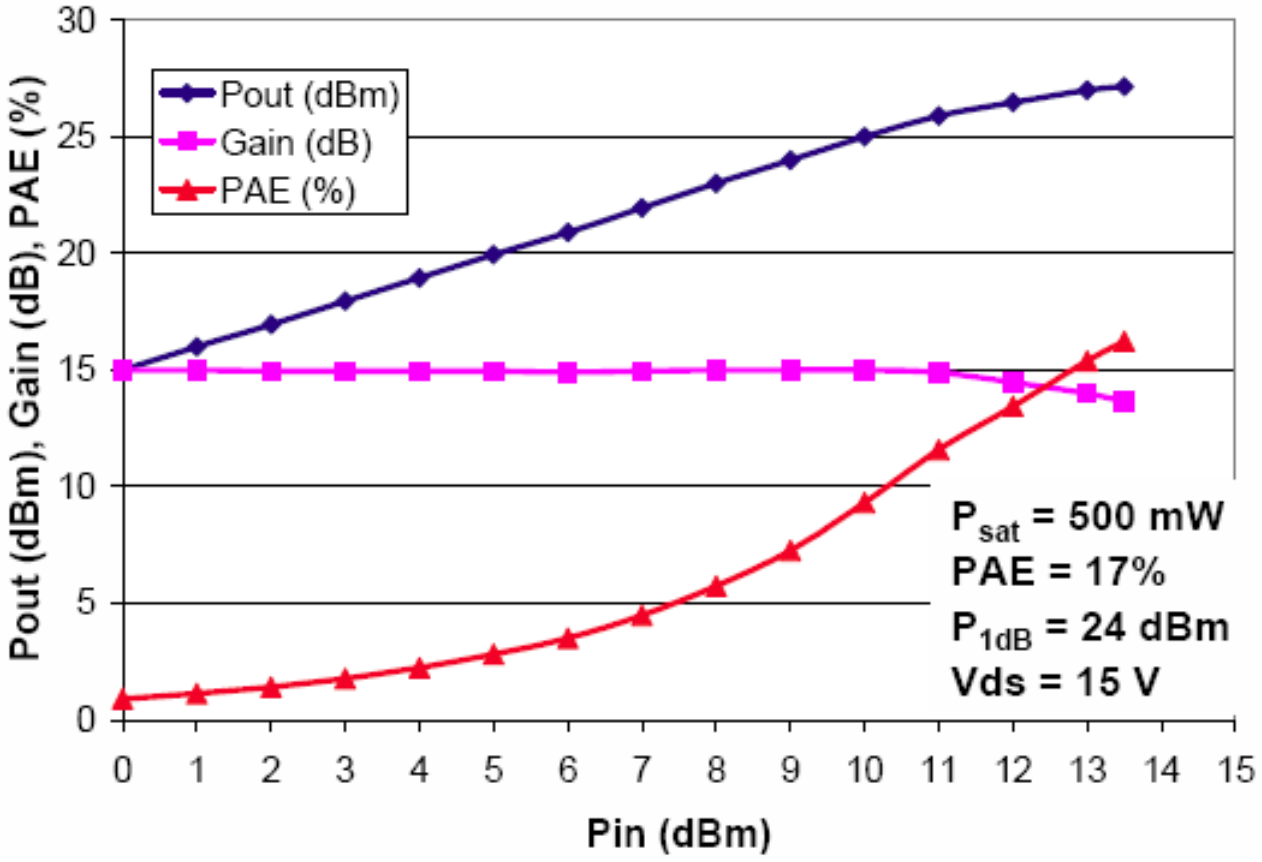
Measured small signal gain of 70 GHz 500 mW GaN MMIC PA.

Performance meets design goal.

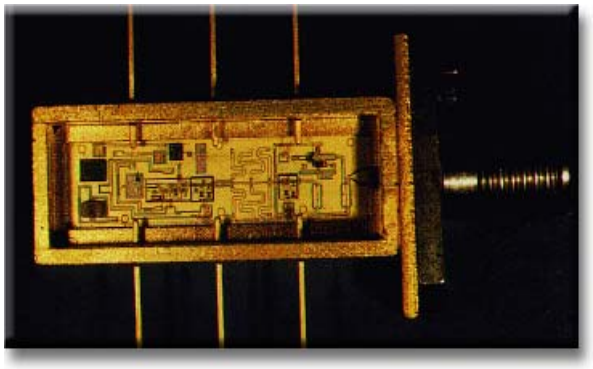
GaN mmwave PA

HRL LABORATORIES

Output power of 70 GHz MMIC measured at a frequency of 76 GHz



Integrated coplanar 24 GHz sensor

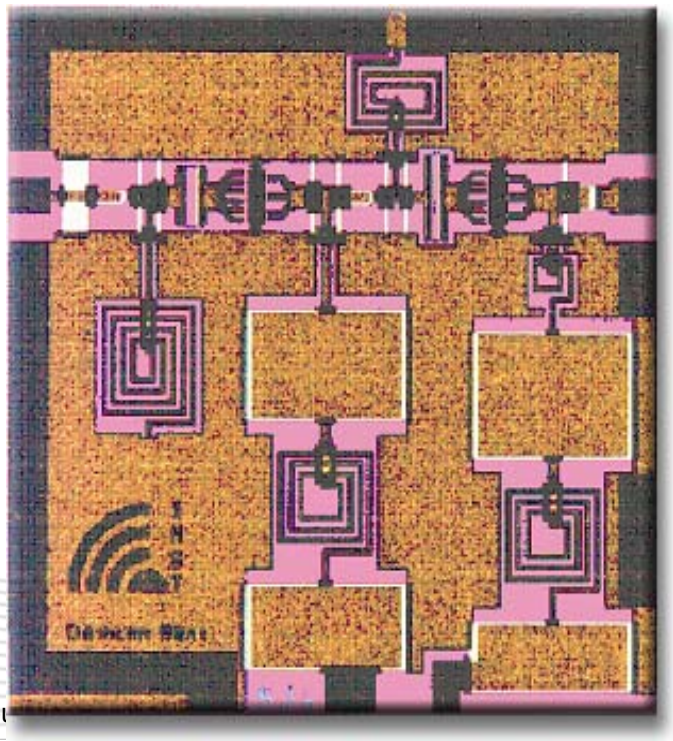


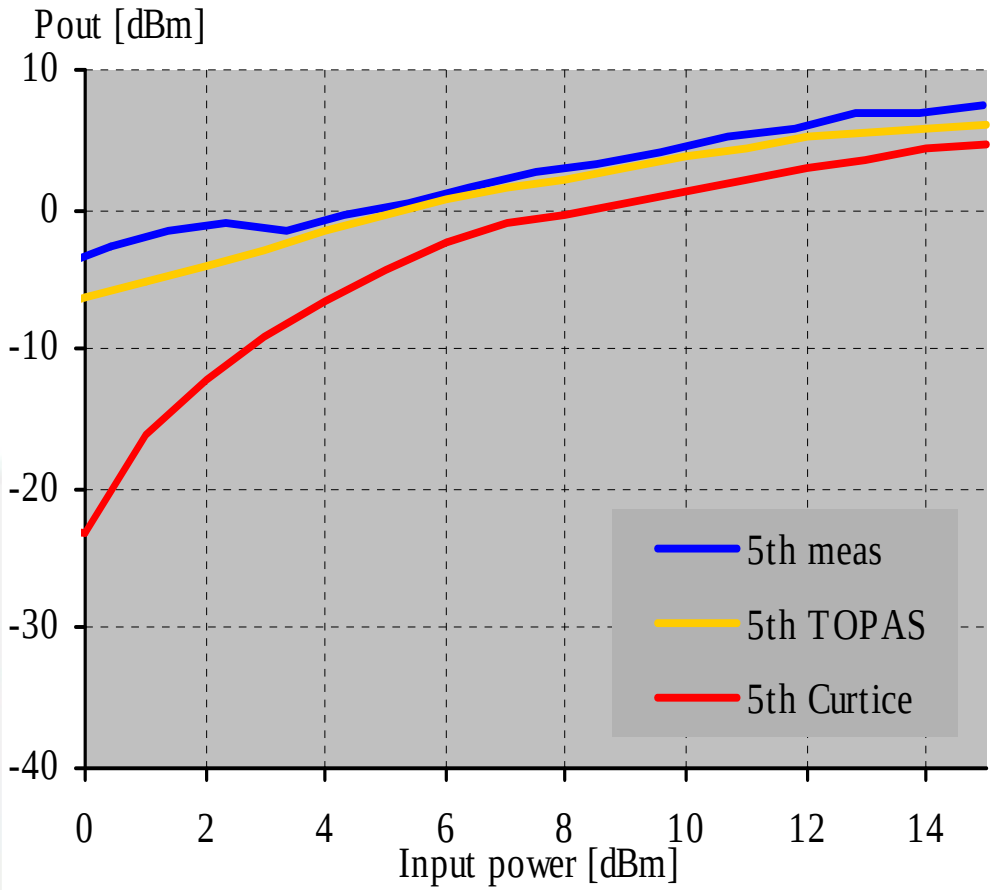
World‘s 1st 24 GHz coplanar sensor designed at IMST

Rosemount 24 GHz level sensor

Integrated GaAs circuits – 24 GHz sensor

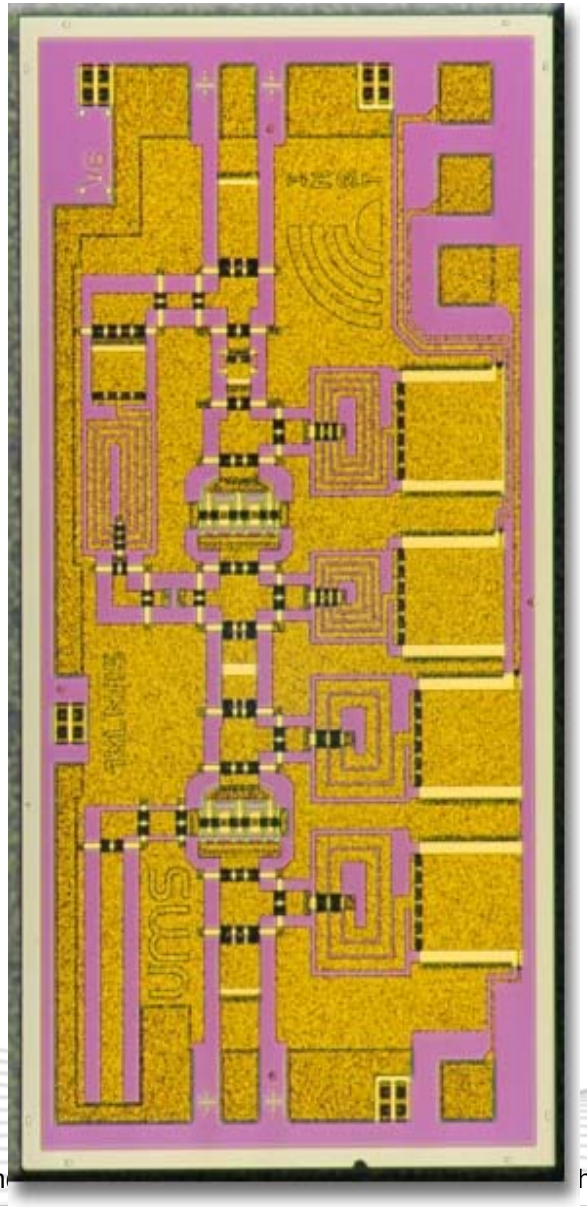
Simulated using



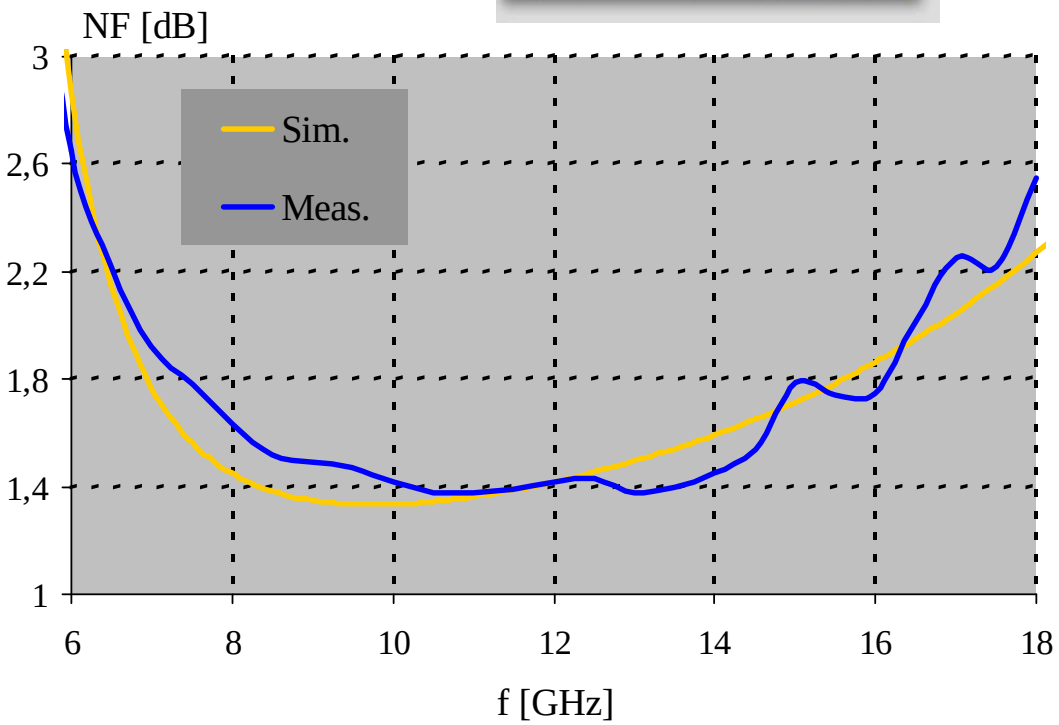


Frequency times 5 multiplier

GaAs circuits – 10 GHz LNA



Simulated using



Low noise amplifier

Core Chip Design : 2NLNA4PS2

Specifications:

- → Ku-band core chip including the 2-stage LNA and the 4-bit phase shifter
- → Technology: OMMIC - ED02AH
- → LNA bias supply: $V_{G1,2}$ = -0.2 V, $V_{D1,2}$ = 2.0 V, I_{D1} = 28.2 mA, I_{D2} = 29.0 mA
- → PS control voltages: V_C = 0 V / -2 V
- → f = 10.7 ... 12.7 GHz
- → $S_{11} \leq$ -13.3 dB (all states)
- → $S_{22} \leq$ -11.6 dB (all states)
- → S_{21} = 13.2 ... 14.4 dB (all states)
- → RMS amplitude error = 0.4 dB
- → RMS phase error = 2.6 °
- → A = 2.17 × 2.05 mm^2 = 4.45 mm^2

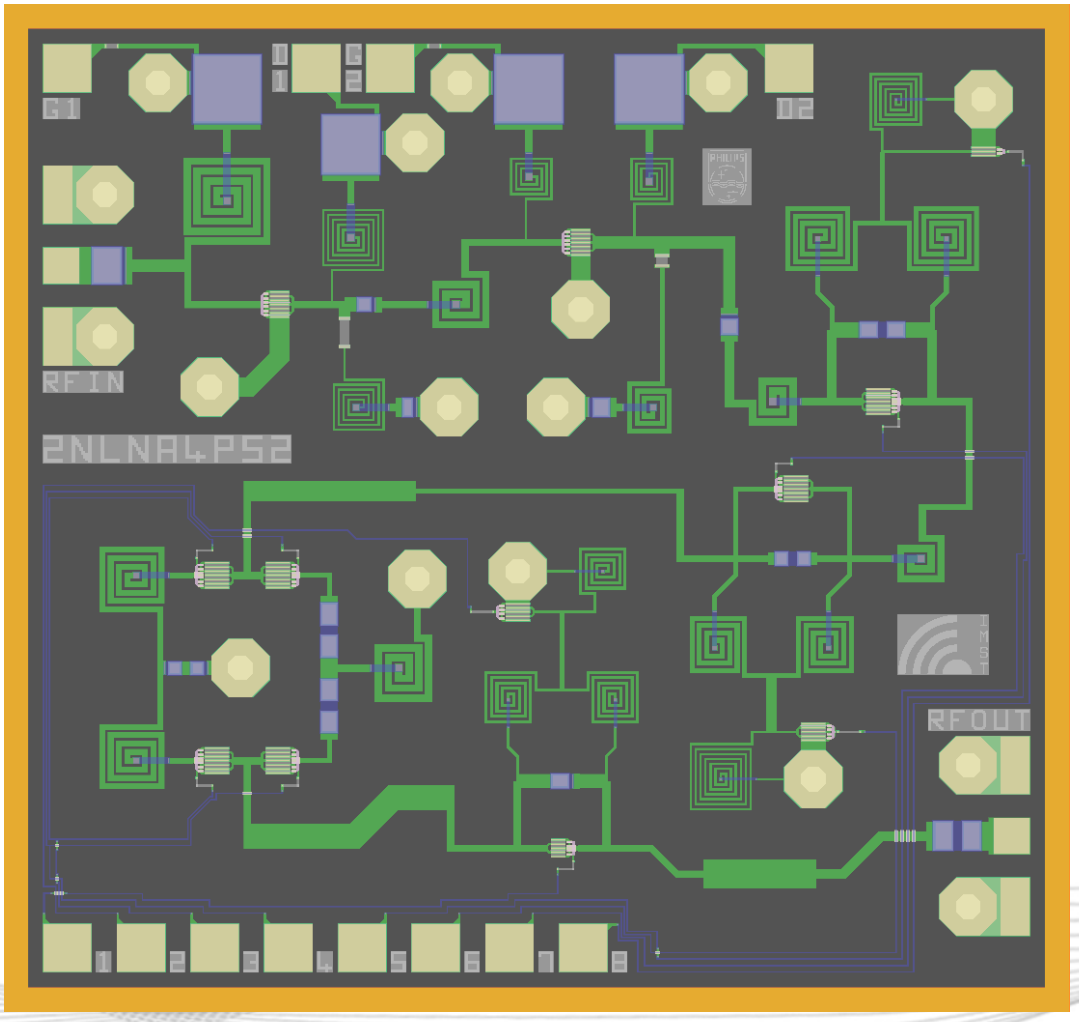
  ⇒ including half dicing street

  ⇒ including DC pads (#8) for the PS control (not necessary if using the DC control circuit)

  ⇒ excluding DC control circuit (serial to parallel converter + buffers)

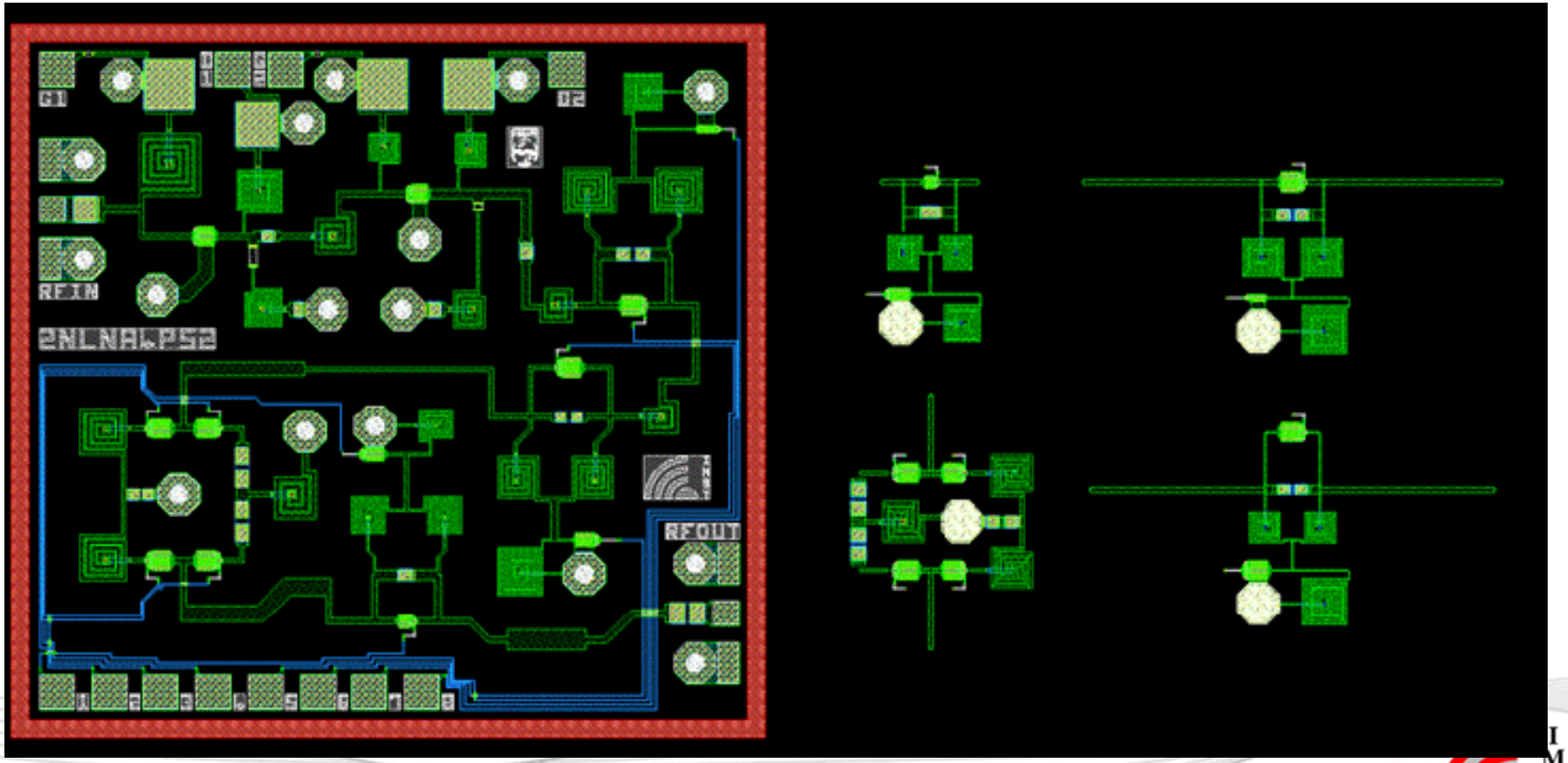
Core Chip Design : 2NLNA4PS2

Layout:

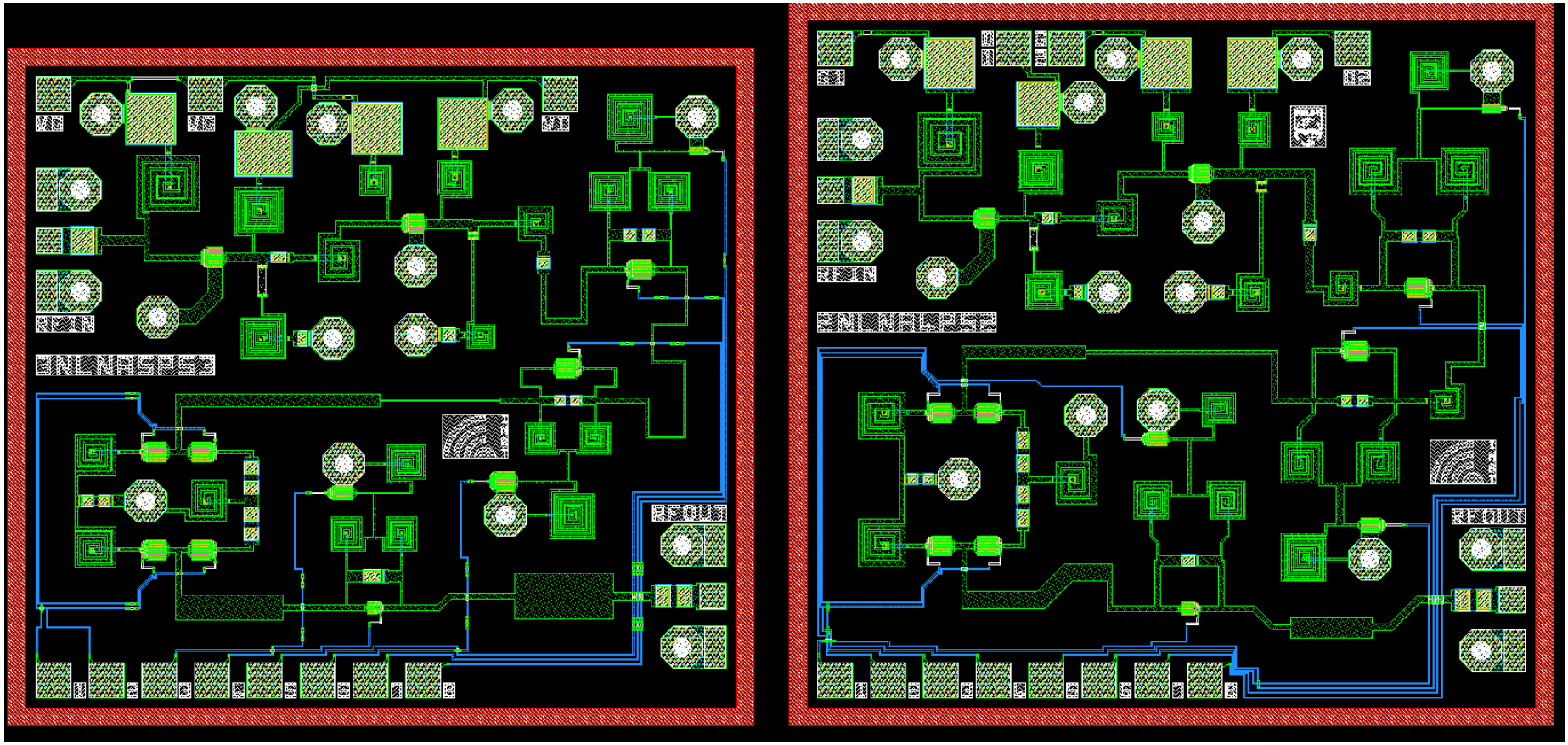


Momentum simulation

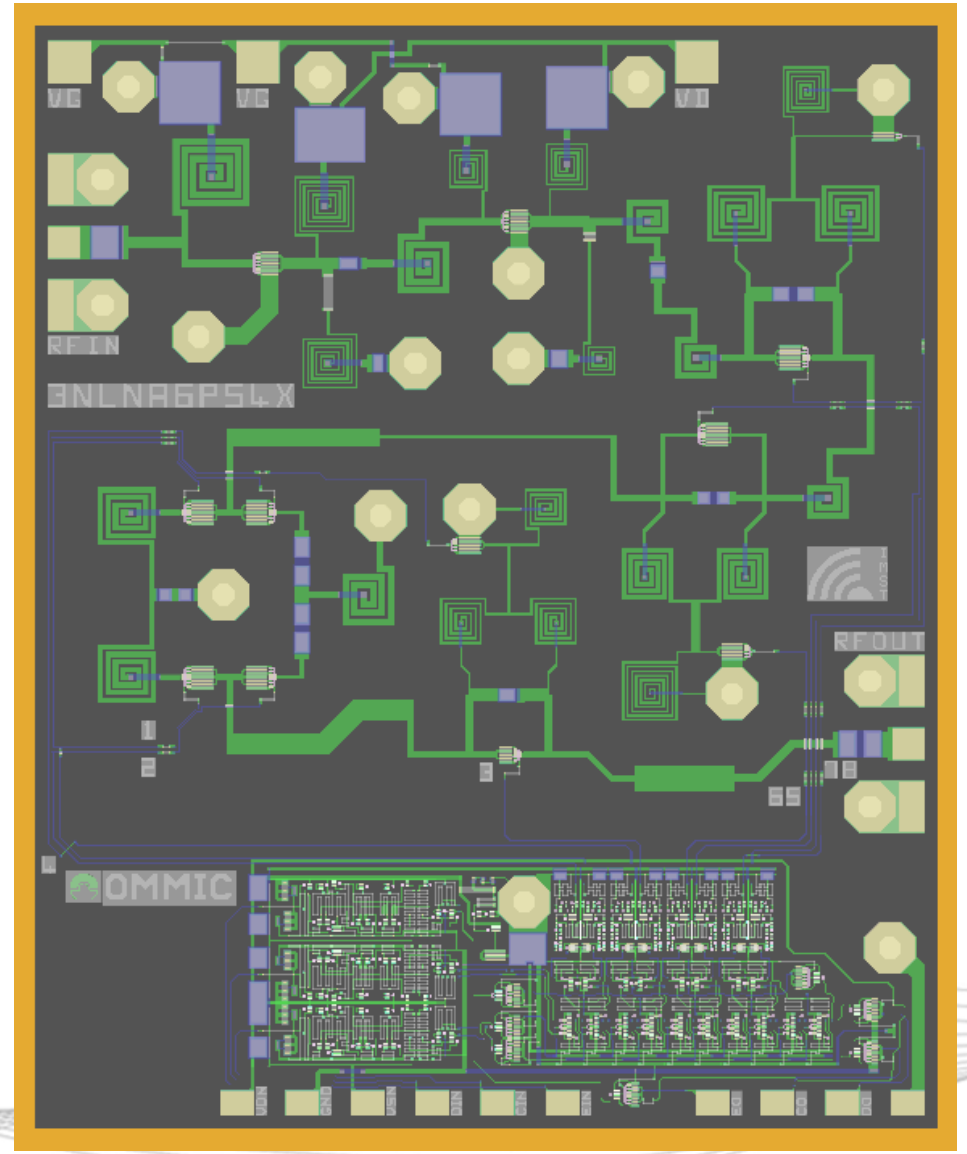
→ Higher integration possible



Size reduction



Including logic

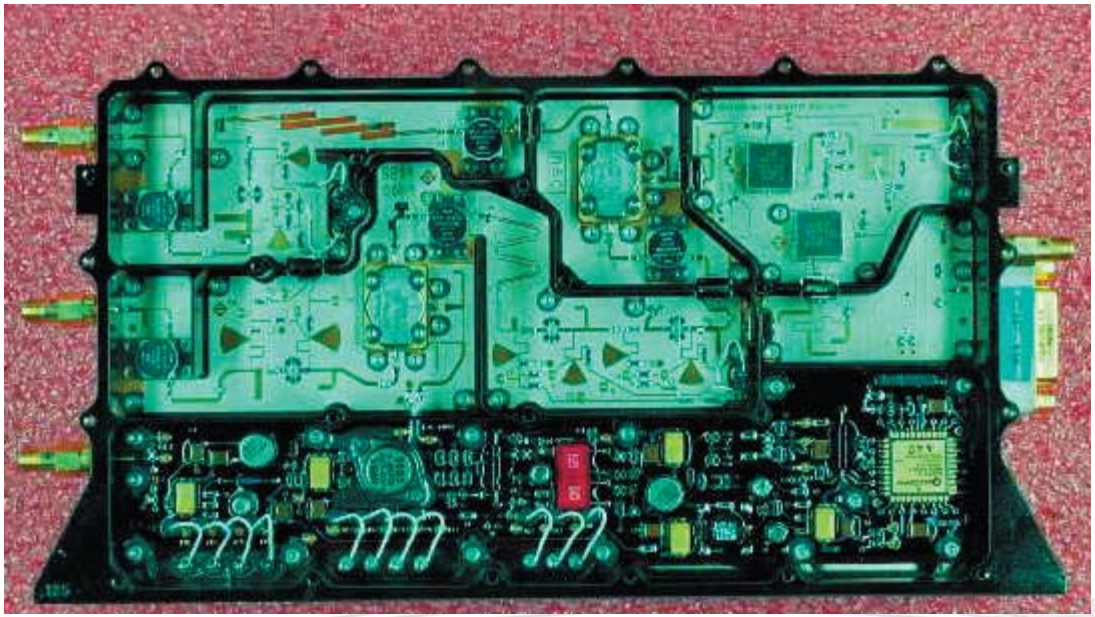


System example synthesizer

→ Large size (LO)

→ Heavy

→ Single frequency



→ small and integrated chip

http://www.saabgroup.com/en/ProductsServices/BusinessUnit/saab_ericsson_space.htm
http://products.saabgroup.com/PDBWebNew/GetFile.aspx?PathType=ProductFiles&FileType=Files&Id=6071

Phase noise

Simplified Leeson equation

$$L(f_m) = \frac{FkTG}{8Q_L P}\left(\frac{f_r}{f_m}\right)^2$$

$$|S_{21}| = \frac{1}{G} = 1 - \frac{Q_L}{Q_0}$$

G:	Gain of active part
F:	Noise figure of active part
Q_L:	Loaded Q of resonator
f_r:	Resonance frequency
f_m:	Offset frequency from carrier
P:	Output power of active part
S_{21}:	Transmission coefficient of resonator at resonance

VCO requirement

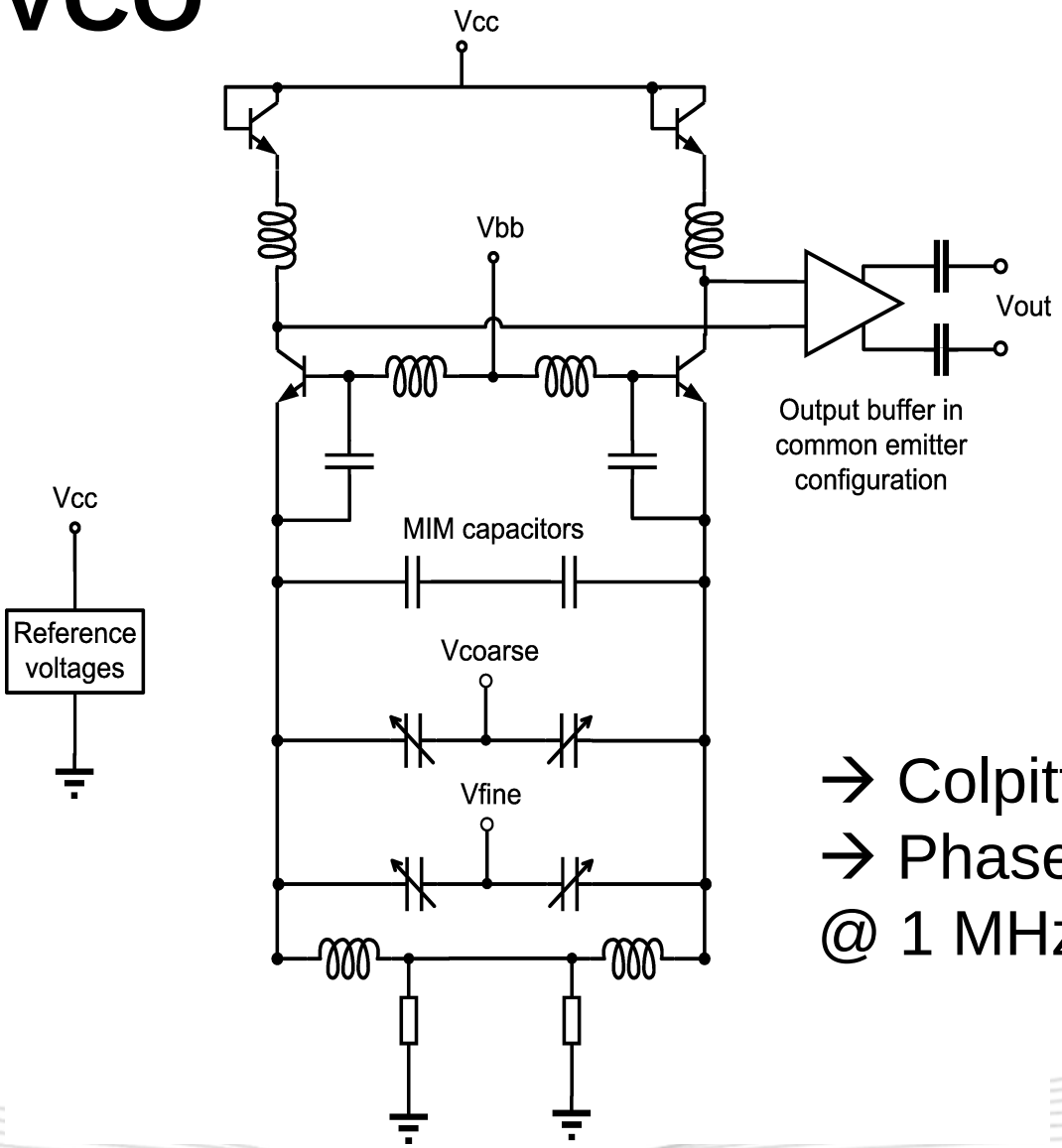
→High quality factor of the resonator

→Large voltage swing (high output power)

→High breakdown voltage for active part transistor technology

→Use a transistor with low 1/f noise

VCO



→ Colpitts
→ Phase noise: -115 dBc/Hz
@ 1 MHz offset (20 GHz)

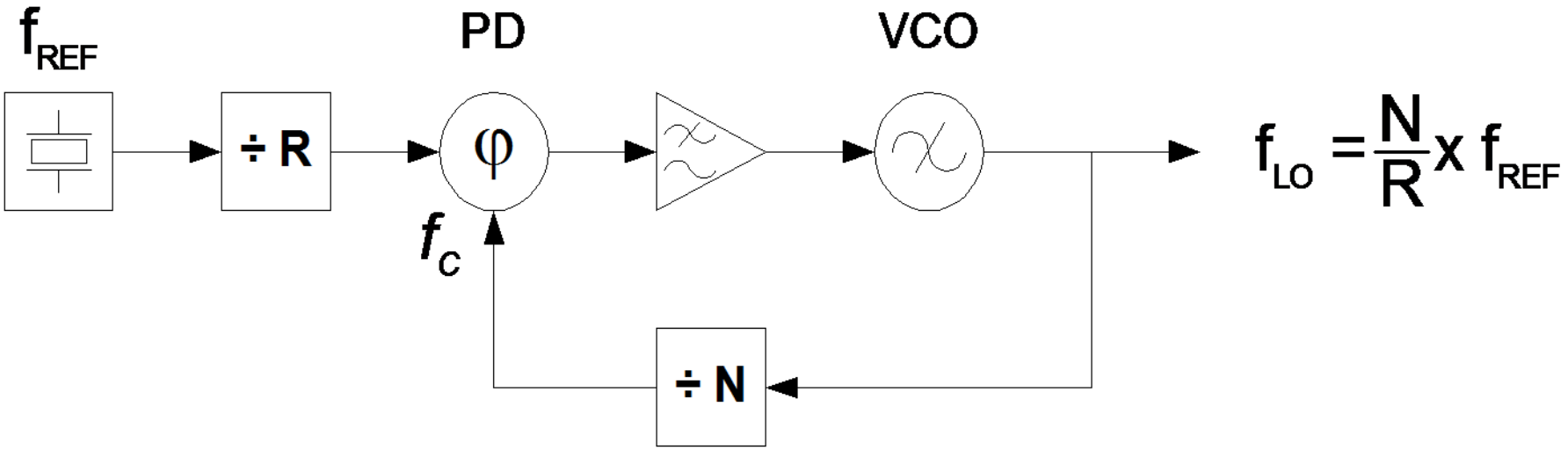
PLLs

→Close to the carrier phase noise is determined by the reference crystal

→Inside PLL loop the phase noise of a synthesizer is determined by the PLL (phase detector). VCO noise is attenuated.

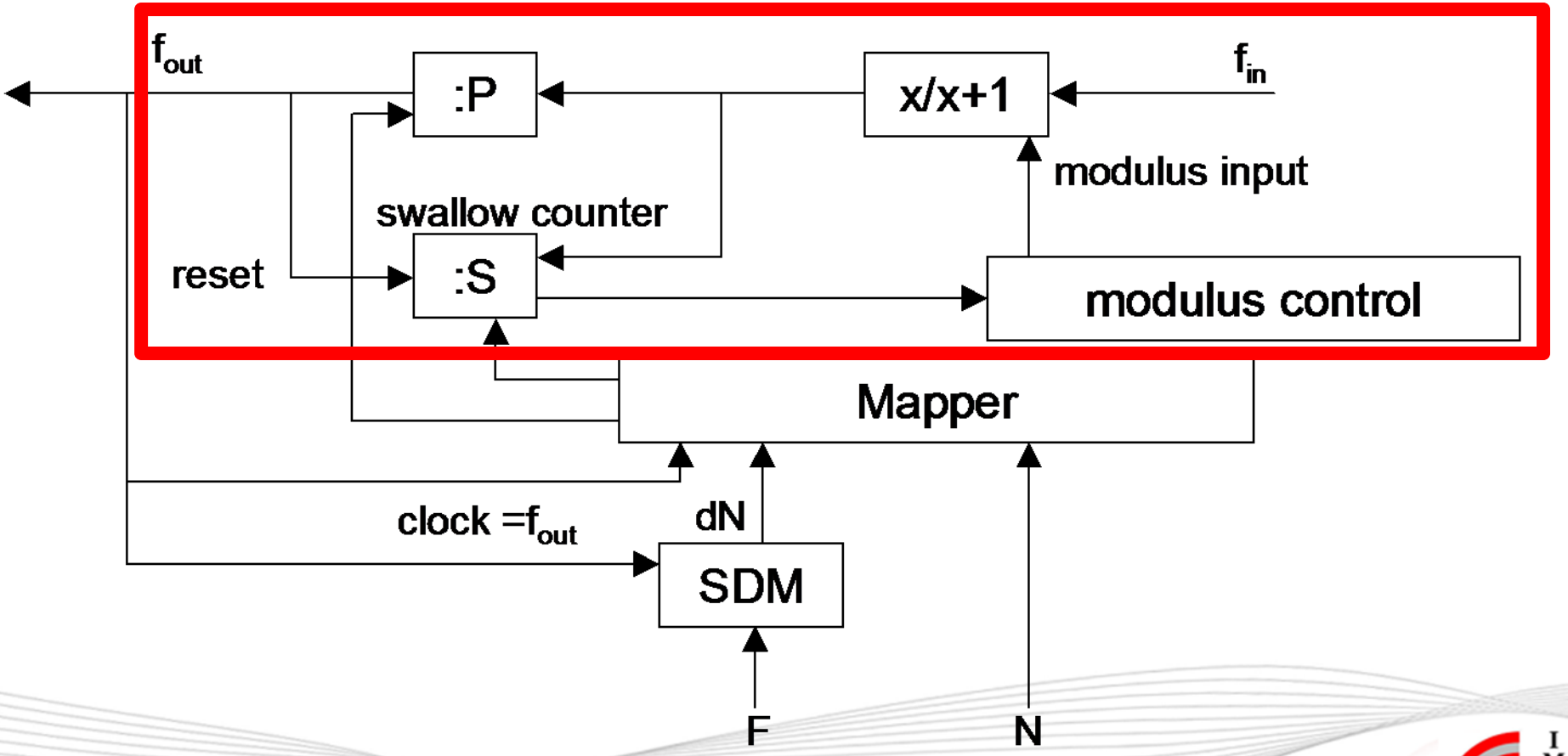
→Output PLL loop the phase noise of a synthesizer is determined by the VCO phase noise

Integer-N PLL with reference divider



How to generate arbitrary frequencies?

→ Build a programmable 1/N-divider



Continous division (example x=8)

→ Divide S times by x+1 and P-S times by x

N=(x+1)*S+x*(P-S)=8*P+S, P>S

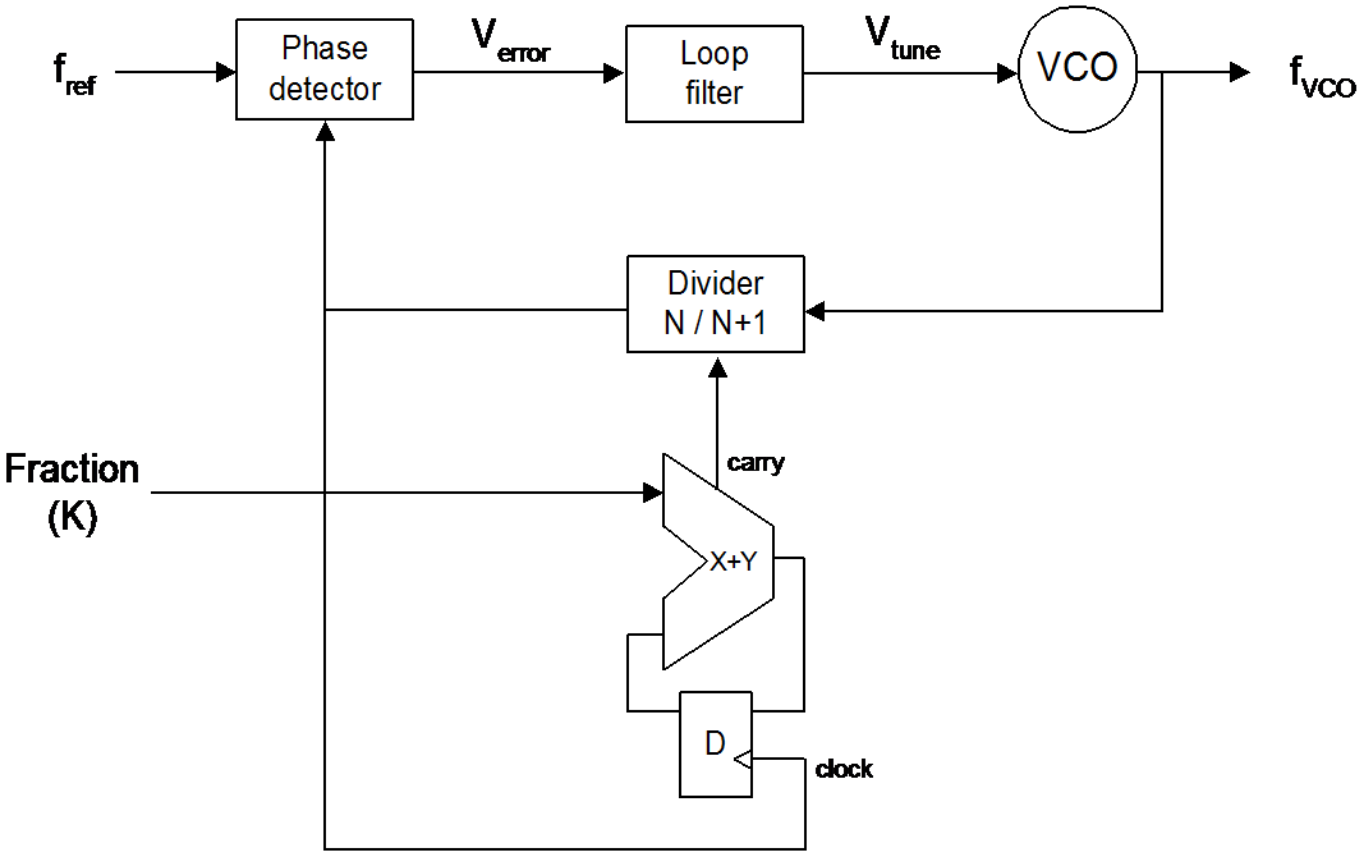
...

P=6,S=0..6: N=8*6+0..8*6+7=48..54, 55 not possible

P=7,S=0..7: N=8*7+0..8*7+7=56..63
P=8,S=0..7: N=8*8+0..8*8+7=64..71

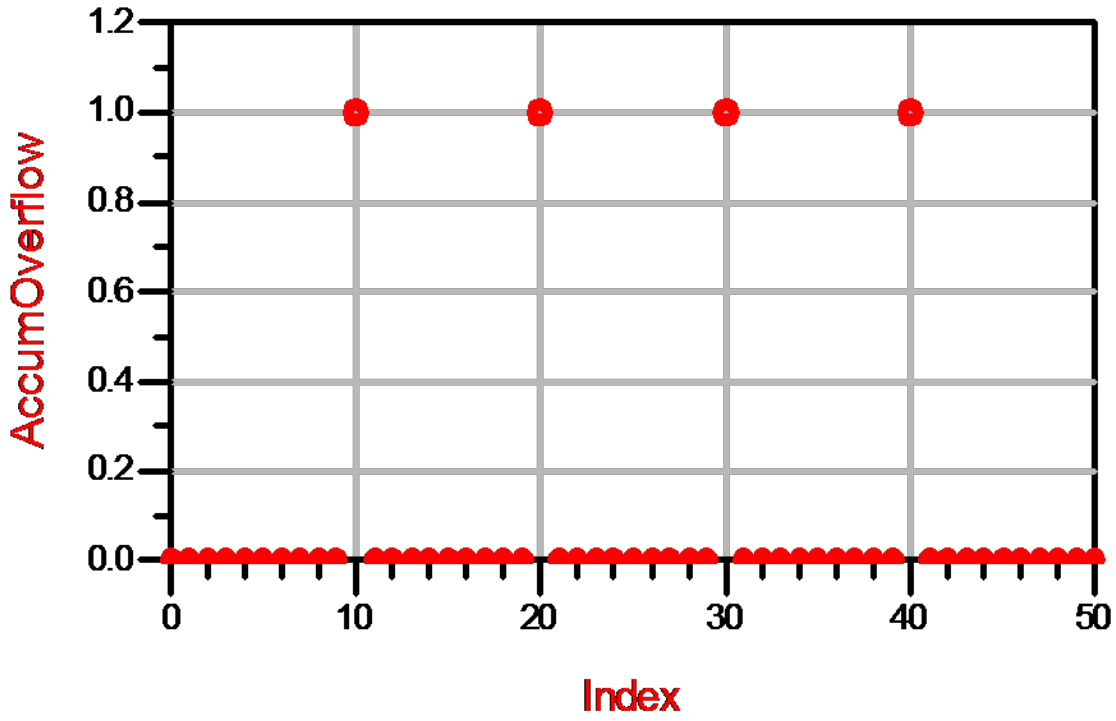
...

Simplified fractional-N PLL example



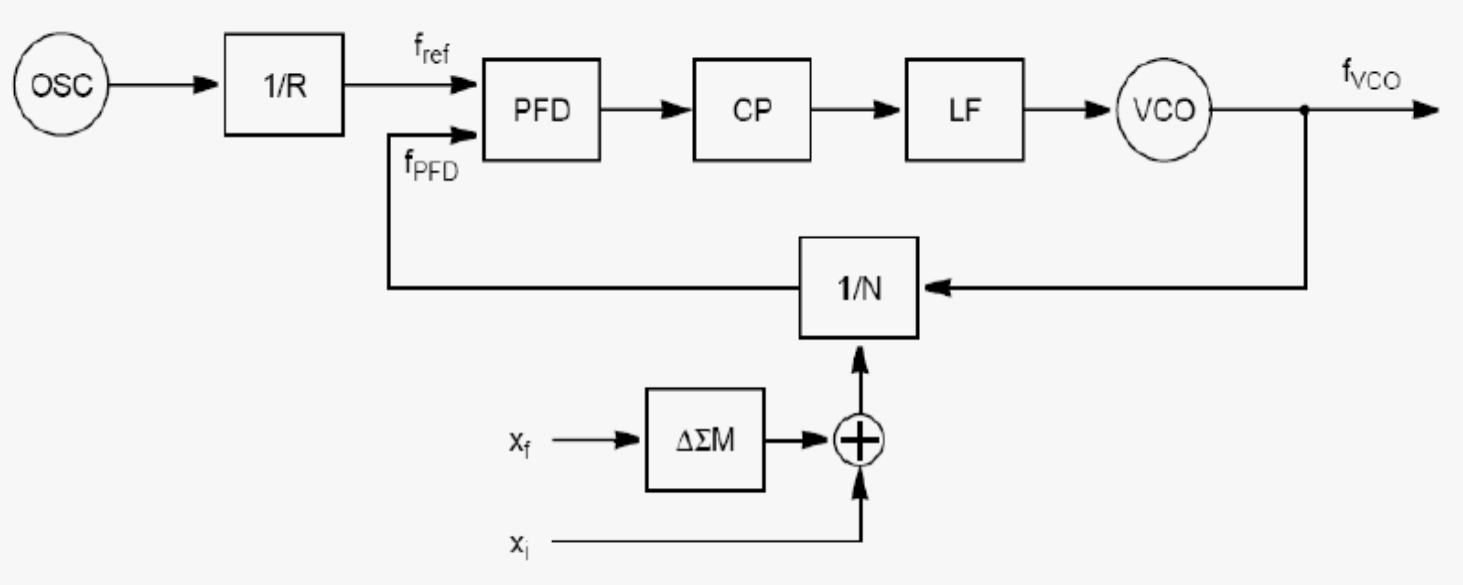
Ratio: 10.1: Divide 9 times by 10 and one time by 11 (next page)

Accumulator



This division schema generates large spurs.

Sigma Delta Modulator (SDM)



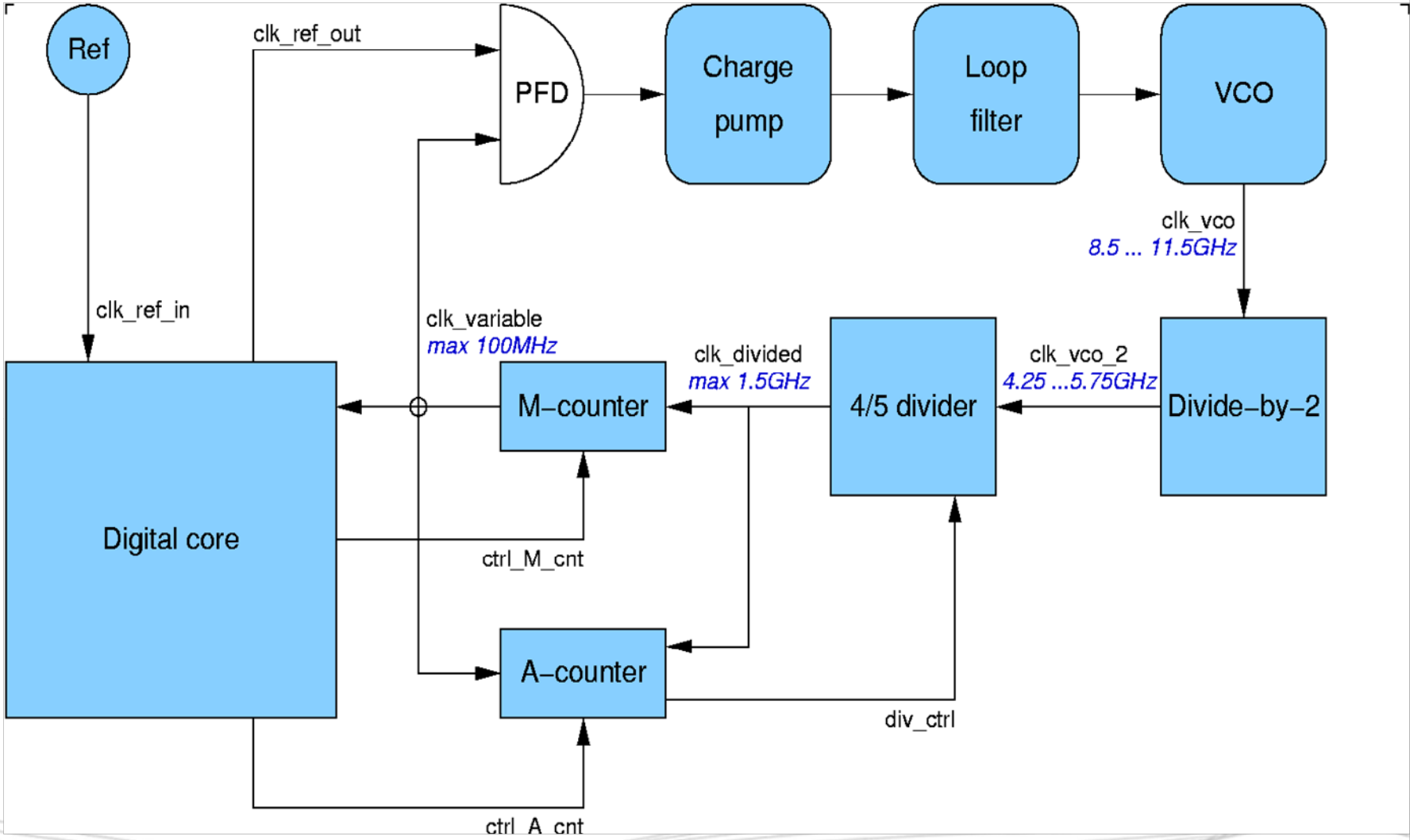
Modulator input: Only fractional part x_f
SDM generates series of integer numbers n_i
$n_i \in M$, 2^{μ} values are available for M

$$x_f = \bar{n}_i = \lim_{N\to\infty} \frac{1}{N} \sum_{i=1}^{N} n_i$$

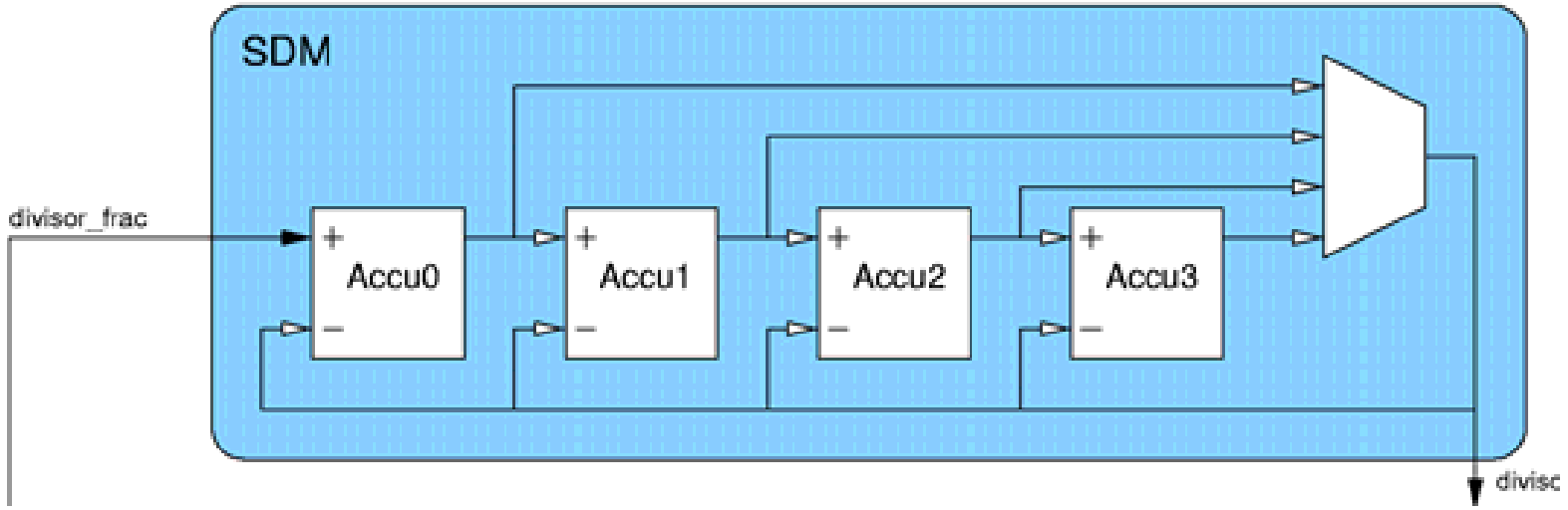
Time average value at SDM output

Example: 2, -4, -2, 3, 0, 3 –1, -3, 2, 1, ... for $x_f = 0.1$

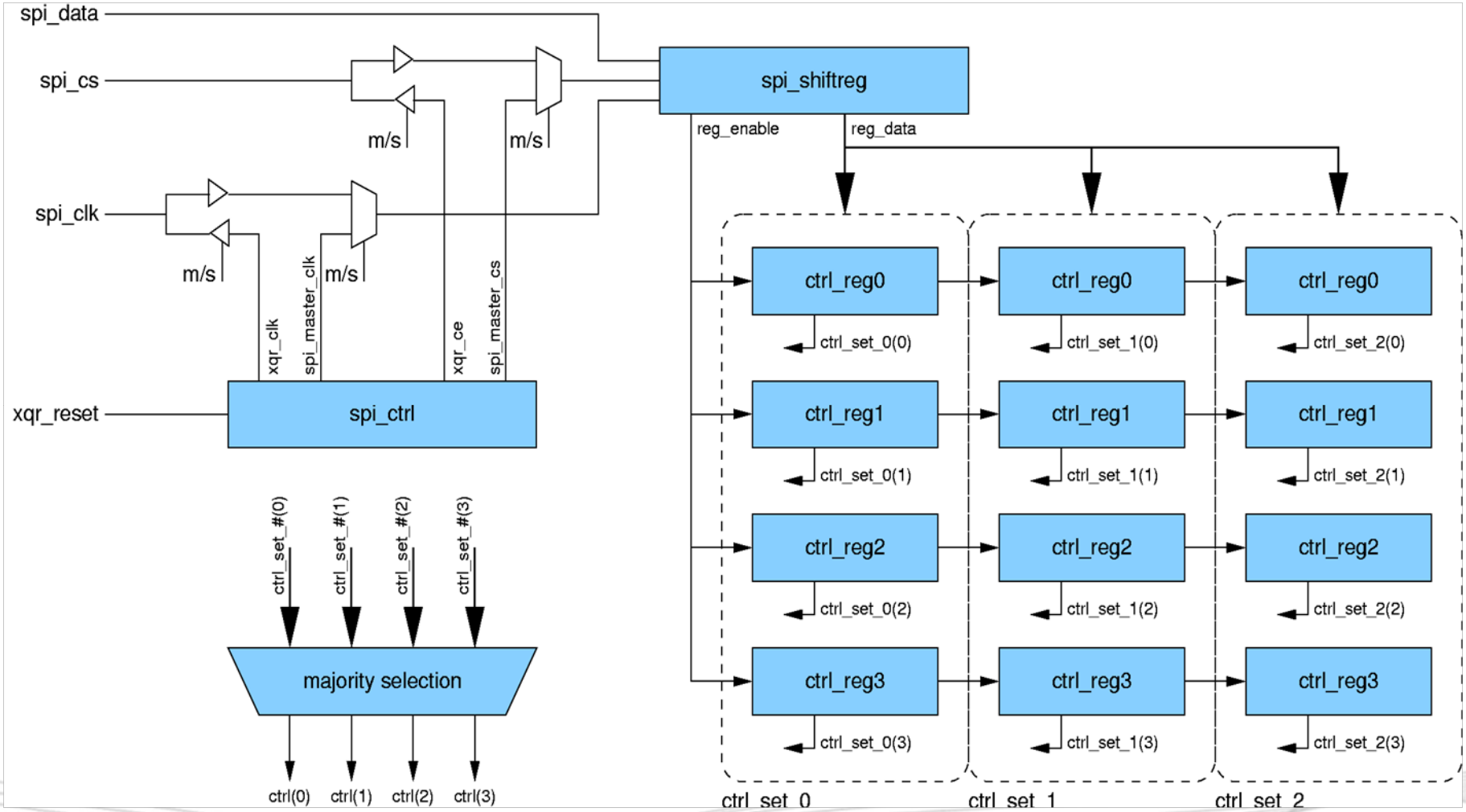
Synthesizer architecture (1)



Synthesizer architecture (2)



Synthesizer architecture (3)



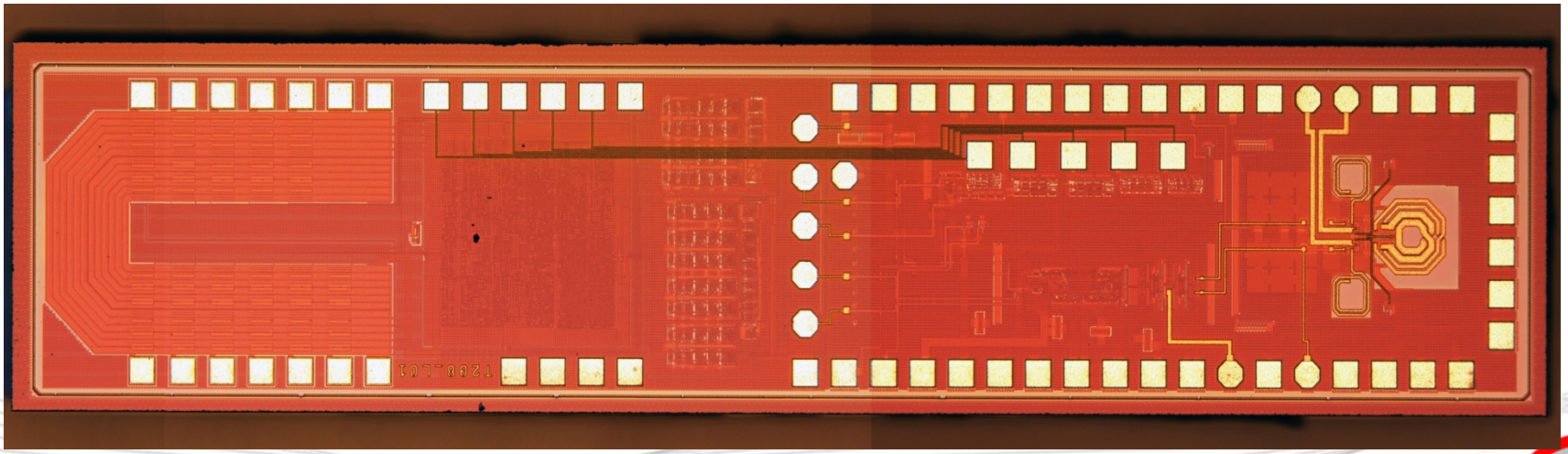
SiGe Design

→ World best 1-chip synthesizer

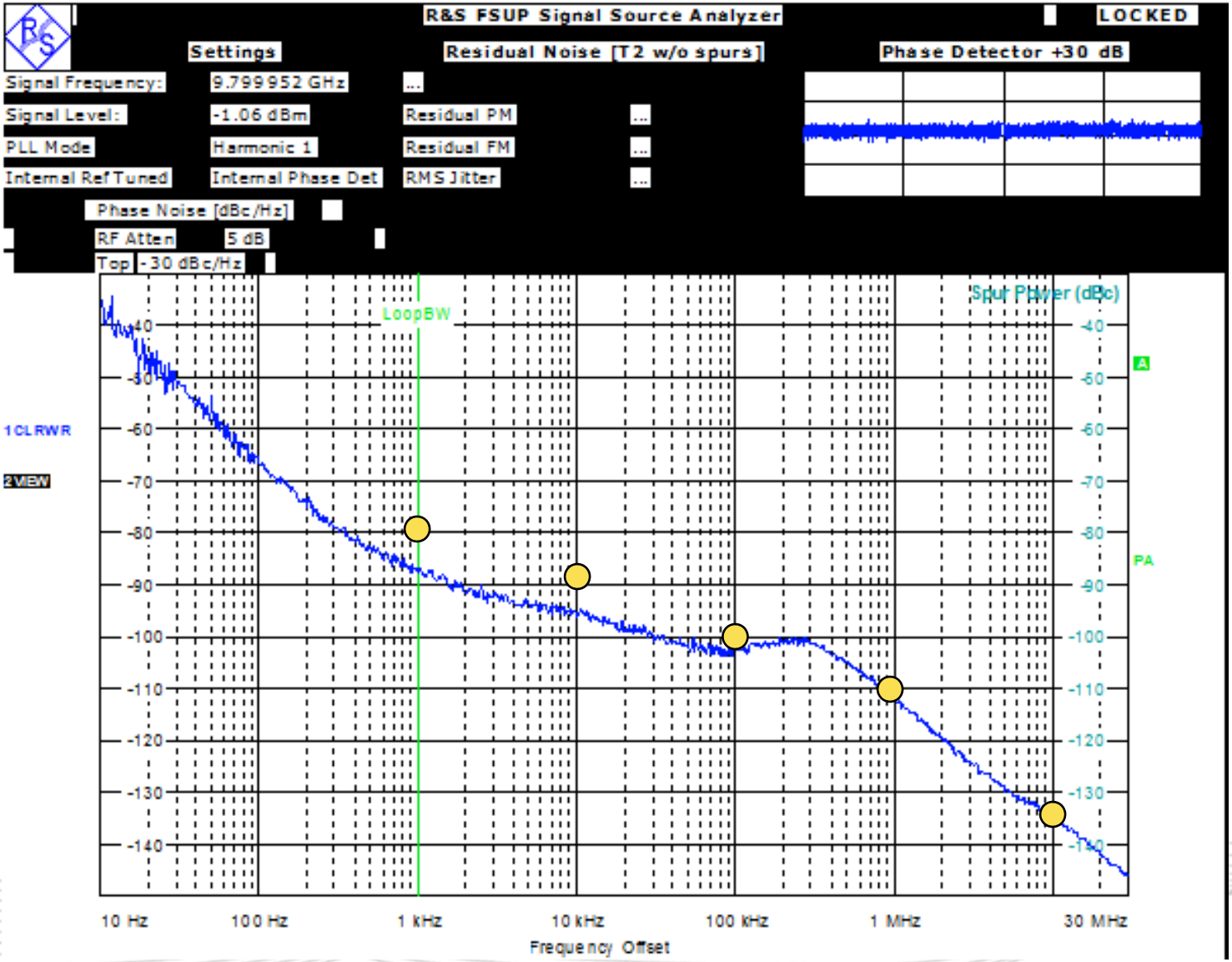
→ 250 MHz-24 GHz PLL

→ Integrated 17…20 GHz or 8…12 GHz VCO

→ Fractional-N



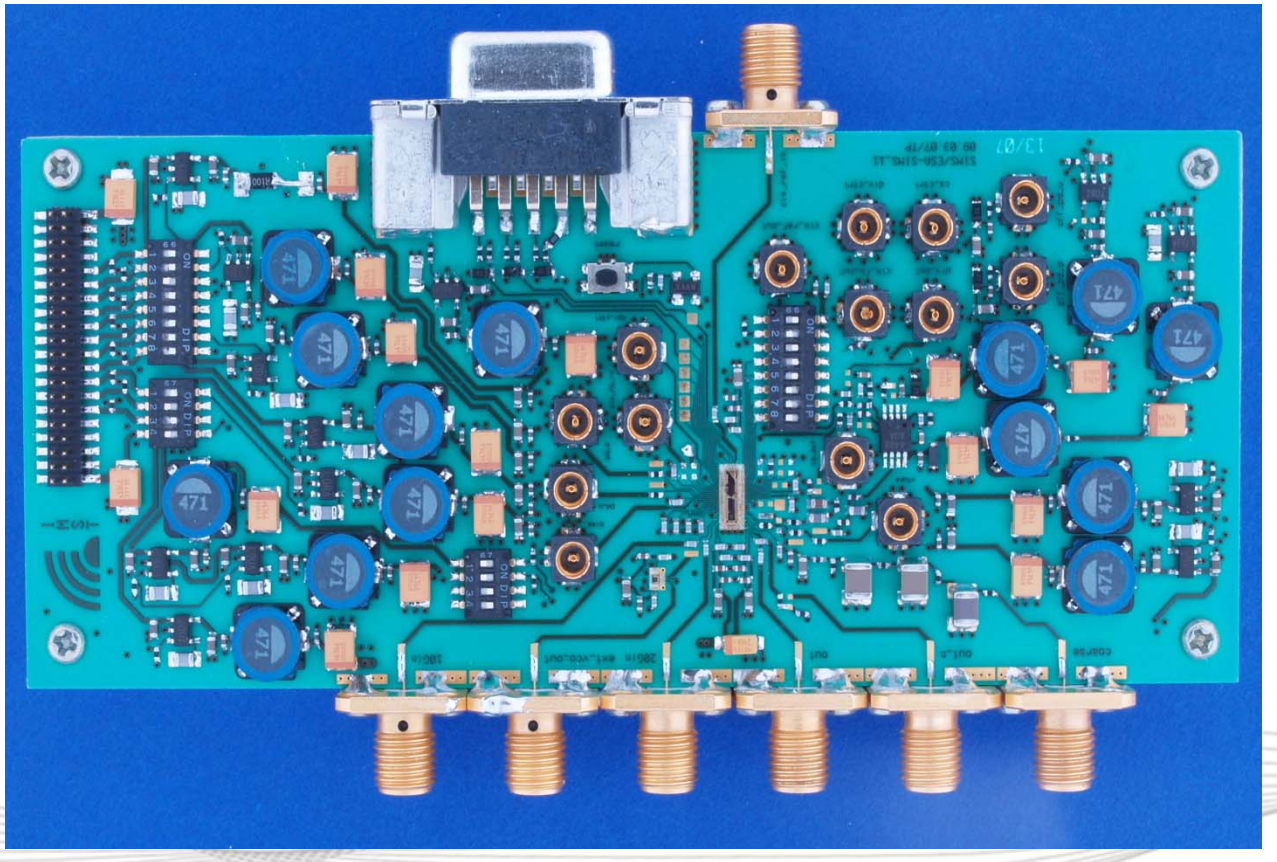
Measurement results



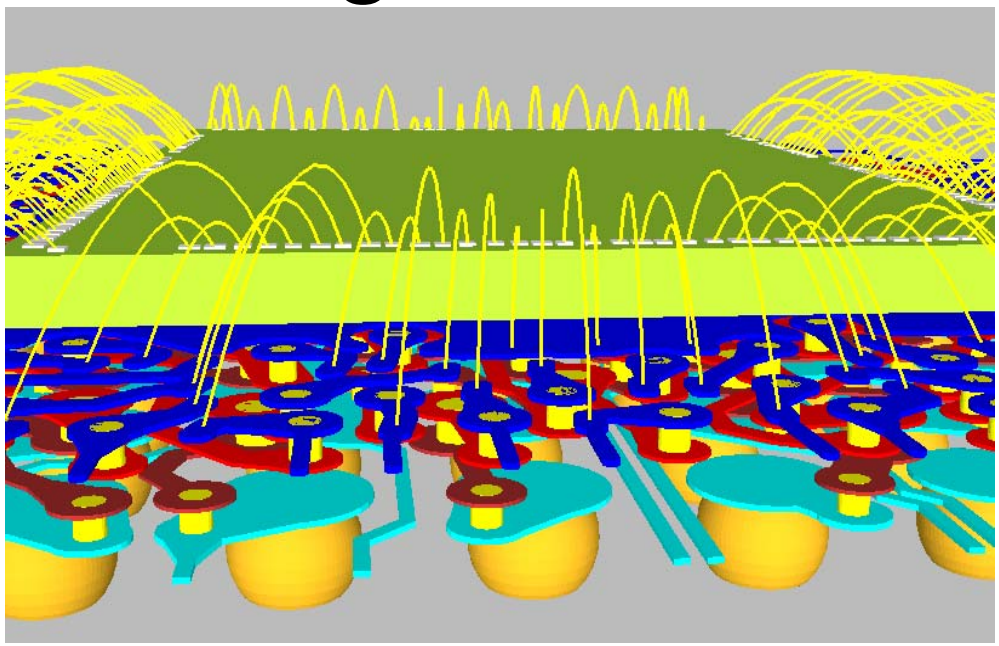
Synthesizer application test board

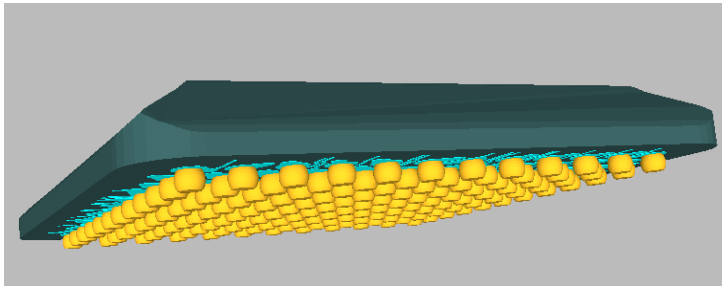
→PC interface

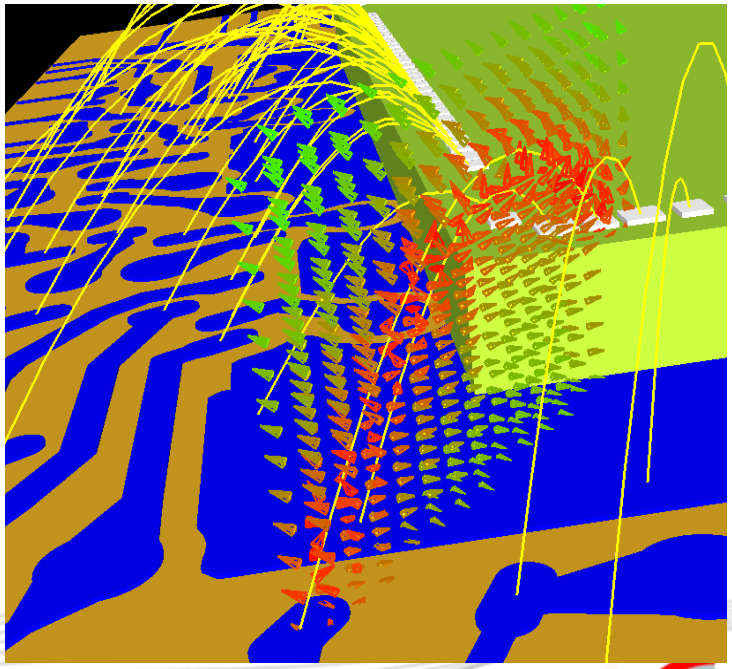
→Many test ports



Packages







→ BGA simulation

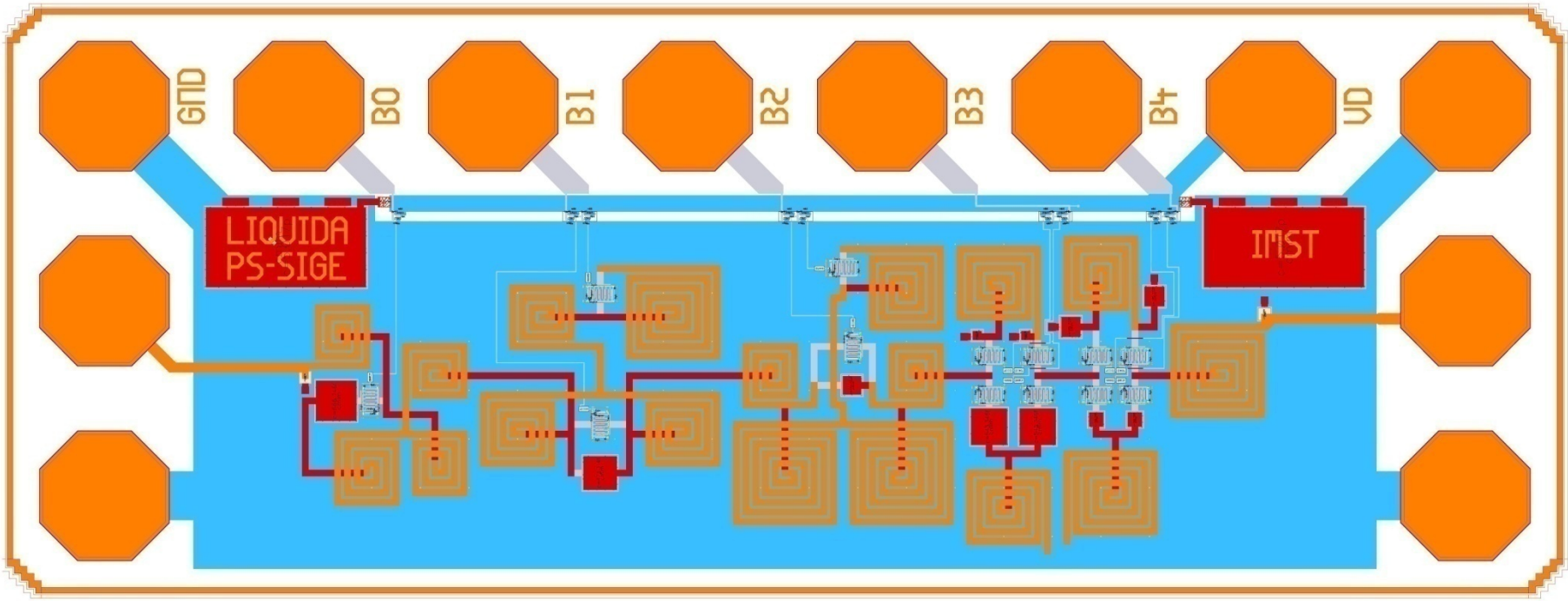
→ Equivalent circuits

→ S-parameter files

→ Magnetic field

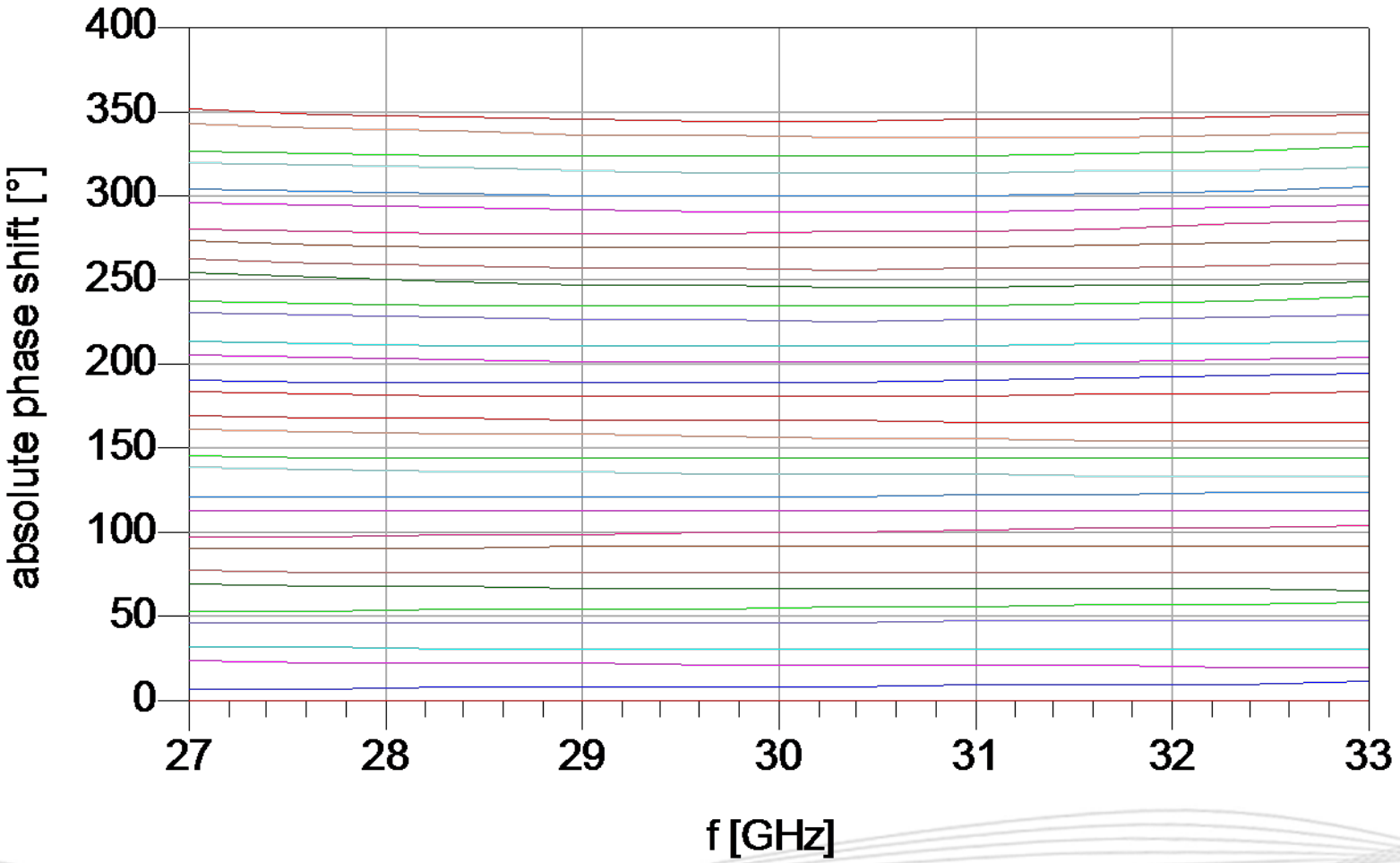
World smallest phase shifter (ka)

Size 960 x 360 µm², Core 620 x 210 µm²



V_D = 3 V, $V_{C\ (B0\text{-}B4)}$ = 0 V / 3 V (active / not active)

Phase diagram



Any questions?