

# IEEE Region 6 Awards 2011-2012 NOMINATION FORM

(for Area Awards, and also for Region 6 Awards)

(This Nomination form is to be used by Sections for Area Award Nominations for all categories. This form is also to be used by Sections-via-Areas for Region 6 Award Nominations. Please use one form per Nomination.)

Area →  Central,  NE,  NW,  Southern,  SW

## Award Category of the Nomination:

- Outstanding Engineer Award
- Outstanding Leadership and Professional Service Award
- Outstanding Section Award
- Outstanding Corporate Service to Engineering Community Award
- Outstanding Student Branch Award
- Director's Special Award / Area Chair's Special Award

Name (Individual/Section/Student-Branch/Company): Perry Lea

Address: Hewlett-Packard, 11311 Chinden Blvd, Boise, ID 83714

Phone: 208-396-6532 e-Mail: perry.lea@hp.com

Occupation: Firmware Engineer

Title/Position: Distinguished Technologist

IEEE Grade: Senior Member Date of Grade: 5/11/2002

Company: Type of Business, # of employees, etc. \_\_\_\_\_

Proposed Citation:

For innovative work and outstanding technical leadership in imaging and printing systems and digital system architectures.

**Supporting information to be attached, as appropriate and applicable:**

- (a) Engineering Career (Brief Summary), (b) Education, (c) Research/inventions, (d) Contributions to engineering literature, (e) Contributions to IEEE activities, (f) Contributions to the community
- Outstanding accomplishments of the Section
- (a) Company contributions to engineering, (b) Company support of IEEE activities, (c) Company contributions to the community (monetary and other relevant contributions)
- Outstanding accomplishments of the Student Branch
- Region 6 Director's Special Award / Area Chair's Special Award

### **(a) Engineering Career (Brief Summary)**

In Perry's role as hardware/firmware architect at HP, he has developed many important technical concepts and patents resulting in faster imaging, higher quality, lower power, at lower costs for HP LaserJet, Page Wide Array, and Digital Sender products. Concurrent with his engineering work at HP, he has recently completed his dissertation research with Columbia University. This research advances the technology of heterogeneous multicore systems on a chip (SOCs) with the development of new techniques to control energy dispersion in multicore processors.

2011 HP – Imaging and Printing Group

#### **Distinguished Technologist**

- Senior technical advisor to functional staff and director of engineering.
- Recognized HP leader of imaging systems and future technologies.
- Charter new ASIC designs, imaging pipelines, firmware architectures, and value driven features.
- Interactions with HP Labs and global HP business units on areas of ASIC design, processor architectures, imaging systems, and nanoscale synthesis techniques.

2003 – 2011 HP - Core Technology Laboratories / Embedded System Laboratory

#### **Master Architect of Technical Staff**

- Principal hardware/firmware architect for core imaging lab. Responsible for future imaging architectures including parallel arrays, ink, dry electro-photographic systems, and optical scanning systems.

- Lead a team of 38 scientists and engineers in involved in imaging, IO, mass storage, user interfaces, real time operating systems, power management, and ASIC design.
- Architected, developed, and deployed novel technologies around the areas of computation geometry, high performance imaging, co-development, power management, embedded multi-core communications, SIMD vector acceleration, and memory management for embedded devices.

2000 - 2003 HP - Core Technology Laboratories

### **Engineering Scientist**

- Acted as technical lead and architect for first parallel inline color systems.
- Led a team of six engineers in the delivery of initial board turn-on, new ASIC verification, schedules, requirements, and processor turn-on. Performed planning of tasks and work assignments for engineering staff. Prepared processes to ensure rapid and timely integration and product delivery.
- Responsible for LaserJet 4600, 5500, and 9500 product stewardship and market delivery from original design to release to manufacturing.

1995 - 2000 HP – LaserJet Systems Group

### **Firmware Design Engineer**

- Designed a system wide model of the LaserJet imaging system resulting in a tool used for discrete event simulations that allowed our organization to understand imaging bottlenecks, predict future performance requirements, and explore new architectural concepts.
- Consultant on the LaserJet imaging performance path. Performed investigations in compression technology, parallel algorithms, processor investigations, memory throughput, processor analysis, and compiler efficiency.
- Primary lead for the EPFL university research program. Owner of the EPFL development plans and lifecycles. The results were successful completion of three projects: DSP/MMX incorporation into the HP graphics engine layer, compiler improvements outside of assembly for MIPS processors, and display list redundancy cleanup.
- Coordinated research work with HP Labs in Palo Alto and Bristol.

1995 HP - Boise Printer Research

### **Software Engineer**

- Worked with a small team responsible for the delivery of the LaserJet 4j driver.
- Developed the bi-directional parallel IO with Windows 3.1 and proprietary NEC hardware.

- Represented HP to the Chinese Academy of Science for their contract work with HP drivers.

## **Education**

- BS Computer Science, 1994 University of Wisconsin, Milwaukee. Minor Physics
- MS Computer Engineering, 2001 National Technological University
- Engineer's Degree of Electrical Engineering, 2009 Columbia University

## **(b) Research/inventions**

### Patents

- US#6,977,737 - System and method for controlling print performance
- US#7,729,548 - A system for high bandwidth imaging across PC chipsets and custom ASICS
- US#7,929,160 - Page processing and print engine management

### Pending Patents

- 20050063008 - System and method for processing image data
- 20040169885 - Memory management

### Trade Secrets

- Trade Secret technologies recognized by Hewlett Packard in the areas of cache line manipulation, imaging dataflows, and high performance imaging.

## **(d) Contributions to engineering literature**

- Eng D. Dissertation Heterogeneous Multi-core Systems on a Chip, Columbia University, 2009
- Purposeful Multiprocessor Partitioning, IEEE Region 6 Lecture Series, 2006
- Methods of Stochastic Performance Analysis, IEEE Region 6 Lecture Series, 2002
- A Case Study of Modeling and Simulation in HP LaserJets, HP Embedded Conference 1999
- Cache Packing: A Method of Optimal Link Order for Performance and Determinism in Embedded Real Time Systems, HP Embedded Conference 1999

**(e) Contributions to IEEE activities**

- IEEE and IEEE Computer Society member for 19 years; Senior Member since 2002
- Founding member of IEEE Boise Computer Society
- Past officer and Chair of Boise IEEE Computer Society

**(f) Contributions to the community**

- Founder, original chair of University Wisconsin, Milwaukee ACM Student chapter.
- Active member and recruiter for Association of Computing Machinery for 17 years.
- Intern mentor for 5 years with students from Stanford University and Utah State.
- Recruiter for Hewlett Packard at University of Wisconsin and Columbia University.
- Volunteer with Idaho Association for the Blind, Idaho Shakespeare Festival and Idaho Bells for Books literacy program.

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<u>Boise Section</u> Section Name	<u>Chris Gunning</u> Name of Nominator (Section Awards Chair or Section Chair)
<u>/Chris Gunning/</u> Signature of Nominator (Section Awards Chair or Section Chair)	<u>Section Chair</u> Title of Signer/Nominator
<u>208-484-3564 / cgunning@ieee.org</u> Phone / e-Mail	<u>April 30, 2011</u> Date
<hr/> Signature of Area Awards Chair or Area Chair (for Region Awards)	<hr/> Date

*Note: This nomination form with attached summary and description of service and accomplishments must be submitted by the Section Chair to the respective Area Awards and Advancement Chair, by April 30, 2008. Nominations received after this deadline may not be considered for awards.*