CMOS parametric circuits – an alternative on CMOS towards Gbps communication

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Abstract

With the advent of the era of high-data rate (above Gbps) communication, one of promising ways to increase the data rate is to utilize wider bandwidths, which are more readily attainable in the mmWave frequency range (from 30 to 300 GHz). In the meantime, to reduce dimensions of the hand-held devices and minimize energy loss in the interfaces between radio frequency front-end and data processing units, researchers attempt the integration of the digital and analog circuitry onto a single chip, forming a so-called system-on-chip (SoC).

CMOS is the most successful and widely used IC technology for digital applications. Therefore, CMOS analog circuitry design has drawn massive attention of researchers working on deploying the concept of SoC. However, due to the limitation of the CMOS MOFET operating frequencies, the performance (such as gain, noise figure, etc…) of the CMOS analog circuitry is not always adequate at mmWave frequencies. Thus we ponder whether the analog circuitry design on CMOS be replaced with other semiconductor process or are there other techniques that will keep analog circuitry alive on CMOS?

Parametric circuits utilize time-varying reactance devices (such as diode, varactor, etc…) to amplify and mix the signals. They originate in 1920s' at the times when the MOSFET and integrated circuit (IC) technology have not been invented yet. The early research conducted at Lincoln Laboratory, MIT, for Radar system development during WWII and afterwards in 1960s' the intensive researches on discrete-element parametric circuits had been prosperous. The advantages of the parametric circuit include the high operating frequencies, low noise, and large achievable power gain. These advantages make parametric circuits as alternatives to MOSFETs for high-data-rate applications, especially on IC technology. For a CMOS technology with the cut-off frequency of MOSFETs reaching 100 GHz, for the time-varying device, such as accumulation-mode MOS varactor (AMOSV), belonging to the same technology are capable of operating at frequencies as high as several hundreds of giga-hertz. The minimum noise figure can be as low as 2 dB at 100 GHz.

In the tutorial, the CMOS parametric circuit designs based on AMOSV will be introduced. The large- and small-signal models as well as the conversion matrix of AMOSV will be derived in details. Example designs of parametric amplifier, mixer, and frequency multiplier will be also covered in the tutorial.

Keywords – High-data-rate communications, Gbps communication, RFIC, Parametric circuit, AMOSV, CMOS

Planned duration of the tutorial: 2 hours

Biography

Zhixing Zhao is currently towards his Ph.D. degree at University of Calgary. He obtained his B.Eng in Jilin University, China and M.Sc. in University of Calgary, Canada. His research interests are on radio-frequency integrated circuit design, especially on wireless high-data rate front-end design on CMOS.

Sebastian Magierowski obtained his Ph.D. in Electrical Engineering from the University of Toronto in 2004. He was a faculty member in the Department of Electrical and Computer Engineering at the University of Calgary before joining York University in 2013. His research interests center on the implementation of analog and digital integrated circuits (ICs) for high-speed communications and low-power computation. In particular he has worked on millimeter-wave CMOS RFICs for wireless, integrated microwave ICs for wireless LANs and sensor networks, wire-line signal monitoring ICs, and custom CMOS cores for mobile robot path planning.

Leonid Belostotski (S'97–M'01) received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Alberta, Edmonton, AB, Canada, in 1997 and 2000, respectively, and the Ph.D. degree from the University of Calgary, Calgary, AB, Canada, in 2007. A large portion of his M.Sc. thesis program was spent with the Dominion Radio Astrophysical Observatory, National Research Council (NRC), Penticton, BC, Canada, where he designed and prototyped a distance measurement and phase synchronization system for the Canadian Large Adaptive Reflector telescope. Following his graduation, he was with Murandi Communications, Ltd., as an RF Engineer, during which time he designed devices for high-volume consumer applications and low-volume high-performance devices for the James Clerk Maxwell Telescope, Mauna Kea, HI, USA. He is currently an Associate Professor with the University of Calgary, the Director of the Micro/Nano Technologies (MiNT) Laboratory, University of Calgary, and the President of his own engineering consulting firm. His research interests include RF and mixed-signal ICs, high-sensitivity receiver systems and antenna arrays, and terahertz systems. Dr. Belostotski was the recipient of the IEEE Microwave Theory and Techniques 2008MTT-11 Contest on "Creativity and Originality in Microwave Measurements" and the Analog Devices, Inc. Outstanding Student Designer Award in 2007.