Chameleon: A Dual-Mode Bluetooth/WiFi Receiver Design


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Outline

• Previous work: Bluetooth Receiver in CMOS 0.35µm

• System Level Design
  – Technology features
  – Main Bluetooth and Wi-Fi specs
  – Previously reported architectures
  – Proposed dual-mode architecture
  – Impact of non-idealities on the BER performance

• Building Blocks
  – LNA
  – Mixer
  – VCO and PLL
  – VGA
  – ADC

• Experimental Results
0.35μm CMOS Bluetooth Low-IF Receiver IC

Developed during 2001 and 2002 at the AMSC.

Authors: Wenjun Sheng, Bo Xia, Ahmed Emira, Chunyu Xin, Ari Ari Valero-Lopez, Sung Tae Moon and Edgar Sanchez-Sinencio.
0.35\(\mu\)m CMOS Bluetooth Low-IF Receiver IC

- Publications:
  - 2002 RFIC Conference, Best Student Paper Award (third place).
  - Journal of Solid-State Circuits: January 2003 (Receiver) and August 2003 (Demodulator).
  - Transactions on Circuits and Systems – II: November 2003 (Complex Filter).
## Chameleon Receiver: Timeline

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<th>Phase</th>
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<td>Baseband BER simulations</td>
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Chameleon Receiver

- Previous work: Bluetooth Receiver in CMOS 0.35µm

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- Experimental Results
Technology features

- IBM SiGe BiCMOS 6HP 0.25um
- Transit frequency ($f_T$) 47GHz
- 6 aluminum metal layers
- Analog metal (4um thick, 0.00725 $\Omega/\square$)
- Varactor diode (intrinsic base-collector diode)
- Metal to metal cap (1.4fF/um$^2$)
- MOS cap ($3.1 \pm 15\%$fF/um$^2$)
- Poly resistors ($210 \pm 20\%, 3600 \pm 25\%$)
Standards Overview

<table>
<thead>
<tr>
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<th>Bluetooth</th>
<th>802.11b</th>
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<tr>
<td>Data rate</td>
<td>1Mb/s</td>
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<td>Power</td>
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<td>DSSS-CCK</td>
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Dual-Mode Receiver Architecture

- 3 possible alternatives for Bluetooth and Wi-Fi dual mode architectures:

- **Low-IF and DCR**
  - Best fit for each standard 😊
  - Sharing ↓ 😞

- **Low-IF and Low-IF**
  - Power ↑ 😞 😞
  - Sharing ↓ 😞

- **DCR and DCR**
  - Area and power ↓ 😊
  - Sharing ↑ 😊
  - DC offset & 1/f noise ↑ 😞
Previously Reported Dual-Mode Receivers

- DCR for WiFi, low-IF for Bluetooth.
- Shared RF front-end.
- Separate baseband circuits

Previously Reported Dual-Mode Receivers

- Double downconversion to avoid LO self mixing and injection locking between PA and VCO.
- DCR for Wi-Fi and low-IF for Bluetooth.
- Shared RF and programmable dual-mode baseband.

Proposed Dual-Mode Architecture

Direct-conversion BT/WiFi receiver architecture
Remarks

• Direct-conversion architecture is used for both standards to save power and avoid the image problem in IF architectures.
• LNA & Mixer are shared between BT and Wi-Fi.
• Gm-C LPF with programmable bandwidth is used to accommodate both standards.
• Parallel Pipeline ADC architecture is used:
  – BT: sampling rate = 11MHz, 11bits
  – Wi-Fi: sampling rate 44MHz, 8bits
• Due to the short allowed settling time, the VGA has only two gain steps in BT mode and the signal level at the ADC input will vary by 24dB.
• In Wi-Fi mode, gain steps of 2dB are employed.
Impact of DC offset and DC offset correction on the BER performance (Wi-Fi mode)

A: 0 offset. B: 5% offset, C: 10% offset, D: 15% offset E: offset cancelled with 4 HP poles at 5KHz, F: offset cancelled with 4 HP poles at 10KHz.
Wi-Fi Interferer Rejection Requirements

• In the presence of a modulated interferer at 25MHz with a power 35dB above the signal of interest, the receiver should show 1E-5 BER for an SNR 6dB above the minimum sensitivity.

• The channel selection filter should reject a strong interferer while not affecting the spectrum of interest.
Impact of the channel selection filter characteristics on the BER performance (Wi-Fi mode)

- 5th order Butterworth filter with $f_C=5.5$MHz with (B) and without an interferer (A).
- 4th Chebyshev filter with $f_C=6$MHz with (D) and without an interferer (C).
Impact of the mismatch between I and Q channels on the BER performance (Wi-Fi mode)

- A: Receiver performance including channel selection filter and DC offset correction.
- B: Performance with a $10^6$ error in the generation of I and Q signals.
- C: Performance with 1.5dB gain mismatch between I and Q channels in addition to the phase error.
Adjacent Channel Test

Adjacent channel test in Bluetooth mode

- Signal level
- Interferer level

Signal level in dBm

LNA  Mixer  Filter  VGA  ADC
NF, IIP3, and IIP2 contributions

Noise contributions of different blocks

IIP2 contributions of different blocks

IIP3 contributions of different blocks

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Power consumption and area contributions
Chameleon Receiver

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• Experimental Results
Low Noise Amplifier

- Gain = 15/-15dB
- NMOS drive is used for better linearity.
- $C_m$ ensures matching in low-gain mode.
I/Q Downconversion Mixer

- I & Q share the same RF drive stage
- NMOS drive for better linearity
- NPN switch to reduce LO drive and 1/f noise
Frequency Synthesizer

- VCO running at $2f_0$
- I/Q generation using divide-by-2 flip flop.
- Capacitor multiplier to integrate loop filter cap.

![Diagram of Frequency Synthesizer](image-url)
Phase Switching Prescaler

- Phase switching prescaler for reduced power consumption compared with traditional architectures.
- No feedback in flip-flops.
Charge Pump

Cascode current mirrors minimize the current mismatch in Up and Dwn operation.
Capacitance Multiplier

\[ z_{in} = \frac{z_0}{M + 1} \]

Total Current: 150 μA
VCO

- LC tuned negative-g_m VCO
- Analog metal inductor
- Varactor diode
- DC-decoupling for driver base to improve linearity and noise
- Bypass capacitor improves phase noise 2dB
- L=1.5nH, Q=13
Channel Selection Filter

- 5th order Butterworth OTA-C filter.
- Passive 1st pole is used to relax the biquad (OTA) linearity requirements.
- Programmable bandwidth through switching R&C.

![Diagram of Channel Selection Filter](image)
Biquadratic Section

\[ \omega_0 = \frac{g_{m1}}{C} \quad Q = \frac{g_{m1}}{g_{m2}} \quad V_{DC} = 1.6V \]

Direct connection between consecutive OTAs in the filter is exploited in the implementation of the CMFB circuit.
Dual-mode OTA

- Source degeneration
- Current scaling
  \( I_{bias} \times R = \text{constant} \)
- The standard is chosen by switching \( R \) (coarse tuning)
- Fine frequency tuning using bank of capacitors \( C \)
Variable Gain Amplifier

- 0-62dB gain, 2dB steps in Wi-Fi
- 0/24dB (one stage) gain in Bluetooth
- RC HPFs used to reject dc offset
- VGA stage with constant output offset
Constant output offset VGA

- The gain is controlled by $d$:
  \[ Gain = \frac{G_{11} + dG_{12}}{G_2} \]

- The output offset is independent of $d$.
  \[ output \ offset = \frac{G_{11} + G_{12}}{G_2} V_{os} \]

- This assumes that the offset in $Vi$ is completely removed by the RC HPF.

- **Problem**: $G_{11}$ and $G_{12}$ will load the HPF $\Rightarrow$ we have to use a buffer at each input resistor
Constant output offset VGA, Cont’d

- A buffer is used to drive each input resistor.
- The feedback factor is independent of the gain. This makes the OpAmp design easier.
- Bandwidth and phase margin are independent of the gain.
- Note that the capacitor C does not load the previous stage since it is in series.
- However, the parasitic capacitance of the top and bottom plates to ground will load the previous stage!
Time-Interleaved Pipeline ADC

- Programmable resolution and sampling rate.
- On line digital calibration.
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• Experimental Results
Receiver Die Photo

Deep Trench Isolation

Frequency Synthesizer
RF Front End
Baseband Filter
VGA
ADC
Testing Board
Receiver Sensitivity

Bluetooth = -91dBm  Wi-Fi (11Mb/s) = -86.5dBm
Receiver Linearity

Both BT / Wi-Fi modes

\[ IIP2 = 10\text{dBm} \quad IIP3 = -13\text{dBm} \]
LO Phase Noise

-124 dBc/Hz @ 3MHz
LPF Programmability
SNR Measurement for ADC

**BT**

64.2 dB at 11MSample/s for the 550 kHz BT signal

**Wi-Fi**

59.7 dB at 44MSample/s for the 5.5 MHz 802.11b signal
### Comparison Table

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<th>[1]</th>
<th>[2]</th>
<th>This design</th>
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<td>BT</td>
<td>WiFi</td>
<td>BT</td>
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<tr>
<td><strong>Supply voltage</strong></td>
<td></td>
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<tr>
<td></td>
<td>2.5V</td>
<td>1.8V</td>
<td>2.7V</td>
</tr>
<tr>
<td><strong>ADC area (w/ pads)</strong></td>
<td>10mm²</td>
<td>10mm²</td>
<td>16mm² (transceiver)</td>
</tr>
<tr>
<td><strong>Rx area (w/ pads)</strong></td>
<td>N/A</td>
<td>16mm²</td>
<td></td>
</tr>
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<td><strong>ADC area (w/ pads)</strong></td>
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<td>-</td>
<td>-</td>
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<td><strong>Filter bandwidth</strong></td>
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<td>7.5MHz (LPF)</td>
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<td><strong>Sensitivity</strong></td>
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<tr>
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<td>20dBm</td>
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*Note: This design refers to the current design. The values for [1] and [2] are compared against the current design.*
Summary

• Direct conversion architecture for BT / Wi-Fi allows maximum level of block sharing
• Lower consumption than previous dual-mode implementations (27.9 mA / 30mA)
• Shared RF front-end and programmable baseband components
• Programmable channel selection filter with constant linearity
• AC coupled VGA with constant output offset
• On-chip time interleaved pipeline ADC