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**CURVATURE COMPENSATED  
BiCMOS BANDGAP WITH 1 V  
SUPPLY VOLTAGE**

**F. Maloberti**

***Texas A&M University***

**[franco@ee.tamu.edu](mailto:franco@ee.tamu.edu)**

# OUTLINE

- Introduction
- Bandgap references
- Low-Voltage Bandgap
- Operational Amplifier
- Startup Circuit
- Curvature Compensation
- Experimental Results
- Conclusions

# INTRODUCTION

- ❑ Voltage references generators with a minimum (or zero) variation with temperature are important element for precise electronics
- ❑ A voltage reference is normally based on a given ingredient; it can have a positive or a negative voltage coefficient
- ❑  $V_T$  has **positive** coefficient
- ❑  $V_{BE}$  has **negative** coefficient
- ❑ Properly combining  $V_T$  and  $V_{BE}$  it is possible to compensate the positive coefficient of one constituent with the negative coefficient of the other one
- ❑ The voltage achieved by a bandgap is typically **1.2 V**

- ❑ **Evolution of IC** → Submicron technologies (reduced oxide thickness) and low-power **low-voltage** applications
  - ➡ Reduced power supply voltages (1.8 V down to 1.2 V)
  - ✗ The threshold voltage of transistors scales less than the supply
  - ✌ New circuit techniques for the design of analog building blocks
- ❑ Bandgap voltage generator
  - ➡ Reference voltage → **1.2 V**
  - ✗ If the supply voltage is lower than 1.5 V → Conventional implementations of the bandgap reference circuit cannot be used
- ❑ Proposed bandgap reference circuit in standard BiCMOS technology
  - ✌ Output voltage → 0.65 V with 0.5 mV variation from 0° C to 80 ° C
  - ✌ Supply voltage → 1 V with 0.8 V MOS threshold voltages

# BANDGAP REFERENCES

- ❑ The band-gap operates on the principle of compensating the negative temperature coefficient of  $V_{BE}$  with the positive temperature coefficient of the thermal voltage  $V_T$ .
- ❑ The temperature coefficient of  $V_{BE}$ , at room temperature, is  $-2.2 \text{ mV}/^\circ\text{C}$ ; while, the positive coefficient of the thermal voltage is  $0.086 \text{ mV}/^\circ\text{C}$ .
- ❑ A full compensation at room temperature is obtained by combining the term with positive temperature coefficient and the one with negative temperature coefficient to give

$$V_{BG} = V_{BE} + nV_T = V_{BE} + n\frac{kT}{q}$$

where  $n$  must be equal to  $25.6 (=2.2/0.086)$ .

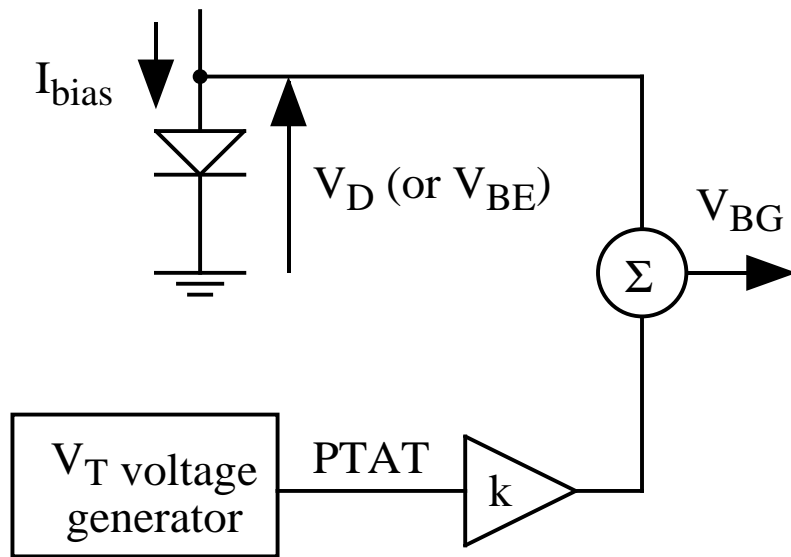
# WHY THE NAME: BANDGAP?

- Since the value of  $V_{BE}$  for low currents is close to  $0.650V$ , and  $V_T$  at room temperature is  $25.8\text{ mV}$ , the value of  $V_{BG}$  is  $1.26\text{ V}$ . Such a value is just slightly more than the silicon energy gap (expressed in volts it is  $1.21\text{ V}$ ). Therefore, we normally call the circuits that achieve temperature compensation *band-gap reference*.

NOTE: The name bandgap can be misleading: what is generated it is not a physical constant.

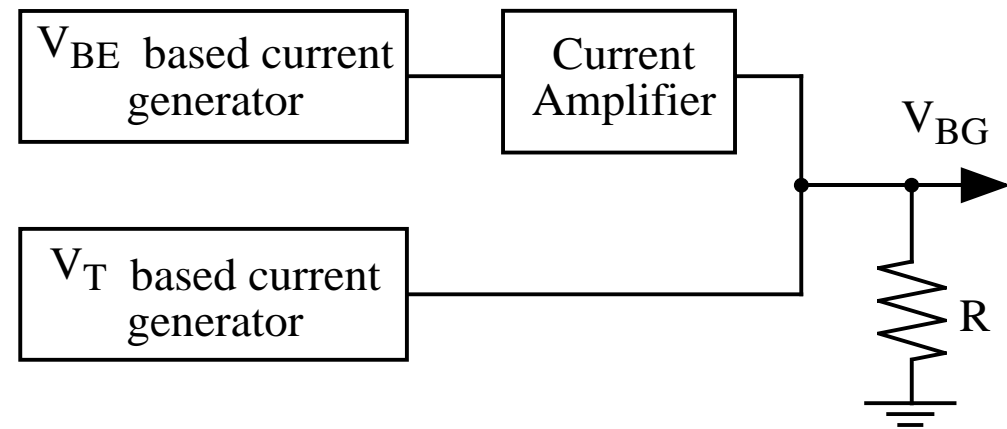
- ➡ Since  $V_T = kT/q$  is proportional to the absolute temperature, we often refer to it using the acronym *PTAT*.

# CONCEPTUAL IMPLEMENTATIONS



a)

a) Voltage mode approach

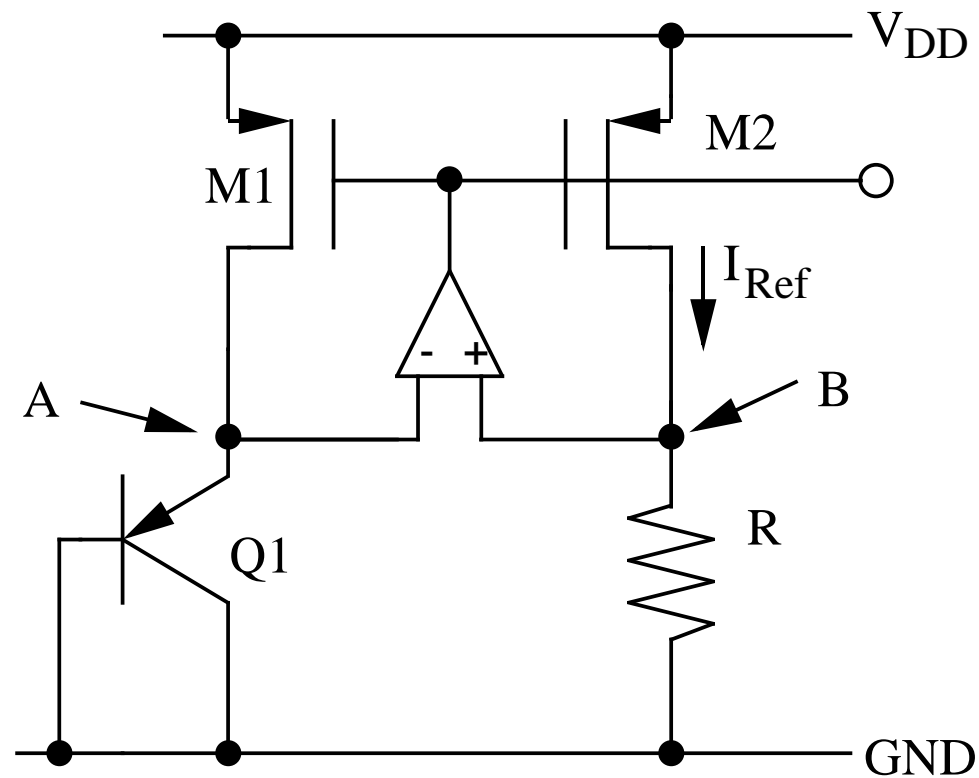


b)

b) Current mode approach

# BASIC INGREDIENTS

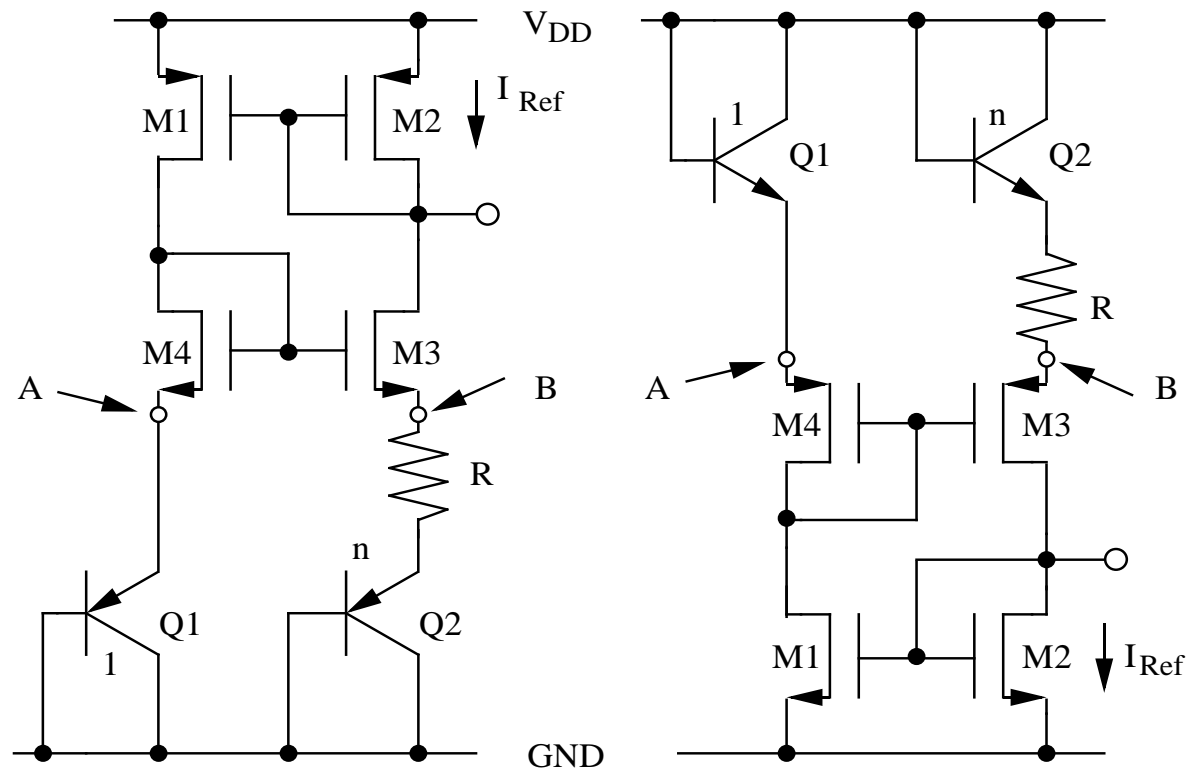
- $V_{BE}$  and  $V_{BE}$  based current generator



- Offset of the Op-amp can be a problem



## ❑ PTAT Current based generator

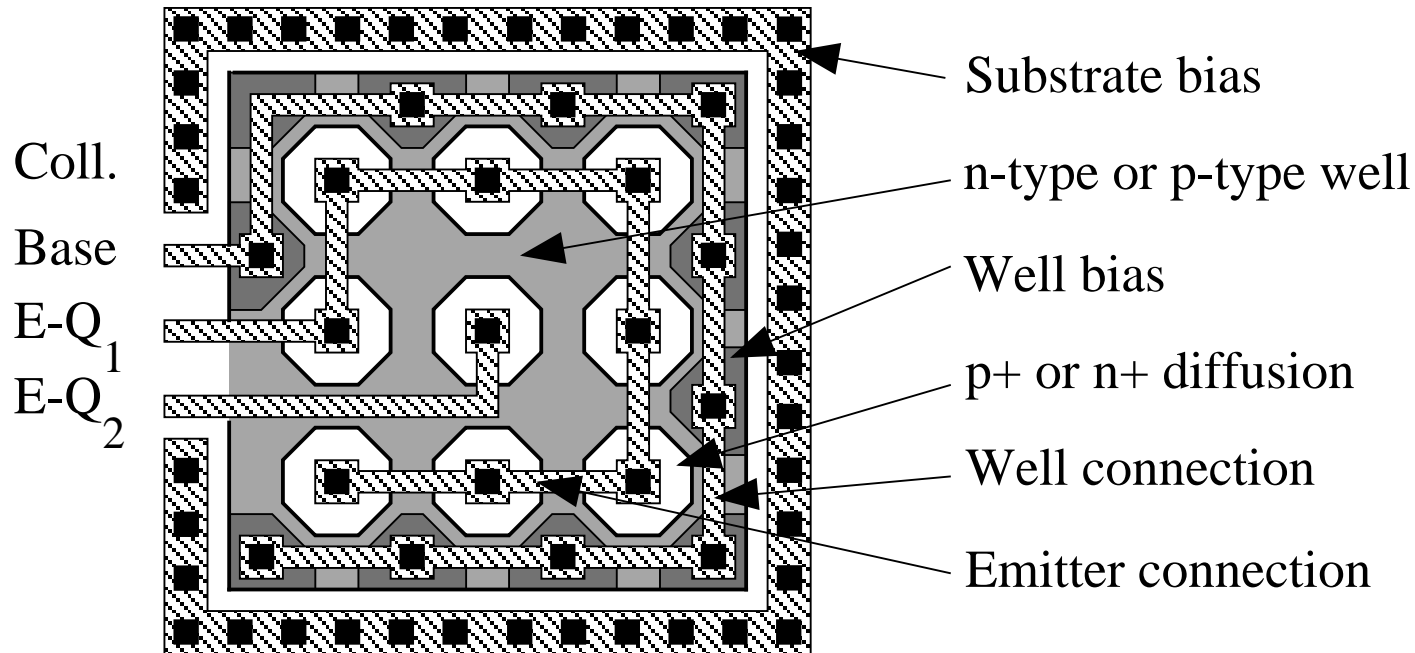


$$V_{BE1} = V_T \ln \frac{I_1}{A I_{SS}} ; V_{BE2} = V_T \ln \frac{I_1}{n A I_{SS}}$$

$$R I_1 = V_{BE1} - V_{BE2} = V_T \ln \frac{I_1}{A I_{SS}} \frac{n A I_{SS}}{I_1}$$

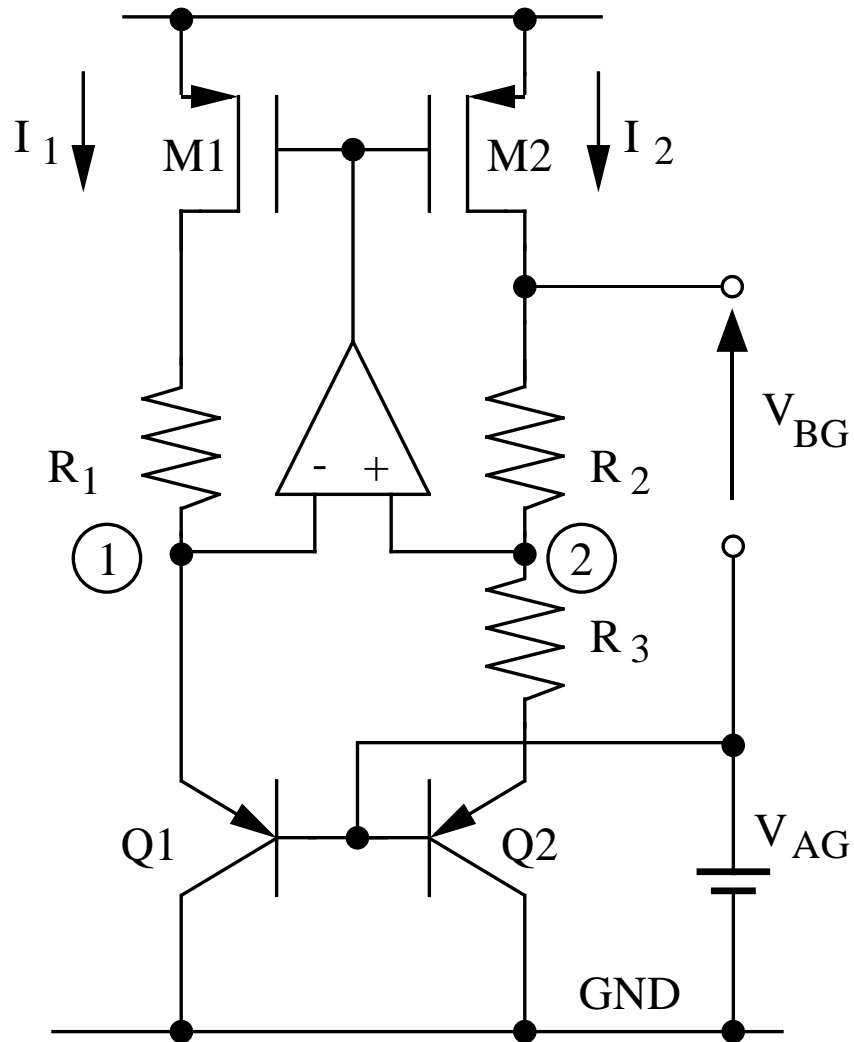
$$I_1 = \frac{V_T}{R} \ln(n)$$

# VALUE OF “N” AND LAYOUT



□ N= 8 or N=24 are good numbers for layout

# VOLTAGE MODE BANDGAP



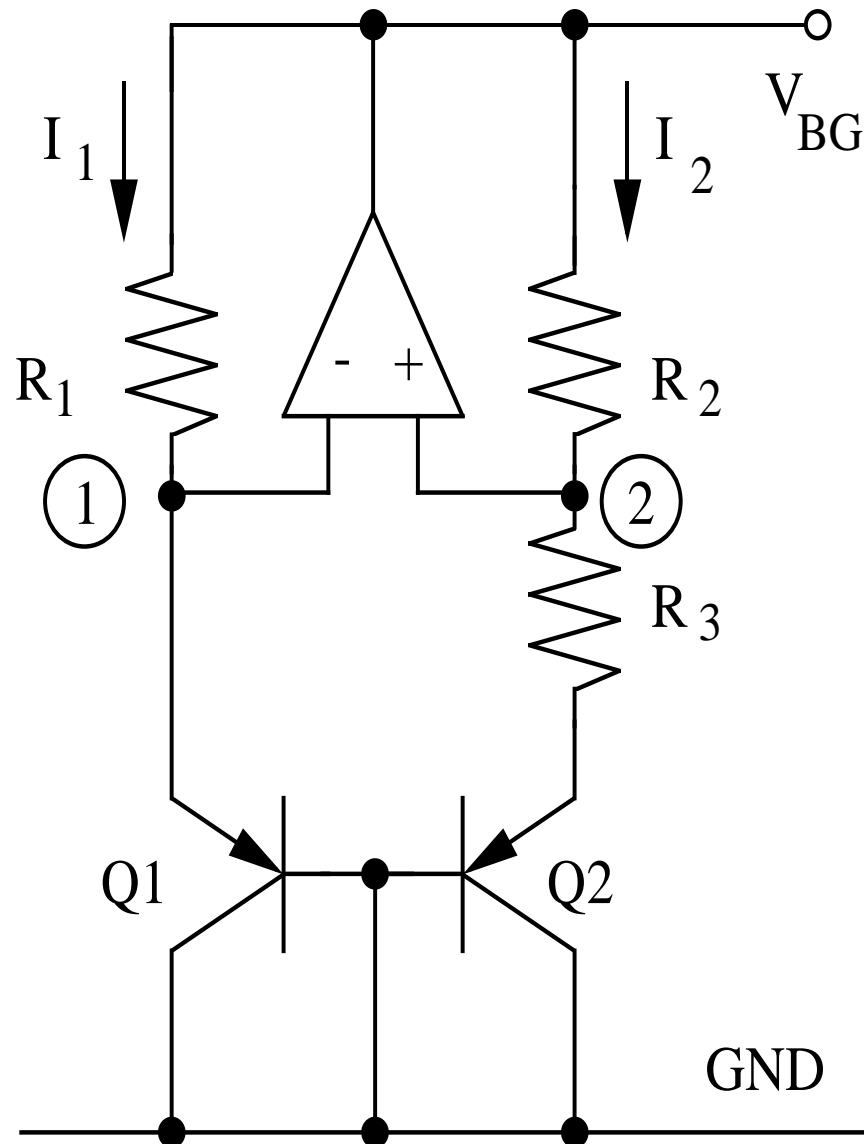
$$\frac{I_1}{I_2} = \left(\frac{W}{L}\right)_1 / \left(\frac{W}{L}\right)_2$$

$$V_{BG} = V_2 - V_{AG} + R_2 I_2 = V_{BE1} + \frac{R_2}{R_3} \Delta V_{BE}$$

$$V_{BG} = V_{BE1} + V_T \frac{R_2}{R_3} \ln \frac{(W/L)_1 A_2}{(W/L)_2 A_1}$$

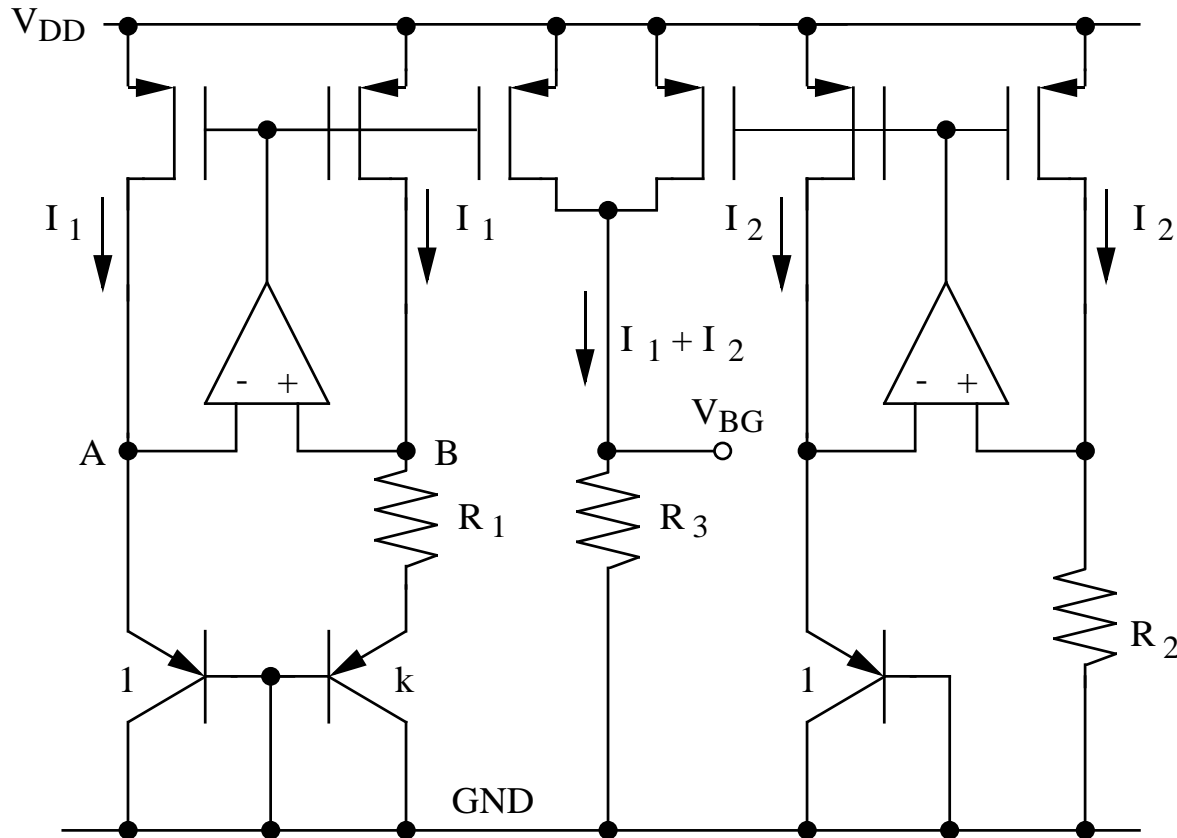
$$m = \frac{R_2}{R_1} \ln \frac{(W/L)_1 A_2}{(W/L)_2 A_1}$$

# ANOTHER VOLTAGE MODE SOLUTION



The matching of currents  $I_1$  and  $I_2$  depends on  $R_1$  and  $R_2$ .

# CURRENT MODE BANDGAP



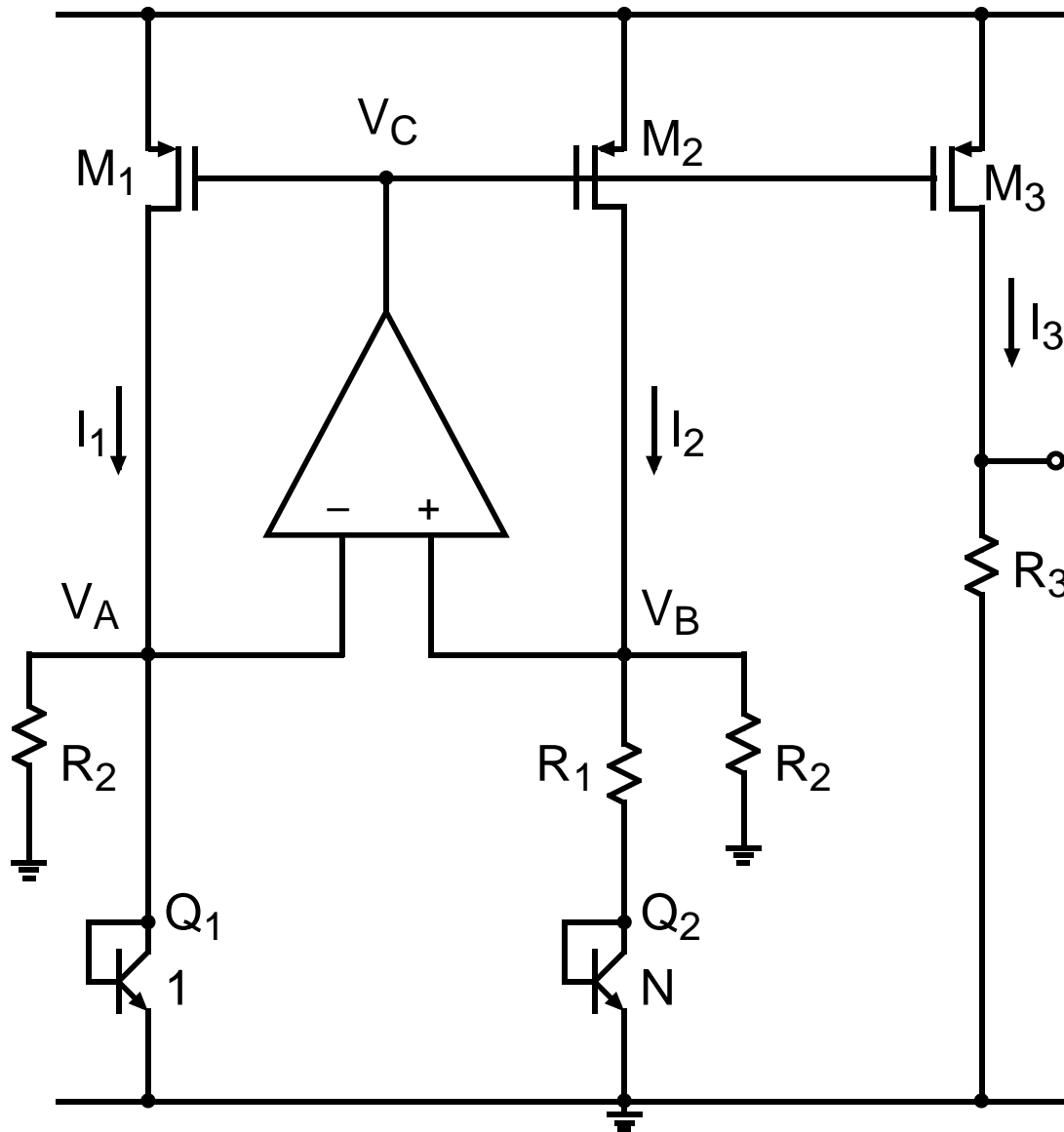
$$V_A = V_B = V_{BE}$$

$$I_1 = \frac{V_T \ln(N)}{R_1}$$

$$I_2 = \frac{V_{BE}}{R_2}$$

$$V_{BG} = \left( \frac{V_T \ln(N)}{R_1} + \frac{V_{BE}}{R_2} \right) \cdot R_3$$

# MERGING THE TWO BRANCHES



$$\begin{cases} V_A = V_B = V_{BE} \\ I_1 = I_2 = \frac{V_T \ln(N)}{R_1} + \frac{V_{BE}}{R_2} = I_3 \end{cases}$$

$$V_{ref} = V_T \left( \frac{R_3 \ln(N)}{R_1} \right) + V_{BE} \left( \frac{R_3}{R_2} \right)$$

$$n = \frac{R_2 \ln(N)}{R_1} = 25 \text{ and } \alpha = \frac{R_3}{R_2}$$

$V_{ref} \rightarrow$  Temperature independent

# LOW-VOLTAGE OP-AMP

✌ The described architecture is good for generating low voltage band-gap

BUT

we need a LOW-VOLTAGE Op-Amp

❑ Band gap minimum supply voltage is  $V_{DD} = V_{BE} + V_{sat, p}$

✌  $V_{DD} = 1\text{ V}$  is sufficient to operate the circuit

✗ The operational amplifier has to operate from  $V_{DD} = 1\text{ V}$

THEREFORE

❑ The operational amplifier is the most critical block

➡ Input common-mode voltage  $\rightarrow V_{BE} \cong 0.65\text{ V}$

➡ Output voltage  $\rightarrow V_{Cut} = V_{DD} - V_{th, p} - V_{sat, p} \cong 0.15\text{ V} \div 0.2\text{ V}$

# OP-AMP DESIGN CONSIDERATIONS

## ❑ Choice of architecture

- ➡ No speed limitations
- ➡ DC gain: around 60 dB
- ➡ Very low offset

## ❑ Constrains

- ✗ Input stage → No MOS input differential pair
- ✗ Output stage → No cascode structures

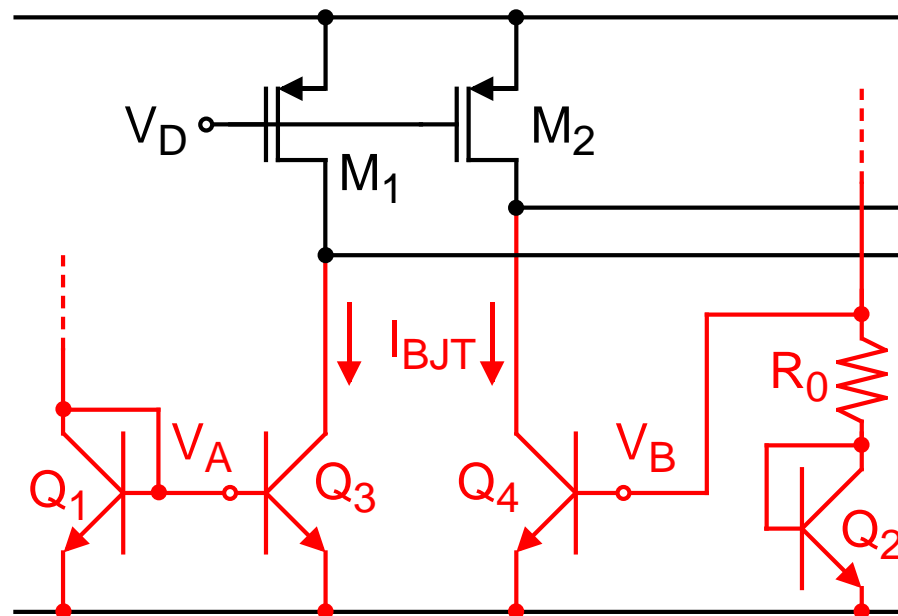
## ❑ Observations

- ➡ if  $V_{th} < 0.5 \text{ V}$  @  $V_{DD} = 1 \text{ V}$  → all MOS operational amplifier
- ➡ if  $V_{th} > 0.5 \text{ V}$  @  $V_{DD} = 1 \text{ V}$  → use bipolar transistors
- ➡ The input common mode voltage is  $V_{BE}$

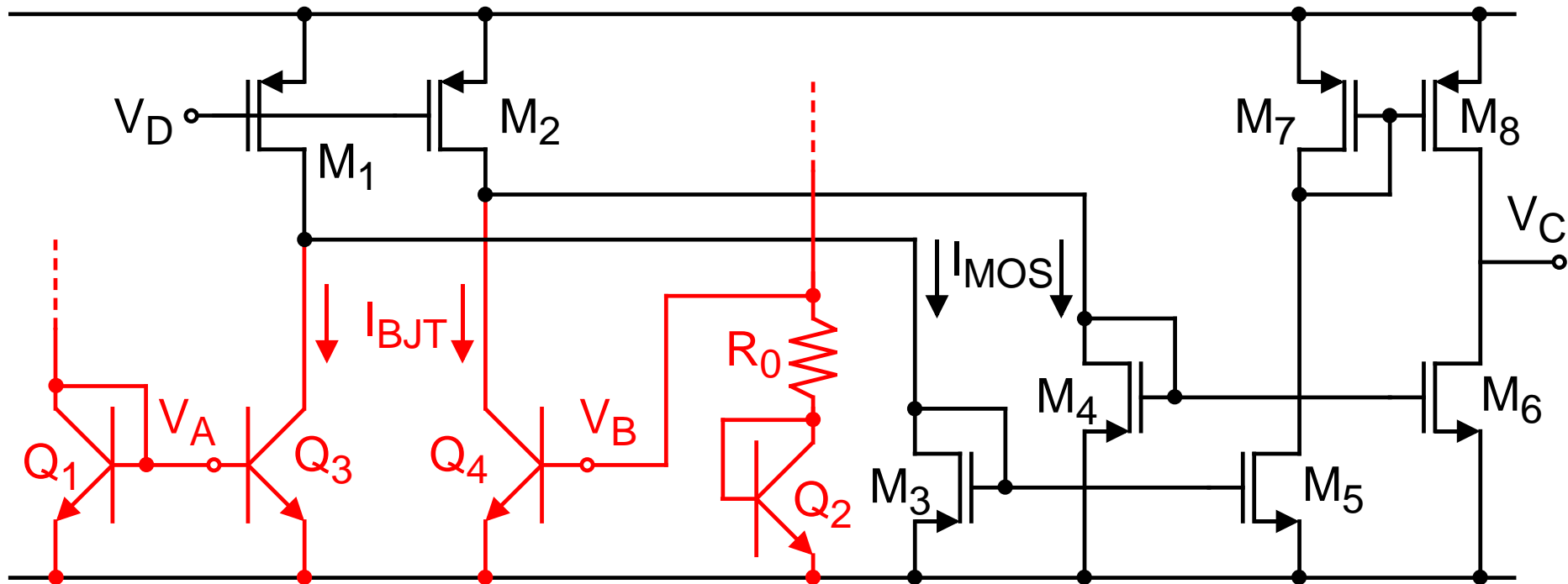


# TECHNOLOGY AND OP-AMP

- ❑ Since the threshold of CMOS is high, we had to use BiCMOS
- ❑ Why using an input differential pair?
  - ➡ to control the tail current
  - ➡ to reject a common mode input component
  - ✌ Those requirements are not essential in our circuit

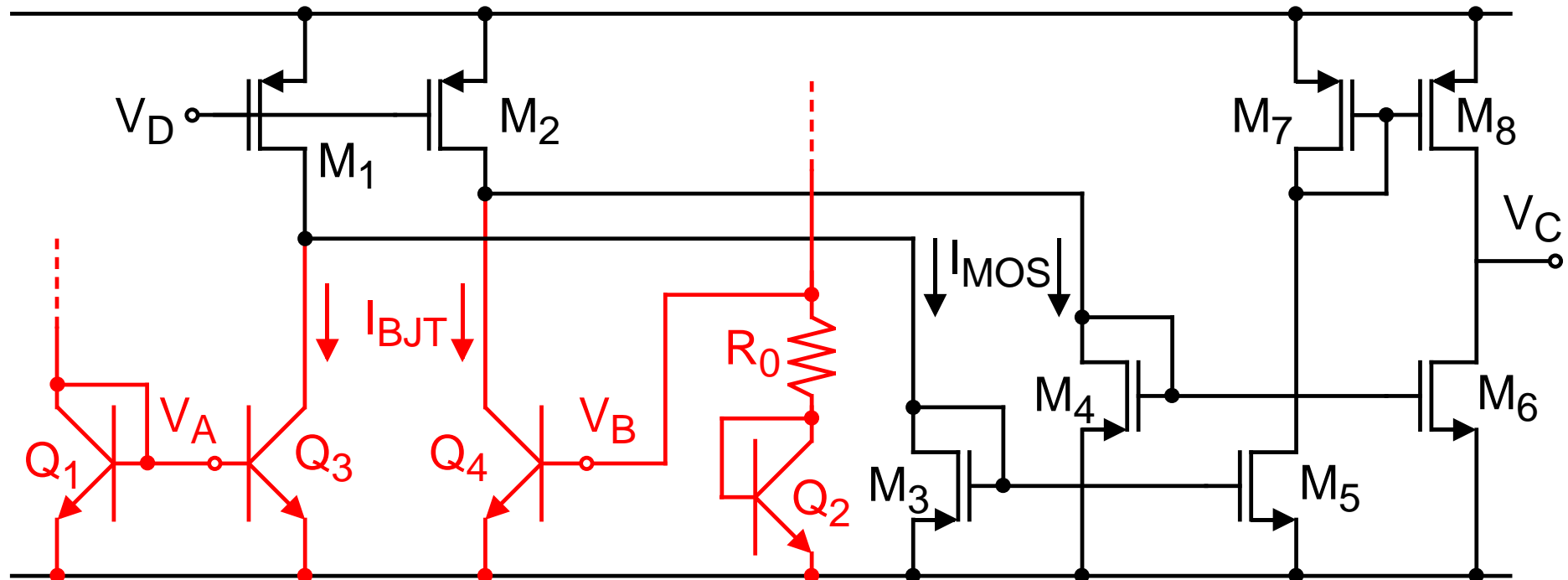


# OPERATIONAL AMPLIFIER



- ❑ Two-stages operational amplifier
- ❑ Input stage with grounded bipolar transistors
  - ✌ No current source required to provide the bias current
- ❑ Bias current  $\rightarrow V_A = V_B = V_{BE} \rightarrow I_{Q3} = I_{Q4} = I_{BJT} = V_T \ln(N)/R_0$

# OFFSET OF THE OP-AMP



- ❑ M3 and M4: matched conditions
- ❑ Output voltage  $\rightarrow V_{\text{Cut}} = V_{\text{DD}} - V_{\text{th}, p} - V_{\text{sat}, p} \cong 0.15 \text{ V} \div 0.2 \text{ V}$
- ❑ Drain of M7  $\rightarrow V_{\text{D7}} = V_{\text{DD}} - V_{\text{th}, p} - V_{\text{sat}, p} \cong 0.15 \text{ V} \div 0.2 \text{ V}$

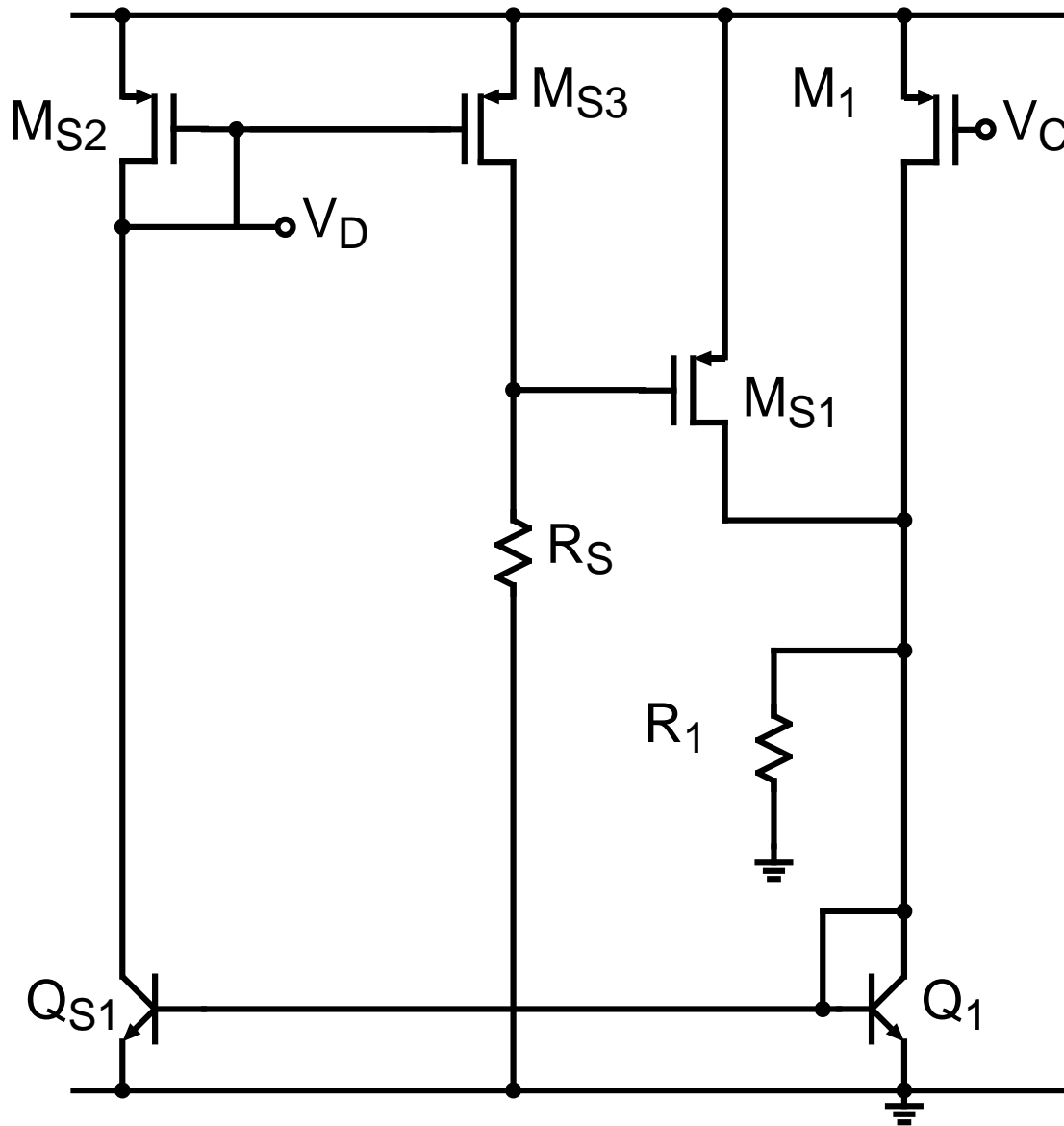
# OPERATIONAL AMPLIFIER

Simulated Performance	
Parameter	Value
Technology	0.8 $\mu\text{m}$ BiCMOS
p-MOS Transistor Threshold Voltage n-MOS Transistor Threshold Voltage	840 mV 800 mV
DC Gain	60 dB
Gain-Bandwidth Product	1.2 MHz
Phase Margin	63°
Systematic Offset Voltage	625 $\mu\text{V}$
Supply Voltage	1 V
Current Consumption @ T = 25° C	35 $\mu\text{A}$

# STARTUP CIRCUIT

- In every bandgap circuit there are two stable operating points
  - ✌ Desired operating point  $\rightarrow I_{Q_1} = I_{Q_2} = V_T \ln(N)/R_0$ ,  $V_{ref} \neq 0$
  - ✗ Undesired operating point  $\rightarrow I_{Q_1} = I_{Q_2} = 0$ ,  $V_{ref} = 0$
  
- The operational amplifier systematic offset during the startup phase can cause metastability in the bandgap circuit
  - ➡ The operational amplifier has to startup at least as fast as the bandgap circuit
  - ✌ Operational amplifier bias current  $I_{BJT} = I_{Q_1} = I_{Q_2}$
  - ✌ All of the currents in the operational amplifier and in the bandgap circuit are matched
  - ➡ No operational amplifier systematic offset during startup

# STARTUP CIRCUIT



- $I_{Q_1} = 0 \rightarrow I_{Q_{S1}} = 0$ 
  - ↳  $M_{S2}$  and  $M_{S3}$  are off
  - ↳  $V_{GS, M_{S1}} = V_{DD}$
  - ↳  $I_{M_{S1}}$  flows into  $Q_1$  and  $R_1$
  - ↳ The circuit leaves the undesired operating point
  - ↳  $I_{Q_1} \rightarrow \frac{V_T \ln(N)}{R_0}$
- In normal operating conditions
  - ↳  $I_{Q_1} \neq 0 \rightarrow I_{M_{S3}} R_S \cong V_{DD}$
  - ↳  $M_{S1}$  switches off

# CURVATURE COMPENSATION

- Simple bandgap circuits: temperature compensation is at first order

└  $V_{BE}$  does not change linearly with temperature

$$V_{BE}(T) = V_{BG} - [V_{BG} - V_{BE0}] \frac{T}{T_0} - (\eta - \alpha) \ln \frac{T}{T_0}$$

- ➔  $\eta \cong 4 \rightarrow$  Depends on the bipolar transistor structure
- ➔ Temperature independent current ( $I_{TI}$ ) in the transistor  $\rightarrow \alpha = 0$
- ➔ PTAT current ( $I_{PTAT}$ ) in the transistor  $\rightarrow \alpha = 1$

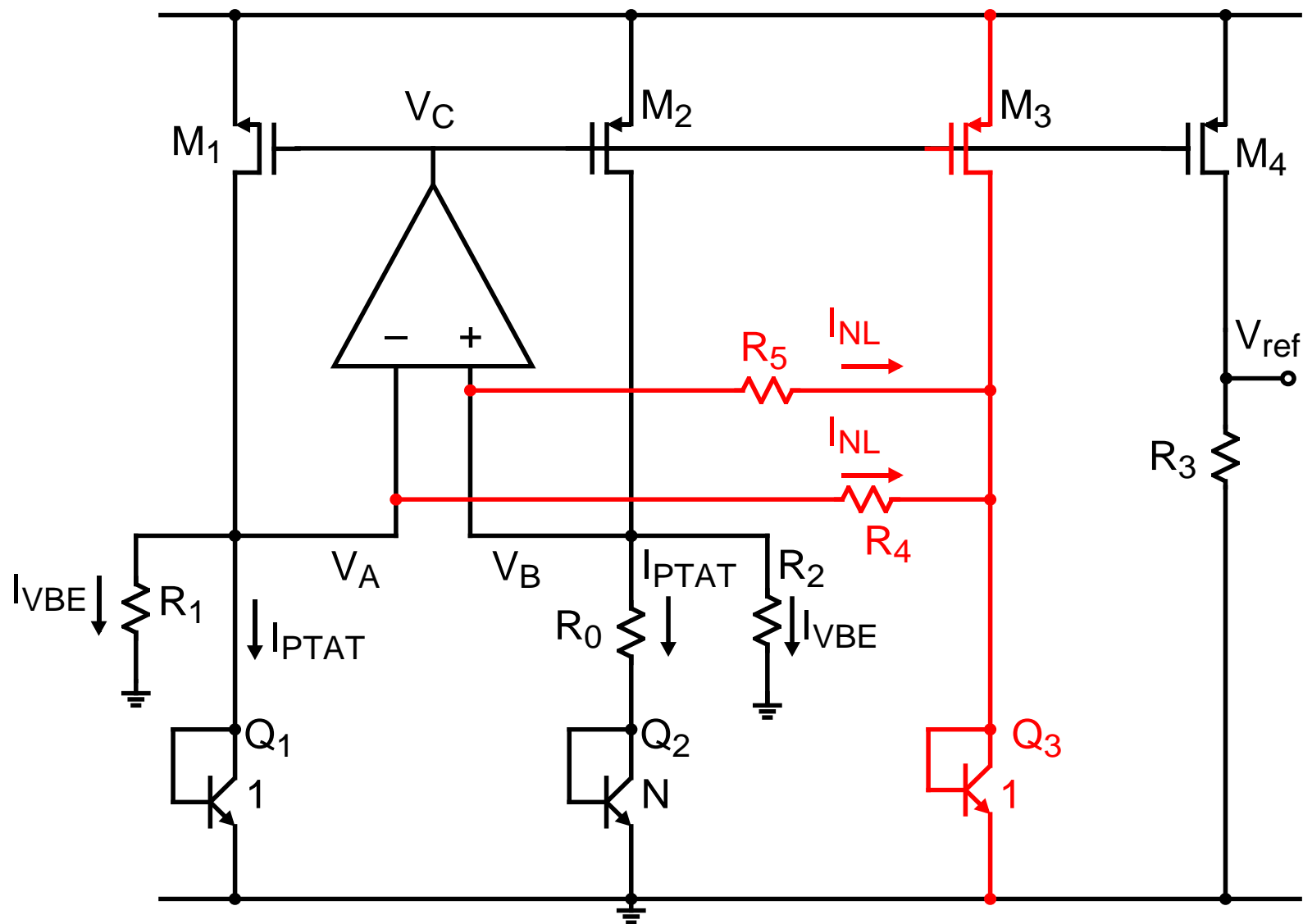
- $V_{BE@I_{TI}} - V_{BE@I_{PTAT}} \rightarrow$  Nonlinear term  $\rightarrow$  Correction

➔  $I_{Q_1} \rightarrow$  PTAT current

➔  $I_{M_1} \rightarrow$  Temperature independent current

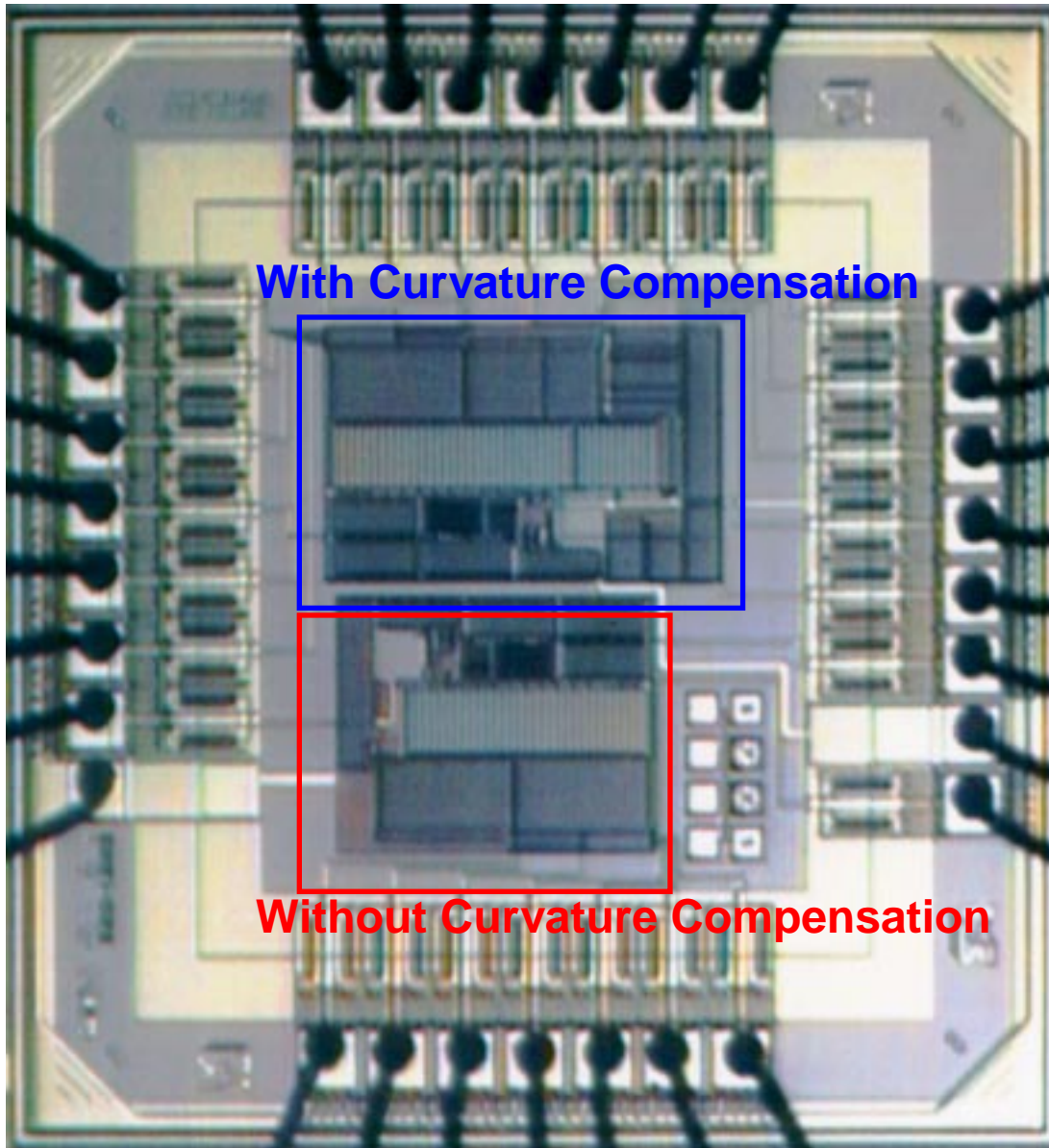
✌ Simple generation of the nonlinear term

# CURVATURE COMPENSATION



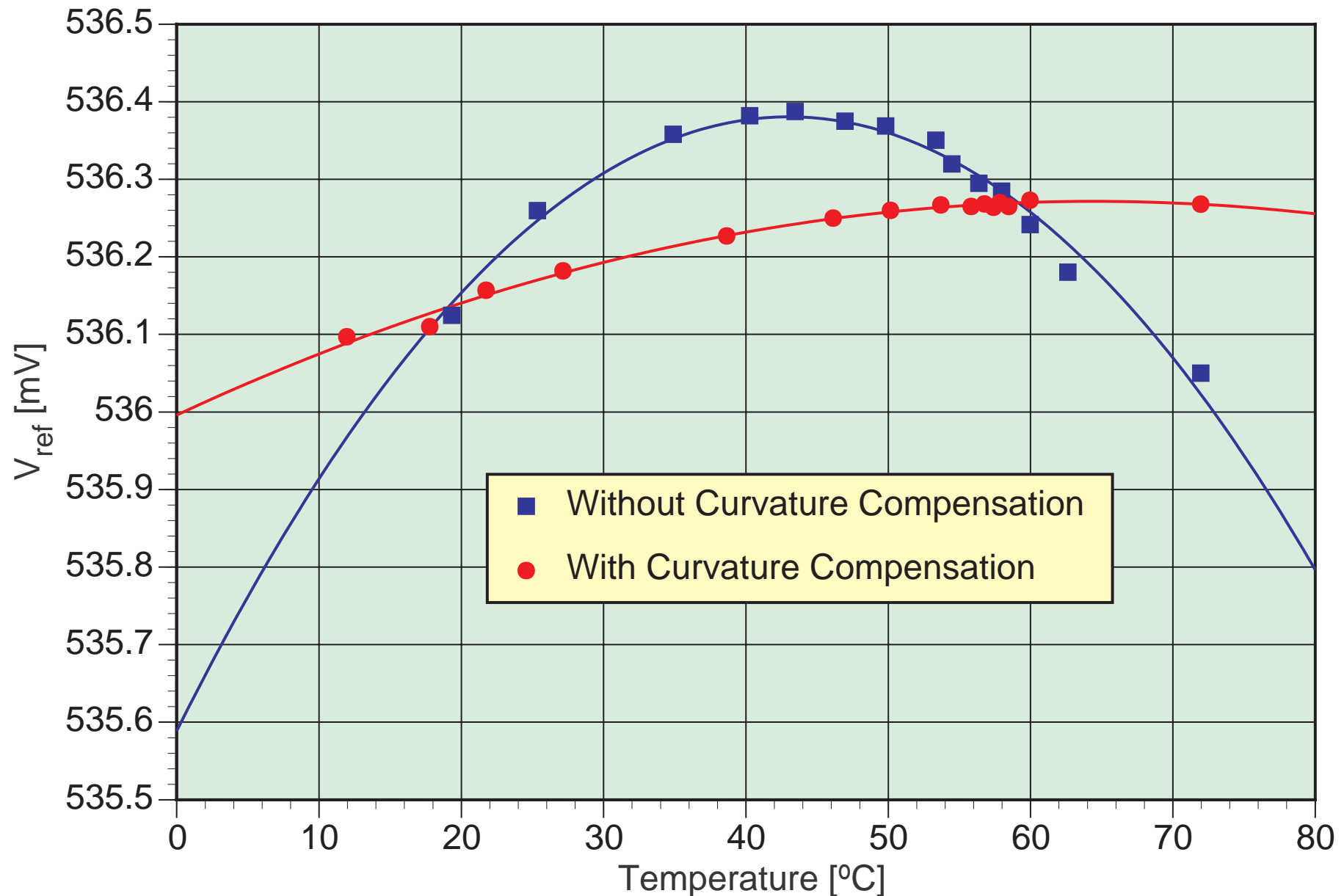


# CHIP MICROGRAPH

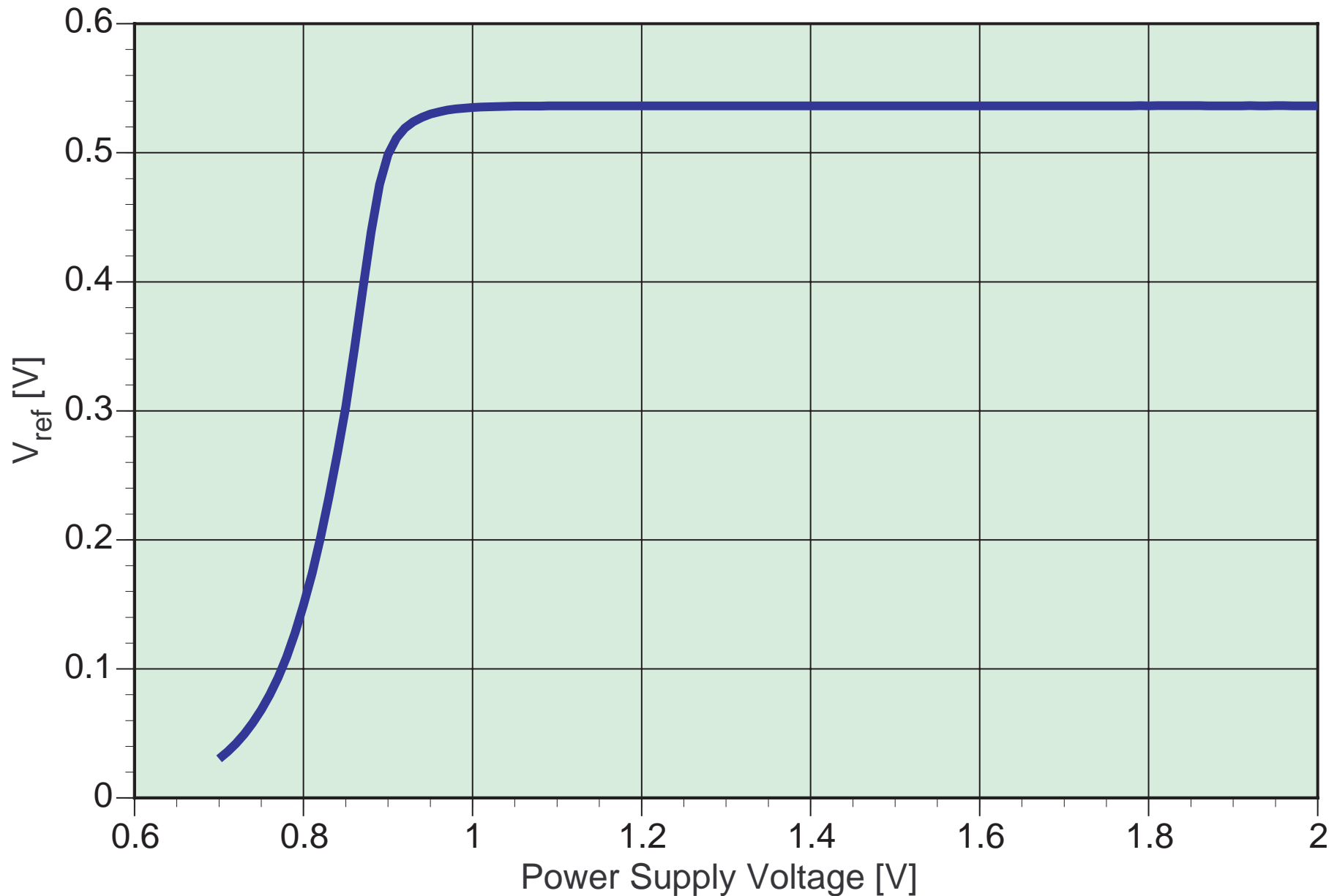


- ❑ Technology
  - ➔ 0.8  $\mu\text{m}$  BiCMOS
  - ➔ Double poly
  - ➔ Double metal
- ❑ Total area including pads
  - ➔ 3 mm<sup>2</sup>
- ❑ Core area
  - ➔ 0.20 mm<sup>2</sup>
  - ➔ 0.25 mm<sup>2</sup>
- ❑ Trimming of resistors
  - ➔  $R_0$ ,  $R_4$  and  $R_5$
  - ➔ 8 pins per resistor

# EXPERIMENTAL RESULTS



# EXPERIMENTAL RESULTS



# PERFORMANCE SUMMARY

Parameter	Value
Power Supply Voltage	1 V
Technology	0.8 $\mu\text{m}$ BiCMOS
Bandgap Cell Area Without Curvature Compensation With Curvature Compensation	0.20 $\text{mm}^2$ 0.25 $\text{mm}^2$
Power Consumption @ 25° C	92 $\mu\text{W}$
Reference Voltage @ 25° C	536 mV
Temperature Variation (0° C ÷ 80 ° C) Without Curvature Compensation With Curvature Compensation	800 $\mu\text{V}$ 300 $\mu\text{V}$
Voltage Coefficient	114 $\mu\text{V/V}$

# CONCLUSIONS

- ❑ Low voltage ( $V_{DD} = 1\text{ V}$ ) bandgap can be achieved with current-mode structures **AND** low voltage, low offset op-amps
- ❑ A current mode structure permits to achieve curvature compensation in a simple way (no extra op-amps)
- ❑ Experimental results show that it is possible to achieve 0.5 V reference with 1 V supply and a well controlled temperature behavior.

# THANK YOU!