A 700+ mW Class D Audio Amplifier with direct battery hookup in a 90 nm process

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Abstract

A “battery connect” compatible class D (switching) amplifier which is fully integrated in a 90 nanometer digital CMOS process is presented. The integration of the amplifier requires no additional masks, processing, or cost. This presentation includes a brief description of the circuit techniques that enable direct battery (2.7 – 5.4V) connection and allow support > 6.7 VP2P (700 mW into 8 ohms) output swing from a 4.2 V supply using devices that operate solely with low gate voltages. The achieved SNR over an audio (20Hz to 20 kHz) bandwidth > 98dB (1W) and the total harmonic distortion (THD) is better than 0.03% at 500 mW. Efficiency is greater than 75% above 375 mW. The power supply rejection ratio (PSRR), which is a crucial parameter in modules connected directly to the battery, is measured at 70dB at 217 Hz. The area of the switching amplifier is < 0.44mm2, where the power devices occupy approximately 20% of the total.

Agenda

- Introduction
- Motivation
- PWM Modulation
- Architectures
- Deep Sub-Micron Technology Considerations
- Design Solution
- Testing Challenges
- Simulation & Measurement Results
- Conclusion

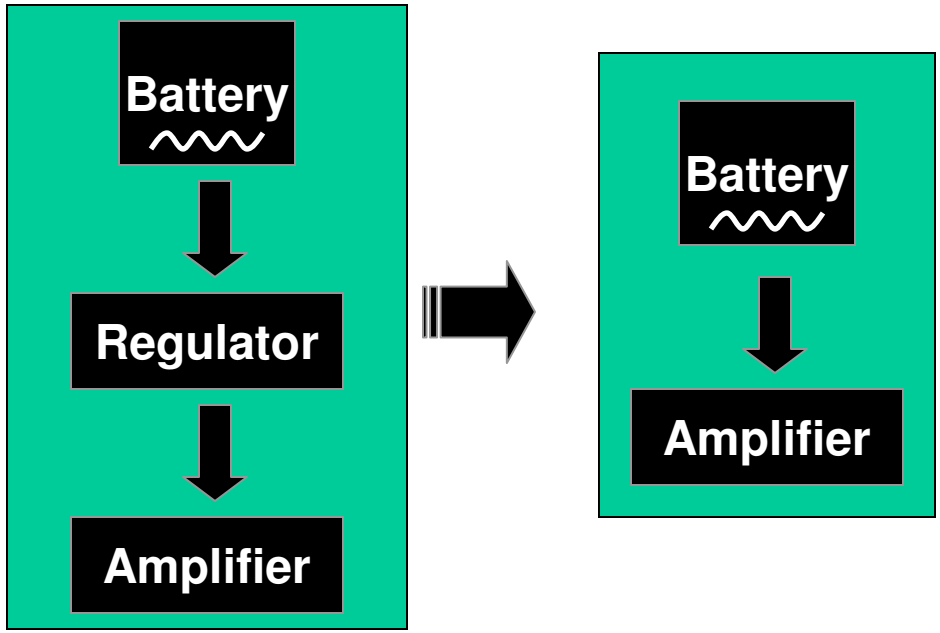
Introduction

- Audio output demands continue to increase for mobile devices
  - Poly-phonic Ringers
  - Handset Speakers
  - Stereo Outputs
  - Multi-channel 3D Audio
  - Speaker Phones
- Power Efficiency in Mobile Electronics
  - Heat Dissipation
  - Battery Life

Typical Application

Audio Demands

- Specific challenges in battery supplied systems
  - PSRR
  - HEAT
  - Battery life
- Performance metrics
  - Output power
  - THD
  - SNR
  - Efficiency



Power Budget

– The future of mobile devices –

- Digital Processor Cores are even more power hungry
- More “Audio” power amplifiers for today’s typical mobile devices
  - Speaker phone
  - Polyphonic ringer
  - MP3 Stereo
  - Earphone
- Smaller area involves greater heat dissipation
- *Switching Amplifiers help alleviate thermal concerns*

Motivation: Class D…

- Has improved *Efficiency* across the range of power delivered with respect to Class A, AB, & B
- Can directly replace Class A, AB, or B in traditional systems
- Is advantageous for integration in 90nm technologies and beyond

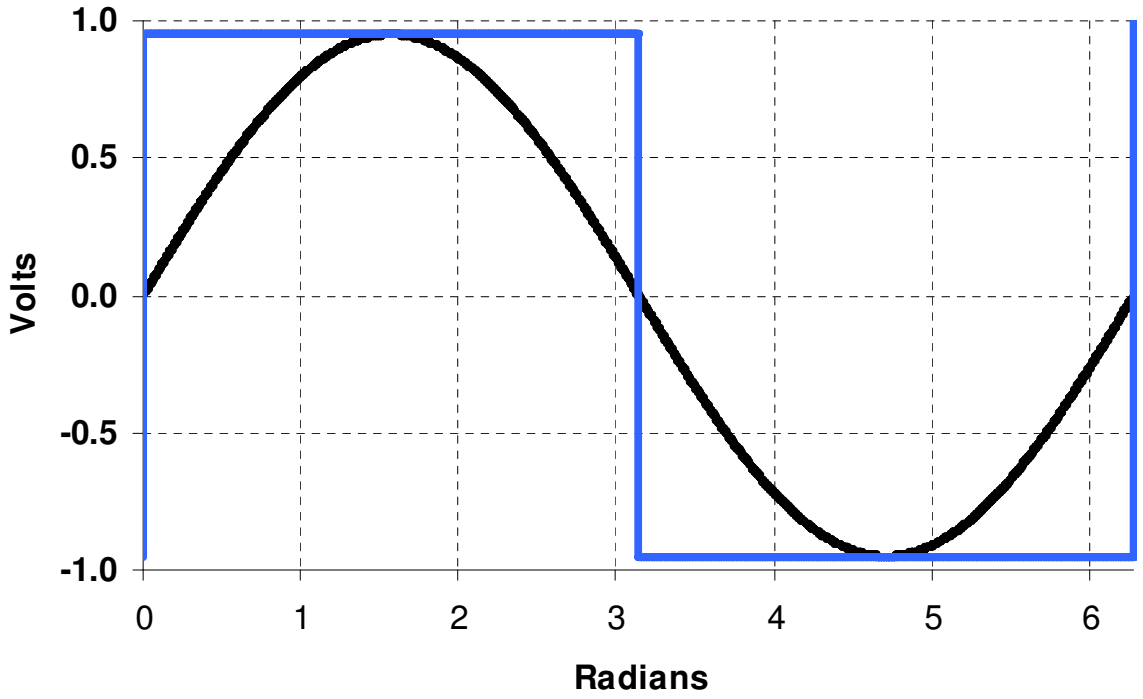
Power Efficiency

$$Eff = \frac{\int_T I_{load}(t) * V_{load}(t)dt}{\int_T I_{battery}(t) * V_{battery}(t)dt + \int_T I_{ldo}(t) * V_{ldo}(t)dt}$$

$$Eff_{MAX-ClassD} = \frac{R_{load}}{R_{load} + R_{dsonNMOS} + R_{dsonPMOS} + R_{parasitic}}$$

Continued

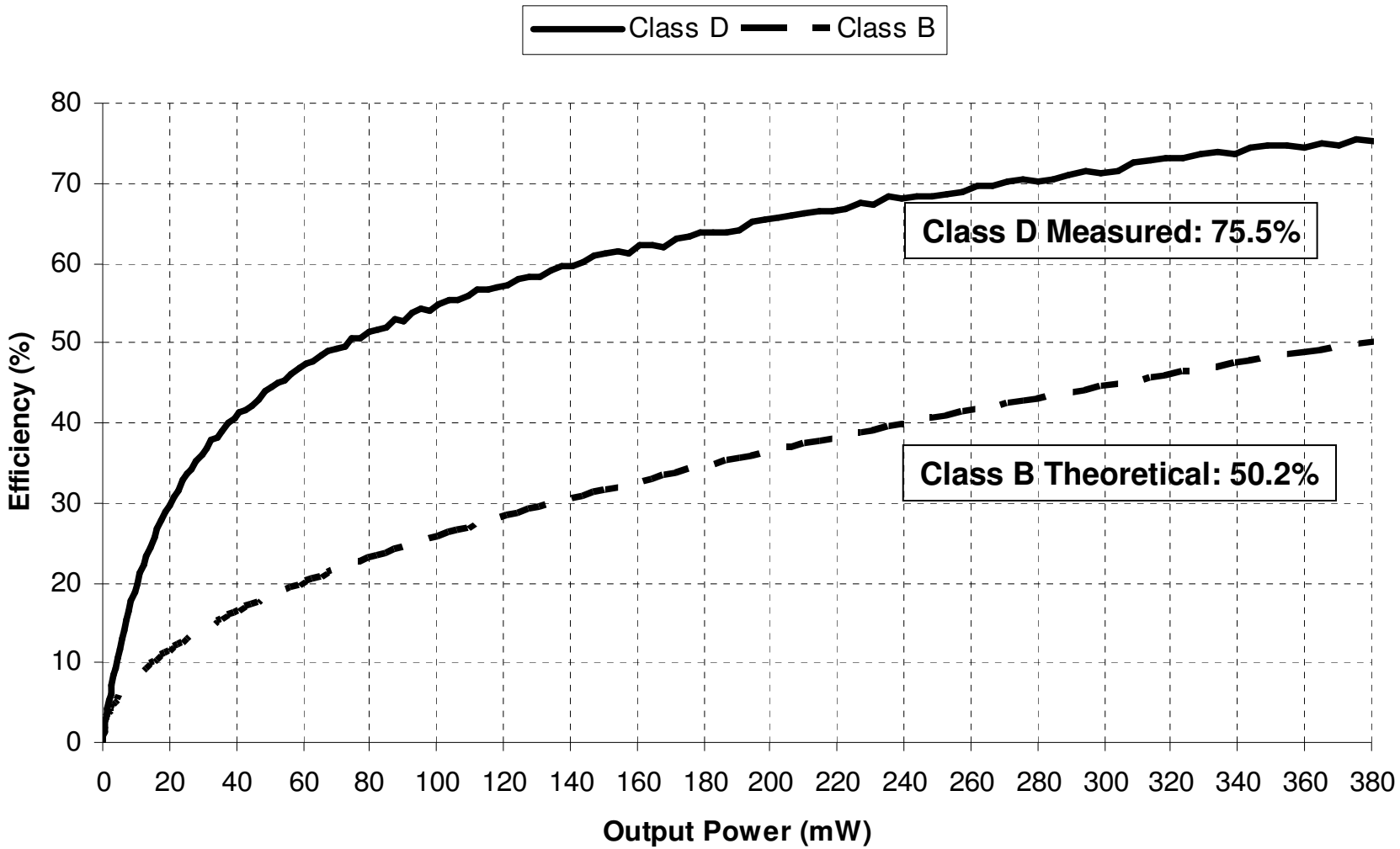
Efficiency Comparison



- Assuming a simple resistive load
- Class D output can be approximated as a square wave.
- Class D Efficiency is proportional to V_{max}
- Class B Efficiency is proportional to the half sin wave integral

$$\eta_{ClassB} = \frac{\pi * V_{amp}}{4} \Rightarrow \eta_{ClassB} = 0.7854 * V_{amp} \qquad \eta_{ClassD} = \frac{R_{load}}{R_{load} + R_{dson}}$$

Efficiency Comparison

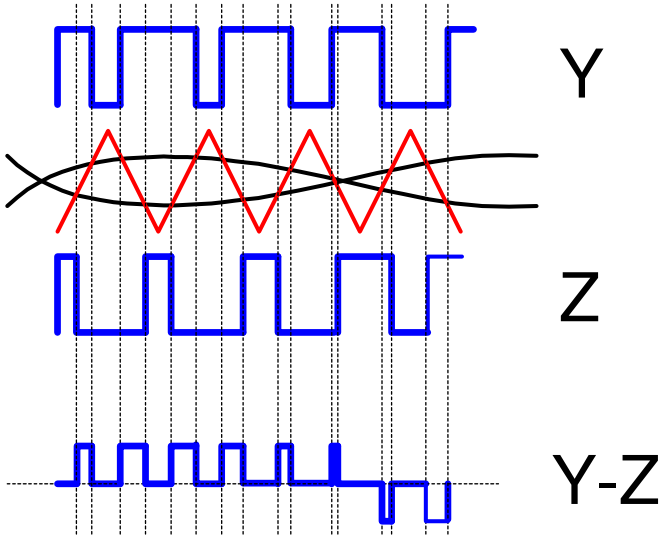


"Energy not delivered to load is dissipated thermally"

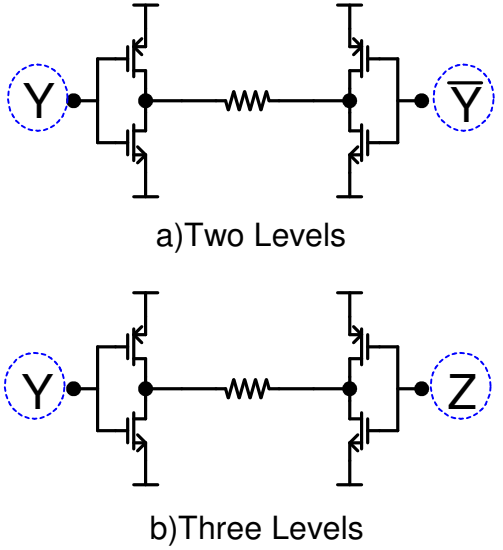
Pulse Width Modulation

- Two basic types of modulation
  - Binary (or AD)
  - Ternary (or BD)
- Three ways to generate modulation
  - Leading edge
  - Trailing edge
  - Double edge
- Typical Schemes
  - Natural Sampling
  - Uniform Sampling
  - Hybrid Sampling ← Many possibilities

Pulse Width Modulation



Modulation Levels

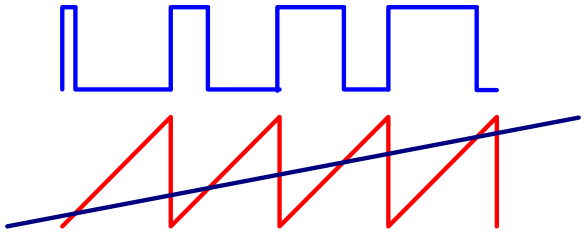


The two Configurations

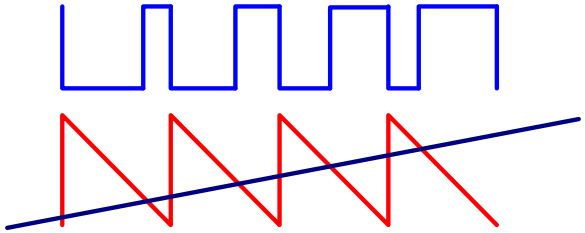
*Graphics provided by Francisco Ledesma

Pulse Width Modulation

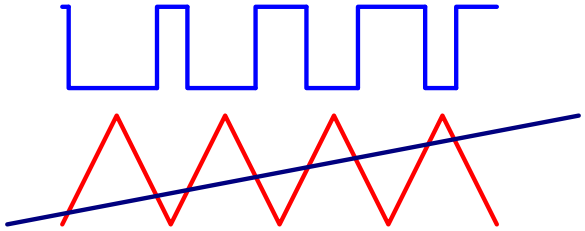
Trailing



Leading



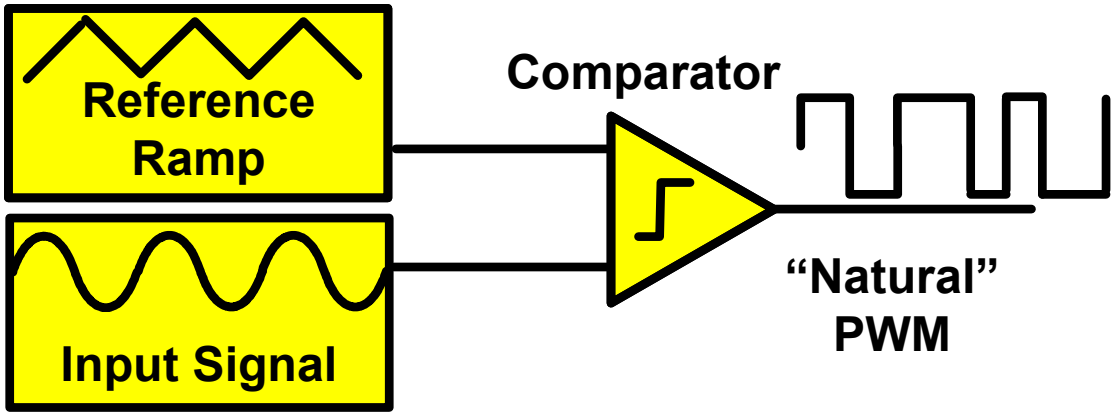
Double



Modulation Edges

*Graphics provided by Francisco Ledesma

Pulse Width Modulation



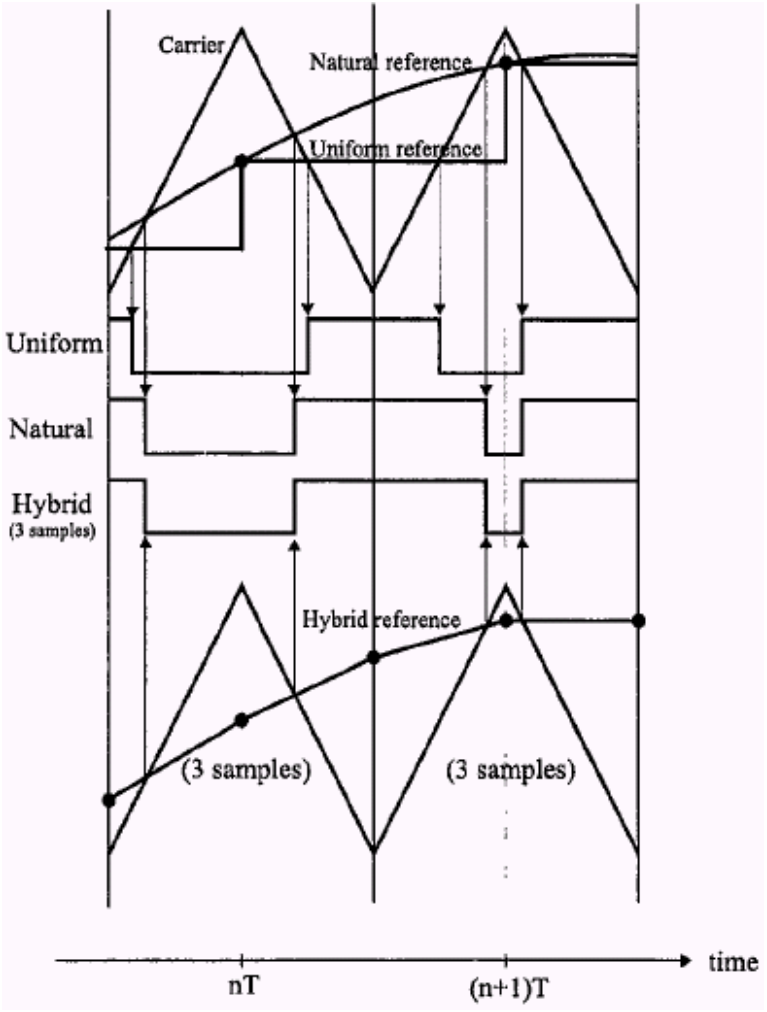
- Natural Sampling
  - Infinitely precise edges
  - No distortion added
  - Comparator performance
  - Reference linearity

*Graphics provided by Francisco Ledesma

Pulse Width Modulation

Comparison between a few modulation sampling schemes

- Natural – Theoretically ideal
- Hybrid – Approaches Natural
  - Information lost
  - Faster Carrier→ Increased Performance but lower efficiency
- Uniform – Sample and Hold
  - Information lost
  - Interpolation method impacts performance
  - Faster Carrier→ Increased Performance but lower efficiency



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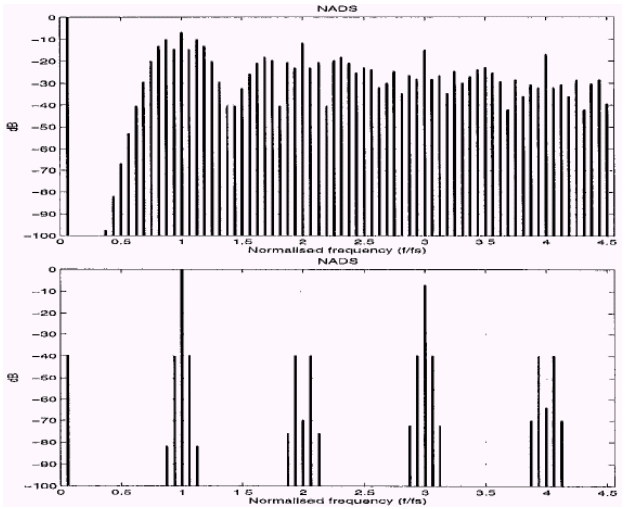
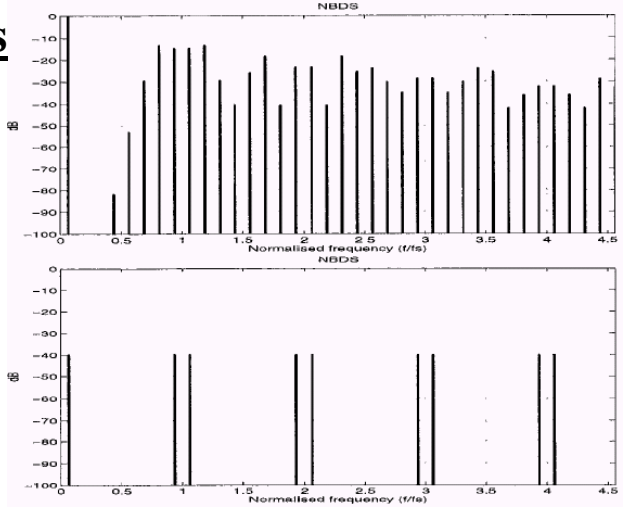
Pulse Width Modulation

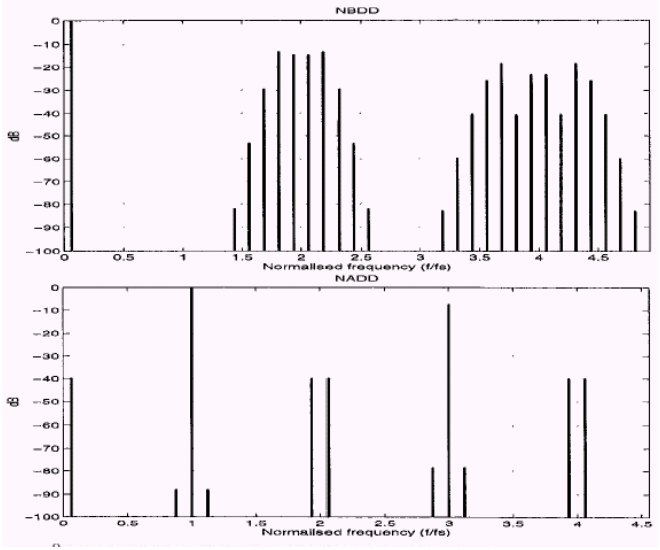
Natural Sampling Spectrums



←Natural Single Sided Binary Modulation

Natural Single Sided Ternary Modulation →





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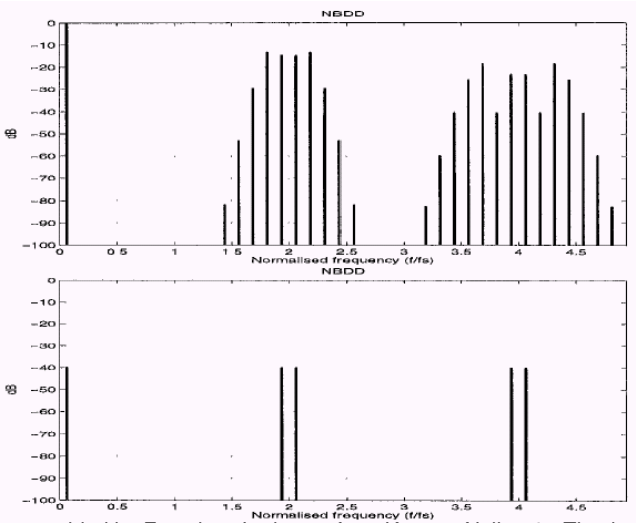
Natural Double Sided Ternary Modulation →



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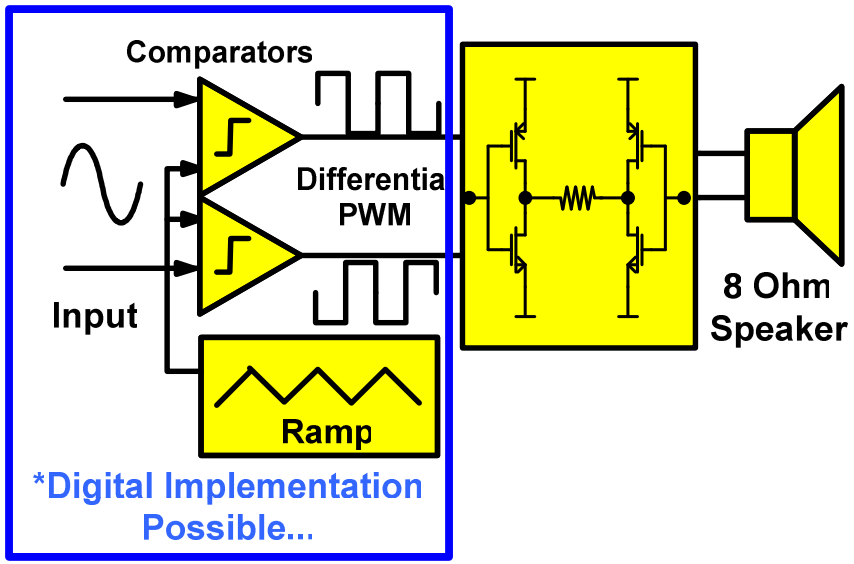
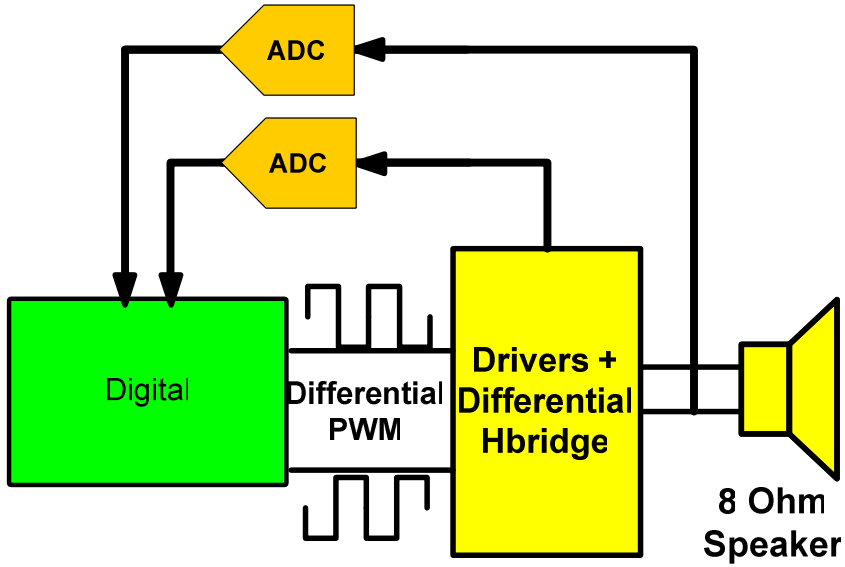
Architectures

- ***Open Loop Bridge***
  - More Efficient
  - Smaller Area
    - Possibly Bridge Only if PWM data is pre-existing
  - Approximately 0 PSRR
  - Output Amplitude is proportional to power supply voltage and loading conditions → **no gain control**
  - No error source correction method as with feedback system
    - THD may suffer
    - Noise may suffer
  - In practice on Cellular phone for low quality applications
    - Ringers
    - Buzzers



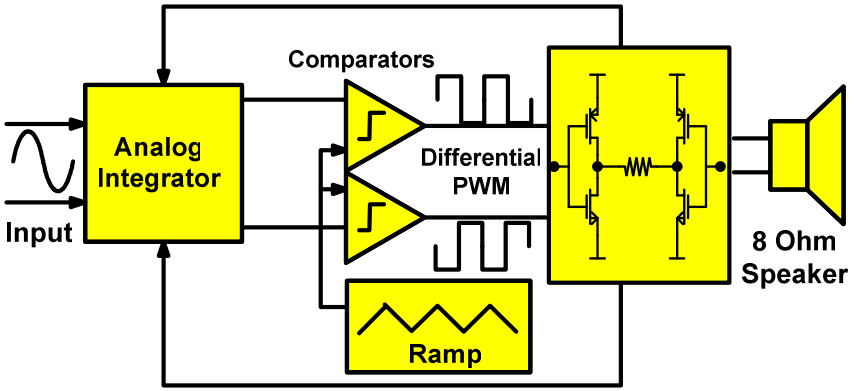
Architectures

- ***Open Loop Bridge with Digital P.S. and Load correction methods***
  - Sample power supply with ADC and pre-condition the signal to correct for power supply changes
  - Start up calibration loop → measures load and also pre-conditions the signal based upon the pre-existing load
  - Stability is major factor
  - Digital processing required
    - Mixer
    - Programmable Equalizer
    - Significant area and power increase
  - In practice for extreme performance high power applications



Architectures

- ***Closed Loop System***
  - Provides mechanism with corrects for Power Supply noise and Errors
  - Fixed Gain
  - Load independent Gain
  - Area and Efficiency are acceptable for the application
  - Feedback system also corrects for other error sources in the system
  - Direct replacement for existing continuous time amplifiers
    - ***Competitive to AB in Performance & Area***
    - ***No system changes required***



Architectures Summary

- ***Open Loop Bridge***
  - More Efficient
  - Smaller Area (Bridge Only)
  - Approximately 0 PSRR
  - Output Amplitude is proportional to power supply voltage and loading conditions → **no gain control**
  - No error source correction method as with feedback system
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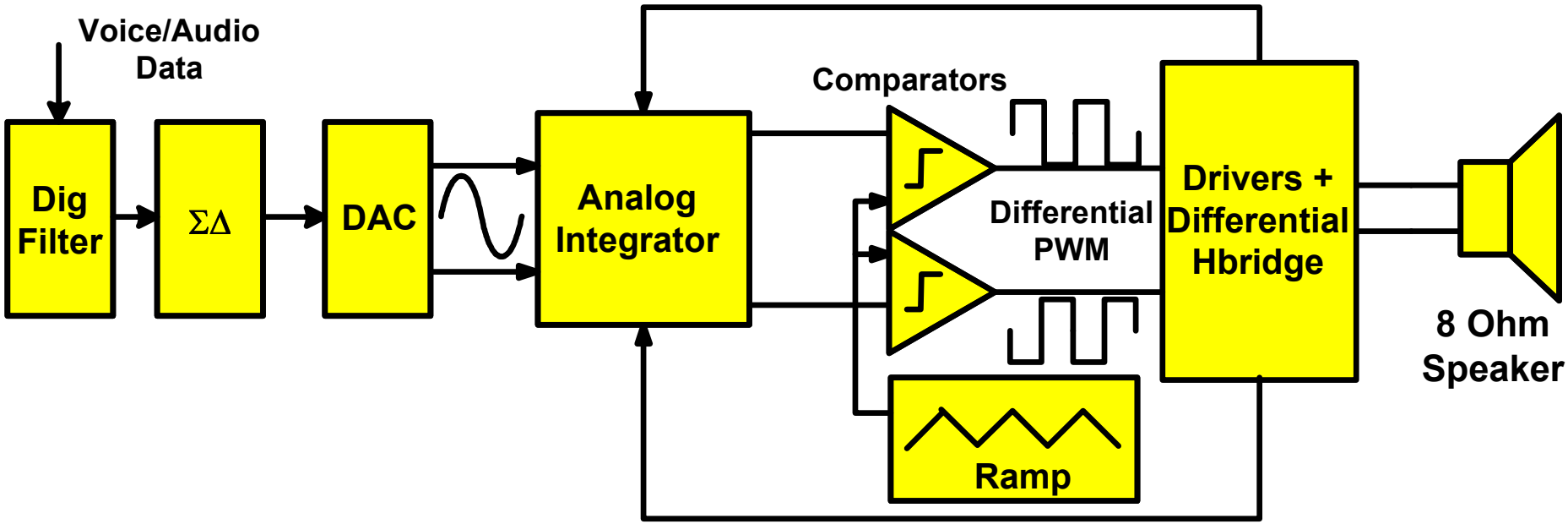
  - Feedback system also corrects for other error sources in the system
  - Direct replacement for existing continuous time amplifiers
    - ***Competitive to AB in Performance & Area***
    - ***No system changes required***
  - ***Chosen Architecture***

Audio Channel with Class D



Stability Criteria

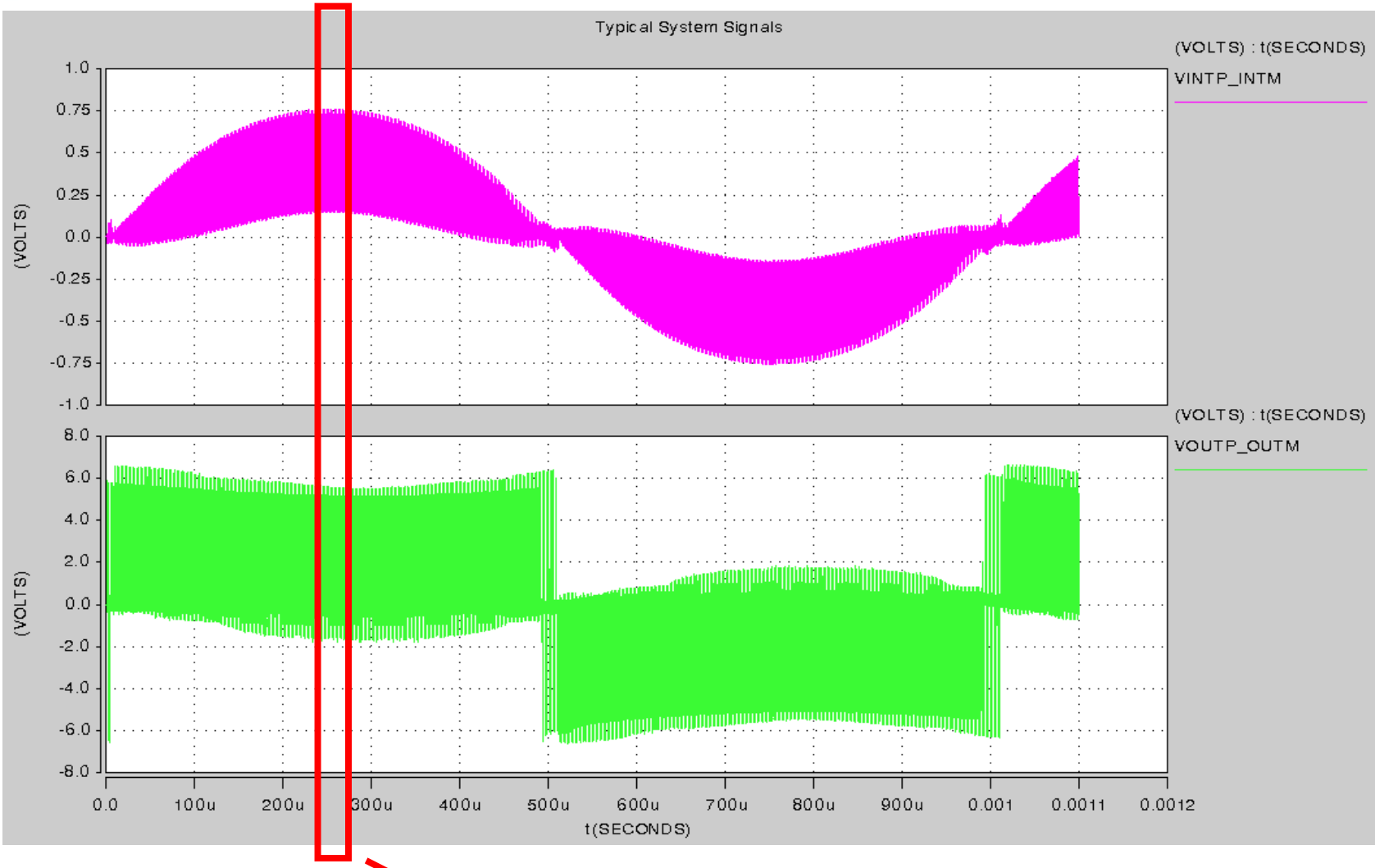
- At first glance the system is first order and should there for be inherently stable
- However, there is a secondary stability criterion which must be meet
  - If the slew rate of the integrator exceeds that of the ramp from which the PWM carrier is derived then the system becomes unstable
  - In a system where the average input and output common modes are equal, Equation (1) defines stability
  - Where the input and output common modes are not equal equations (2) & (3) outline the stability criterion

$$F_{INTPole} \leq \frac{F_{Ramp}}{\pi} \qquad (1)$$

$$4 * V_{Aramp} * F_{ramp} \geq \frac{1}{C_I}\left(\frac{V_{CMA} \pm V_I}{R_{IN}} + \frac{V_{CMA} \pm V_O \mp V_{CMO}}{R_{FB}}\right) \qquad (2)$$

$$V_{CMA} = V_{CMINPUT} + \left(V_{CMOUT} - V_{CMIN}\right) * \left(\frac{R_{IN}}{R_{IN} + R_{FB}}\right) \qquad (3)$$

Typical Signals



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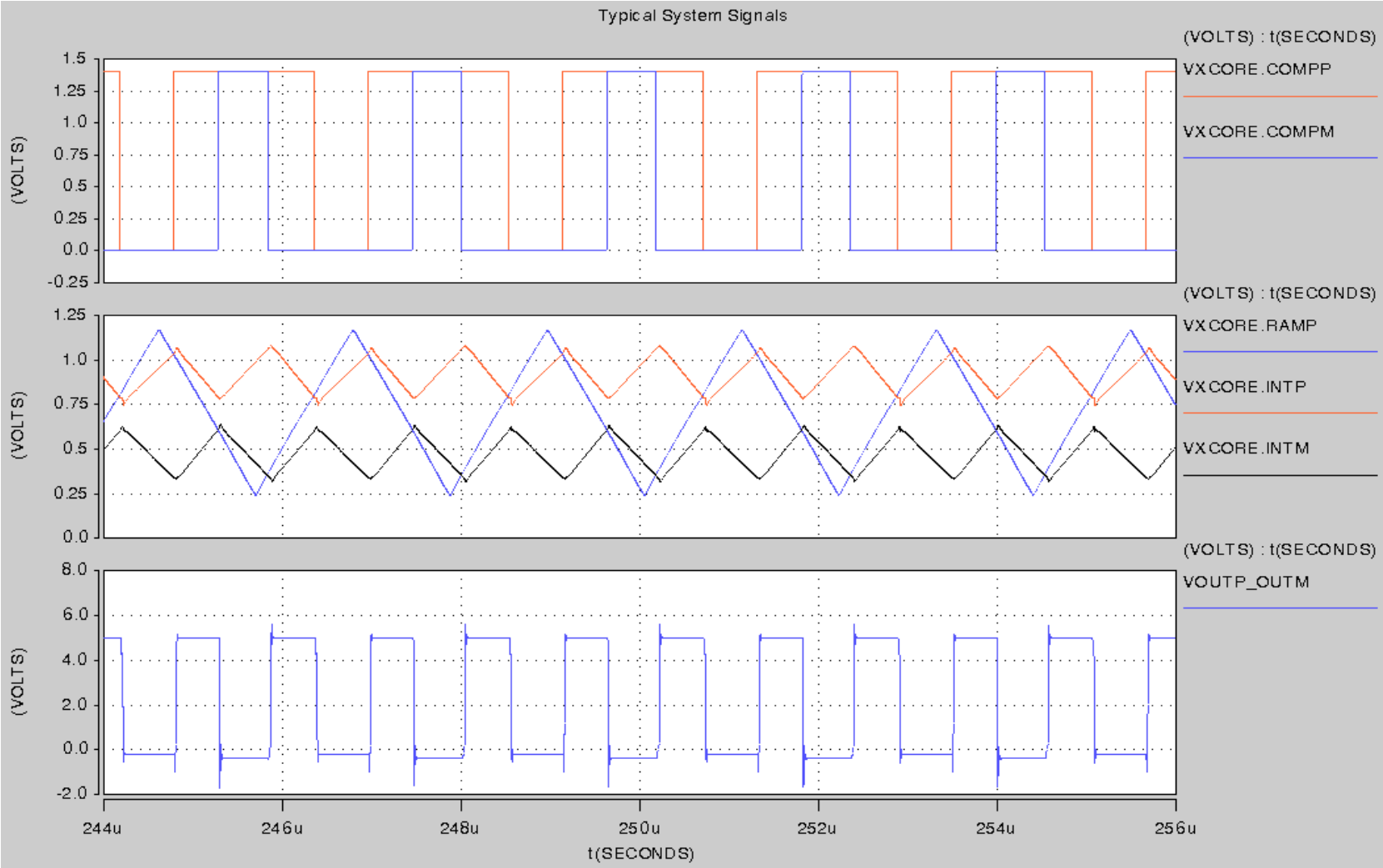
Typical Signals



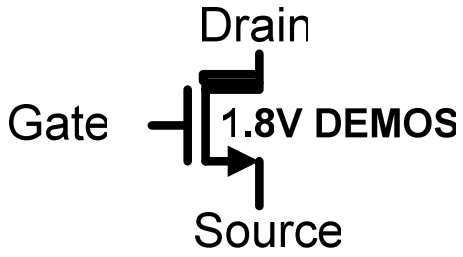
Integration Advantages in Deep Sub Micron CMOS

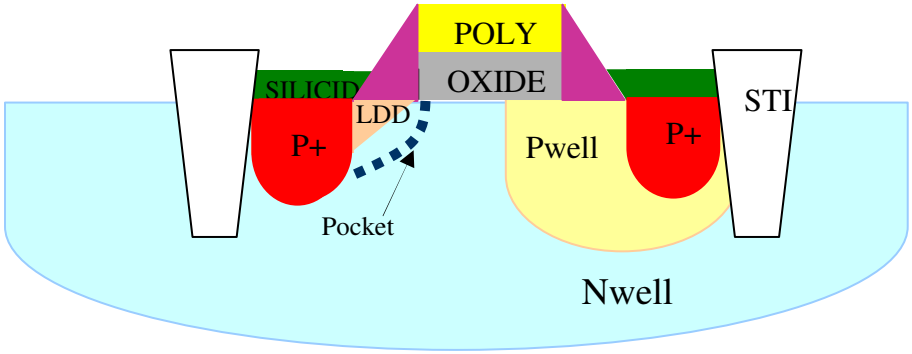
- Processing advantages
  - Higher I_{drive} per area
  - Faster devices & sub circuits
  - Reduced area & minimum feature size
  - Direct battery connection at no additional cost
- Embedded solutions
  - System partitioning
  - Flexibility

Design Challenges in Deep Sub Micron Technologies

- We need a direct battery connection: Reliability Issues
  - Maximum Drain to Source voltage
  - Gate Oxide Integrity
- Device leakage currents
  - Channel Leakage
  - Gate Leakage
  - Drain/Source to Body Leakage

Drain Extended Devices



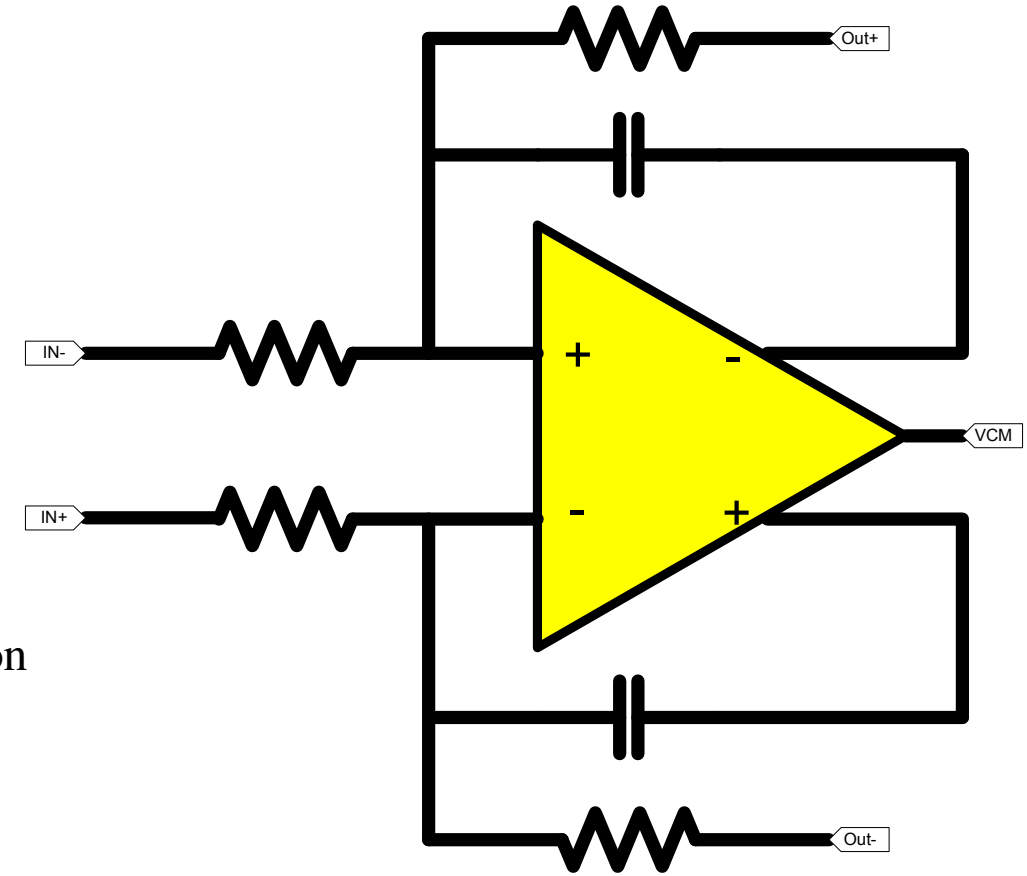


Drain Extend PMOS cross section

- Make High Voltage Design Possible for no extra cost!!!
  - Free from processing perspective (no extra masks or steps)
  - Using Core or thin gate oxides high voltage design is made possible
  - Drain is "extended" away from gate
  - Allows the Gate to Drain voltage to be much greater while other terminals still must meet core device reliability standards
  - Matching?
  - I_{DRIVE} is reduced
  - C_{GD} is much greater than core devices
  - FT is much less than core devices

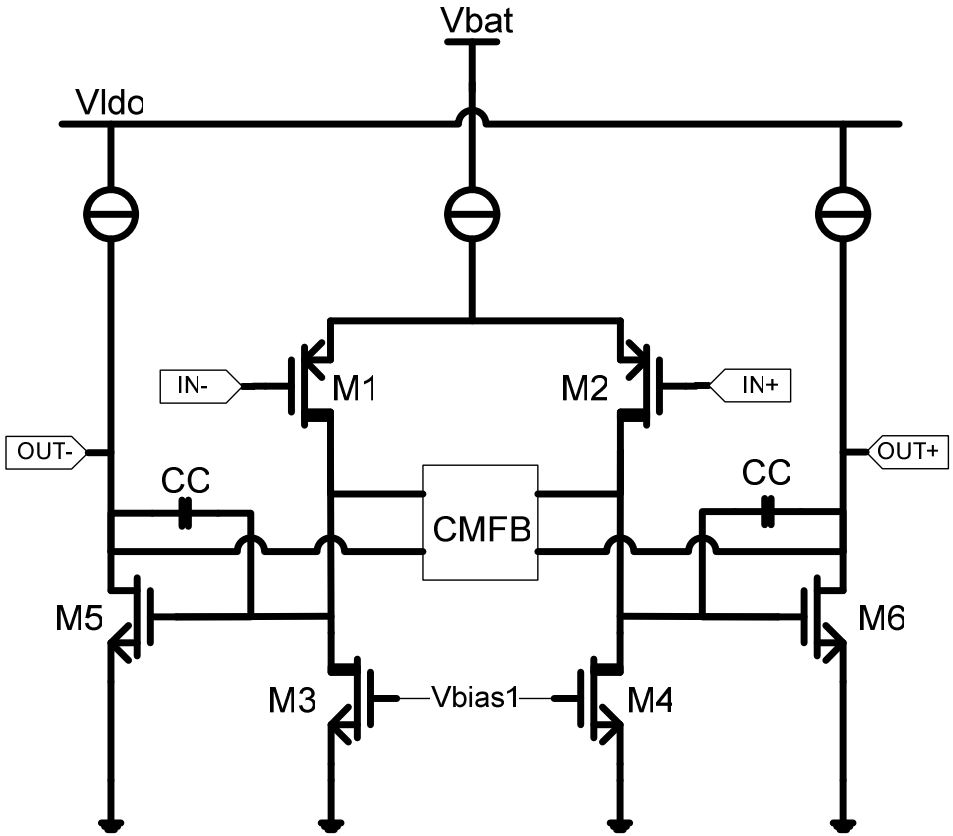
Integrator

- Input Common Mode Range
- High DC Gain
- Good Common Mode Rejection
- High Linearity
- Low Noise
- Low Power
- Good PSRR
- Low Area
  - Amplifier
  - Passives
- Performance depends mainly upon Amplifier
- Passives must be linear



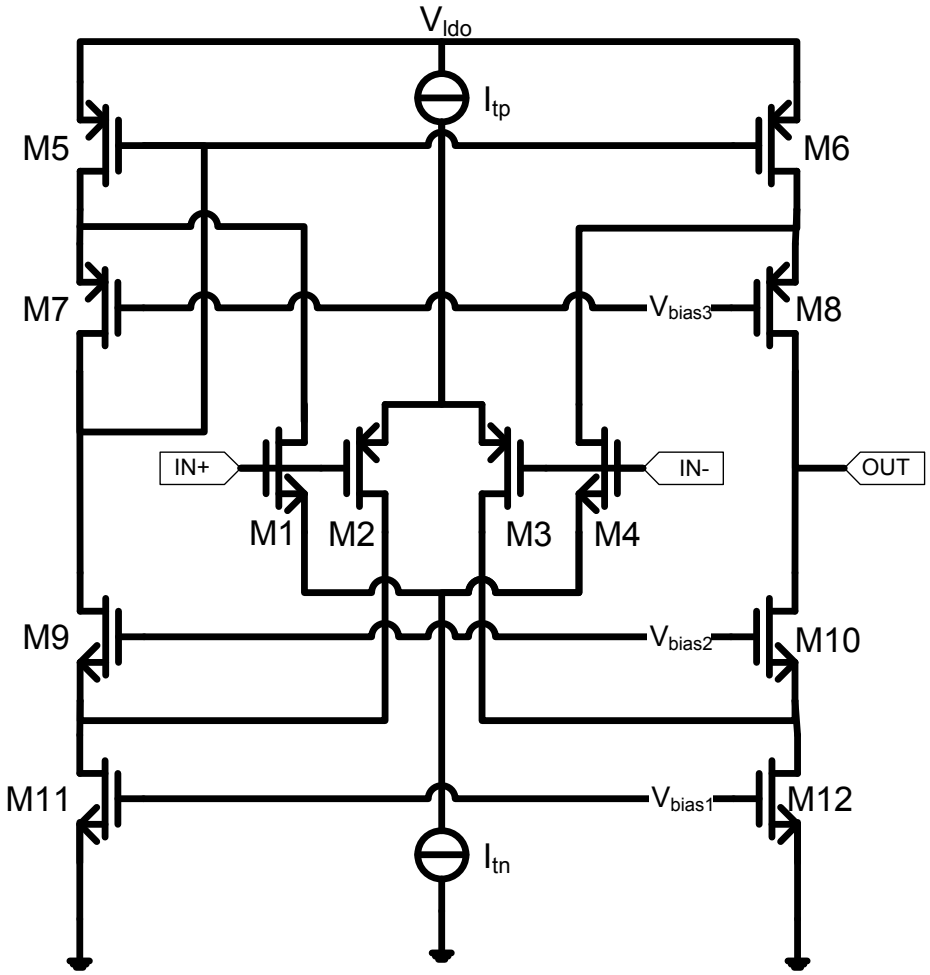
Integrator Amplifier

- Input Common Mode Range
- High Gain
- High Phase Margin
- High Gain Margin
- Band width at least 10X greater than Modulation frequency
- Low power
- Low area
- Good common mode feedback performance
  - Gain
  - Phase Margin
  - Gain Margin
- Linearity must be a significant margin above overall loop specification
- Noise must be a significant margin above overall loop specification
- Large output swing (compared to V_{LDO})



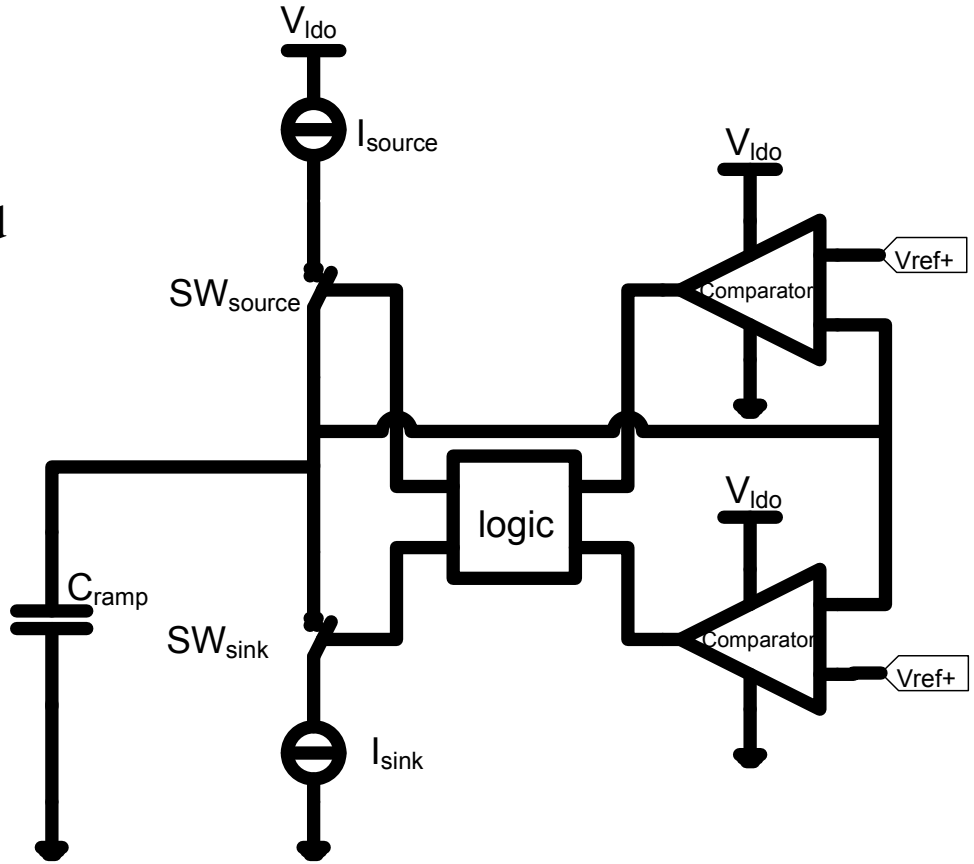
Comparator

- High Gain
- High speed
  - Rise & Fall time
  - Propagation delay
- Low power
- Low area
- Low Noise
- Rail to rail input range – comparing a large scale ramp signal to the integrator output



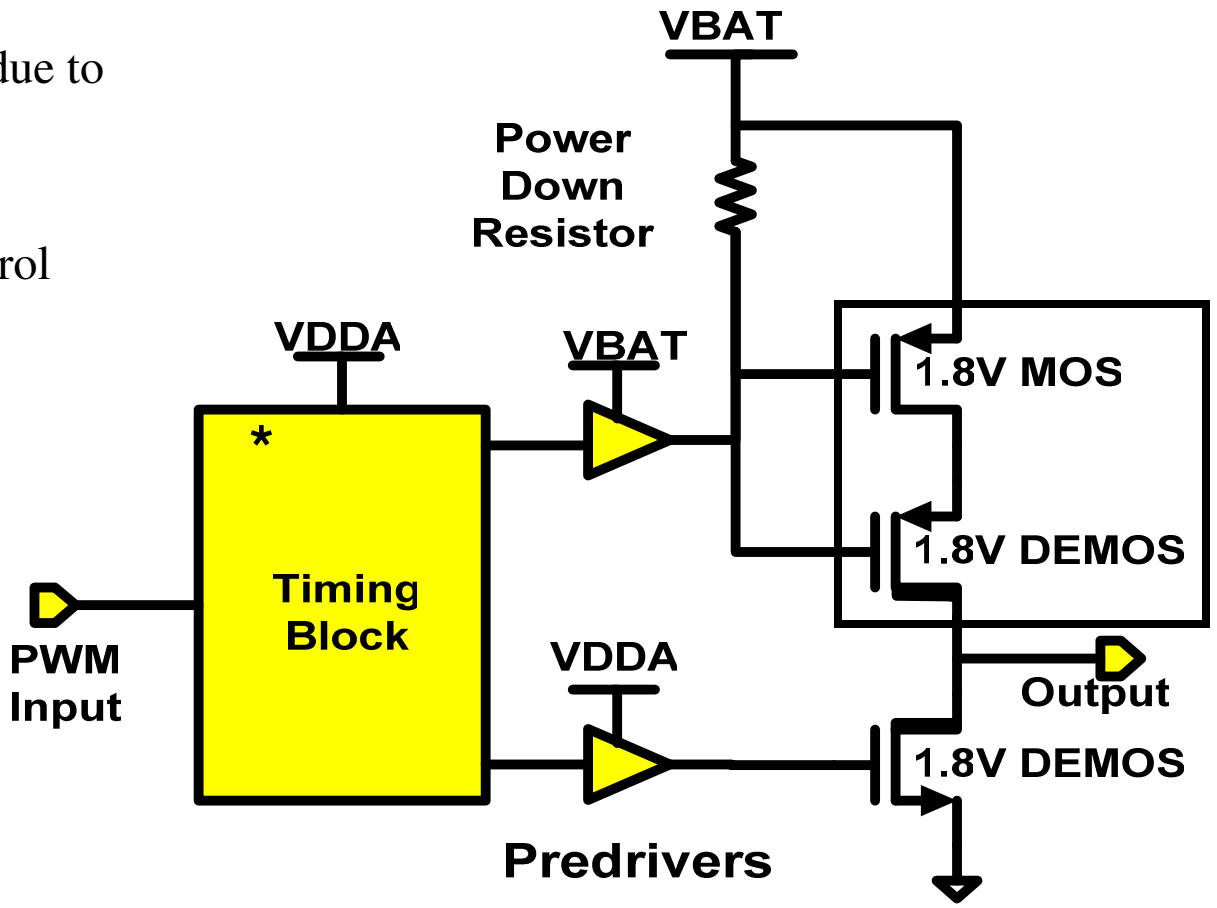
Ramp Generator

- Provides the triangular wave form required for “Natural Sampling”
- Must be linear for good Signal THD
- Must have large swing range for good stability versus area trade off of overall design
- Should have minimal frequency drift versus process, voltage, and temperature
  - PLL
  - Trim
  - Auto calibration



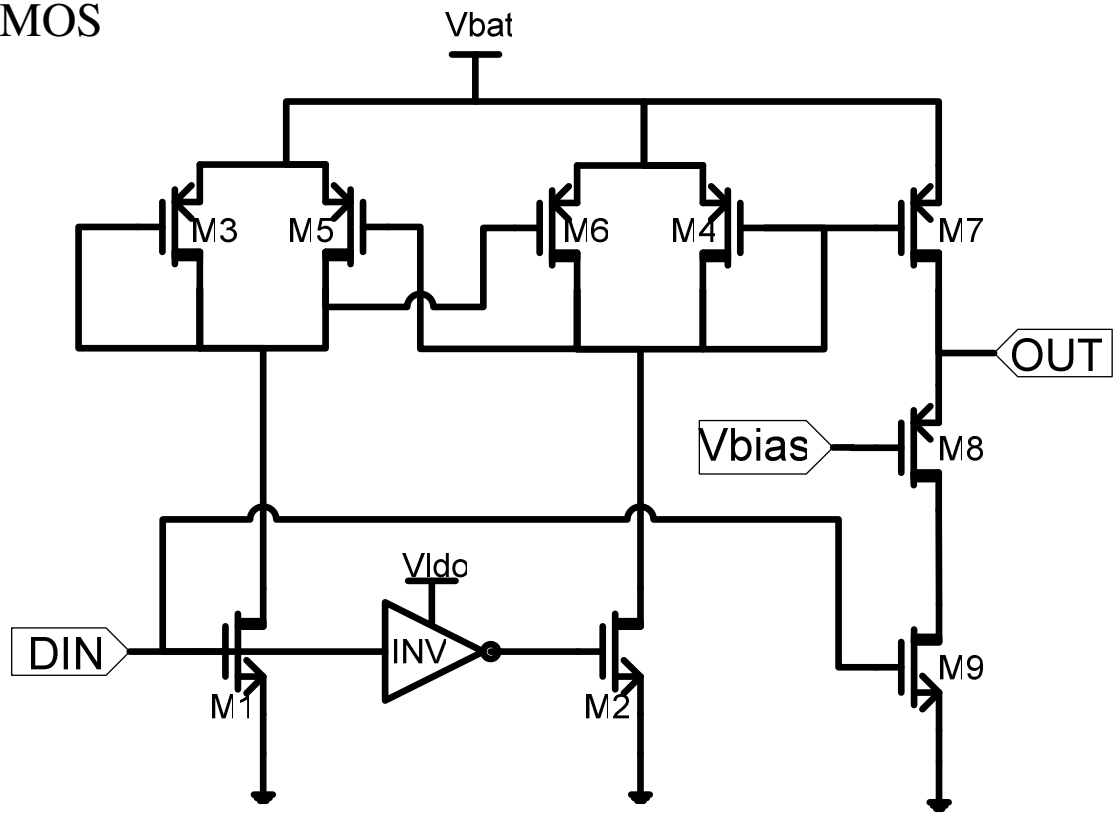
Half Bridge Circuits

- Timing Block
  - Shoot-through current
  - Output node glitches due to parasitic inductances
- Pre-drivers
  - Independent gate control
  - Reliability concerns
- Output Devices
  - Low leakage
  - Low R_{DSON}
  - Minimum Area
  - Reliability Concerns



Half Bridge: PMOS Driver

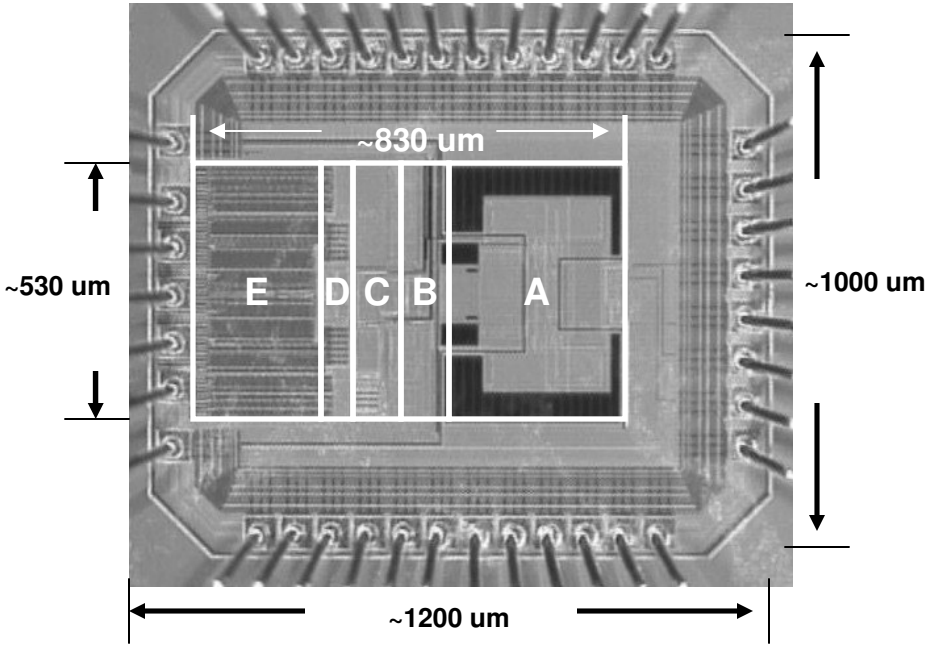
- Must Address reliability concerns and protect the gate of the Power PMOS device
- Minimal Propagation Delay
- Minimal Rise and Fall times
- Low Power
- Low Area



Class D System

- (A) – Loop Filter
- (B) – Comparator
- (C) – Ramp Generator
- (D) – POWER PMOS gate drive circuit
- (E) – Output MOSFET Devices

Die micrograph



Block Specifications

- ***Integrator***
  - DC Gain (amplifier)
  - Bandwidth (amplifier)
  - Noise
  - CMRR
  - THD
  - Power & Area
- ***Comparator***
  - Input Range
  - Gain
  - Noise
  - Propagation Delay
  - Rise & Fall time
  - Power & Area
- ***Ramp Generator***
  - Linearity
  - Noise
  - Amplitude
  - Frequency
  - Power & Area
- ***Bridge***
  - R_{DSON}
  - Propagation Delay
  - Rise & Fall time
  - Power & Area

Typical Specifications for Mobile Audio

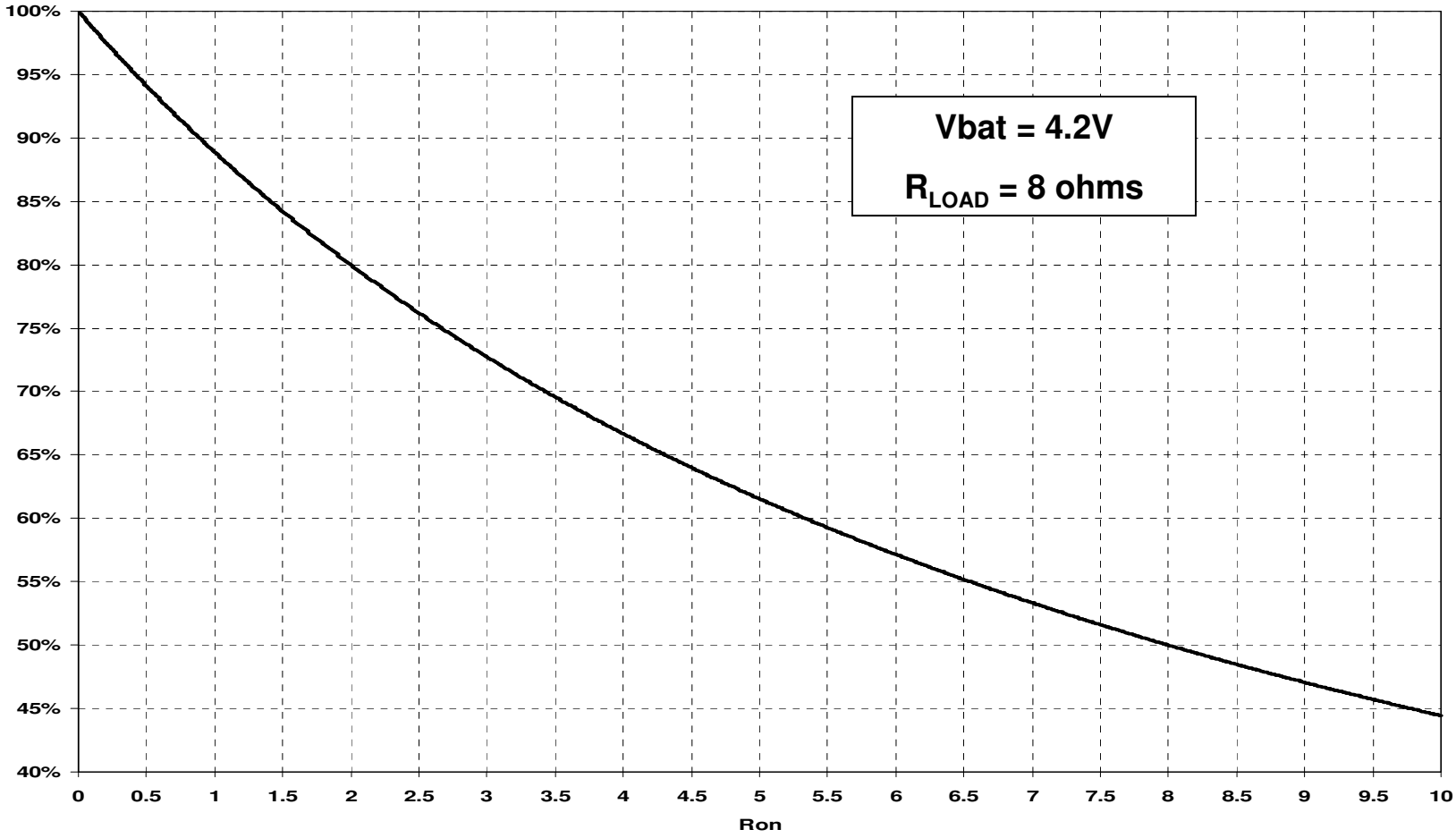
Function	THD (dB)	SNR (dB)	Power (mW)	PSRR (dB) @217Hz	Load (ohms)
MP3 Audio (stereo)	90	93	32 16	65	16 32
Polyphonic Ringer	60	76	500	65	8
Handset	60	76	500	65	8
Speaker Phone	60	76	500 1000	65	8 4!!!

More on Efficiency…

Non Ideal impacts on Class D Efficiency

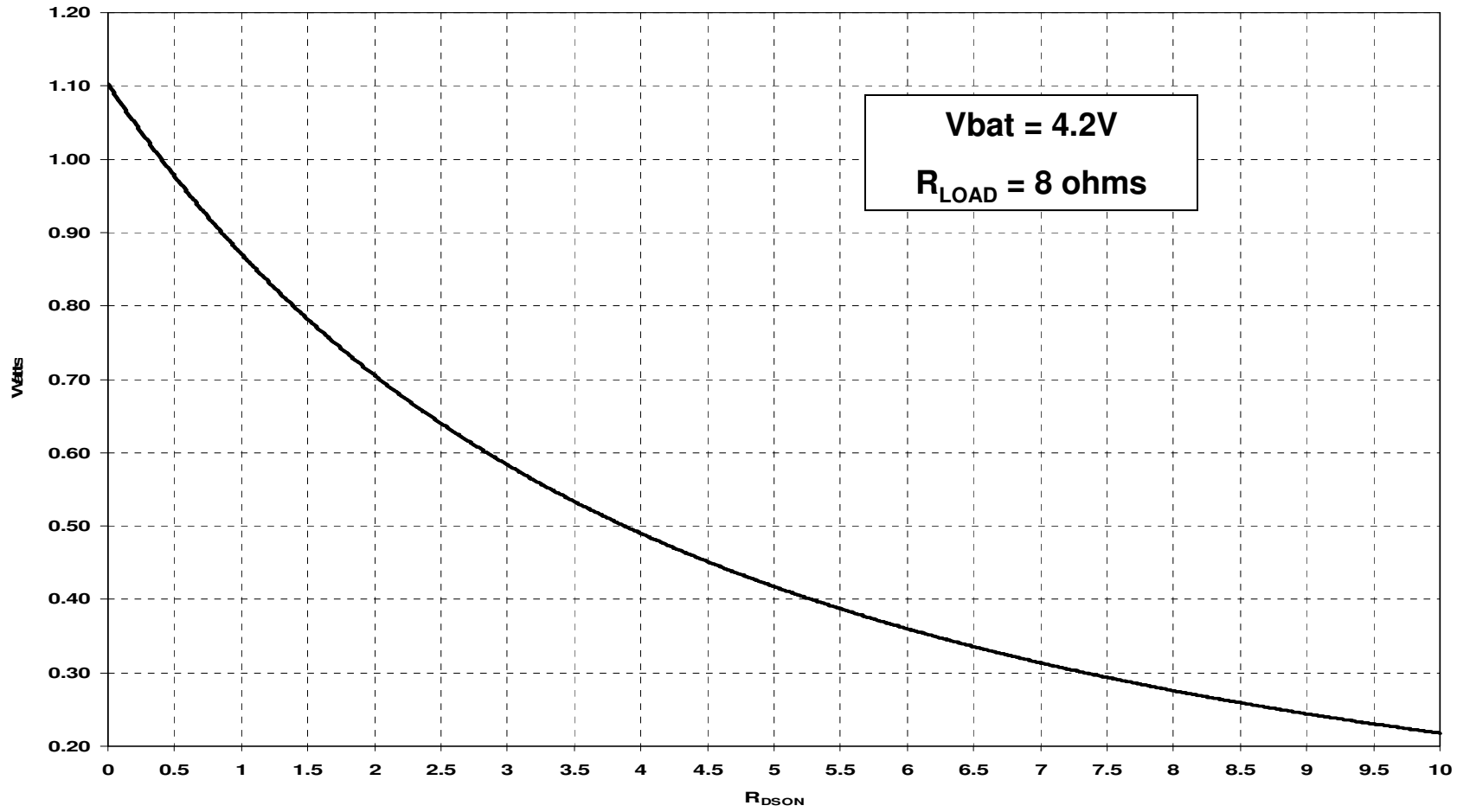
- Quiescent power
- Power MOSFET R_{DSON}
- Switching Current in the bridge
- Shoot Through current in the bridge
- Current in the MOSFET body diodes during switching due to package and load inductances
- Non-ideal supplies
  - Output Resistance of source
  - Board trace route resistance & inductance
- Trapezoidal wave form vs. Square wave
  - The rise and fall period will reduce the maximum Efficiency
  - Efficiency loss is proportional to $T_{Rise/Fall}/T_{Period}$
  - Exacerbated by small pulse widths at zero crossings

More on Efficiency (cont)



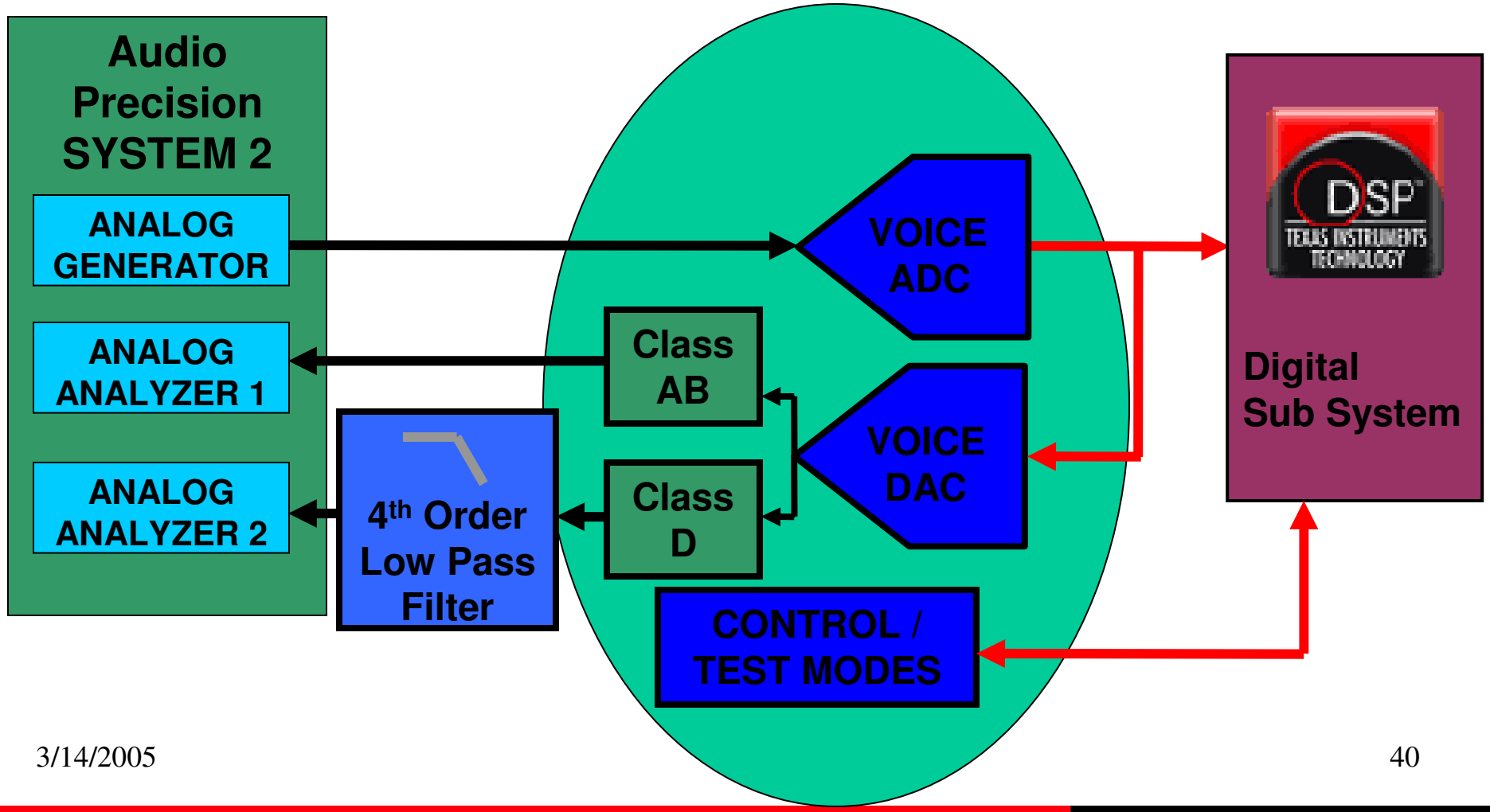
Effect of R_{DSON} on Power Efficiency

Delivered Power



Effect of R_{DSON} on Power Delivery capabilities

Testing Methodology



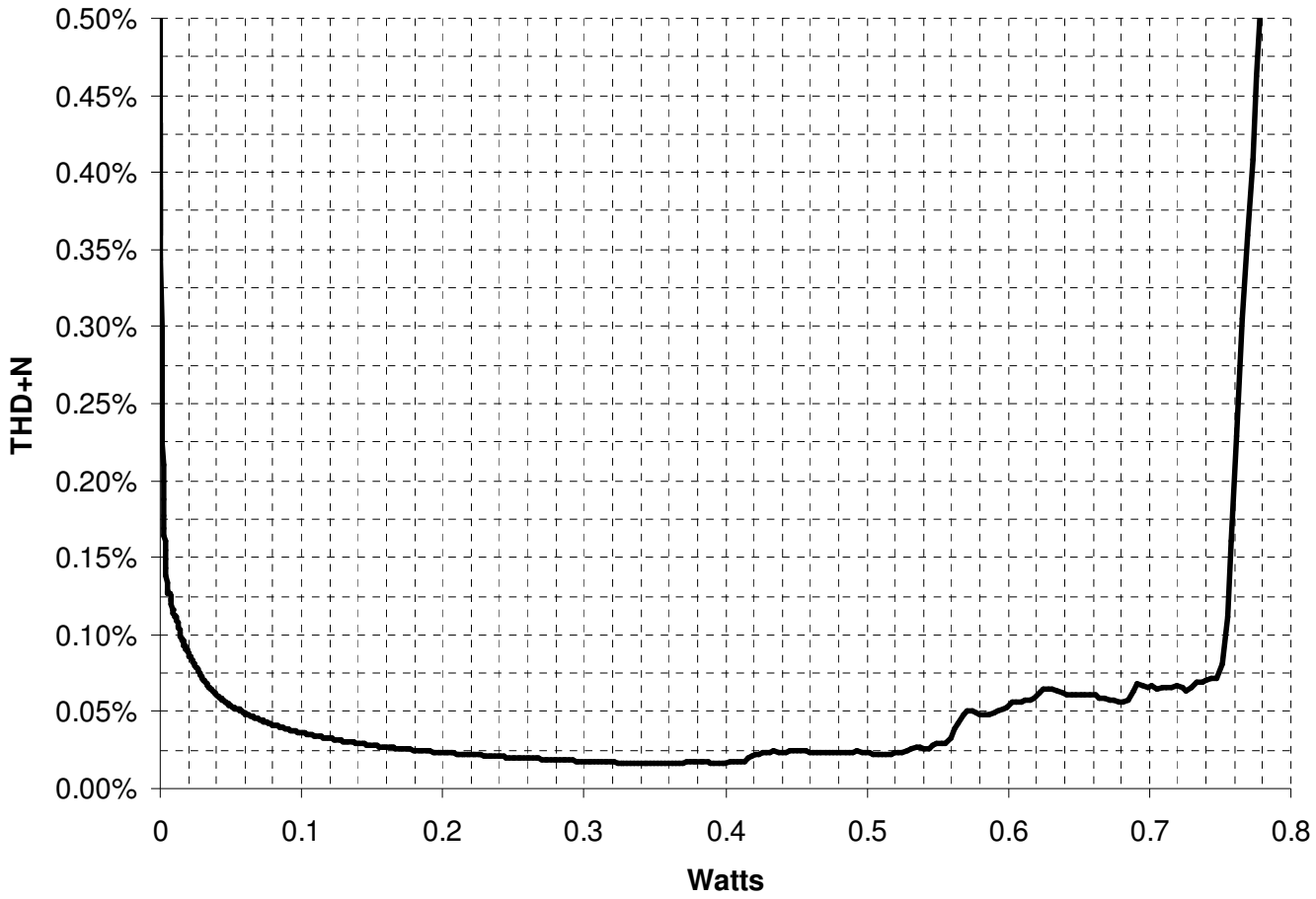
Testing Challenges

- Highly non-linear PWM characteristics create undesired out of band energies
- Provide clean references for device operation within the system
- Measure PSRR with heavy demands on the supply from class D
- Ensuring the *Reliability* of the devices under lab testing conditions
  - Proper power supply sequencing
  - Special care during debug situations
- Board design with special consideration to the current and power levels required by Class D
- Extra filtering for accurate capture of data compared to continuous time power amplifiers

Measurements

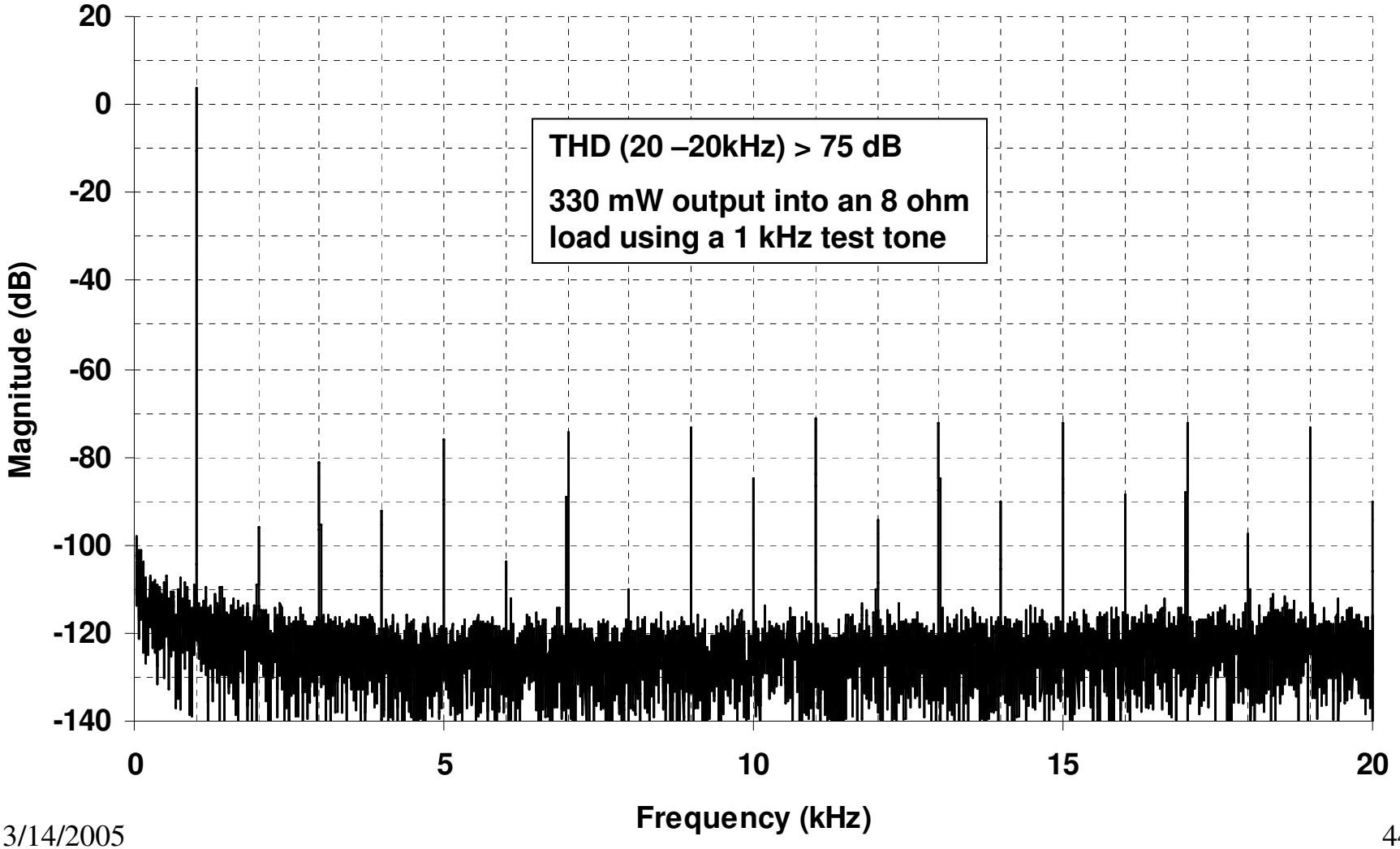
- Greater than 700 mW is delivered to 8 ohms
- THD Performance is better than 75 dB
- SNR Performance measured above 98 dB (referred to 1W)
- 75% Efficiency has been measured
- PSRR @ 217Hz is greater than 70 dB
- Power Supply Intermod of 217 Hz around 1 kHz output tone < -83 dBc
- Area is ~0.44 mm^2
- System functional with 2.4 V < $V_{battery}$ < 6 V

THD vs. Power Delivered



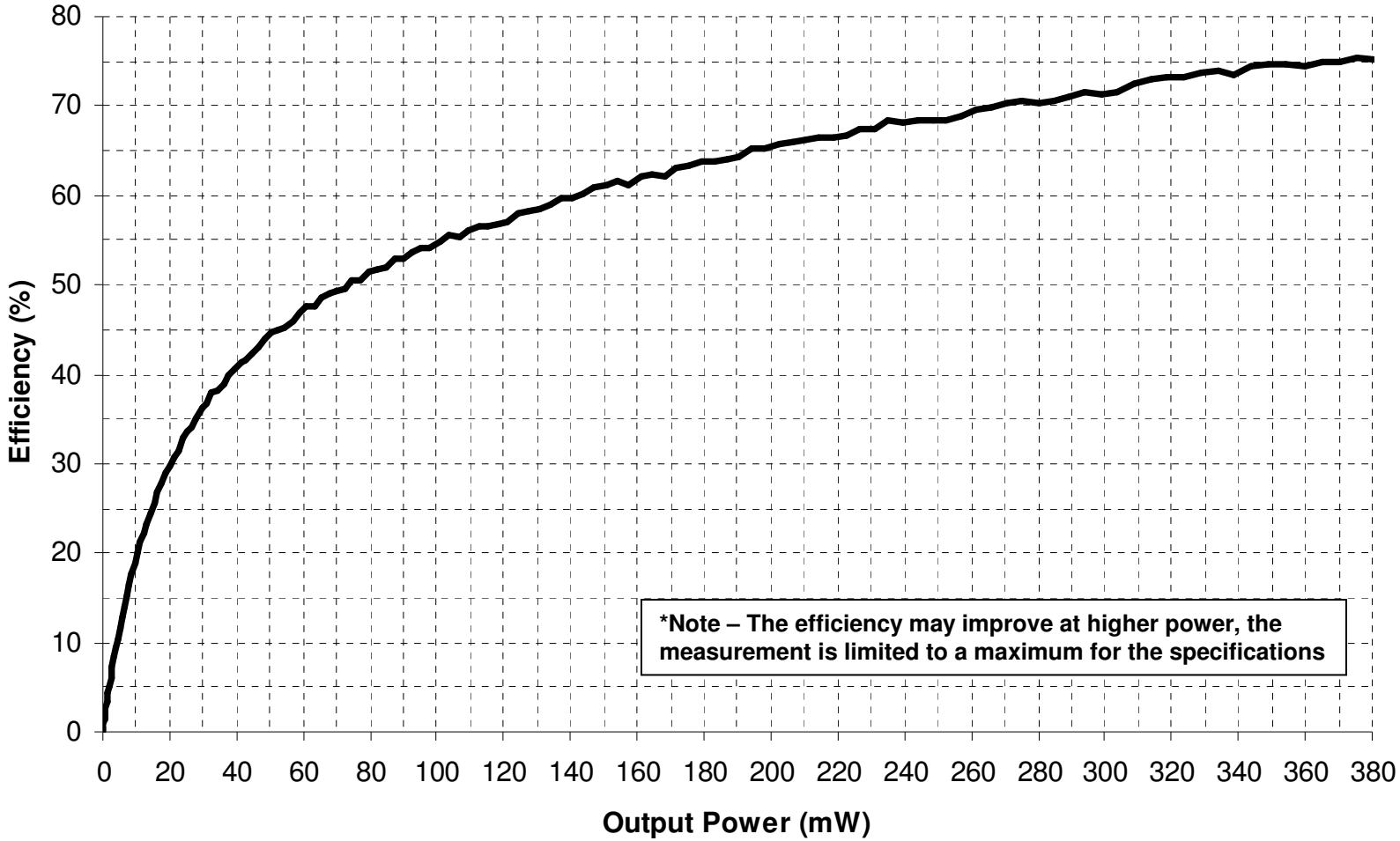
Peak performance measured from 20 –20kHz is >75 dB (< 0.02%) at ~300 mW using a 1kHz test tone

Full Power Spectrum

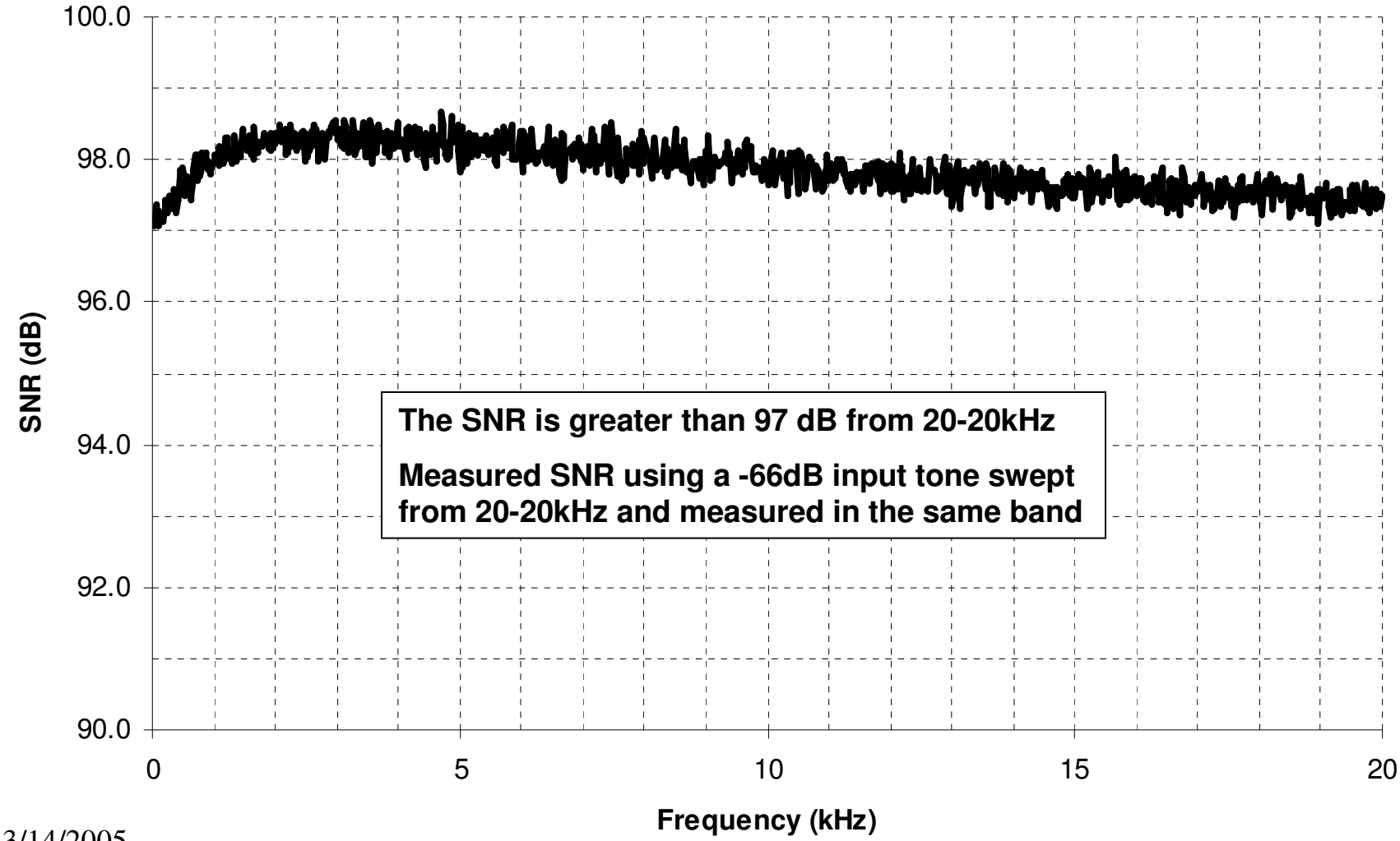


Efficiency vs. Power

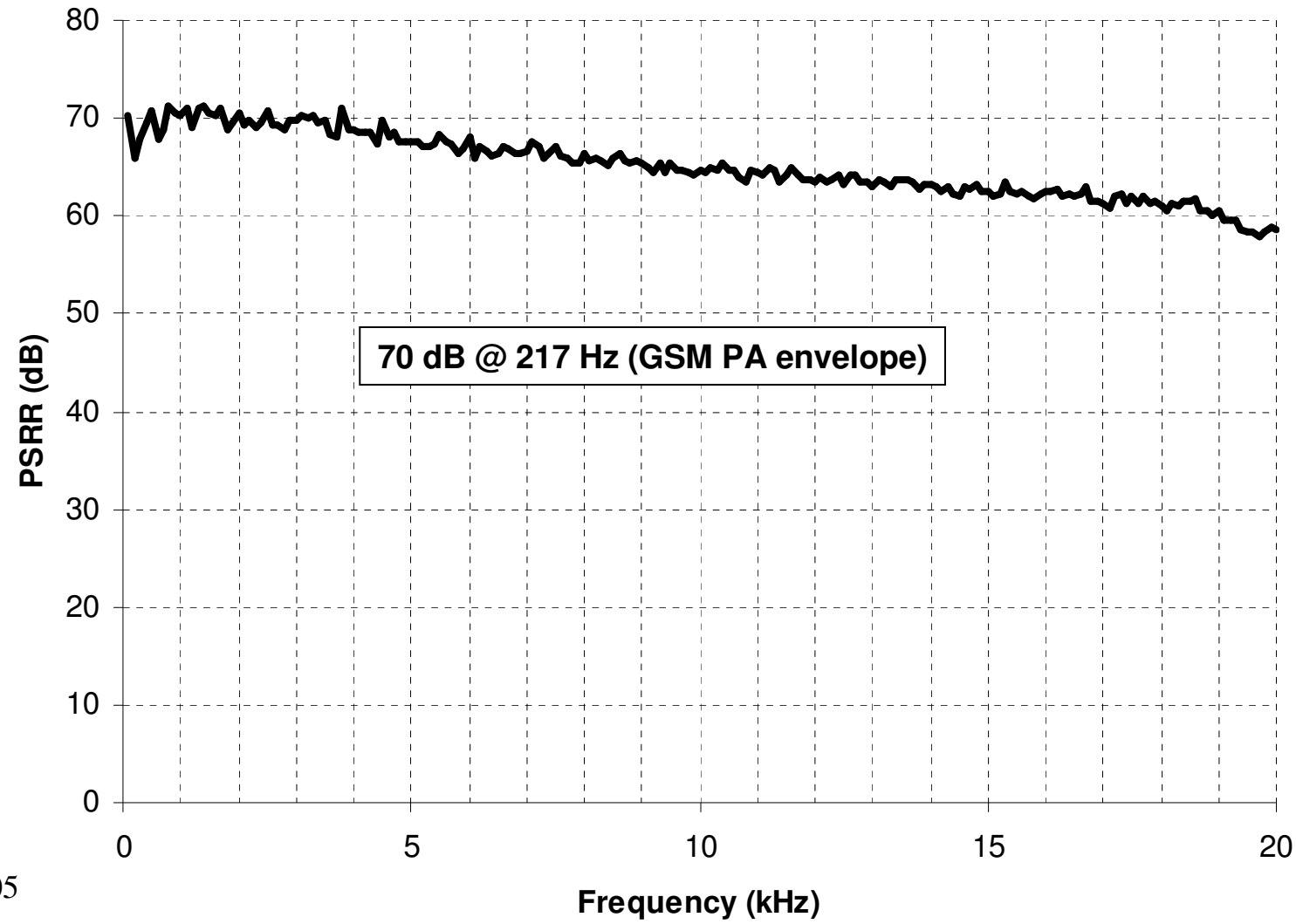
Efficiency of 75.5% is measured at ~380 mW using a 1kHz test tone*



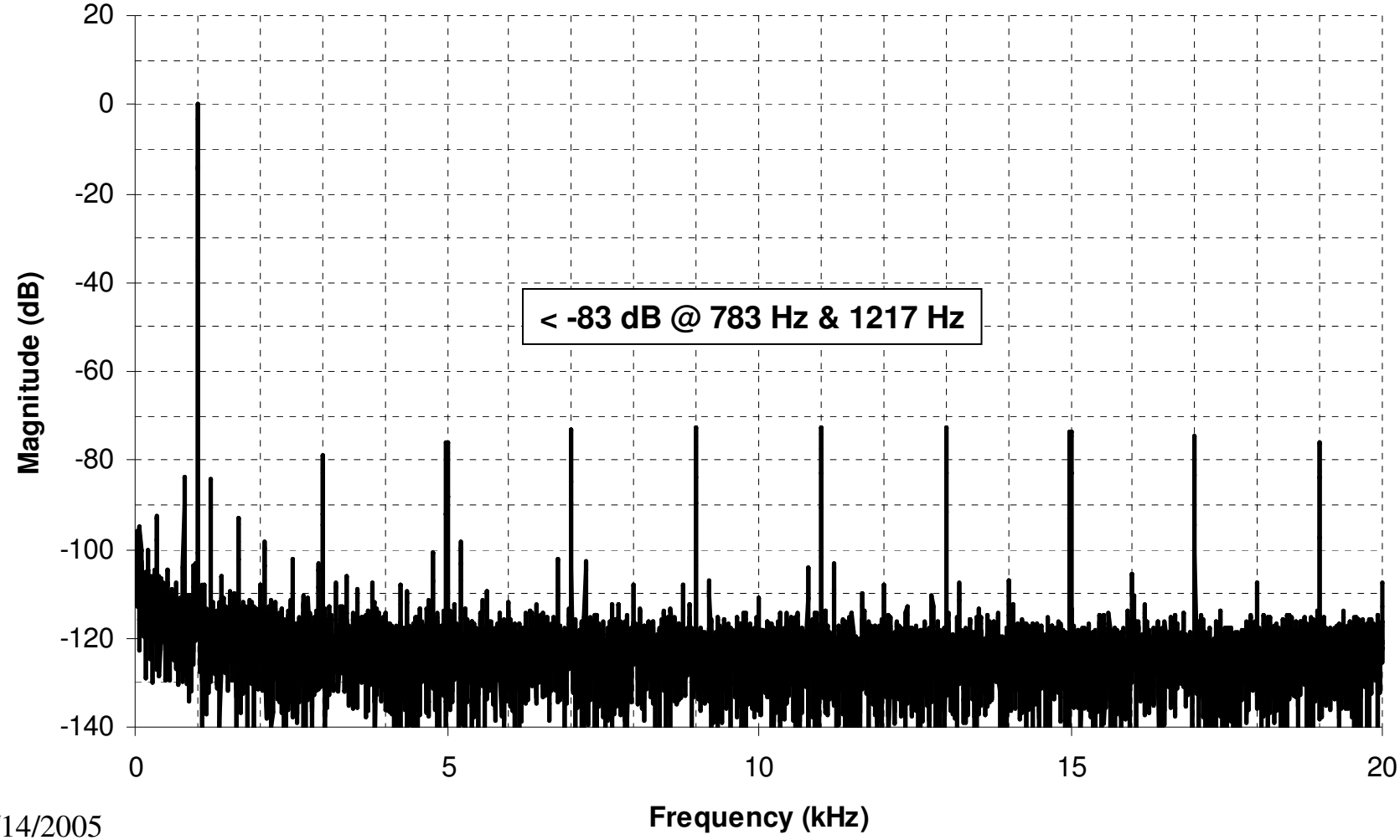
SNR vs. Frequency



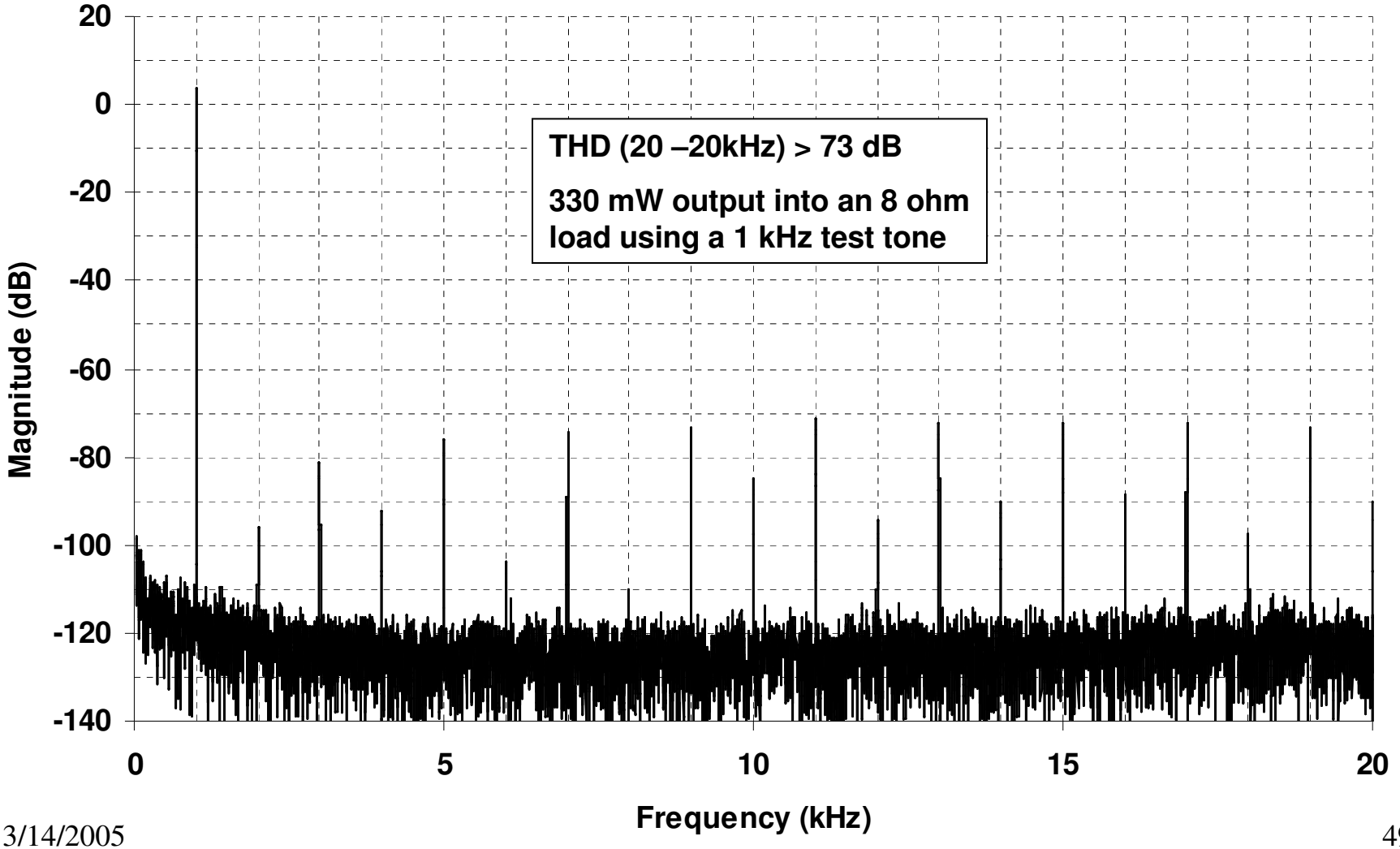
PSRR vs. Frequency



PS Inter-modulation Test Spectrum



PS Intermod Spectrum (No Disturbance)



Conclusion

- High Efficiency power amplifiers are essential to the future of Audio Enabled Mobile devices
- Integration of Audio Power Amplifiers provides cost efficient and flexible system partitioning options
- High efficiency & power Audio performance Class D amplifier has been demonstrated in 90 nm digital CMOS technology
  - 73 dB THD
  - 70 dB PSRR @ 217 Hz
  - 83 dB Power Supply Inter-modulation Rejection around Carrier
  - 93 dB SNR (referred to 330 mW)
  - 75% Efficiency
  - > 700 mW output
  - 0.44 mm^2

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