Highly integrated, re-configurable RF Receivers with an example of WCDMA, G/G/E receiver front-end without inter-stage SAW filter in 90nm CMOS

Naveen Yanduru
Texas Instruments Inc.
Outline

• The need for highly reconfigurable “multi-band, multi-mode” receiver.

• Multi-band receiver: Design directions and challenges.

• Multi-mode receiver: Architecture and design strategy for a reconfigurable receiver.

• A WCDMA, GSM/EDGE “multi-mode” RF receiver front-end in 90nm CMOS.

• Conclusion.
Plethora of wireless applications for the mobile terminal

**Voice, Data:**
- GSM/EDGE
- WCDMA
- WLAN
- WiMAX

- GPS
- Bluetooth
- DVB-H
Multiple bands across the frequency spectrum

GSM E GSM

DCS PCS IMT2K ISM

0.6G 0.8G 0.9G 1.6G 1.8G 1.9G 2.1G 2.4G 2.6G 3.5G 5.2G 5.8G

WCDMA

WiMAX

Bluetooth

WLAN (802.11a/b/g)

GSM/EDGE

DVB-H

GPS

Multiple receiver bands,
Mobile standards
MIMO/Diversity
Co-existence

Need for efficient receiver hardware re-use
Need for receiver hardware re-configurability

- Multiple Standards
- Duplex Schemes \((FDD/HFDD/TDD)\)
- Signal Bandwidths \((narrow\ band,\ spread\ spectrum)\)
- Modulation \((Amplitude\ with\ PAR,\ Phase\ only)\)
- Multiple Bands
- Highly Re-Configurable “Multi-Mode” Receiver
- True Software Defined Radio Receiver \((Multi-Band,\ Multi-Mode)\)
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Pre-Select Filter Bottleneck

- Pre-Select Filters (Duplexer/SAW/BAW) are band specific.

- Dedicated RX input pins, Matching Networks, LNA input stages are required.
Can we overcome this bottleneck?
High dynamic range RF ADC

• Nyquist rate as high as 10GHz.
• Dynamic range requirement of 100dB or more.

• Complete spectrum is converted to digital.
• A very powerful receiver!

• State of the art ADCs are not able to meet this required performance.
Integrated Tunable RF Bandpass Filters

- Dynamic range issues based on low Q of on-chip inductors.
- Issues with channel based tuning and tuning range.
- Input $g_m$ linearity is still an issue.

RF filtering using MEMS

- MEMS based RF filters using switchable capacitors for tuning have been shown.
- Low loss switches can be used to switch between various RF filters.

Issues with MEMS such as reliability, yield and complexities in integrating mechanical structures with transistors need to be considered.

The loss in the switch will degrade sensitivity.

Clock driven discrete time filtering after RF down conversion

Input linearity of the LNA and Mixer in the absence of any RF filtering needs to be addressed.


Discrete time analog filtering (cont.)

Switched Capacitor filter

- Advantages
  - Digital process friendly base-band filtering.
  - Easy programmability of base-band filtering between modes and for notches.

- Disadvantages
  - Main issue of linearity of LNA, mixer needs to be addressed.
Blocker cancellation RF Front Ends

- **Advantages**
  - Removes in-band and out-of-band blockers.
  - Relaxes linearity for the Mixer.

- **Disadvantages**
  - Mismatch issues with gain and phase inversion between the main and aux. path.
  - LNA linearity still a challenge,
  - Phase noise requirement is shifted to up-conversion mixer of Aux. path.


Some other approaches including blocker detection using fast RSSI and subsequent reduction in RF gain have been investigated.

But these schemes along with other schemes discussed are not able to match the RF performance of a receiver with pre-select filter.
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Direct Conversion as Receiver Architecture

Advantages:
- Reduced hardware (Image rejection/filtering, Signal processing, Synthesizer)

Issues:
- Second order inter-modulation/“self-mixing” issues with modulated blockers.
- Flicker noise.
- LO leakage and dc offsets.

A “Near-Zero or Low-IF” architecture can be used if image rejection requirements are not too difficult.
2\textsuperscript{nd} order inter-modulation distortion in direct conversion receiver

Figure showing IM2 distortion from modulated TX blocker in FDD mode.

Any modulated blocker with non-constant envelope (AM) causes this distortion.

Distortion in the presence of LO leakage in Direct Conversion Receivers (1)

$\omega_1 - \omega_2$, $\omega_2 - \omega_1$ at the output of the mixer looks like an IM2 component. *(Can misleadingly imply an IP2 issue!)*

**But really it is the LO leakage and IP3 that is the problem!**


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Distortion caused by an AM blocker will have similar issue like the two tone case shown earlier.
Performance re-configurability in RF front end

A high dynamic range RF Front End design without any inter-stage external filter is the starting point.

Need to be able to program this front end for various combinations of noise/linearity/power.

Need to have little degradation in overall performance between various programming modes.

Linearity/(Noise*Power) $\sim$ Constant

High Linearity mode – FDD mode, higher input signal conditions.

Low Noise mode – TDD mode, sensitivity conditions.

Low Power mode – high input signal, low level of blockers.
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A WCDMA, GSM/GPRS/EDGE “multi-mode” RF Receiver Front End in 90nm CMOS without inter-stage SAW filter
A tri-band WCDMA receiver with inter-stage SAWs
A tri-band WCDMA receiver *without* inter-stage SAWs
Advantages of SAW removal in a tri band WCDMA receiver

• Integration
  – Saves 3 SAW filters
  – 15 matching components
  – 9 pins on the IC
  – Board area

• More suitable for RX path to be configured as dual mode (WCDMA/GGE)
Input $IP2 = 2P_{TX} - P_{IM2} - \text{"Adj\_N"}$

Where,

$P_{IM2}$ is the input referred IM product;

“Adj\_N” is the adjustment factor which depends on no. of channels in the TX leakage

Linearity bottleneck in WCDMA receiver
- IIP3 from TX leakage, blocker

\[
\text{Input IP3} = \frac{(2P_{BLK} + P_{TX} - P_{IM3} + \text{"Adj\_N"})}{2}
\]

Where,

\(P_{IM3}\) is the input referred IM product;

"Adj\_N" is the adjustment factor which depends on no. of channels in the AM blocker.

Input \( IP3 = \frac{(3P_{\text{ADJ}} - P_{\text{IM}} + \text{“Adj\_N”})}{2} \)

Where,

\( P_{\text{IM}} \) is the input referred Spectral re-growth product;

“Adj\_N” is the adjustment factor which depends on no. of channels in the AM blocker.

### Key RF Performance Specifications

<table>
<thead>
<tr>
<th>RF Parameter</th>
<th>GGE Mode (GSM/GPRS/EDGE)</th>
<th>WCDMA Mode</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF</td>
<td>2.5</td>
<td>3.0</td>
<td>dB</td>
</tr>
<tr>
<td>IIP3</td>
<td>-18</td>
<td>-7</td>
<td>dBm</td>
</tr>
<tr>
<td>IIP2</td>
<td>40</td>
<td>44</td>
<td>dBm</td>
</tr>
<tr>
<td>Signal Bandwidth</td>
<td>0.2</td>
<td>3.84</td>
<td>MHz</td>
</tr>
</tbody>
</table>

- Higher LNA gain in GSM mode
- Adjust base band filter corner based on signal bandwidth
- Trade IP3 with current in GSM mode.
Receiver Block Diagram

Pros & Cons

• Pros
  + Design in 90nm CMOS
  + Highly integrated receiver

• Cons
  – Uses 2.4V supply for the mixer (rest of the chip uses 1.4V)
  – Use of bond-wire inductor for the tuned LC LNA load
LNA

Gain Control

Current/Linearity/Gain Control
RF Amp and Mixer

Current, Linearity, Gain Control

Signal BW Control

Output DC offset compensation circuit

VDD=2.4V

Rload

VDD=1.4V

LON

LOP

Mixer pole capacitor bank

VOUTP

VOUTM

VCM

VREF

VGP

VGC

VDD=2.4V

VCM

VGP

VDD=2.4V

Ls

VINP

VINM

M1

M2
VGA

Gain, Linearity, Current Controls

Signal BW Control

Gain, Linearity, Current Controls

VREF=VDDA/2
## WCDMA measured performance - Band III

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage gain</td>
<td>37.3 dB</td>
</tr>
<tr>
<td>NF</td>
<td>2.90 dB</td>
</tr>
<tr>
<td>In band IIP3</td>
<td>-10.8 dBm</td>
</tr>
<tr>
<td>Out of band IIP3 (CW blockers at TX and TX+47.5MHz)</td>
<td>-7.3 dBm</td>
</tr>
<tr>
<td>Out of band IIP3 (CW blockers at TX and TX-95MHz)</td>
<td>-3.75 dBm</td>
</tr>
<tr>
<td>Out of band IIP2 (2 CW blockers at TX freq.)</td>
<td>47.0 dBm</td>
</tr>
<tr>
<td>Parameter</td>
<td>Measured performance</td>
</tr>
<tr>
<td>---------------------------------------------------------------------------</td>
<td>-----------------------</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>37.3 dB</td>
</tr>
<tr>
<td>NF</td>
<td>2.90 dB</td>
</tr>
<tr>
<td>NF under blocking (3MHz blocker at -23dBm), includes reciprocal mixing</td>
<td>8.64dB</td>
</tr>
<tr>
<td>IIP3 (blockers at 800kHz and 1600kHz offset)</td>
<td>-10.8 dBm</td>
</tr>
<tr>
<td>IIP2 (self-mixing of blockers at 6MHz offset)</td>
<td>44.0 dBm</td>
</tr>
</tbody>
</table>

**GGE measured performance – DCS band**

## More Measured performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>S11</td>
<td>-14 dB</td>
</tr>
<tr>
<td>Output DC offset (after correction)</td>
<td>50 uV</td>
</tr>
<tr>
<td>Gain imbalance (WCDMA)</td>
<td>0.4 dB</td>
</tr>
<tr>
<td>Gain Imbalance (GGE)</td>
<td>0.3 dB</td>
</tr>
<tr>
<td>Phase imbalance (WCDMA)</td>
<td>4°</td>
</tr>
<tr>
<td>Phase Imbalance (GGE)</td>
<td>1°</td>
</tr>
<tr>
<td>Out of Band IIP2 (WCDMA) (CW blockers at RX+TX and TX)</td>
<td>34.7 dBm</td>
</tr>
</tbody>
</table>
VGA voltage gain curve

Voltage Gain vs VGA Gain Setting

RX Voltage Gain [dB]

VGA Gain Setting [dB]

-14  -12  -10  -8  -6  -4  -2  0  2  4  6  8  10  12

LNA High Gain Mode

LNA Mid Gain Mode
NF vs. VGA Gain Setting

VGA Gain Setting [dB]

NF [dB]

-14 -10 -6 -2 2 6 10

LNA High Gain - NF
LNA Mid Gain - NF
Measured spectral re-growth based on number of channels in adjacent channel

- High PAR/increase in channels in adjacent channel will cause increased spectral re-growth.
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Conclusion

- The need for “multi-band, multi-mode” receivers to support SDR is highlighted.

- Multi-band receiver: Various approaches and directions in trying to achieve this goal are presented.

- Multi-mode receiver:
  - A multi-mode receiver front end in 90nm CMOS is presented.
  - The high performance achieved eliminates the need for inter-stage SAW filter.

- Once a clear winner showing the performance and requirements for multi-band receiver emerges, we will have the RF receiver for SDR.
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References


