

Components, Packaging, and Manufacturing Technology Society



Newsletter

The Global Society for Microelectronics Systems Packaging



Vol. 25, No. 1, March, 2002 (ISSN 1077-2999)

www.cpmt.org
www.enh.ieee.org/soc/cpmt/newsletter

President's Report: 2001 year-end review

2001 was a difficult time for many of us given recent economic challenges not only in the U.S. economy but throughout the world, as well as the events of September 11th. Despite these, the CPMT Society has enjoyed continued growth and improvement. Hundreds of volunteers have been working hard throughout the year to continue providing value to CPMT Society members in the areas of conferences, workshops, publications, short courses and chapter activities.

I want to thank each and everyone of the volunteers for their dedication to our Society.

Recent Accomplishments

****Start of Student Branch Chapters**: The first two CPMT Student Branch Chapters have been formed at the Georgia Institute of Technology, Atlanta, Georgia USA and in Romania. The Student Branch Chapter in Romania consists of students from several different institutions and reports to the IEEE Romania Student Branch, which, in turn, reports to the IEEE Romania Section. Efforts are underway to establish additional Branch Chapters at the University of Arkansas and in Malaysia and China.

****Global Membership Growth**: Global membership has grown to over 4100 -- close to a 7% increase over the year 2000 -- making CPMT one of the fastest growing Societies in IEEE.

****Implementation of Electronic Manuscript Submission System**: Our CPMT Transactions (Components and Packaging Technologies; Advanced Packaging; Electronics Packaging Manufacturing) are all operating through the new IEEE Manuscript Central for electronic manuscript submission and review process management. Early indications already confirm that this system will significantly speed up the time from manuscript submission to publication.

****Development of Marketing and Public Relations Campaign**: Work is underway to better position our Society as the leading global professional organization in the field by building stronger brand identity and global recognition. Professional expertise has been brought in to assist in the development of effective marketing and communication programs, as well as media outreach.

****Awards Program Changes**: Changes have been implemented in our Awards Program to better recognize the achievements of our members and outstanding contributors in our technical fields. In the past, most of these recognitions have been from within the US. A new award has been established to recognize outstanding technical achievement; cash prizes for all awards have been increased; a major new IEEE-level Technical Field Award has been approved by the IEEE Society.

****CPMT Joins IEEE Sensor Council and Nanotech Committee**: The CPMT Society has become a member of two new IEEE Technical Councils/Committees: the Sensors Council and the Nanotechnology Committee. By virtue of this membership, CPMT Society members are eligible to subscribe to Sensors Journal and Transactions on Nanotechnology at low member rates.



**Rao Tummala,
President of
CPMT Society**

**Professor at
Georgia Institute
of Technology**

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 Joe Brewer, 904 445 8971
 Membership--Ralph Russell, email:
 cpmt-membership@ieee.org
 Chapter Development--R. W. Russell, II,
 cpmt-membership@ieee.org
 Nominations--John Segelken, 1 540 633 5781

**Next News Deadline:
 June 5, 2002**

CPMT SOCIETY NEWSLETTER

EDITOR	PUBLICATIONS VP	TRANSACTION EDITORS:
David W Palmer Org 1716, MS0874 Sandia National Lab P.O. Box 5800 Albuquerque, NM 87185 505 844 2138 FAX 844 7011 d.palmer@ieee.org	Paul B. Wesling Compaq Computers 10435 N. Tantau Ave CAC07-38 Cupertino, CA 95014 408 285 9555 p.wesling@ieee.org	Avram Bar-Cohen, editor Part A University. of Minnesota 111 Church St SE, ME Dept Minneapolis, MN 55455 612 626 7244, Fax 612 624 1398 Peter Krusius, editor Part B EE Department, Cornell University . 607 255 3401, fax 607 255 4777 Walter Trybula, editor Part C 512 356 3306, w.trybula@ieee.org

Composition and Layout: Alina Deutsch — Proofreading: S. Puccetti

International Relations-- Leo Feinstein, 508 870 0051; Europe:Ephraim
 Suhir, 908 582 5301; Far East: W. T. Chen, 65 874 8110
 Joint Committee on Semiconductor Manufacturing--G. C. Cheek

Technical Committee Chairpeople

TC-1 Electrical Contacts, Connectors and Cables--
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 TC-2 Discrete and Integral Passive Components—
 Leonard Schaper, Univ. of Arkansas, 1 501 575 8408
 TC-3 IC and Package Assembly – Dan Baldwin, 1 404 894 4135
 TC-4 Manufacturing Design & Process—Walt Trybula, 1 512 356 3306
 TC-5 Materials--Rajen Chanchani, 1 505 844 3482
 TC-7 Environmental Stress & Reliability Test--Kirk Gray, k.a.gray@ieee.org
 TC-8 Semiconductor Processing & Manufacturing--John Reekstin,
 714 762 5077; Court Skinner, 1 408 453 9460
 TC-9 Thermal Management & Thermomechanical Design--
 Tony Mak, 1 972 371 4364
 TC-10 Fiber Optics & Photonics—Frank Shi, email: FGSHI@uci.edu
 TC-11 Electrical Test -- Bruce Kim
 TC-12 Electrical Design, Modeling and Simulation--
 Madhavan Swaminathan, 404 894 3340
 TC-13 Power Electronics Packaging--Doug Hopkins, 607 729 9949
 TC-14 Systems Packaging—Lisa Pallotti, HP, 1 972 497 4127
 TC-16 RF and Wireless-- Craig Gaw, 602 413 5920
 TC-17 MEMS and Sensor Packaging—Eric Jung, email: erju@izm.fhg.de
 TC-18 Wafer Level Packaging—Luu Nguyen, 1 408 721 4786
 TC-19 Education--Rao Tummala, 404 894 9097
 TC-21 Green Electronics Manufacturing and Packaging, Hansjoerg Griese.
 Email: griese@izm.fhg.de
 TC-22 Contract Manufacturing, Srinivas Rao, Solectron, 1 408 956 6478

Representatives

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 AVS--James Morris, 1 607 777 4774
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****IEEE Components, Packaging, and Manufacturing Technology Society Newsletter is published quarterly by the Components, Packaging, and Manufacturing Technology Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. \$1.00 per member per year (included in Society fee) for each member of the Components, Packaging, and Manufacturing Technology Society. Printed in U.S.A. periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE CPMT Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved, copyright (c) 2002 by the CPMT Society of IEEE. Authors and Artists given full permission for further use of their contributions. This Newsletter was printed in the U.S. of America. For circulation information call IEEE customer Service 908 981 1393, or FAX 9667.

Sand in their Shoes: Your Board Meets in Florida

Nothing could stop the CPMT Board of Governors from leaving the cold of the winter and the drought of El Nino to meet in the warm rain of West Palm Beach Florida. The meeting continued the Board's focus on strategic investments in our Society's future.

President Rao Tummala welcomed the new members-at-large to your board: Rolf Aschenbrenner, Rao Bonda, Rajen Chanchani, Corey Koehler, Connie Swager, and Naoaki Yamanaka. Rao restated the CPMT vision to clearly become THE global society for our technologies.

He then announced several new appointments:

Constitution and Bylaws Chair -- Tony Mak
TC-10 Optoelectronics & Photonics Chair -- Frank Shi
TC-17 MEMS & Sensor Packaging Chair -- Eric Jung

Rao also announced continuing leadership roles for

Ron Gedney -- Secretary
Merrill Palmer -- Treasurer
Technical -- Phil Garrou
Global Chapters -- Ralph Russell
Global Awards -- John Segelken
Publications -- Paul Wesling
Vision Statement -- Rao Tummala
Conferences -- Jim Morris
Education -- Al Puttlitz
Student Programs -- Bill Brown
Industry Programs -- John Stafford
CPMT Marketing -- Connie Swager
ECTC & CPMT Liaison -- C. P. Wong

Rao has a reserve platoon of 6 Board members for new assignments: Alina Deutsch, Corey Koehler, Johan Liu, Koji Nihei, Ephraim Suhir, and Naoaki Yamanaka.

"Our challenges are before us with the Global Economic Downturn that has particularly hit the technology companies of our members, and the Central IEEE financial red ink which is quickly draining CPMT's financial reserves. These reserves are a measure of our ability to strategically invest. However, we still have the momentum of many accomplishments on our side."

- *Established 26 CPMT Chapters around the world
- *Started 2 Student chapters
- *Grown to 4122 global members
- *5 Archival publications
- *28 Global conferences and workshops
- *46 Years of publications on 9 CD-ROMS
- *18 Technology & Education committees
- *125 IEEE Fellows
- *1 Nobel Laureate

As part of the move to strengthen chapters, **Ralph Russell**, Chair of Chapter development, has begun accepting Mentors for each of the existing Chapters. A Mentor is a Board member that can easily bring CPMT knowledge, networking, and resources to their Chapter. In a flurry of volunteers, 25 Chapters now have at least 1 mentor.

C. P. **Wong** described the success of several Asian and European meetings.

* APAC 2001 in August at Beijing China served 120

* First International Adhesives Conference in Potsdam Germany reached 140
* EMAP in November in Seoul Korea worked for 90
* APACK in December at Singapore served 90
* There was a 30 year IEEE Chapter celebration in Hong Kong in December

Treasurer Merrill Palmer clarified the lien that Central IEEE has on our Society funds and how the TAB is trying to wean the IEEE administrative establishment from this easy money. He also discussed the valuable income from the CPMT share of the IEEE Book Broker Program. Adding subsequent data, Merrill showed income of

1997 -- \$62K
1998 -- 79
1999 -- 144
2000 -- 143
2001 -- 219
2002 -- \$250K (est.) (definitely not small potatoes)

The upcoming ECTC event was discussed from many angles. There is a great selection of papers with the need to have 5 or 6 simultaneous sessions. There will be 2 poster sessions and 14 short courses. The Board must help get the word out on this meeting to the members, particularly in the face of the uncertain world economy. President Tummala took on as an action item the forging of a stronger continuing partnership with the ECA for the benefit of future strong ECTCs.

There was some confusion as to the projected Transaction budgets in 2002, which Merrill Palmer agreed to nail down. VP **Paul Wesling** is open to suggestions for the soon to be open Transaction Editor position. (On March 18 Paul announced the new Editor, see article.)

Since CPMT Chapters often initiate their own local and international meetings, Chair Ralph Russell will work to incorporate these events into our CPMT website calendar. Our members need more advanced notice to make distant meetings and avoid conflicting CPMT schedules.

In a similar effort to keep the full strategic force behind CPMT meetings, **VPs Phil Garrou and Jim Morris** will coordinate our TC contribution to each CPMT meeting.

Ellen Lepper of Potomac Communication Group will provide Power Point Templates for all CPMT Society presentations. This will help build brand identification for our multi-armed activities to our many members and potential members. They see us but they don't see us.

Chair Ralph Russell reported that the CPMT was the fourth fastest growing Society among the 31 societies in the IEEE last year. We have 4122 members. He agreed to report on the recent membership growth by global region. This information should help the Board direct meeting places and lecturers in an optimal way.

Rolf Aschenbrenner and Johan Liu led a discussion on the meeting plans in Europe for 2003 and beyond.

VPs Phil Garrou and Al Puttlitz led a lively discussion on increasing the number of CPMT distinguished lecturers perhaps by tapping into the 125 active IEEE Fellows in our Society.

Phil and Naoaki Yamanaka also agreed to find a Chair for TC-6, our High Density Circuit Board Committee. This important position has been vacant too long. Phil is also constantly leading the debate on expanding and consolidating the number of Technical Committees. A proposal is on the table

for an Optical System Performance TC; everyone not back at the snack table gave vigorous opinions.

Bill Brown, Chair of Student Chapters, is following up on the status of Hong Kong Branch Chapter formation. Paul Wesling has agreed to help Bill establish a CPMT website for students.

VP Anthony Chan and Executive Director Marsha Tickman again pulled off the complex logistics needed to handle these important Board meetings. Our thanks to them and everyone who attended.

■ Submitted by the Fly on the Wall



Treasurer's Report

In 2001 CPMT had total revenue of \$1,495K and total expenses of \$1,497K, for a net operating loss of <\$2K>. However, CPMT financial reserves will be reduced by approximately \$965K due to long-term unfavorable returns on investments in 2001 and the allocation to CPMT of our share of the approximately \$30,000K Institute-level operating deficit for the year. Still, CPMT starts 2002 with over \$2,000K total financial reserves.

CPMT Publications and Conferences netted \$432K and \$328K, respectively, in 2001, compared with total dues income of just over \$33K. Overall interest and investment income was \$162K net loss due to loss in market value of long-term investments. CPMT Executive Office and Committees expenses were just over \$447K for the year, which is \$119K less than was budgeted. Expenses during the year included \$114K for a major marketing initiative to increase CPMT visibility, recognition, and interest throughout the world. The CPMT share of 2000 Technical Activities Board expenses was \$50K.

The approved CPMT budget for calendar year 2002 deficit is \$362K after absorption of \$563K in charges for IEEE Institute-level expenses. Projected 2002 CPMT income is \$1,654K, with expenses of \$1,453K prior to the Institute-level charge. This budget assumes net income of \$432K net from publications and \$384K net from meetings and conferences, both of which may be optimistic unless the economy improves significantly. The 2002 budget continues existing programs and services, emphasizes completing the marketing program implementation, funds student programs and international programs, and staffs electronic processing of Transactions papers.

The year 2003 budget is now being prepared.

Recommendations for projects or programs to provide increased value to members, or of efforts to discontinue, are invited to be submitted to CPMT officers during March and April 2002.

There is continuing great concern among CPMT officers about Institute-level and Infrastructure deficits. These have been ongoing for several years but prior to 2000 were paid from now-depleted Institute reserves and the investment income generated by those reserves. 2000 was the first year that Societies and other sub-entities with reserves had those reserves taxed to cover the Institute budget deficit. Due to stock market reverses, the "hit" for 2001 will be even worse than for 2000. However, over \$3.5.M was cut from IEEE corporate expenses during 2001 and efforts continue to further reduce these costs. The overall IEEE budget for 2002 is balanced.

■ Merrill Palmer, CPMT Treasurer

MEMBERSHIP & CHAPTER DEVELOPMENT REPORT

Thanks are extended to all CPMT members for helping make 2001 a fabulous year for recruiting new members. The CPMT was the 4th fastest growing IEEE Society in 2001 with a growth rate of 5.7%. We currently have more than 4122 members.

New membership initiatives launched to promote "value" of membership (timed for the 2002 membership cycle) include:

- ** New and returning member welcome kits that include membership cards, member lapel pins, and revised brochures
- ** Recognition items such as luggage tags to raise the visibility of the CPMT "brand"
- ** Print ads that extend the reach of our core membership messages

We now have 35 global CPMT Society Chapters. Twenty-four of these chapters are outside of the USA. New initiatives to facilitate the start-up of new chapters, improve access to existing chapter resources and encourage Chapter of the Year award participation include:

- ** Redesign and configuration of the Chapter section of the CPMT web site at <http://www.cpmt.org>
- ** New homepage template for local Chapter highlights
- ** Updated Chapters directory

The CPMT Society is the premier forum for today's leading professionals engaged in the design, development and manufacturing of advanced microsystems packages. Invite your colleagues to join us.

■ Ralph W. Russell, II
Director, Global Chapters and Membership.



THE MOST-REQUESTED CONFERENCE PROCEEDINGS

Some of us are fortunate enough to be able to attend one or two IEEE conferences each year, to meet again with technologists in our specialties and hear first-hand about the latest developments.



Still, you can't get to them all, and some developers are restricted, for financial reasons, to only attending local events.

The CPMT Society has three ways for you to obtain the published papers for the other dozen symposia you would have LIKED to attend this year:

First, many of these books (and CDs) are on the CPMT website:

www.cpmnt.org/proceedings/. There you'll find volumes for sale going back, in some cases, for 15 years. This site is great for North America orders, or for non-NA engineers who can send a personal or company check (we aren't set up for credit cards).

Second, for recent Proceedings (say, since 1998), you can easily purchase them from the IEEE's website: shop.ieee.org. You can use a credit card here, and (from North America) you can use their toll-free number: +1-800-678-IEEE. Ordering and shipping is quick and easy.

Third, if you spot a reference to a paper from one of our conferences, and would like a copy of it, IEEE has their "ASK*IEEE" service which will retrieve any particular paper (or list of them) for a nominal charge, and either mail or FAX it/them to you. More information is on their website: www.ieee.org/services/askieee/.

So, which Proceedings are the "most-requested" ones? Over the past several years, the two "winners" are those from the ECTC and from SEMI-THERM. Many people order the past three or four years of ECTC (probably engineers or librarians who has JUST discovered this conference), and the "recent-10-years" package from SEMI-THERM is a hot seller. Next conferences (in number of shipments) are I-THERM, IEMT, and ICT.

New books that are recently in stock: the EMAP (Electronic Materials and Packaging) 2001, held recently in Korea, with 5 keynote talks and 75 papers covering the spectrum from materials to packaging and reliability, and the ICT (Int'l Conference on Thermoelectrics) for 2001 in Beijing has been shipping since January.

You can help share technology developments within your company. Have your librarian or department administrator order useful or missing volumes, for your staff's use. This allows you to protect your private copy for your OWN use!

■ Paul Wesling, CPMT Vice President

TC-1 Upcoming Meetings

48th IEEE Holm Conference on Electrical Contacts

Oct 21-23, 2002 Holiday Inn International Drive, Orlando Florida.

2002 Intensive Course on Electrical Contacts

June 10-13, 2002 at Omni Shoreham Hotel, Washington, D.C.

Both are CPMT TC-1: Electrical Contacts sponsored events.

Details of both can be found on our website

www.ewh.ieee.org/soc/cpmt/tc1/

Chi H. Leung, AMI DODUCO

cleung@amidoduco.com

Power Electronics Packaging committee Meets at APEC

The Power Electronics Packaging Committee met on 12 March during the IEEE Applied Power Electronics Conference (APEC) and discussed future initiatives. At the present the committee supports solicitation of papers for the major society conferences and initiates a workshop every other year. The meeting focused on initiating the next International Workshop on Integrated Packaging in 2003. Both the Power Electronics Society (PELS) and Components, Packaging and Manufacturing Technology Society (CPMT) were financial sponsors of the previous two workshops and expressed support for the third.

A second discussion focused on committee direction and meeting the future needs of those involved in packaging. Power electronics packaging has evolved as a commonly recognized concurrent part of power electronics design, and both the electrical and packaging designers have equal interest. The committee will split its strategies and have distinct foci on technology and applications. This is envisioned as closer affiliation between PELS and PSMA (Power Sources Manufacturers Association) to meet the needs of electrical design engineers.

The committee is greatly interested in new members. Due to shifts within companies, committee membership has varied substantially. If you are interested in being an active committee contributor or just an observer (an 'activist in waiting'), please contact Dr. Hopkins at D.Hopkins@IEEE.Org and make your preference known.



Prof. Douglas C. Hopkins,
SUNY – Buffalo
CPMT Chair TC-13

2002 IEEE Systems Packaging Japan Workshop

The 2002 IEEE Systems Packaging Japan Workshop was held February 4-6 at the NTT Musashino R&D Center just west of Tokyo. Despite the poor economic conditions, the workshop was highly successful, with 86 professionals in attendance. The workshop was held in English for the benefit of all foreign visitors. Following are just a few highlights of this informative workshop.

The workshop began with keynote speaker Hisao Kasuga of NEC discussing packaging technology in the future, particularly the JISSO roadmap. JISSO is the Japanese acronym for a total solution for interconnecting, assembling, packaging, mounting, and integrating system design. The roadmap projects extensive development of stacked 3-D structures, both with ICs on flex as well as ICs stacked directly, sometimes with through vias. Many of the same arguments heard in the US for SiP (system in package) v. SoC (system on chip) were presented.

The High Performance Systems Packaging session is always a highlight of these workshops, and this was no exception. Hubert Harrer, of IBM Böblingen, described the packaging of the Z Series 900. The large MCM supports 35 chips and handles 1300W. For the first time there was a direct comparison between an IBM-produced module, with 101 glass ceramic and 6 thin film layers, with a Hitachi-produced module, with 84 glass ceramic layers. Hitachi was able to eliminate thin film and save ceramic layers because of finer design rules (297 micron pitch v. 396.)



Len Schaper presents plaque of appreciation on behalf of the CPMT BOG to Tohru Kishimoto of NTT, General Chair of 2002 SPJW

Erich Klink, also of IBM, described the packaging for IBM's Unix servers. This MCM is much simpler, but still requires 71 glass ceramic layers to support 4 ICs, each with over 7000 C4 bumps. The module has 5200 I/O, and 4 modules are used in a 32-way system.

Kazuhiko Umezawa of NEC described the hardware in the iPX7800 server. Their MCM contains 4 processors, control, and L2 cache. ICs are in .15 μm CMOS. Processors contain 38M transistors and run at 420 MHz. The MCM has 20 ceramic layers for power, and 8 layers of thin film wiring (4 signal layers.) Gold wiring and polyimide dielectric layers are used.

Signals from board to board also run at the 420 MHz clock frequency.



Participants ready to enjoy their bento box lunch.

In the session on Packaging for High Frequency and Wireless Applications, Yasuhito Takahashi of Fujitsu described low cost plastic packaging for GHz devices, and focused on several varieties of built-up-multilayer (BUM) substrates to support flip chip packages with up to 3500 BGA connections, and ICs with 165 μm bump pitch.

Kazuhiko Iijima, also from Fujitsu, described the MV (multiviva) technology for Wireless Applications. This family of substrates is an all build-up technology with embedded passive components. The substrates use copper clad films, laser drilling, and selective plating to create plane pairs. Some varieties laminate completed films with adhesive layers containing conductor-filled laser drilled vias. Other substrates continue building up sequentially from the first layer of film. Thin passive components were selectively embedded in the adhesive-based technology.

Following a full day of technical presentations, the evening banquet featured toasts and speeches, much beer and sake, and splendid food, including enough sushi to feed an army.



Listening to a speech before the banquet

Tuesday began with the session on Packaging Technology for Optical Communications Systems. Hideyuki Takahara described



NTT's method of optical interconnection for flip chip ICs using an optoelectronic chip on flex with a 3-layer flex film with the embedded optical waveguide. The emphasis was on low thermal expansion material to allow precise alignment for a linear array. Very low loss was achieved with $\pm 1 \mu\text{m}$ alignment accuracy.

A session on MEMS technology included an interesting look at the technology espoused by Ball Semiconductor, presented by Masataka Yoshida. As the company name implies, these folks are able to make ICs on the surface of 1 mm balls of silicon. They connect from one ball to another, and to the outside world, with rings of solder bumps. This radical technology eliminates the need for a cleanroom, as all processing is done within tubes.

The highlight of the afternoon was the opportunity to tour the NTT Telecommunication History Museum in Musashino. Starting with meticulously copied Western Electric electromechanical switching systems from the post-WW II era, NTT has evolved its own distinct, world class, leading edge technology. The museum is first rate, and well worth a visit.

Wednesday's first session was on future packaging technology. Len Schaper, of the University of Arkansas, compared several 3-D packaging technologies, and concluded that through-silicon vias in stacked thin ICs are a potential breakthrough technology that will enable new architectural possibilities because of the density of Z-axis interconnects.

Walter De Raedt, of IMEC, examined the potential for multilayer thin film substrates incorporating integrated passives to enable microwave systems in package applications. He presented several examples of combiners, filters, power dividers, etc., implemented in the advanced substrate technology.

Tomonori Fujii, from ASET, discussed the chip joining and inspection technologies used to form 3-D silicon stacks. Gold/gold thermocompression bonding is effective even with $18 \mu\text{m}$ square gold bumps. The resulting $3 \mu\text{m}$ gap was underfilled with a composite material using $.3 \mu\text{m}$ filler particles. ACF material was also used to connect the stack; $1 \mu\text{m}$ particles resulted in 20 - 30 particles per bump being trapped. SAM was used to detect voids in connection and underfill.

Toshiro Hiraoka of Toshiba presented perhaps the most novel talk of the workshop, in describing a method for creating wiring layers using photo-induced selective plating to make both wires and vias in a microporous sheet of polymer material. The 20 - $80 \mu\text{m}$ thick material is coated with a sensitizer, and then exposed. Where a via is desired, the exposure intensity is increased. Low intensity only affects the surface and allows a wire to be plated in the subsequent electroless plating step. The process can be double sided to create a flex-like structure. The material is impregnated with resin after the copper is plated. Though this development is at its early stages, the potential is most exciting.

Following another splendid bento box lunch, the workshop concluded with a session on Electronic System Integration for System Packaging. Two talks from the ASET laboratory were excellent. Osamu Ibaragi described the Optoelectronic Hybrid Integration Technology work. He showed an optoelectronic MCM (OE-MCM) using a waveguide film laminated to a circuit board, and providing $.3 - .5 \text{ dB/cm}$ loss for 100 Gbps signals. He also described an optical fiber board in which a UV curable resin was cured by illumination from the optical fibers to be connected; the resulting cured resin formed the waveguide core. These cores were "clad" by applying a layer of a different resin.

Kenji Takahashi updated the ASET work on 3-D chip stacking with through-silicon vias on $20 \mu\text{m}$ pitch. They have done a great deal since their ECTC papers last year to reduce the voids in copper vias by plating improvements, both in current control and in chemistry. They still have problems in the handling of $50 \mu\text{m}$ thick wafers. They are examining ultrasonic gold-gold flip chip attach for chip stacking. An ASET goal for 2002 is to build an OE-MCM incorporating 3-D chip stacks.

Overall, this was an excellent workshop with truly leading-edge talks, at a splendid facility. Progress in packaging technology at the system level continues to deliver great strides in system performance.

- Report submitted by Dr. Len Schaper, Director, High Density Electronics Center, University of Arkansas.

TC-1 News from 2001

TC-1: Technical Committee on Electrical Contacts, Connectors, and Cables

The scope of this Committee is to be the focal point within the IEEE CPMT Society for electrical contacts, electrical connectors, and interconnecting cable. Its membership consists of individuals having an interest in the research, development, manufacture, and utilization of electrical contacts and devices that contain them. The Committee holds regularly scheduled meetings and functions through the Holm Organization and through task forces having specific objectives. The

Committee sponsors or supports conferences, publications, educational, standardization, and other activities.

The 2001 IEEE Holm Conference on Electrical Contacts was held in Montreal September 10 to 12. This was the 47th Annual conference in North America where professionals presented and discussed the latest developments in the field of electric contacts. This year, we had 91 attendees including 47 from USA, 27 from Europe, 10 from Asia, and 1 from Africa. The lower than usual registration is obviously because of the slow economy.

In the middle of the morning session on September 11, we were all shocked by the newsbreak about the tragedy at the



World Trade Center. The conference was briefly suspended while we all had to call home and make contingency plans for travel. When the conference reconvened after an hour of interruption, we had a moment of silence for the unfortunate loss of lives and pray for world peace.

The technical program was very successful with 42 papers in 10 sessions. Papers were presented on electric contacts in switches, relays and connectors, new contact materials and coatings, arc fundamentals, thermal models, finite element analysis and corrosion. More details of the program and abstracts can be found in our web site.

On Monday night (9/10), we also had a successful social event to the La Sucrerie de la Montagne in the countryside of Montreal. We discovered the beauty of a natural maple-grove and enjoyed the hospitality of the Quebecois pioneer era. This annual Monday social event is becoming a tradition when the conference attendees get to chat more freely with their colleagues. We had over 60 participants with many spouses attending also.

In the awards luncheon, we presented the 2000 Holm Conference Prize Paper Award to Dr. Eisuke Takano for his paper "Contact Current Distortion Due to Tunnel Effects". Gerry Witter, TC1 Chairman, also announced the establishment of the Morton Antler Invited Lecture through endowment of a grant from the Antler family. Mort has been a long time Holm conference contributor, lecturer and organizer. The first invited lecture will be in 2002.

TC-1 also runs a 3-4 days intensive course on electrical contacts annually with up to 40 students. The course has been very successful in teaching engineers the physics and practice of contact designs and selections. The course is a favorite for switch, relay, circuit breaker, contactor, and connector engineers from automotive, power distribution and telecommunication fields. The 2001 course was held in Pittsburgh June 10-14. The 2002 course will be June 10-13 in Washington DC.

For more information on many special events organized by this committee such as annual IEEE Holm conference, intensive course, international conference, CD-ROM library and link to other societies, please visit our web site at www.ewh.ieee.org/soc/cpmt/tc1.

■ submitted by Chi Leung, cleung@amidoduco.com



■ Poster session at Beijing Local Chapter Meeting

IEEE/CPMT Beijing Local Chapter Technical Meeting Report

A very successful IC electronics packaging technical meeting, organized by the IEEE/CPMT Beijing Local Chapter, was held on December 30, 2001 on the campus of Tsinghua University. At this meeting, Dr. John H. Lau of Agilent Technologies was invited to give a presentation titled: "IC Packaging Trends". There were more than 80 attendees from 11 different units.

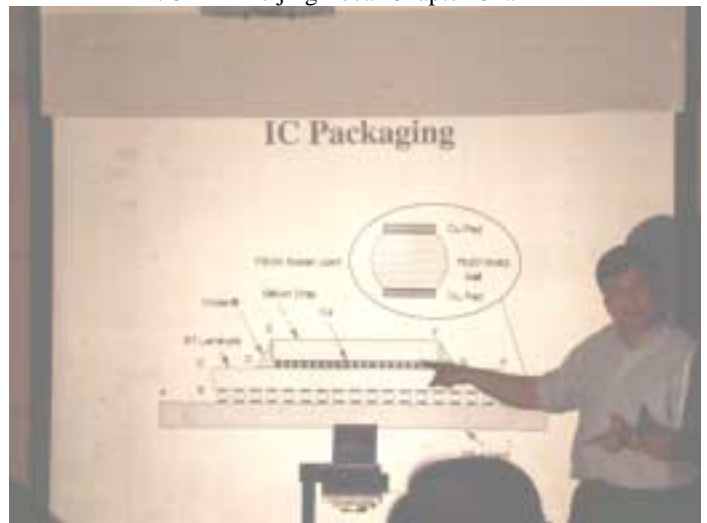
At 9:00AM, Professor Ma Jusheng, IEEE/CPMT Beijing Local Chairman, welcomed everybody and introduced some important people at the meeting. Afterwards, Mr. Zhao Guangyun, Secretary General of Electronic Components Society of the Chinese Institute of Electronics, introduced the objectives and organization of IEEE/CPMT. Finally, Mr. Guo Yishu of Ministry of Information Industry introduced the history and functions of IEEE/CPMT. After their brief presentation, many attendees showed their interests in joining the IEEE/CPMT Society.

At 9:40AM, with a very warm welcome, Dr. John H. Lau started his excellent presentation. The contents were very rich and fresh. He talked about IC technology trends, WLCSP (wafer level chip scale package), SOC (system on chip), SOP (system on package), Lead-Free soldering, and Solderless technologies such as adhesives (ICA, ACA, and NCA).

We all enjoyed Dr. Lau's presentation very much. During the presentation, he asked us questions (to make important points) and wanted us to give him (or to think of) the answers. This presentation-style created very active discussions. He also wanted us to ask him questions and he answered all the questions systematically and clearly. The presentation finished at about 12:20PM with thunderous applause.

This meeting was a great success! It is not only because of Dr. Lau's exceptional presentation, but more than half of the attendees are young people. This reflects a great future of Chinese IC packaging technologies. At the same time, this meeting introduced the IEEE/CPMT Society to the Chinese people who are working in IC packaging areas.

■ Professor Ma Jusheng
IEEE/CPMT Beijing Local Chapter Chair



John Lau giving presentation at Tsinghua University

Scandinavian CPMT

Building on a base of 12 members in Denmark, 43 in Norway, and 58 in Sweden, a Joint Scandinavian CPMT Chapter was formed in 2001. In addition to leaders in each country, the Board of Governors provided help through Rolf Aschenbrenner, C.P. Wong, Jim Morris, Ephraim Suhir, and Johan Liu.

A series of CPMT workshops were held in Sweden with a number of invited technical speakers from around the world including USA. In addition, a series of packaging seminars were started which have an email invitation sent to all Scandinavian members. Another step taken to activate CPMT was the creation of a student chapter in Sweden. The Scandinavian members have also been active supporters of the CPMT Polytronics meetings through its many different manifestations.



presentation of **Johan Liu**, Sweden

The year 2002 will see increased coordination with the Finish CPMT Chapter and other North Europe members. One possible focus will be an CPMT/IEMT European Conference in 2003. In addition, CPMT can encourage more growth in Europe by holding some Board of Governor events and having plenty of global volunteer presence at Scandinavian and other European CPMT events.

■ taken from

Vice President Paul Wesling Announces New Transaction Editor

Prof. Ganesh Subbarayan at the University of Colorado will assume a four-year appointment as Editor for the IEEE Transactions on Advanced Packaging. He will phase in this role over the next few months.

Ganesh received his PhD in mechanical engineering from Cornell, then worked at IBM in Endicott. His research areas parallel the topical areas of the Transactions: microsystem packaging modeling, reliability assessment, design and manufacturing, and optoelectronic/MEMS packages. He has been an active participant in technical conferences (I-THERM as Program Co-Chair, InterPACK as Program Track Chair, and IEMT), and serves this year as Program Chair of ASME's 2002 International Congress. He has taught a number of relevant courses, including "Electronics Packaging" and "Design for Manufacturing."

Ganesh has published 30+ conference papers and over 20 archival papers, including 3 in our IEEE Transactions and many in the ASME Journal on Electronics Packaging. He has three patent disclosures.

He received an NSF Career Award in 1998, has received grants from NIST's ATP program and several from SRC. He is a

co-editor of two ASME volumes on "Advances in Electronic Packaging", is finishing up a book on "Optimization in Electronics Packaging" this spring, and is working with Professors Joshi, Sammakia and Dr. Ramakrishna on a book on "Thermomechanical Characterization of Electronic Packages".

CPMT Japan Chapter Report

■ submitted by Naoaki Yamanaka, CPMT BoG
IEEE CPMT Japan Chapter has reorganized as follows:

Chair: **Noboru Ichinose** -- Waseda University

Vice Chairs:

Naoaki Yamanaka -- NTT Network Innovation Labs

Nasayoshi Umeno -- Chuo University

Secretary: **Nobuo Iwase** -- Toshiba Research
Consulting Company Ltd.

Treasurer: **Kaoru Hashimoto** -- Fujitsu Laboratories

We have two new IEEE CPMT Japan Board members, Prof. Umeno, and Naoaki Yamanaka.

The Japan Chapter is planning to support the following two workshops and a conference. In addition, outstanding papers from the Conference will be published in IEEE CPMT Transaction by CPMT Japan Chapter.

2002 IEEE System Packaging Japan Workshop.

Feb. 4-6 2002 at NTT Musashino, Tokyo

<http://www.ewh.ieee.org/soc/cpmt/tc14/jspws02.html>

2002 International Conference on Electronics Packaging, ICEP

April 17-19, 2002 at Dai-ichi Hotel Seafort, Tokyo

<http://www.jieep.or.jp/jieepweb/icep/2002icep.html>

The 6th VLSI Packaging Workshop of Japan

Nov. 11-13, 2002 at Kyoto Research Park, Kyoto

<http://homepage1.nifty.com/ieeetokyo/chapter/cpmt/vlsip.html>

If you need more information, please contact IEEE CPMT Japan secretary, Dr. Nobuo Iwase

(mailto: nobuo.iwase@toshiba.co.jp)



Naoaki Yamanaka is new on CPMT Board of Governors

The CPMT Society Announces its 2002 Award Winners

Top honors... best of the best... first rate. Each year, the IEEE Components Packaging and Manufacturing Technology Society (CPMT) honors its peers through a prestigious Awards Program. Individuals, teams and chapters are recognized for their technical excellence, achievement, leadership and service. The Society is pleased to announce the following CPMT Society award winners for 2002.



**** The David Feldman Outstanding Contribution Award - Prof. Herbert Reichl** (Fraunhofer IZM, Germany) for his technical leadership and outstanding contributions to the microelectronics packaging industry. He is the Head of the Research Center for Microperipheric Technologies-System Integration, TU Berlin, and founded and directs the Fraunhofer IZM. In addition, he is active in various CPMT Society-sponsored conferences and workshops. Prof. Reichl is an IEEE Fellow and considered to be one of the premier leaders in electronics packaging education and technology in the European community.



**** Outstanding Sustained Technical Contribution Award - Prof. Avram Bar-Cohen** (University of Maryland, USA) for his contributions to thermal design, modeling and analysis and for original research on ebullient and liquid-phase cooling. An IEEE Fellow since 1993, Prof. Bar-Cohen serves as Editor-In-Chief for the IEEE Transactions on Components & Packaging Technologies and is an elected member of the CPMT Society Board of Governors. He is also known for achievements outside his particular job, such as mentoring a group of Russian thermal engineers in

Siberia - visiting them, developing sponsorships so they could attend conferences and helping to edit technical papers.



**** Electronics Manufacturing Technology Award - Mr. Scott Kulicke** (Chairman and CEO, Kulicke & Soffa, USA) for his leadership and vision in transforming Kulicke & Soffa from a premier wire-bonding supplier to a global leader in semiconductor interconnecting technologies. He was the founding Chairman of SEMI/SEMATECH, Inc., an organization of semiconductor equipment and materials suppliers supporting the goals of SEMATECH (the consortium of U.S. semiconductor manufacturers and the U.S. Government for manufacturing competitiveness) and served as Chairman of the U.S. Department of Commerce's Technical Advisory Committee on Semiconductors.



**** Exceptional Technical Achievement Award - Prof. C.P. Wong** (Georgia Institute of Technology, USA) for his pioneering work in polymeric materials for electronics packaging applications and for the introduction and development of silicon gels to achieve reliability without hermeticity in plastic IC packaging. He is considered a world-renowned expert in the research and development of polymeric materials in electronics packaging. Prof. Wong is an IEEE Fellow, an elected member to the Board of Governors and former President of the CPMT Society. In addition, he is an elected member of the National Academy of Engineering, which is considered one of the highest honors one can receive in the industry.

**** Outstanding Young Engineer Award** - There was such phenomenal talent in this category that two co-recipients were chosen to share the award. (Shown in alphabetical order)

Ms. Christine Kallmayer (Fraunhofer IZM, Germany) for her contributions to various packaging technologies including Au-



Sn solder interconnections and flex-based packages and for her active participation in technical conferences sponsored by the CPMT Society.



Dr. Li Li (Motorola, Inc., USA) for her contributions to flip chip interconnect bumping materials and process development and embedded passive design and implementation in RF modules, and for her service to the CPMT society via conferences and IEEE transactions.

The awards will be presented at the 52nd Electronics Components & Technology Conference (ECTC) in San Diego, California, USA, during the CPMT Society luncheon. The exception is the Electronics Manufacturing Technology Award, which will be presented at the International Electronics Manufacturing Technology (IEMT) Symposium and SEMICON West 2002 in San Jose, California, USA, July 17-19.

Congratulations to all of the winners.

For more information about the CPMT Society Awards Program, please contact:

Rao Bonda, Ph.D.
Chair, Awards Program
Phone: +1 480 413 6121
Fax: +1 480 413 4511

email:
rao.bonda@motorola.com



Luu Nguyen Wins Fulbright

Luu Nguyen, Chair of CPMT TC-18 Wafer Level Packaging, has been officially awarded a Fulbright-Nokia Fellowship. The Board of Directors of the Fulbright Center and the Finnish Fulbright Commission reached this decision in late February. Luu Nguyen will work at the Helsinki University of Technology during the Fellowship period. He will give a series of 5 to 6 seminars and a one-day workshop based on his on-going work at National Semiconductor as presented through CPMT conferences and publication. He will also be working on lead-free issues and Design-For-Manufacturing of opto-electronic modules. Luu will also use this experience to get more input for his book on Wafer Level Packaging.



The Fulbright Program is the US government flagship exchange activity with other countries. Since its inception in 1946, more than 88,000 U.S. Fulbrighters have studied, taught, or conducted research in 140 countries around the world, and more than 146,000 foreign citizens have come to the U.S. under Fulbright auspices. The competitive

awards can be used for research, lecturing, or lecturing/research. The Fulbright Program is administered by the US Department of State. Overseas, the program is administered by binational Fulbright Commissions or by the Public Affairs of the US Embassies. The Presidentially appointed Fulbright Foreign Scholarship Board is responsible for the final selection of all Fulbright grantees.

This year, for the first time, Fulbright established the Fulbright-Nokia Fellowship in Electronics, Information, and Telecommunications Technology. It allows an applicant to work with a Finnish host institution from 4 to 9 months in those areas specified.

More information about the Fulbright program can be found at www.iie.org/cies/us_scholars/

Upcoming German CPMT Activities Tutorial on Flip

Chip and Chip Scale Package

in Munich during Semicon Europe

April, 15 - 16, 2002 -- Organizer: PacTech GmbH

4th International Workshop on Area Array Packaging Technologies

in Berlin, after Semicon Europe

April, 22 - 23, 2002 Organizer: IEEE CPMT - German Chapter

<http://www.pactech.de/docs/AAWS2002.pdf>

Tutorial on Flip Chip and Chip Scale Package

in Munich during Electronica

November, 11 - 12, 2002 -- Organizer: PacTech GmbH

4th International Workshop on Area Array Packaging Technologies

in Berlin, after Electronica.

November, 18 - 19, 2002

Organizer: IEEE CPMT - German Chapter

Submitted by Dr. Elke Zakel, zakel@pactech.de

Conference Calendar

Here is the approximate timing of most of the ECTC sponsored meetings. If you make it to two of the more than 40 meetings listed then your IEEE/CPMT dues have been rebated by registration fee discounts. If you make it to all CPMT meetings you save a lot because you can sell your home since you will never be there. Find a meeting that matches your current work and volunteer for the organizing committee or submit a paper.

January

IEEE computer Packaging Japan Workshop -- Japan
IEEE Systems Packaging Workshop -- Europe
Military and Space Electronics Conference and Exhibition -- Los Angeles

March

Chip Co-Design Workshop -- Europe
Wafer Level Packaging Workshop (**WLP**) -- Atlanta
International Symposium on Advanced Packaging Materials -- Atlanta
Academic Packaging Conference -- Worldwide
Semiconductor Thermal Measurement & Management Symposium (**SemiTherm**) -- San Jose

April

International Conference on Benefiting from Thermal & Mechanical Simulation in Microelectronics (**EuroSIME**) -- Europe
International Electronics Manufacturing Technology Symposium (**IEMT-Europe**) -- Europe
International Conference on Electronics Packaging (**ICEP**) -- Omiya Japan

May

International Spring Seminar on Electronics Technology (**ISSE**) -- Central Europe
Spring Workshop on computer & System Packaging -- USA
European VLSI Packaging & Microsystem Packaging -- Europe
Symposium on Design, Test, Integration & Packaging of MEMS/MOEMS -- Europe
IEEE Workshop on Signal Propagation on Interconnects (**SPI**) -- Europe
Electronic Component & Technology Conference (**ECTC**) -- USA
Intersociety Conference on Thermal & Thermomechanical Phenomena in Electronic Systems (**I-Therm**) -- USA

June

Holm Intensive Course on Electrical Contacts -- USA/Canada
MCM/SOP Applications Workshop -- USA
International Symposium on High Density Packaging & Component Failure Analysis (**HDP**) -- Shanghai
International IEEE Conference on Polymers & Adhesives in Microelectronics & Photonics (**Polytronic**) -- Europe

July

Inter-Society Packaging Conference (Interpack) -- Hawaii
International Workshop on Integrated Power packaging (**IWIPP**) -- USA

August

International Symposium on Electronic Packaging Technology (**ISEPT**) -- Beijing

September

Annual IEEE/DPC Napa KGD Packaging & Test Workshop -- Napa Valley CA
Electronics Goes Green -- Europe
Advanced Semiconductor Manufacturing Conference and Workshop (ASMC) -- USA/Europe
International Workshop Thermal Investigations of ICs & Systems (**THERMINIC**) -- Europe
Holm Conference on Electrical Contacts -- USA/Canada

October

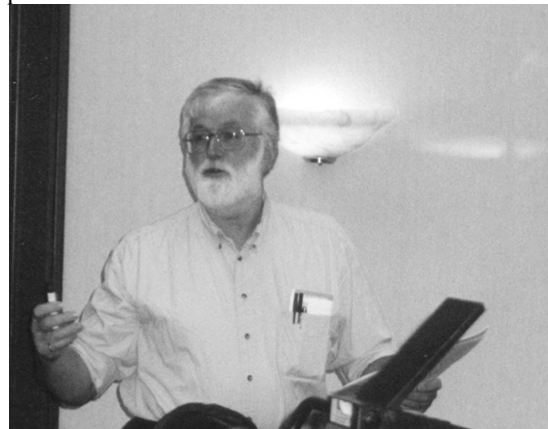
International Electronics Manufacturing Technology Conference (**IEMT**) -- Santa Clara CA
IEEE Workshop on Accelerated Stress Testing (**AST**) -- USA
International Symposium on Semiconductor Manufacturing (**ISSM**) -- San Jose CA
IEEE Fiber Optics, Photonics, Optoelectronics Assembly, Packaging & Manufacturing Interactive Workshop (**OEP**) -- USA/Europe
Future Directions in IC and Package Design Workshop (**FDIP**) -- USA
Topical Meeting on Electrical Performance of Electronic Packaging (**EPEP**) -- USA

November

International Workshop on Smart Card Technologies & Applications -- Germany
Area Array Packaging Workshop -- Germany
International Symposium on Electronic Materials & Packaging (**EMAP**) -- Far East
VLSI Packaging Workshop of Japan -- Japan

December

Area Array Packaging Workshop (**APACK**) -- Singapore
Electronics Packaging Technology Conference (**EPTC**) -- Singapore



Vice President of Conferences, James Morris

Web Database for USA Engineer Consultants

The newly designed IEEE-USA Consultants Database is now live on the Web at www.ieeeusa.org/consultants. This premier service matches prospective clients with the world's finest electrotechnology and information-technology professionals-for-hire.

The completely rebuilt database offers many new and enhanced features, making it more powerful and easier to use. The site, which last year logged more than 30,000 visits, is the ideal online meeting place for consultants and prospective clients.

For about 20,000 consultants, the database includes a profile of their credentials, contact information and their website link.

Editor's Turn

Thank you, fellow-members, for providing the great news and photographs for this issue. For example Len Schaper, Rao Bonda, Rao Tummala, Nobuo Iwase, Naoaki Yamanaka, Merrill Palmer, Ralph Russell, Elke Zakel, Luu Nguyen, Kristine Martin, Jack Balde, Margie Ballinger, Chase Palmer, Al Puttlitz, Jerry Witter, Ma Jusheng, Alina Deutsch, Larry Gilg, Paul Wesling, Xiaoming Xie, Chi Leung, and Marie Ericsson. There are many more helpers we must also thank.

This issue was also an example of the increased **productivity** that comes from the **Internet**: last minute location of an award winner photo from their home web page, checking details of many upcoming meetings, finding prices of books, and checking on the process for becoming a Senior Member of IEEE. Also a big "Thanks" to those who called or emailed their reasons for liking a paper or a web version of this Newsletter and any CPMT publication. I am pleased so many read and benefit from our publications, even though there is no uniform vote for the "right" future format for these publications.

During the last month I had the honor of writing **recommendations** for two members of CPMT that have accomplished much and are being nominated as "Fellow of the Institute". It was rewarding to pause from the daily list of chores and stand in awe of decades of professional and volunteer accomplishments performed by some of our members. Most engineers consider their own progress as work-as-usual even though it often adds up and makes a big difference to our profession and economy. We cannot celebrate all the time, but we must mark our change in-kind a few times during our careers. One way we can all recognize the progress of our CPMT colleagues is to help others **achieve the Senior Member standing** (first apply for yours at <http://www.ieee.org/organizations/rab/md/smfirms.htm>). Remember that if a member has 10 years of activity in IEEE fields (including years of Graduate Education) they probably qualify for this title.

Now for something completely different!

Once again there were many activities competing with the editing of this newsletter; my income producing job and my income losing tax filing being the two major ones. However, I have added yet another diversion that dilutes any editorial focus --- Internet Radio! Just after learning to control my hourly desire to surf for any changing world and financial news on the Internet, I am faced with thousands of radio stations that sing out to be sampled. Most cities have approximately 50 local broadcast radio stations that used to seem like more than anyone could want. However, by finding Internet schedules for thousands of broadcast radio stations from all over the world (and a few just originating in "http://-world") one can easily saturate their waking hours. It reminds me of the first time a child sees the shelves of their city's library and realizes they will not be able to read everything that is written.

So what surprises and changes has this surfing resulted in? **First** there is the happy discovery that most of the best jazz stations were in Germany and England (Jazzradio.net, soft jazz FM). **Second** was the discovery of stations unlike those in my home town: RTR-FM in Perth Australia has some really great music, comedy, and talk shows that are worth the diurnal phase

change. KAOS of Evergreen State College in Olympia Washington also has comedy and excellent radio personalities selecting music and commentary. **Third** was the discovery of lots of continuous music stations (few ads or words) with focused music taste: classical, new age, techno; for example, when stressed at work I now stream "Astreaux World" softly on my computer speakers. The beauty of radio is that one can listen while driving a car, or washing the dishes. If the data stream is music, one can listen while performing most solitary tasks.

One strange unintended consequence of saturation radio is that by keeping German Jazz stations playing softly throughout the night one wakes up in the morning magically knowing the weather throughout Europe. Other consequences might be corporate bandwidth shortage as more engineers go mellow (one could always burn a CD with MP3 versions of a radio station over-night) and the loss of local supporters for broadcast stations (particularly those with lots of on-air advertisement interruptions).

Technically it is possible to use a 56Kbps dial-up modem to listen to stations but this eats up about 1/2 your bandwidth and does tie up the phone. The happiest web radio listeners seem to be those with DSL or TV cable hook-ups or University/ company large Internet pipes to their desktops. In the PC world the common media "browsers" include NullSoft WinAmp MP3 player, Windows Media Player, and RealPlayer. Websites that let you find the radio stations of your dreams include Broadcast.com, The Green Witch, Imagine Radio, Realguide-stations, Spinner.com, KRS Radioworld, Netradio network, Radio Spirits, Sonicnet Flashradio, Yahoo Radio, Vtuner, and Live365. For the last 4 months I have used the last two and have only sampled their offerings. You can also do a web search on call letters if you happen to know what station you are looking for.

So will Internet radio be used for good (make engineers more productive, globally informed, and emotionally stable) or for evil (distract engineers or give them liberal-arts tendencies)? Will we soon have CPMT radio? Stay tuned.

New IEEE Job Site Goes to Work for Technical Job Seekers

WASHINGTON, D.C. (8 June 2001) - A new IEEE Job Site at www.ieee.org/jobs features the IEEE e-Recruiter™ job service that makes the job-hunting process easier and more effective for technical professional job seekers. The online service, sponsored by IEEE-USA and IEEE Spectrum, allows IEEE members worldwide to create and submit a profile of their background and the characteristics they'd like in a new job.

The service, powered by Hire.com's e-Recruiter™ software, then scours its extensive database for positions that match what the job hunter is looking for in employment. New job postings are continually being added, and the job seeker is notified by e-mail if there is a profile match. And the process can be conducted anonymously.

For more information or to register and submit a profile, visit www.ieee.org/jobs. The CPMT Society web page also lists job openings for practitioners in the area of packaging. Listings can be included by sending input to deutsch@ieee.org.

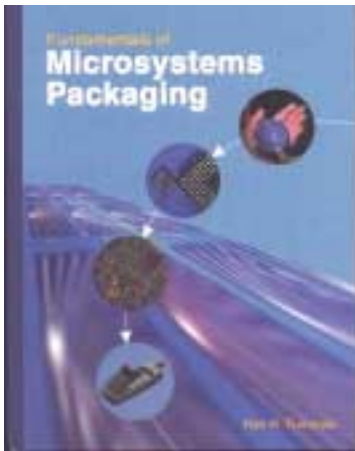
{e-Recruiter is a registered trademark of Hire.com. All other trademarks or registered trademarks are properties of their respective companies.}

Book Review

Fundamentals of Microsystems Packaging

by Rao R. Tummala, Georgia Institute of Technology
 Publisher McGraw Hill, 2001, pages = 967. ~ \$90.

More Universities are attempting graduate classes in Microelectronics Packaging. There are only a few books that try to cover the broad discipline and project the vision an engineer must have to navigate their projects through the packaging. Many professors and many experienced engineers have used Transaction articles and trade journal review articles to get up to speed, however this new book offers a more inclusive and integrated approach. In a way, a book like this is needed to make our discipline visible to the general engineering and management community.



The book establishes quickly a sense of the importance to the economy and design of packaging. The history of electronics is also carefully outlined so that the importance of the advances in all levels of packaging can be understood. These are perhaps the most important parts of the book in establishing perspective and the heft of the discipline, but alas, most university classes will be too rushed to do anything but skip over these introductory

chapters.

The stage is set by introduction to reliability concerns including thermal issues. Then chapters are dedicated to most of the important areas of concentration: single chip, IC assembly, wafer level packaging, passive devices, opto-electronics, RF, MEMs, and encapsulation. The board level and higher system assemblies are also addressed to the extent that they dictate constraints on Microsystem packaging.

The book has good problems at the end of chapters and highlights review pages of word definitions and important constants and material properties. It makes an excellent text. In addition, the writing is smooth with a nice sense of humor that makes it also a good evening read for those already having a day job.

There is nothing that seems to be lacking (except the time to absorb it all), but it may be of use for future editions to include a CD-ROM that could have some video clips of packaging production lines. There is nothing like the blur of a wire bonder, the sounds and sight of a package molding machine pumping out parts, or the endless row of cell phones emerging from a manufacturing line to inject reality into pages of design rules and details.

■ reviewed by the editor

■

IEEE Salary Calculator

Are you alternating between being so happy that you have a great job with lots of money and being depressed because you are sure your Dilbertian employer is undervaluing your contributions? Well then you sound like an engineer that needs to use the IEEE Salary Calculator to put some reality in your engineer-employer dialog.

"It will report the complete range of full-time income from primary sources being paid to IEEE-USA members -- electrical, electronics or computer engineers and scientists -- in specified employment situations.

"The 'complete range of full-time income' means that the system will report both a most typical result -- the median or 50th percentile, the value that is in the middle of the distribution of pay - and also eight additional percentile values, from the 10th (low) to the 90th (high). This range data provides a context for assessments of the effects of such unmeasurable influences on pay as the skill and talent of individual technical professionals."

--- From the web site <http://www.ieeeusa.org/careers/salarycalculator/>

If you filled out the salary survey forms last year you already received a free account on this system. I believe it costs \$10 to get a one-year subscription...well worth it if you are even losing one hour of sleep because you don't know what the salary market values are for your career. You answer 10 questions such as your company's business, your highest education, your geography, your specialty, and your years on the job. Then you see the salary spread for those in your situation. You can re-enter the terms to see which are the most sensitive parameters for your situation (what if I earned another degree? what if I worked here 10 more years?).

So what did I learn? Since I work in the overlap of CPMT and MTT Society technical projects, I **first** learned that there is no market advantage to being in either specialty. This contradicts the hot market for new MTT type graduates we have seen in the last few years...on the other hand I am not a spring chicken. So maybe this means that after a while experience wins and you should follow the path of your own and your company's interests...or maybe not.

Second I learned that the "responsibility level" is a big influence on salary. For example, the difference between GSA 13 and GSA 14 type job descriptions was 10% in salary. This may explain the many times we see people hiring staff and creating structure under their position despite the fact that it looks like a few person job at best.

Third, it was clear that the spread of salaries for any category was a factor of 2...so some things besides the obvious 10 questions lead to some being paid twice what others are (at least for us old-timers). Although this web approach has the same information as many salary data books it is more responsive to the many questions that one asks when looking at a chart.

All this brings me back to one of the lessons I learned from a grizzled engineer (many years ago before I became grizzled). Everyone was complaining about the raises that were just announced. He chuckled and asked me the following questions:

**Do you enjoy the work and your team-mates? (the answer was and remains YES)

**What percentage underpaid do you feel? (the answer was and remains about 5-10% for most engineers)

**What percentage is the average annual raise? (3 - 6% normally, usually 1-2% beyond inflation for engineers)

**How much would you have to have invested or earned from being an adjunct professor to make up the difference?

**How many additional years will you have to work to get the salary (cash flow) you think you deserve today?

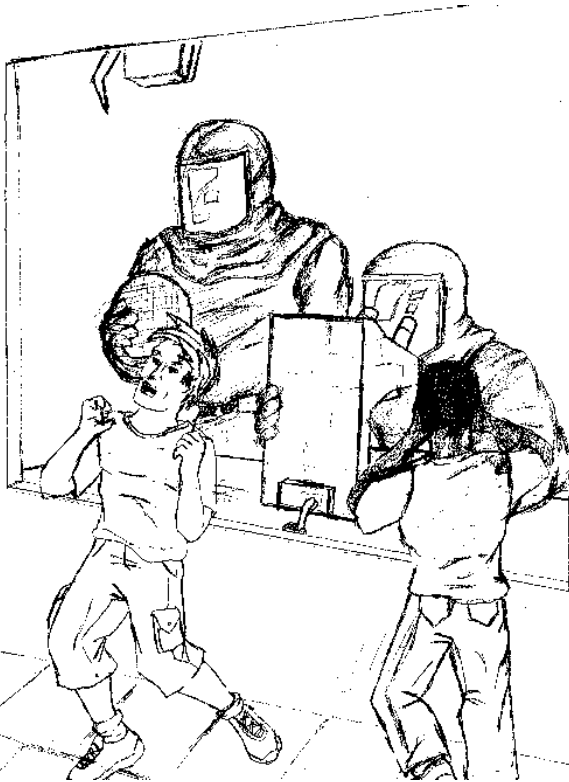
These questions set a perspective that quickly dissipated the tempest and palace revolt that was brewing around the coffee pot. As engineers we like our self-made tempests so it took a few boxes of donuts by the grizzled-one over the next few months for forgiveness to surface.

There is more to salary than numbers.

■ the editor

Cartoon

The danger of children touring Microsystems Facilities



"I see Die-People"

TWO WEEK SHORT COURSE SERIES

May 13 - 24, 2002

The next offering for the PRC two-week short course series is scheduled for May 13-24, 2002. The series will consist of individual modules that will cover systematically and comprehensively all the critical technologies from systems to devices including microelectronics, photonics, MEMS and systems packaging. The modules will be instructed by faculty from Georgia Tech and industry experts.

RF/Wireless Packaging: Status and Challenges

Optoelectronics

MEMS Packaging and Applications

Integral Passives

Next Generation Microvia (Hands-on)

Wafer Scale Packaging

Low Cost Flip Chip Processing & Analysis (Hands-on)

Thermal Management of Microelectronic Devices

Polymers for Microelectronics: Process and

Characterization (Hands-on)

Thermomechanical Reliability

Signal Integrity with Emphasis on Power Distribution

for Digital Systems

Detailed information will be available on the PRC web site, www.prc.gatech.edu, after January 15

■ submitted by Margarita C. Bolet

9th Annual KGD Packaging and Test Workshop

- Napa, California - - September 8 - 11, 2002

The 9th Annual KGD Packaging and Test Workshop will be held on September 8 - 11, 2002 in Napa, California. The technical committee is seeking presentations on relevant topics to the die products industry. You can obtain a copy of the call for papers at

http://www.dieproduct.com/cfp_2002.pdf

Presentations are being sought in the following areas (among others):

Applications of Die Products

Die Products Manufacturing

CEM die strategies

Special issues for testing mixed technology

Testing of Passive/Active Substrates

Wafer Level Test/Burn-in

Test Economics and Cost Analysis

Market Forecasts

SIP-SOC Comparisons

Flip Chip developments

Technology Integration

MEMS & Sensor Technology

Abstracts are due by June 15, 2002. Authors will be notified by June 30.

Contact info@napakgd for more information.

■ Larry Gilg

ITHERM 2002

May 29-June 01, 2002
San Diego, CA

CALL FOR SHORT COURSE PROPOSALS

The **ITHERM** Organizing Committee is now soliciting proposals for Pre-Conference Short Courses to be taught on the day before the start of the Conference technical program. We seek proposals for One Day Short Courses to be taught in roughly eight hours by one or more instructors. The topic of the course can be in any area relevant to the Science, Engineering, Design, and Practice of Thermal and Thermo-mechanical Phenomena in Electronic Systems. Criteria for selecting the courses will include relevance and immediacy of the proposed topic as well as demonstrated expertise and experience of the instructors.

To propose a short course, submit a Two Page proposal by email or as an attached document to the Short Course Chair:

Prof. Alfonso Ortega
The University of Arizona
AME Department
P.O. Box 210119
Tucson, Arizona
Tel: 520-621-6787
Fax: 520-621-8191
Email: Ortega@u.arizona.edu

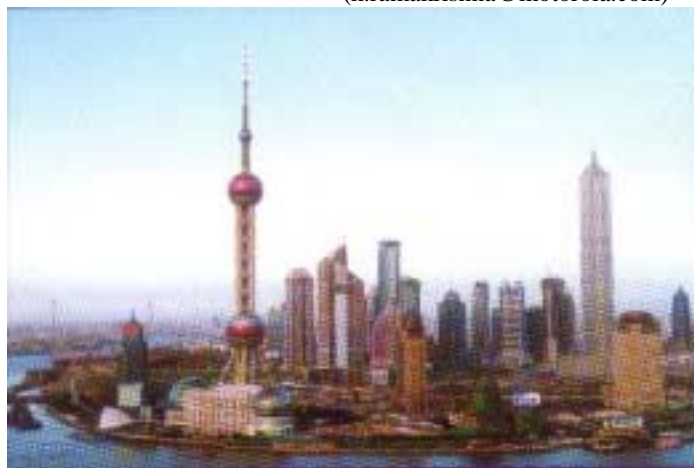
Deadline for Proposal Submission is December 14, 2001. Short Courses will be announced by January 15, 2001.

The proposal should contain the following information in Two Pages:

- Short Course Title
- Instructor Name(s)
- One Paragraph Course Description
- Statement of Intended Audience and Prerequisite Knowledge Level Expected of Student
- Outline of Course Preferably in One-Hour Increments
- Instructors Previous History in Offering This or Similar Course at Other Venues

In addition to the proposal please attach a short form CV for each instructor, including demonstration of relevant expertise by education and training, publications and presentations, and experience in course instruction.

- This message was created by Koneru Ramakrishna (k.ramakrishna@motorola.com)



Site for HDP'2 Meeting

HDP-2002 High Density Packaging

(June 30-July 3, Galaxy Hotel, Shanghai)

Jointly Organized by DaimlerChrysler SIM Technology and Chalmers University of Technology, Sweden

In Cooperation with IEEE-CPMT Society, USA Society IEEE CPMT Sweden Chapter -- Shanghai Institute of Microsystems and Information Technology

Announcement and Call for Papers

Electronics manufacturing, assembly and packaging technology is playing a key role for the progress of the microelectronics industry in the world. China is not an exception. Therefore, many multinational companies are establishing new facilities in China for expanding their global business and interest. Following the successful previous conferences, we are proud to announce the Fifth International IEEE Symposium on High Density Packaging and Component Failure Analysis in Electronics Manufacturing (HDP'02).

The Symposium will cover the **following areas and subjects:**

- High density packaging including electronics and opto-electronics packaging, CSP, BGA, Flip-chip, Chip on Board, Surface Mount Technology and other novel emerging technology
- High density substrate including integrated passives and active devices
- MEMS design, packaging and assembly
- Electronics manufacturing issues
- Component failure analysis techniques including non-destructive X-ray, ultrasonic microscopy, IR-microscopy etc.
- Simulation and modeling for packaging and electronics manufacturing processes
- Thermal management
- Environmental design and materials development including life cycle analysis and end of life strategy etc.
- Cost reengineering, improvements and analysis for electronics packaging processes and products

Documentation: The documentation from the Symposium will be published in a proceeding with CD ROM with a full length papers (max 12 A4 pages) in English.

Journal publication: In addition, high quality papers will be selected for consideration to be published as special editions of the IEEE CPMT Transactions, "Soldering and Surface Mount Technology" or Journal of Electronics Manufacturing

Languages: English will be used. Simultaneous translation into Chinese is made to suit the Chinese delegates.

Symposium Chair: Xiaoming Xie, DaimlerChrysler SIM Technology Co., Ltd, China.

Symposium Co-chair: Johan Liu, Chalmers University of Technology, Sweden.

You are welcome to submit an abstract with max 300 words that cover the topic, experimental approach, results and conclusions for the paper by March 25, 2002 to Dr. Xiaoming Xie at xiaoming.xie@daimlerchrysler.com. Notification of abstracts will be made by April 5, 2002, Final paper is requested by April 30, 2002.

We are also interested in having exhibitors from materials, equipment suppliers to exhibit their products.

System Packaging Workshop

The TC-14 Systems Packaging Committee Spring workshop Program is now available. The meeting is from May 14 - 16 and will be held in the Research Triangle Park in North Carolina. The registration fee will be \$ 275 and the hotel daily rate is \$115, Registration information is posted on the web site.

Look to the web site for more information

2002 US Systems Packaging Workshop

Address: <http://www.ewh.ieee.org/soc/cpmt/tc14/usspws02.html>

Technical Program

May 14 – Tuesday - - Registration: 10:00 - 11:45 AM

Lunch: 12:00 to 1:00 PM

1:15 - 5:00 PM

Session 1: Optoelectronic Packaging

Richard LaBennett, MCNC & Glenn Rinne, Unitive

Optical MEMS Test Challenges and Solutions

Joe Schneider, Advent Optronics

Integration vs. Hybridization of Optoelectronic Modules

Paul Magill, JDS Uniphase

Assembly of 2-D VCSEL Arrays Using Flip-chip Packaging Methods

Alan Huffman, Richard LaBennett, Salvatore Bonafede, Chad Statler; MCNC

Challenges in Optoelectronic Packaging

Mohan Kirloskar, Velio Communications

The Evolution to Optics in Printed Circuit Boards

David Hass, Sanmina

Polymer OLED Overview

Allan Beikmohamadi, DuPont

5:30 PM – Reception - - 6:45 PM - Dinner

8:00 - 10:00 PM

Keynote: The Semiconductor-Packaging Partnership

Evan Davidson, IBM

Session 2: RF Packaging

Scott Best, Coventor - - Tim Mobley, Dupont

High Frequency, Integrated 3-D Packaging

Jim Logothetis, Merrimac Industries, Inc.

Characterization, Design, and Applications of RF LTCC Components

--R. F. Drayton and D. Kollmann, University of Minnesota, D.I. Amey, B.E. Taylor, T.P. Mobley, and L.A. Bidwell; DuPont Microcircuit Materials

MEMS Relays for RF Applications

Henry Wynades, JDS Uniphase

May 15 – Wednesday - - 7:00 to 8:15 AM - Breakfast

8:30 - 11:45 AM

Session 3: Medical / Bio Packaging

Monty Reichert, Duke University--Mark Johnson, Biotronik Inc.

Bioactive Coatings for Microelectronic Devices

Stephen Massia, Department of Biomedical Engineering - Arizona State University

Packaging of Neuroelectrodes

Patrick Wolf, Duke University

Technical Challenges in Developing a Wireless Communications System for Implantable Medical Devices

Mark Johnson, Biotronik USA

Congestive Heart Failure Monitoring Utilizing Wireless Blood

Pressure-Weight Scale System -- Suresh B. Neelagaru, MD;

Cardiac Electrophysiologist, CareMatix

Biocompatible Coatings for Implantable Medical Devices

Helmut Eckhardt, Premetic Inc.

Medical Implants & Other Biomedical Devices Using Microflex

J-Uwe Meyer, Fraunhofer Biomedical Technologies

Session 4: Applications

Bob Large, Lambda Tech., Ted Tessier, Amkor Technologies

Advancements in RFID, Michael Arneson, Matrics

1:15 PM - Plant tours of Unitive, MCNC and Dupont

5:30 PM – Reception -- 7:00 PM - Dinner

7:45 - 10:00 PM

Invited

Packaging of a MEMS Gyroscope

Dimitry Grabbe, Worcester Polytechnic Institute

Session 5: Signal Integrity

Paul Franzon, North Carolina State University

Bob Evans, Cisco Systems Inc.

ASIC System Timing and Signal Integrity Methodology at Cisco Todd

Westerhoff; Hammerhead Networks, Billerica, Mass. --Real

Pomerleau; Cisco Systems, RTP, NC

High-Speed Serial Communications Interfaces

Clay Cranford; IBM, RTP, NC

Future Trends in the Electrical Performance of Connector Systems

Jay Diepenbrock, IBM, RTP, NC

May 16 – Thursday - - 7:00 to 8:15 AM - Breakfast

8:30 - 11:59 AM

Session 6: Planar Optical Interconnect

Richard Otte, Promex Ind.--Bruce Booth, Optical Cross Links

Silicon on Sapphire Planar Waveguides

Harry Charles; Johns-Hopkins University, Baltimore, Maryland

Polymer Based Waveguides

Bruce Booth, Optical Cross Links, Inc.

Active Planar Waveguides

Peter Brooks; Symmorphix, Inc., Sunnyvale, CA

The Role of Optical Interconnect vs. Electrical Interconnect

Bala Natarajan, Intel Corporation, Invited

Optical Interconnection Technology on the Printed Circuit Board Level

Elmar Griese; Siemens, Paderborn, Germany, Invited

Issues Related To Utilizing Planar Optical Backplanes

Richard Otte; Promex Industries, Inc.



submitted by
John Balde,
CPMT Liaison to
Systems
Packaging

Announcement

3rd International Conference on Thermal and Mechanical Simulation in (micro-) Electronics **EUROSIME 2002**

www.eurosime.com -- April 14 – 17, 2002
Paris, France

EuroSimE 2002 will address the results of both fundamental research and industrial application for thermal and mechanical solutions of (micro)-electronics, focussing on advanced simulation and experiments technologies. The aims of this conference:

*Promote further development and application of advanced simulation methodology and experiment technology for electronic industry

*Disseminate competence and results obtained from relevant research projects

*Promote the integration and co-operation of competencies at international level

*Strengthen communication and co-operation between industry, universities, and research institutes

Courses (Sunday April 14th 2002):

****Practical Application of Computational Fluids Dynamics (CFD) Analysis to the Prediction of Board-Mounted Electronics Heat Transfer**

Peter Rodgers, Ph.D., Electronics Thermal Management, Ltd.

****Thermomechanical Reliability of Microelectronic Packaging**

Jianmin Qu, Ph.D., Professor in Mechanical Engineering at Georgia Institute

****Thermo-mechanical durability of lead free solders**

Abhijit Dasgupta, Professor, Mechanical Engineering, University of Maryland

****State-of-the-art and trends in advanced packaging**

Rolf Aschenbrenner, Fraunhofer Institut für Zuverlässigkeit und Mikrointegration, Berlin, Germany

Advance conference program (April 15-17, 2002):

Session 1 : Trends in microelectronics

Session 2 : The state of the art in thermo-mechanical solutions for microelectronics

Session 3 : Virtual prototyping

Session 4 : Reliability of solder interconnections

Session 5 : Thermal design and modeling

Session 6 : Education

Session 7 : New modeling methodologies

Session 8 : Application and devel. of thermal modeling

Session 9 : Interface strength

Session 10 : Thermal performance modeling & sim.

Exhibitors special session

Session 11 : Materials characterization and modeling

Session 12 : Modeling for new technologies

Session 13 : Process and reliability modeling

Session 14 : Design for reliability

More information: <http://www.eurosime.com/>,
compete@mta.fr, tel.: +33 1 4451 7400

ECTC Short Courses- May 28

Short Course Committee: Larry Mann-chair, Ron Scotti, Al Puttlitz

There will be 14 Short Courses in Total:

Morning:

No.	Title
1	Fiber-Optics Structures: Design for Reliability Ephraim Suhir
2	RF/Wireless Packaging: Status and Challenges – Part 1 Manos Tentzeris and Joy Laskar
3	Polymers for Electronic Packaging – Materials, Processes, and Reliability: Part 1 – C. P. Wong The Fundamentals of Packaging and Materials Science & Engineering
4	Optoelectronics Components and Modules for Datacom & Telecom, Bill Ring
5	Microelectronics Packaging and Interconnections – A Worldwide Perspective, Jan Vardaman
6	Power Packaging Techniques, Douglas C. Hopkins
7	Wafer Scale Packaging, Patrick Thompson

Afternoon

8	RF/Wireless Packaging: Status and Challenges – Part 2, Manos Tentzeris and Joy Laskar
9	Polymers for Electronic Packaging – Materials, Processes, And Reliability: Part 2, C.P. Wong
10	Active Optical Components, Torsten Wipiejewski
11	System on Package “SOP”, Rao Tummala
12	Advanced Organic Substrate Package Design and Manufacturing for RF & Broadband Applications, Hassan Hashemi
13	Designing MEMs for Reliability, Herb Shea, Suzanne Arney & Arman Gasparyan
14	Micovias & Wafer-Level Chip Scale Packages for Low-Cost High Density Interconnects, Ricky Lee

The short courses cost \$325 for one or \$525 for one each morning and afternoon course. You avoid the delay of on-site registration by doing advanced registration.

See [www.ectc.net/reg.htm]

This is the best place to get yourself or your boss up to speed on CPMT Society technology. Sign up today.



**Al Puttlitz,
CPMT Vice-
President
of
Education**

Forthcoming CPMT Conferences

VP Jim Morris

2002

Wafer Level Packaging Workshop

Atlanta GA March 1-3, 2002

Contact: wlp@ee.gatech.edu www.prc.gatech.edu

8th International Symposium on Advanced Packaging Materials

Atlanta GA March 3-6, 2002

Contact Rajen Chanchani chanchr@sandia.gov

Jianmin Qu jianmin.qu@me.gatech.edu 404-894-5687

Semiconductor Thermal Measurement & Management Symposium

San Jose CA March 12-14, 2002

Contact: Bonnie Leigh Crystall cscomm@earthlink.com

(520)323-2870 fax: (520)323-2863

<http://thermengr.com>

Academic Packaging Conference

Dresden, Germany 19-22 March

Contact: Klaus Wolter wolter@iet.et.tu-dresden.de

Thomas Zerna academic2002@iet.et.tu-dresden.de

www.iet.et.tu-dresden.de/education2002/index.html

22nd Capacitor & Resistor Technology Symposium (CARTS 2002)

New Orleans 25-29 March 2002

Contact: CARTS 1-256-536-1304 fax: 1-256-539-8477 www.cti-us.com

EuroSimE 2002

Paris, France 15-17 April 2002

Contact: Olivier de Saint Leger Compete@mta.fr

+33-1-44517400 fax: +33-1-44517401

Bart Vandeveld vandevel@imec.be

+32-16-281-513 fax: +32-16-281-501

www.eurosim.com

Tutorial on Flip Chip and Chip Scale Package

in Munich during Semicon Europe

April, 15 - 16, 2002

Organizer: PacTech GmbH

4th International Workshop on Area Array Packaging Technologies

in Berlin, after Semicon Europe

April, 22 - 23, 2002

Organizer: IEEE CPMT - German Chapter

2002 International Conference on Electronics Packaging (ICEP)

Tokyo, Japan 17-19 April, 2002

Contact: 2002 ICEP Secretariat imaps-j@jiep.jp

<http://www.jiep.or.jp/index.html>

Symposium on Design, Test, Integration & Packaging (DITP 2002) of MEMS/MOEMS

Cannes-Mandelieu, France 5-8 May 2002

Contact: http://tima.imag.fr/news/orga_conf.asp (second page)

6th IEEE Workshop on Signal Propagation on Interconnects (SPI)

--May 2002

Contact: Flavio Canavero +39-011-564-4060 fax: +39-011-564-4099

canavero@polito.it

Ivan Maio +39-011-564-4100 fax: +39-011-564-4099 maio@polito.it

www.tet.uni-hannover.de/SPI

25th International Spring Seminar on Electronics Technology (ISSE'02)

Prague, Czech Republic 11-14 May, 2002

Contact: Pavel Mach mach@feld.cvut.cz

CPMT TC-14 System Packaging Workshop

Research Triangle Park, May 14-16, 2002

Contact: Dan Amey email: Daniel.I.Amey@usa.dupont.com

52nd Electronic Component & Technology Conference

San Diego CA May 28-31, 2002

Contact: www.ectc.net

8th Intersoc. Confer. Thermal & Thermo-mechanical Phenomena in Electronic Syst's (I-THERM)

San Diego, CA May 29 - June 1, 2002

Contact: Paul Baltes; epd@enr.arizona.edu

Univ. of Arizona; Engrg. Prof. Development; 1224 N. Vine Ave.;

Tucson, AZ 85719-4552

Tel: +1 520 621 5104; fax: +1 520 621 1443

2002 Intensive Course on Electrical Contacts

June 10-13, 2002 at Omni Shoreham Hotel, Washington, D.C.

www.ewh.ieee.org/soc/cpmt/tc1/

POLYTRONIC 2002

2nd International IEEE Conference on Polymers & Adhesives in

Microelectronics & Photonics

Zalaegerszeg, Hungary June 23-26, 2002

Contact: Peter Bojta bojta@ett.bme.hu

www.ett.bme.hu/polytronic2002

4th International Symposium High Density Packaging & Component Failure Analysis (HDP'02)

Equatorial Hotel, Shanghai, China June 30-July 3, 2002

Contact: Tiebing Wang tiebing@pe.chalmers.se

Xiaomin Xie xmxie@itsvr.sim.ac.cn

48th IEEE Holm Conference on Electrical Contacts

Oct 21-23, 2002 Holiday Inn International Drive, Orlando Florida.

www.ewh.ieee.org/soc/cpmt/tc1/

11th Topical Meeting on Electrical Performance of Electronic Packaging, EPEP'02

Oct. 21-23, 2002 in Monterey, CA

Contact Paul Baltes: epd@enr.arizona.edu

Web: www.epep.org

Future Directions in IC and Package Design Workshop

Oct. 19, 2002 in Monterey, CA.

Contact: A. Deutsch deutsch@ieee.org

Madhavan Swaminathan madhavan.swaminathan@ece.gatech.edu

Web: www.epep.org

Tutorial on Flip Chip and Chip Scale Package

in Munich during Electronica

November, 11 - 12, 2002

Organizer: PacTech GmbH

6th VLSI Packaging Workshop of Japan

November 12-14, 2002

Kyoto, Japan -- contact:

<http://homepage1.nifty.com/ieeetokyo/chapter/cpmt/vlsip.html>

4th International Workshop on Area Array Packaging Technologies

in Berlin, after Electronica.

November, 18 - 19, 2002

Organizer: IEEE CPMT - German Chapter

4th International Workshop on Smart Card Technologies & Applications

Germany November 18-20

Contact: elke.zakel@ieee.org 49-(0)-30-467-815-55/fax 49-(0)-30-467-

815-51

www.pactech.de/CPMT-Germany

4th Electronics Packaging Technology Conference (EPTC'2002)

Singapore December, 2002

Contact: Jasmine Leong ept@pacific.net.sg

Charles Lee Charles.Lee@infineon.com

<http://cicfar.ee.nus.sg/eptc.html>

International Conference on Electronics Packaging

April 17 - 19, 2002
Dai-ichi Hotel Seafort
Tennoz Isle, Tokyo, Japan

Theme: "New Packaging Waves from Asia"

Sponsors: IEEE CPMT Japan Chapter and JIEP/IMAPS Japan.
Information Contact: 2002 ICEP Secretariat imaps-j@jiep.jp
<http://www.jiep.or.jp/index.html>

April 17

WAI: High Speed / High Frequency Packaging

Chairperson: R. Tummala (Georgia Institute of Technology), O. Ibaragi (ASET)

"Directions in RF Module Packaging" (Session Invite), S.-K. Chiang, Prismark Partners / U.S.A.

WBI: Pb-free Solders

Chairperson: M. Otsuka (Shibaura Institute of Technology), H. Sawai (Oki Electric Industry)

"JIEP Low Temperature Soldering Project" (Session Invite) K. Suganuma, Osaka University / Japan

Invited Speech

Chairperson: S. Denda (Nagano Prefectural Institute of Technology), K. Hashimoto (Fujitsu Laboratories)

"Device Packaging in the Year 2020", Dr. C. E. Bauer, TechLead Corporation / U.S.A.

Asia Session April 18

TA1: Advanced Packaging

Chairperson: C. E. Bauer (TechLead), M. Tsukamoto (Matsushita Electric Industrial)

"Recent Advances in Integral Passives Research at Georgia Tech" (Session Invite), R. R. Tummala, S. Bhattacharya, S. Dalmia, P. M. Raj, T. Ogawa, S. H. Lee, R. Mani, A. Bavisi, F. Ayazi, Georgia Institute of Technology / U.S.A.

The Growth of the Flip Chip Market: New Applications and Developments (Session Invite), E. J. Vardaman, TechSearch International / U.S.A.

TB1: Plating

Chairperson: E. Zakel (Pac Tech), A. Okuno (Sanyu Rec)

TA2: Optoelectronics

Chairperson: S.-K. Chiang (Prismark Partners), Y. Ando (Fujikura)

TB2: Materials

Chairperson: Z. Kachwalla (CSIRO), I. Kaneko (Musashi Institute of Technology)

TA3: Interconnection I

Chairperson: J. Maattanen (Elecoteq Network), H. Matsubara (Sharp)
"High Speed Laser Solder Jetting Technology for Optoelectronics and MEMS Packaging" (Session Invite), E. Zakel, L. Titerle, T. Oppert, R. Blankenhorn, Pac Tech / Germany, U.S.A.

TB3: Simulation

Chairperson: H. Nishida (International Display Technology) E. Takagi (Toshiba)

"Study of Beyond GHz Signal Integrity Under TEM Wave Mode Analysis in Multi-channel Transmission Lines" (Session Invite), K. Otsuka, C. Ueda, Meisei University, Y. Odate, T. Usami, University of Tokyo / Japan

April 19

FA1: 3D Packaging

Chairperson: M.-K. Iyer (Institute of microelectronics), S. Uegaki (Kyocera)

FB1: Interconnection II

Chairperson: Y.-B. Sun (Kyonggi University), I. Watanabe (Hitachi Chemical)

"New Concepts in Flipchip Bump Technology" (Session Invite), S. Denda, Nagano Prefectural Institute of Technology / Japan

FA2: Design and Testing

Chairperson: S.-L. Fu (I-Shou University), S. Oka (Mitsubishi Electric)

FB2: Thermal Management

Chairperson: C. Zardini (University Bordeaux I), S. Kitajo (NEC)

FA3: Substrates

Chairperson: H. Quinones (Asymtek), H. Hozoji (Hitachi)

FB3: Reliability

Chairperson: F. Uchikoba (TDK), T. Kobayashi (Tohoku Epson)

Area Array Packaging Technologies

4th International Workshop on Flip Chip, CSP, Wafer Level packaging

April, 22-23, 2002, Berlin, Germany

Special Sessions:

Optoelectronics Packaging

MEMS Packaging

Organizer: IEEE CPMT German Chapter

Conference Chair: Dr. Elke Zakel, PacTech GmbH (D)

For complete program, registration forms, and more **information**:

<http://www.pactech.de/CPMT-Germany>

Sample of Advanced Program

April 22

Invited Speakers:

Lubomir Cergel, Motorola, Switzerland

Horatio Quinones, Asymtek, USA -- "Fluid Jetting for Next Generation packages"

Ken Gilleo, Cookson Electronics, USA

Papers

*System in Package Assembly: Required Technology Toolbox, Marcos Carnezos, ChipPac, USA

*Thermal Characterization of Flip Chip Connected Devices:

Experimental Data and Simulations, Carla Bassani, Alcatel, Italy

*New Material Deposition Technologies and Concepts for Advanced Packaging, J. Kloser, EKRA, Germany

*From Wafer Bumping to Wafer Level CSP, Elke Zakel, PacTech GmbH, Germany

*Application of a Visual Bumped Wafer Inspection System, Ignace Verhamme, ICOS Vision Systems, Belgium

*Real 3D Bump Inspection, Matthias Strossner, Siemens AG, Germany

*High Accuracy Equipment, Gunther Kurbis, Finetech, Germany

*Wafer Level Solder Sphere Printing, J. M. Scheer, Philips CFT DEK, Belgium

*Manufacturing Method and Properties of Soft Solder Spheres for BGA packaging, Muriel Graff, OMG AG, Germany

*SuperCSP - A Wafer Level Chip Size package Technology, Claudio Truzzi, ConvergiX, the Netherlands

April 23

- *Optoelectronics and Automation for First Level Package Assembly, Richard Boulanger, Universal Instruments, USA
- *Packaging of Optoelectronic and MEMS Devices with Fluxless Laser Solder Ball Jetting, Thomas Oppert, PacTech GmbH, Germany
- *Application of AuSn Solder for the Packaging of Optoelectronic Modules, Matthias Hutter, Fraunhofer Institute, Germany
- *Study of the Electrical Performance of Chip-on-Board Devices, Alla Cordery, Oxford, UK
- *Single Pass Reflow Encapsulant- New Advanced Material for Flip Chip Assembly, Chad Showalter, Kester Solder
- *Parameter Study for Solder Joint Reliability of Underfilled Flip Chip Assemblies, Bart Vandervelde, IMEC, Belgium
- *Residue Life Time Prognostics, H. Hieber, ICR Jena, Germany
- *The Reliability of Lead-Free Solder Paste in Mechanical Cycling, Kari Maatanen, Pori School of Technology and Economics, Finland
- *Simulation Tool for Optimizing Heat and Current Allocation in High-Power-Semiconductors..., Frank Sauerland, Fraunhofer Institute, Germany
- *Flip Chip Applications in Smart Cards, Ghassem Azdasht, Smart Pac GmbH, Germany
- *Plasma Cleaning for Microelectronic Packaging, Frank Huysmans, March Plasma Systems, USA

**Dr. Elke Zakel,
Chair Area
Array
meeting.
PacTech
GmbH**



IEEE Virtual Museum

Designed as visual tutorials for pre-college students, the IEEE virtual museum is available at [<http://www.ieee.org/museum>]. The history of the discovery of electricity is one of the main features in this evolving exhibit.

52nd Electronic Components & Technology Conference Highlights

The Advance Program for the 52nd Electronic Components & Technology Conference at the Sheraton **San Diego** Hotel & Marina has been completed and will feature almost **300**

technical papers presented by leaders in their field representing countries from around the world.

The conference is organized into 38 technical sessions, focusing on leading edge developments and technical innovations in several areas, including: low cost and high performance optoelectronic packaging, systems on package technologies, RF and MEMS packaging, high performance package design, simulation and manufacturing, dielectrics, adhesives, and underfill modeling and processes, flip-chip and Pb-free interconnections, wafer-level and chip scale packaging, and reliability test methods and design.

Two technical sessions will specifically explore topics related to engineering education and **web based packaging education** for the 21st century.

In addition to the traditional sessions, **two Poster Sessions** will be offered on Wednesday, May 29 and Thursday, May 30 to give more opportunity for authors and attendees to interact and discuss specific topics.

The **Technology Corner** on Wednesday afternoon, May 29 and Thursday, all-day May 30 will feature exhibits of the newest products and services available.

The 52nd ECTC will feature a **Tuesday evening Panel Session** on "Focus on Component Technology Developed in San Diego, California" organized by Dr. Steve Adamson and Dr. Rao Bonda and a **Wednesday evening Plenary Session** organized by Dr. Phil Garrou.

An all-day educational seminar will be offered on Tuesday, May 28, 2002 consisting of 14 short courses. Dr. Larry Mann and the short course committee have brought together industry experts from a wide variety of disciplines to offer state-of-the-art technology reviews and updates in condensed half-day and full-day formats. Topics to be covered include:

RF/wireless packaging, optoelectronic packaging, optical networks, wafer scale packaging, advanced organic substrate design for RF applications, MEMS design, and polymers for electronic packaging. These courses are eligible for Continuing Education Unit (CEU) credits.

ECTC attendees can receive Conference Proceedings as a CD-ROM or a printed version. Both the CD-ROM copy and printed may be purchased for an additional \$50 charge.

Short Course, ECTC, CPMT and Program Chairman luncheons will be held May 28 - 31, 2002 with guest speakers each day.

The 52nd ECTC Advance Program is available from:

Jim Bruorton, ECTC Publicity Chairman
c/o KEMET Electronics Corporation
P.O. Box 5928
Greenville, SC 29606
Telephone: (864) 963-6621
Fax: (864) 963-6444
Email: margieballinger@kemet.com

or you may visit the **ECTC website** at www.ectc.net and download the information and program from that location.

- Margie Ballinger, KEMET Electronics Corp.



Call for Papers



The 6th VLSI PACKAGING WORKSHOP of JAPAN Nov. 12-14, 2002

Kyoto Research Park, Kyoto, Japan

Sponsored by the IEEE CPMT Tokyo Chapter and the National Institute for Standards and Technology

The VLSI Packaging Workshop of Japan held every second year since 1992 in the ancient capital of Kyoto has become a well-known international workshop of advanced packaging technologies. To monitor the latest trend and focus on the future target, the committee strongly urges you to attend this workshop and participate in the discussion. Bring your latest research results and exchange your opinion with internationally acclaimed experts from industry and academia. Beside engineers involved with packaging, wafer processing experts and circuit designers are cordially invited to bring their breakthrough ideas to solve the current problems of SiP and SoC. Emerging technologies and latest designs in the following areas are of interest to the participants.

- | | |
|--|--|
| + Advanced Fine Pitch Packaging | + Wafer Level Packaging |
| + 3D Packaging & COC (Chip on Chip) | + Manufacturing Technology |
| + Micro Bumping Technology | + Pb Free Interconnections |
| + Laminated Materials & Processing | + Materials for High Speed Application & Wafer Process |
| + RF Components & Modules | + Integrated Passives |
| + Packaging for Optoelectronics | + MEMS Packaging Technologies |
| + Failure Mechanisms & Reliability Improvement | + Cu Chip Assembly and Packaging Challenges |

The workshop will be held in English and each oral presentation will be allowed 30 minutes including 10 minutes for discussion. Authors who give outstanding papers will receive official recommendations for paper submission to IEEE Transactions on CPMT by the Japan Chapter and the Workshop Committee. This workshop will be held at a new location (new KRP facility), and the commercial booths for demonstrating products are available adjacent to the workshop hall.

Submission of abstracts:

Those who wish to contribute to the workshop should send a two page extended summary* of their paper (including figures) to the Program Chair **by June 3, 2002**. The title of the paper as well as the names and affiliations of all authors must be appeared on the summary. If the paper is accepted, the summary shall be written to fit in a four-page format for the workshop's proceedings **by September 2, 2002**. Notification of acceptance will be given **by July 1, 2002**. Please consult our website; <http://homepage1.nifty.com/ieeetokyo/chapter/cpmt/vlsip.html> for more detailed information on the format, the location and the facilities. We are looking forward to your participation. [*: Preferable to follow the format]

Program Chair:

Tomoshi Ohde, Sony Semiconductor Kyushu Corp.
3319-2, Owara, Kunisaki-machi, Higashikunisaki-gun,
Oita-PRF, 873-0511, Japan
Email: Tomoshi.Ohde@jp.sony.com
Phone: +81-978-72-5160, Fax: +81-978-72-5086

General Chair:

Atsushi Nakamura, Hitachi, Ltd.
Email: nakamura-atsushi4@sic.hitachi.co.jp

Vice Chair:

Masahiko Kohno, Dow Chemical Japan
George Harman, NIST

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