Components, Packaging, and Manufacturing Technology Society Newsletter

The Global Society for Microelectronics Systems Packaging

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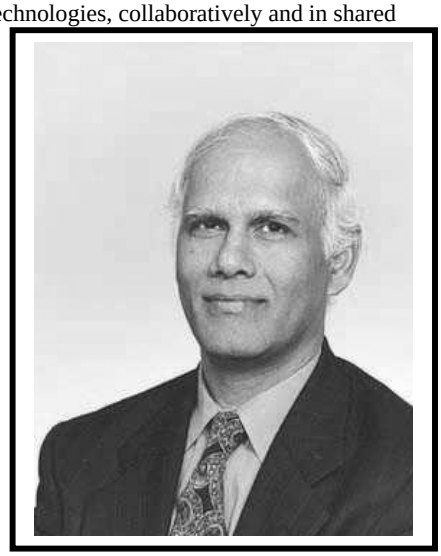
PRESIDENT'S REPORT

Who is minding the store for "next generation research" now that industry is short term focused and manufacturing is going to China?

It has been said many times and in many ways. Private industry is focused on cost- cutting and short-term profits, to please its shareholders. Manufacturing is moving "off-shore" (away from the historic system design companies). So now who is taking on the responsibility to do the leading-edge research that feeds into next generations of electronic products? Contrary to the contemporary hype, brand new technologies take almost a decade to go from concept to marketplace. Look at TFT, MCM, Flipchip or SMT. They have all taken approximately 10 years. So, who is doing leading-edge research that goes into products 5 to 10 years from now?

One answer has to be Universities and National Labs, funded by governments in a pre-competitive environment. But, they are not usually very effective in transferring the newest technologies to private industry. This is due to two factors: (1) Lack of trust by the industry that they can put these organizations in the critical path of their product development needs, and (2) the lack of team and system-approach culture. One way to overcome these factors is for industry to be an integral part of these two organizations by having its engineers partner with Universities and National Labs, as if these are their remote R & D organizations. These partnerships can lead to defining roadmaps, exploring new frontier technologies, collaboratively and in shared fashion, by means of joint projects, and demonstrate proof-of-concepts, consistent with the industry's need to be competitive. How about IP issues then? The IP issues should not prevent partners from working with each other for mutual benefit. The roles and responsibilities of Universities are complementary to Industry. Their job is to create new knowledge and new human resources to benefit the Society. The industry's job is to use this knowledge and these human resources so created by the universities, to design, develop and manufacture competitive products.



A good example is what we do at Georgia Tech in the PRC Program. Funded by NSF, we bring about new paradigms in Packaging at two fronts: (1) to provide unlimited connections to the IC so it is used very efficiently, and (2) to go beyond ICs to form end-product systems, integrating and interconnecting all the components necessary to form that system. We are exploring a new frontier called SOP (System-on-Package) when everybody else is pursuing SIP or SOC for short term benefits. The latter are limited by CMOS IC technologies in that while CMOS is excellent for digital and moderate frequency analog switching, it is not so good for RF or Optical component integration. In addition, most of us foresee Moore's Law fundamental limits in CMOS. The SOP optimizes IC and package-both at design and fabrication levels, thus leading to cost- and performance-effective end-product systems . The concept leads to "Package, and not the board, as the end product System".

Thus, the next generation of electronics technology is being addressed despite the vast changes in the global business landscape.

ECTC is a great success despite Economy, war and SARS.

The ECTC organizers should be congratulated for what they did in New Orleans in May. They have put together an outstanding Program: 300+ technical papers, 14 Professional Development Courses drawing 261 students, 42 technology exhibits and a number of educational programs such as academic conference and student programs. All in all, 726 attendees participated from Asia, Europe and the US. In addition, there were plenary sessions which introduced new topics such as strained silicon and polymeric transistor technology, and a panel discussion that debated how the packaging and manufacturing electronics industry was performing long range R&D**.**

CPMT forms Nano- Packaging Technical Committee.

A new technical committee called Nano Packaging is introduced to stimulate global research. This TC is already planning to hold its first International Workshop in Nano and Bio- packaging as well as start a session at next year's ECTC in Las Vegas.

Welcome new BOG members

It is my pleasure to welcome four new BOG members:
Li Li from Motorola,
David Whalley from Longborough University, UK,
Tim Adams from Dow-Corning, and
Ricky Lee from University of Science and Technology, Hong Kong.

-Rao Tummala, CPMT President

CPMT OFFICERS

President -- Rao Tummala, +1 404 894 9097
Technical VP -- Phil Garrou, +1 919 248 9261
Administration VP -- H. Anthongy Chan, +1 408 924 3656
Treasurer -- John Segelken, +1 540 961 1685
VP Publications -- Paul B. Wesling, +1 408 252 9051
VP Conferences -- James Morris, +1 607 777 4774
VP Education -- Albert Puttlitz, FAX +1 802 879 0466
Senior Past President -- Ralph Wyndrum, +1 732 219 0005
Junior Past President -- John Stafford, +1 602 413 5509
Secretary -- Ron Gedney, +1 703 834 2084
Executive Director -- Marsha Tickman, +1 732 562 5529
IEEE VP TAB -- Ralph Wyndrum, +1 732 219 0005

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L. Merrill Palmer	Walter J. Trybula
E. Jan Vardaman	David C. Whalley

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Distinguished Speakers -- A. F. Puttlitz, FAX +1 802 879 0466
Fellows Search--Rao Tummala-rao.tummala@ee.gatech.edu & David Palmer-d.palmer@ieee.org
Fellows -- C. P. Wong, cp.wong@ieee.org
Constituition & Bylaws -- Tony Mak, +1 972 371 4364
Finance -- Ralph Wyndrum, Jr., r.wyndrum@ieee.org
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Standards -- "Jack" Balde, +1, 908 788 5190
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Membership -- Ralph Russell, cpmt-membership@ieee.org
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Nominations -- John Segelken, +1 540 633 5781
International Relations -- Leo Feinstein, +1 508 870 0051; Europe -- Ephraim Suhir, +1 908 582 5301; Far East -- W. T. Chen, +65 874 8110
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Next News Deadline: September 5, 2003

CPMT SOCIETY NEWSLETTER

Editor: David W. Palmer, email: d.palmer@ieee.org, FAX +1 505 844 7011, Tel: +1 505 844 2138
Composition: Alina Deutsch: deutsch@us.ibm.com
Proofreading: S. Puccetti & Amity Ming

CPMT Archival Publications

Publications VP: Paul Wesling, email: p.wesling@ieee.org, Tel: +1 408 252 9051.
Transactions-CPT editor, Avram Bar-Cohen, Univ. of Maryland, 2181B Martin Hall, College Park, MD 20742 USA, Tel: +1 301 405 3173; email barcohen@eng.umd.edu
Transactions-AdvP editor; G. Subbarayan, Purdue University, ME Department, Tel: +1 765 494 9770; email ganeshs@ecn.purdue.edu
Transactions EPM editor, Walter Trybula, Tel +1 512 356 3306, email w.trybula@ieee.org

Technical Committee Chairpeople

TC-1 Electrical Contacts, Connectors and Cables-- Gerald Witter, Chugai, +1 708 244 6025
TC-2 Discrete and Integral Passive Components— Leonard Schaper, Univ. of Arkansas, +1 501 575 8408
TC-3 IC and Package Assembly – Michele Berry, Intel michele.j.berry@intel.com
TC-4 Manufacturing Design & Process—Walt Trybula, SEMATECH, +1 512 356 3306
TC-5 Materials--Rajen Chanchani, Sandia Labs, +1 505 844 3482, r.chanchani@ieee.org
TC-6 High Density PWB packaging -- John Segelken, jsegelken@Actmicrodevices.com, and Connie Swager, swager@us.ibm.com
TC-7 Environmental Stress & Reliability Test--Kirk Gray, k.a.gray@ieee.org
TC-9 Thermal Management & Thermomechanical Design-- Tony Mak, Dallas Semi, +1 972 371 4364
TC-10 Fiber Optics & Photonics—Frank Shi, UC Irvine email: FGSHI@uci.edu
TC-11 Electrical Test -- Bruce Kim, Bruce.Kim@asu.edu, Tel: +1 480 965 3749
TC-12 Electrical Design, Modeling and Simulation-- Madhavan Swaminathan, G Tech, +1 404 894 3340
TC-13 Power Electronics Packaging--Doug Hopkins, SUNY Buffalo, +1 607 729 9949, d.hopkins@ieee.org
TC-14 Systems Packaging—Yoshitaka Fukuoka, weisti.fukuoka@rose.zero.ad.jp
TC-16 RF and Wireless-- Craig Gaw, Motorola, +1 480 413 5920, c.a.gaw@ieee.org
TC-17 MEMS and Sensor Packaging—Eric Jung, IZM Berline email: erju@izm.fhg.de
TC-18 Wafer Level Packaging—Michael Toepper, IZM Berline toepper@izm.fhg.de
TC-19 Education--Rao Tummala, G Tech, +1 404 894 9097
TC-21 Green Electronics Manufacturing and Packaging, Hansjoerg Griese, Email: griese@izm.fhg.de

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CALL FOR CANDIDATES

The CPMT Society is governed by a Board of Governors composed of officers, 18 elected members-at-large, and various committee chairs and representatives (see inside cover of paper Newsletter for details.)

Annually, Society members are asked to elect six members-at-large for a three-year term of office. Candidates for member-at-large are selected in two ways -- either by the Society Nominating Committee, or by petition.

If you are an IEEE and CPMT Society member in good standing and are interested in serving on the Board of Governors, you can automatically become a candidate via petition by following the procedures below.

The term of office for this election is 1 January 2004 through 31 December 2006. This volunteer positions requires two Board meetings each year: usually meeting the day after ECTC in May and in Dallas the day after ECTC paper selection in November. In addition, most Members-at-Large spend a few hundred hours a year volunteering for Board or Committee activities. IEEE advises that volunteers make sure they can fit these demands in their busy schedule before running for election.

** Prepare a petition that contains your name, member number, and statement of your qualifications for office.

** Provide lines for signatories. Each line should include space for a printed name, member number, and signature.

** Have the petition signed by a MINIMUM of 25 CPMT Society members in good standing (Student grade members are not eligible to sign.)

Membership status of all signatories will be validated. It is suggested that you gather more than 25 signatures in order to assure meeting the minimum required number of valid signatures.

** Submit your petition by no later than Friday, July 25, 2003 to:

CPMT Society Nominations Committee
c/o Marsha Tickman
IEEE CPMT Society Executive Office
445 Hoes Lane, PO Box 1331
Piscataway, NJ 08855-1331 USA
or FAX to 732-981-1769.

If you have questions or need additional information, contact Marsha Tickman at the above address, by phone at 732-562-5529, or by e-mail at

m.tickman@ieee.org.

Dennis Olsen, this year's Outstanding Contribution Award from our Society, surrounded by CPMT admirers. **3**

And The Winner is . . .

The historic French Quarter of New Orleans, Louisiana provided a festive backdrop for this year's CPMT Society Awards Luncheon on May 29, at the 53rd Annual Electronic Components Technology Conference (ECTC). Traditional Mardi Gras masks, beaded necklaces and zydeco music celebrated the traditions of the city and allowed the guests to have a little fun on their break from the technical sessions.

CPMT Society President, Rao R. Tummala praised the Society for giving "lagniappe." In New Orleans, lagniappe means "a little something extra," and is what the Society provides to the IEEE, to the industry, and especially to its members and participants. As he introduced the officers and guests at the head table, he took a moment to recognize each of them for their special contributions to the Society.

It was then time for the awards. Here is a list of the winners honored at this year's ECTC.

Dennis Olsen, consultant (USA), was presented this year's David Feldman Outstanding Contribution Award for his exceptional service to the CPMT Society and its conferences over the past 20 years. Formerly with Motorola, he earned recognition through a variety of distinguished awards, such as the Patent of the Year Award in 1993. Over the years, Dr. Olsen was issued five patents covering a broad spectrum of electronic packaging, ranging from a state-of-matter patent for lead-free solder alloy to a probe card for testing unencapsulated semiconductors for known good die applications. He continues to demonstrate exceptional service to the Society, the industry and its technology through active leadership in organizing conference programs, serving on numerous committees, and organizing and being elected as the 1st chair of the CPMT Society Phoenix, Ariz. Chapter. He is also a past president of the CPMT Society.

Thiam Beng Lim, deputy director at the Institute of Microelectronics in Singapore, won the Outstanding Sustained Technical Contribution Award for his leading-edge research in advanced packaging technologies and abilities to manage and transfer the electronic packaging research and development to the industry and other research organizations across the world. Dr. Lim has championed Singapore's influence in the electronics industry. His work and dedication have helped it evolve from a low-end high volume manufacturing industry to the development and manufacturing of leading-edge products competing with the best in the world. He is also a founding committee member of the prestigious IEEE CPMT Society's Electronics Packaging Technology Conference (EPTC) held in Singapore. Due to travel constraints this year, he was unable to attend the New Orleans ECTC award ceremony. However, the Society happily accepted the award on his behalf.

Mike McShane of Motorola (USA) and Paul Lin and Howard Wilson (formerly with Motorola) were awarded the

Exceptional Technical Achievement Award for co-inventing the PBGA package that resulted in new and revolutionary applications for electronic packaging technologies. The PBGA package is now accepted worldwide as the preferred packaging technology for new products. . The PBGA package technology has also driven a new supporting infrastructure, such as assembly and test equipment. In 2001, Mr. McShane was recognized as the Microelectronic Packaging Technologist of the Year by Advanced Packaging Magazine and MEPTEC. Mr. McShane was most recently the General Chairman of the 2002 ECTC, and an active senior member of IEEE for 13 years. He is also a past member of the CPMT Society's Board of Governors.He accepted the award on behalf of the team.

Emmanouil (Manos) Tentzeris of the Georgia Institute of Technology (USA) was presented with the Outstanding Young Engineer Award for his contributions to RF circuit design of high performance IC devices and to IEEE and CPMT Society-Sponsored conferences and activities. His numerous contributions include the development of the wavelet-based MultiResolution Time-Domain (MRTD) technique that allows for the system-level simulation of RF-Packaging structures with demonstrated significant savings in memory and execution time requirements on one and two order of magnitude, respectively with respect to the conventional full-wave simulation tools. MRDT was applied for the modeling and the evaluation of the most popular RF packaging structures, mainly of flip-chip, wirebonds and embedded passives, that led to the full-wave system-level analysis of packaged wireless multilayer modules for the first time ever. Prof. Tentzeris is a member of the CPMT Society, and a member of IEEE for over 13 years. He remains active in reviewing technical papers, organizing conferences and other volunteer-leader activities.

Paul Wesling, CPMT Vice President of Publications had the honor of announcing Jacobus D. van Wyk, Colin Kydd Campbell and Rengang Chen of Virginia Polytechnic Institute and State University (USA), as winners of the 2002 Best Paper Award for their paper entitled "Experimental and Theoretical Characterization of an Antiferroelectric Ceramic Capacitor for Power Electronics." It was published in the June 2002 issue of the IEEE Transactions on Components and Packaging Technologies. Unfortunately, the authors were unable to attend the conference. **Dr. Z. Liang** accepted on their behalf.

One student chapter was so impressive that The 2003 Chapter of the Year Award went to the CPMT Student Branch of the Polytechnic University of Bucharest (Romania), for its organization of outstanding programs for members through global collaboration and participation in technical conferences, student contests and local meetings. Paul Svasta, the chapter's advisor accepted the award on behalf of the student chapter leadership.

This year, there were four Special Presidential Recognition Awards presented. **George Harman** of the National Institute of Standards and Technology (NIST), USA, was honored for his dedicated service as a member of the CPMT Society Board of Governors, especially in the role of Fellows Committee Chair. **Johan Liu** of Chalmers University of Technology (Sweden) was lauded for his dedicated service to the CPMT Society's conference activities; especially as founder of multiple meetings that include Adhesives in Electronics, PEP and HDP. And the CPMT Society Technical Committee on Electrical Design, Modeling and Simulation was recognized for organizing outstanding technical activities in the areas of electrical design, modeling ad simulation for the benefit of the CPMT Society, its members, the industry and the academic community.

Madhavan Swaminathan, TC Chair from the Georgia Institute of Technology (USA), was on hand to accept the award for the Committee.

Finally, **Karl Puttlitz**, IBM (USA), was recognized for his election to IEEE Fellow for his development and leadership in the microelectronic packaging sciences and area array interconnection technology.

"The winning individuals, teams and chapters represent excellence in the industry, and the CPMT Society cordially congratulates them on their achievements," said Rao Bonda, Chair of the CPMT Society Awards Program.

--submitted by Kristine Martin (Potomac Communication) and Rao Bonda (CPMT Awards Chair)

SEMI Technology Symposium: International Electronics Manufacturing Technology (STS: IEMT), July 16-18, 2003

The New San Jose Marriott Hotel, 301 South Market Street

The STS: IEMT is an international forum on electronic components and systems manufacturing technology. It is the second largest IEEE/CPMT packaging conference in the United States, and offers a unique venue for engineers and scientists to present and publish their original work. The conference features technical papers on research, development and applications of manufacturing technology for electronic components, assemblies and systems that has been selected by a committee of experts.

STS: IEMT Keynote Speaker: Joseph Adam

Wednesday July 16, 2003, 9:00 AM - 9:45 AM

Vice President Technology Integration, Skyworks Inc. & Co-Chair, ITRS Packaging Technical Working Group

2003 ITRS Packaging Roadmap Overview

The talk will focus on the changing trends of package I/O counts, cost, frequency limits, power, and pitches both off-chip and off-package. The major technology challenges facing the industry in packaging substrates, design tools, new materials requirements, packaging of low K/Cu semiconductors, high frequency design will be described. Six emerging technology segments will be reviewed and the impact of these new segments on the industry will be discussed. These include System In Package, materials, embedded passives, substrates, optoelectronics packaging, and MEMS packaging. The impact that reduced packaging R& D spending and a sustained weak economy will have on the industry will be outlined.

STS: IEMT Session 201: Advanced Processing Technology

Wednesday July 16, 2003, 10:00 AM - 12:30 PM

Chairs: Frank Juskey, AIT, & Dr. Belgacem Haba, Tessera

The key to cost reduction in IC packaging is the implementation of state of the art materials and processes to lower manufacturing costs. This session will offer a diverse selection of papers dealing with laser singulation of packages, new flux and under fill application techniques for flip chip processing, advanced methods of locating packages relative to saw streets, and in situ monitoring for improved processing yields.

Laser Singulation / Dicing of Chip Scale and Silicon Wafer Scale Packages, Todd Lizotte, NanoVia, LP

Unique Fiducial Designs for CSP Singulation Process, Prakorn Vijchulata, AMD (Thailand) Ltd.

Precision Flux Deposition Techniques for Semiconductor Applications, Stuart Erickson, Ultrasonic Systems, Inc.

An Innovative Underfill Process for High-Speed SMT CSP BGA Flip Chip Assembly, James Jian Zhang, Georgia Tech

An Acoustic Sensor for Monitoring Microelectronics Packaging Manufacturing Processes, Frances Williams, Georgia Institute of Technology

Study of Non-Solder, Low Cost and High Performance Flip Chip QFN Package Using Ultra Thin Pd PPF, Se Chuel Park, Samsung Techwin Ltd.

STS: IEMT Session 202: Novel Wire Bonding Techniques

Wednesday July 16, 2003, 10:00 AM - 12:30 PM

Chairs: Paul Lin, & Peter Harper, Motorola Semiconductor

In order to implement Fine Pitch Wire Bonding (50 um pitch or less), many technical issues have to be resolved. Some are directly related to FPWB itself such as FPWB transducer, FP wire diameter and FP capillary. Others are indirect issues such as FPWB yield and its long term reliability, FP wire pull characterization even using in-situ ball shear monitoring. In this session, authors from IDM, end user, equipment & material suppliers and assembly contractor will jointly discuss practical solutions to these issues.

Reliability Ground Rules Change at <50 mm Pitch, Inderjit Singh, NVIDIA Corp.

The Challenge of Testing Ultra Fine Pitch Wire Bonds, Robert John Sykes, Dage Precision Industries Ltd.

Novel Ultrasonic Transducer Design for Fine-Pitch Wire-Bonding, Martin von Arx, ESEC SA

NoSWEEP Technology for Wire Bonding PBGA Applications, Andrew Hmiel, Kulicke & Soffa Industries

In Situ Ball Bond Shear Measurement Using Wire Bonder Bondhead, Jonathan Medding, ESEC SA

Effect on Leadframe Design on Aluminum Wire Bonding, Tan Joo Hong, Infineon Technologies Asia Pacific Pte Ltd.

STS: IEMT Poster Session

Wednesday July 16, 2003, 12:30 PM - 2:00 PM

Chair: Leo Higgins, ASAT Inc.

Poster Sessions have been proven to be a successful means of promoting both research activities as well as currently available technologies. Posters allow a broad viewing audience to access the various informational content topics based upon an individuals interest level and time availability. Session attendees can spend as much or as little time as they like at each of the Posters, as the session timing is non-structured by design to promote open communication. This is an excellent opportunity for the one-on-one discussions between attendees and authors or technical representatives in addressing questions or comments on technologies presented. Please take this opportunity to attend and enjoy the Poster Session, as it is another networking venue format, keeping in mind that your feedback on the Poster Session is also appreciated.

Epoxy Flux --An Answer For Reliable No-Clean Flip Chip Assembly, Ning-Cheng Lee, Indium Corporation of America

Considerations for Minimizing Radiation Doses to Components during X-ray Inspection, Richard C. Blish, II, AMD, Inc.

Extreme High Speed Microvia Drilling Of Chip And Wafer Scale Packaging Products, Todd Lizotte, NanoVia, LP

Control of Solutions for Electrodeposition of Bumps, Peter Bratin, ECI Technology

X-Ray Inspection, Udo Frank, Ph.D., feinfocus Rontgen-Systeme GmbH

Encapsulation of Sensorchips with Advanced Transfer Molding, Anton van Weelden, Boschman Tech.

STS: IEMT Ses 203: "Green" Manufacturing of Electronics

Wednesday July 16, 2003, 2:00 PM - 5:30 PM

Chairs: Luu Nguyen, National Semi & Brian Toleno, Loctite

"Green" manufacturing has gained interest in the last few years as the industry moves to eliminate lead and halogen

compounds from packages and assembly processes. Much of the earlier interest came from consumer electronics demands in Asia. However, with the recently published WEEE Directive, green products are now mandated in Europe beyond July 2006. This timely session covers issues on halogen-free packaging, and lead-free processes related to flip chip and CSP assembly, soldering, and board level reliability.

Qualification & Optimization of Sn Based Soft Solders: A Refinement for Bi Based Leadfree Soft Solders for EFM Volume Production, Bryan Y. Y. Ong, ChipPAC, Malaysia Sdn Bhd

Epoxy Flux For Lead-Free Soldering, Ning-Cheng Lee, Indium Corporation of America

Implementation of Pb-Free Bump Interconnect in Power Packaging, Rajeev Joshi, Fairchild Semiconductor Corporation

Lead Free Package Interconnections for Ceramic Grid Arrays, Mario Interrante, IBM Microelectronics Division, Interconnect Products

Investigation on a Lead-Free Flip Chip Assembly Process, Gerard Kums, Philips Centre for Industrial Technology

Inter-Dependence of Processing and Alloy Composition on the Reliability of Sn-Based Lead- Free Solders in Fine Pitch FCOB Interconnection, Dr. Changqing Liu, Wolfson School of Mechanical and Manufacturing Engineering

Towards a Halogen-Free Package - GREEN Molding Compound, Joanne Kee, Infineon Tech Asia Pacific

STS: IEMT Ses 204: Package Design & Characterization

Wednesday July 16, 2003, 2:00 PM - 5:30 PM

Chairs: Atila Mertol, LSI Logic & Nirmal Jain, Rambus

Package design, mechanical, thermal and electrical modeling and manufacturability of electronic packages become an integral part of the design process for robust package design and cost reduction. This session includes papers that describe methodology to generate compact models of packages and heat sinks from modeling, measurements, electrical performance comparison of wire bonded and flip chip packages, signal integrity analysis and advanced substrates for high speed and high performance packages, design of manufacturability and cost reduction.

A Methodology for the Generation of Dynamic Compact Models of Packages and Heat Sinks from Thermal Transient Measurements, Marta Rencz, Budapest University of Technology and Economics Department of Electron Devices

A Comparison of Electrical Performance between a Wire Bonded and a Flip Chip CSP Package, Rahul Kapoor, United Test and Assembly Center Ltd.

An Approach to Reduce Build Up Layers for Flip Chip - Ball Grid Array (FC-BGA) Substrates, Toshihiko Nishio, IBM Microelectronics Division

An Advanced Packaging Solution for OC-768, 40Gb/s Utilizing IBM Standard Alumina MLC Technology, Warren D. Dyckman, IBM Microelectronics Division, Interconnect Products

Modeling and Simulation of 12.5 Gb/s on a HyperBGA Package, Steven G. Rosser, Endicott Interconnect Technologies Inc.

A Design And Performance Study of 3D Packaging for High Performance Memory Applications, Ilyas Mohammed, Tessera Technologies, Inc.

STS: IEMT Session 205: Wafer Level Packaging

Thursday July 17, 2003, 9:00 AM - 12:15 PM

Chairs: Jan Vardaman, TechSearch Int & Erik Jung, FhG-IZM

Packaging at the wafer level is gaining momentum, especially for low I/O count applications. This session focuses on developments in wafer level packaging (WLP). Presentations provide prospective from WLP users in terms of package needs and requirements. New data from suppliers, including package construction, materials, reliability, and manufacturing issues will be presented. Highlighted are the issues with back-end assembly for wafer level packages.

A New Wafer Level Package Having Solder Bumps On Polymer Structure, Scott Barrett, Kulicke & Soffa Flip Chip Division

New Advancements in Photoimageable Dielectric Resins for Wafer Level CSP Applications, Christopher Esposito, Shipley Far East Ltd.

Time Dependant Materials Issues in the Electromigration of Solder Bumps, Glenn Rinne, Unitive Inc.

Wafer Level Packaging-Reliable Solutions for Evolving Market Requirements, Scott Barrett, Kulicke & Soffa Flip Chip Division

WLCSP Back-End Considerations, Ted Tessier, ST Assembly Test Services Inc.

Backend Processing for Wafer Level Chip Scale Packaging, John Hunt, ASE (US) Inc.

A Memory Suppliers Outlook on Die Products, Dan Skinner, Micron Technologies

STS: IEMT Session 206: Manufacturing Test

Thursday July 17, 2003, 9:00 AM - 12:15 PM

Chairs: O. Ronquillo, NP Test & A. Calamoneri, Test Spectrum

The increasing portion of IC packaging and test cost remains a major concern to the IC manufacturing management. Significant advances in the semiconductor manufacturing technologies and IC design continue. This enables exciting developments of new applications and product functions leaving enough challenges to the testing world.

Overcoming Test Challenges Presented by Embedded Flash Memory, Thomas M. Trexler and Jim Agin, Credence Systems Corporation

Reduce Your Cycle Time By Utilizing Automation for Wafer Test Data Collection, Navin Tandon, Texas Instr.

Current Challenges in Transistor Level Design Verification and its Application in Flip Chip Packaged Devices, Itzik Goldberger, Optonics, Inc., A Credence Company

Open Architecture Test System: The New Frontier, Sergio Perez, Advantest America, Inc.

Technical and Economic Requirements of Integrated SOC Testing, Don Blair, Agilent Technologies

Validating and Characterizing High-Speed Datacom Devices, Tom Napier, NPTest

Reducing the Cost of Package Test, Saeed R. Shakeri, Advanced Interconnect Technologies, Inc.

STS: IEMT Poster Session

Thursday July 17, 2003, 12:15 PM - 2:00 PM

Chair: Leo Higgins, ASAT Inc.

Poster Sessions have been proven to be a successful means of promoting both research activities as well as currently available technologies. Posters allow a broad viewing audience to access the various informational content topics based upon an

individuals interest level and time availability. Session attendees can spend as much or as little time as they like at each of the Posters, as the session timing is non-structured by design to promote open communication. This is an excellent opportunity for the one-on-one discussions between attendees and authors or technical representatives in addressing questions or comments on technologies presented. Please take this opportunity to attend and enjoy the Poster Session, as it is another networking venue format, keeping in mind that your feedback on the Poster Session is also appreciated.

Increased Levels of Integration Drive the Need for New Test Approaches in Wireless Designs, John Lukez, Credence Systems

Integrated Cellular Transceivers: Challenging Traditional Test Philosophies, Edwin Lowery, Agilent Technologies

Testing High-Speed Serial Interface Technology: Is Your Test Solution in Synch?, Steve Lomaro, NP Test

The Daily Living with "Monster" Probe Cards, Frank Pietzschmann, Infineon Technologies AG

Advanced Manufacturing Techniques for Flip Chip Devices, Gheorghe Pascariu, Newport Corporation

STS: IEMT Ses 207: Adv. Packaging: FlipChip, 3D, & SiP

Thursday July 17, 2003, 2:00 PM - 5:30 PM

Chairs: Jeffrey Demmin, Tessera & Vijay Gumaste, National

Many of the significant advances in the functionality and density of today's electronic products are the result of advanced packaging technology that continues to push the limits of the industry's capabilities. This session examines issues related to flip chip, advanced design, system-in-package approaches, and 3D technologies that are driving these advances. All of the papers are focused on high-volume manufacturing, so these are real technologies, not just investigations into the possibilities.

3D Stacked Packages With Bumpless Interconnect Technology, Charles W. C. Lin, Bridge Semiconductor

Flip Chip on Standard Lead Frame: Laminate Performance at a Lower Cost, Frank Juskey, Advanced Interconnect Technologies

Stacked Chip Scale Packages: Manufacturing Issues, Reliability Results, and Cost Analysis, Jeffrey C. Demmin, Tessera Technologies, Inc.

Improved Application Capabilities as a Result of Flip Chip PBGA Technology Development Advancements, Ron Malfatt, IBM

The Technology Benchmarking Study of System-in-a-Package (SiP), Edward Law, ST Assembly Test Services Inc.

WLAN LTC Modules; Advanced Design, Technologies and Manufacturing, Nicolas Gosselin and Stanley Wang, DT Microcircuits

Package Stacking in SMT for 3D PCB Assembly, Dongkai Shangguan, Ph.D., Flextronics

STS: IEMT Session 208: Reliability & Advanced Materials

Thursday July 17, 2003, 2:00 PM - 5:30 PM

Chairs: Reza Ghaffarian, JPL & Harvey Miller, Infrafocus

Reliability and qualification tests are required to be performed when new materials and package techniques are developed. Advanced materials are developed to address un-met needs for better package electrical and thermal performance and reduced cost. They also must meet rigorous tests and reliability qualification for replacement. The papers in this session address not only materials and process; they also provide second level reliability and qualification to meet product implementation. Some of the issues discussed include: use of corner staking to improve reliability of CSP without underfill, reliability characterization for an RF module, process and material characterization and improvement to control thin laminate warpage and via integrity, and flip-chip format trade-offs.

X-BMI Resins as Low-Stress Alternatives to Epoxies for Semiconductor Package Assembly, Chris Perabo, Henkel Loctite Electronics

The Impact of Moisture in Mold Compound Preforms on the Warpage of PBGA Packages, Leon Lin Tingyu, Motorola Innovation Centre

High Reliability BGA Package Improvements on Module Total Cost of Ownership, Kim Blackwell, Endicott Interconnect Technologies Inc.

Manufacturing Issues for 3D Integrated Active Circuits into Organic Laminate Substrates, Erik Jung, Fraunhofer IZM

Characterization of In-Process Substrate Warpage of Underfilled Flip Chip Assembly, James Jian Zhang, Georgia Tech

Processing and Reliability of Corner Bonded CSPs, Brian J. Toleno, Loctite Electronics

Board Level Reliability Evaluation of RF PA Module Vias, Robert Darveaux, Amkor Technology, Inc.

STS: IEMT Session 209: Wafer Bumping Technologies

Friday July 18, 2003, 9:00 AM - 12:00 PM

Chairs: Bill Chen, ASE & Annette Teng Chueng, Corwil Tech

Wafer Bumping is a critical to IC assembly in flip chip. This session will be devoted to the advances in wafer bumping process technology, including novel process for 300 mm wafers, etching of UBM films, improvements in printing, advances in metal deposition & reflow processes, and new applications.

Characterization and Use of Spray Acid Tools for Large Volume Selective Etching of UBM Films Used in Flip Chip Applications, Lakshmi N. Ramanathan, Motorola Inc.

Wafer Bumping Technology for LDI Application by Electroless Nickel Plating, Joong-Do Kim, Samsung Techwin

A Novel Gold Deposition Process for Wafer Applications, Eugene B. Douglass, Shipley

Advances in 300mm Wafer Level Packaging--New Concepts of Material Deposition Technologies, Thomas Oppert, EKRA Eduard Kraft GmbH

Bumping Wafers via Ultrasonically Enhanced Stencil Printing, Gerald Pham-Van-Diep, Cookson Electronics Equipment

The Benefits of a Flux-Free Atmosphere for Wafer Bump Reflow, Fred Dimock, BTU International

STS: IEMT Ses 210: Factory Sim, Automation & Integrat

Friday July 18, 2003, 9:00 AM - 12:00 PM

Chair: Mohammad Khan, AMD & Orion Starr, ChipPAC

Time to market is the key today in a tough business environment. To achieve profitability flawless execution is essential. Rapid availability of information has cut profitability windows even smaller. For flawless execution, planning and cost studies must be carried out in detail. Process and factory simulation tools are used by leading companies to explore all available options before committing resources. Today's

competitive environment does not allow changes to be made to either the factory or the product without serious financial consequences.

This session will cover papers from around the world from authors from leading companies. You will learn how these companies used leading methodologies for rolling out new products.

Customer Driven Innovation Process, Robert Pennisi, Motorola Inc.

Universal Simulation Kit in Micro-Production, Ortun Wiechers, Fraunhofer IPA

Equipment Failure Definition: A Prerequisite for Reliability Test and Validation, Tom Umberg, Delta Design

Pre-Project Facility Layout Planning for Setting-Up Cost Effective Wafer Bumping Process, Wu Ming, ST Assembly Test Service Ltd.

System Availability and Operation Support Modeling, Alex Fashandi, Delta Design

Cycle Time and Variability Reduction in an Optical Assembly Process, Salil Pardhan, Sanmina-SCI Corp.

Towards Next-Generation Design-for-Manufacturability (DFM) Frameworks for Electronics Product Realization, Manas Bajaj, Georgia Tech

Registration:

For more information, and to register, visit: **www.semi.org/semiconwest/stsiemt**

(Editor: Many will see this list of papers when it is too late to attend. However, read the titles and contact the authors directly if you have interest in their presentation. Please support these volunteers since the STS: IEMT is co-produced by SEMI & IEEE's CPMT)

Jan Vardaman (active on CPMT Board and with STS:IEMT conference), Jim Morris, Donna Noctor

CPMT Meeting of Interest to Members 2003

****Int'l IEEE conference Environment on Compatible Microelectronics Packaging, Manufacturing, & Design Technology,** June 23-24, Hong Kong; June 25-27, 2003 Shenzhen, China; angie Wong, wywong@ee.cityu.edu.hk, fax 852 2788 7579.

****InterPACK'02 (Inter-society Packaging Conference),** July 6-11, 2003; Maui, Hawaii; S. K. Bahattacharya, swapan@ee.gatech.edu, fax 1 404 894 0957.

****International Electronics Manufacturing Technology (IEMT) Symposium** July 16-18, 2003; San Jose CA Gloria Lou: glou@semi.org +1-408-943-7048 (fax +1-408-943-7913)

****9th International Workshop on Thermal Investigations of ICs & Systems (Therminic)** September 24-26, 2003; Aix-en-Provence, France Bernard Courtois THERMINIC@imag.fr

****TC-7 2003 Workshop on Accelerated Stress Test & Reliability (AST'03)** October 2-4, 2003; Seattle WA Mark Morelli,Mark.Morelli@Otis.com +1-860-676-6140

Walt Trybula, Editor Transaction

****MST'03 (Microsystems Technologies),** Munich Germany, October 7 - 8, 2003, Erik Jung, erju@izm.fhg.de, fax 49 30 46403 161

****3rd Internat IEEE confer on Polymers & Adhesives in Microelectronics & Photonics (Polytronic 2003),** Montreux, Switzerland, October 20 - 23, 2003, Bernard Courtois, polytronic2003@imag.fr

****5th Electronics Packaging Technology Conference (EPTC'03**), December 10-12, 2003, Singapore; Mahadevan Iyer, iyer@ime.a-star.edu.sg, fax +65 6774 5747.

****2003 IEEE Electrical Performance of Electronic Packaging (EPEP),** Oct. 27-29, 2003, Princeton NJ; Paul Baltes baltes@engr.arizona.edu

****5th International Conference on Electronic Materials & Packaging (EMAP),** Nov 17-20,2003; Singapore; Sung Yi, sungyi@cecs.pdx.edu

****2004 Int'l IEEE Confer on Asian Green Electronics (AGEC),** January 5-9, 2004; Hong Kong/Shenzhen, China; Angie Wong, wywong@ee.cityu.edu.hk

****1st International Workshop in Nano Bio-Packaging,** May 23-24, 2004; Atlanta GA, wlp@ee.gatech.edu

****54th Electronic Components and Technology Conference (ECTC),** June 1-4, 2004, Las Vegas NV, www.ectc.net

-- submitted by Jim Morris, Vice President of Conferences

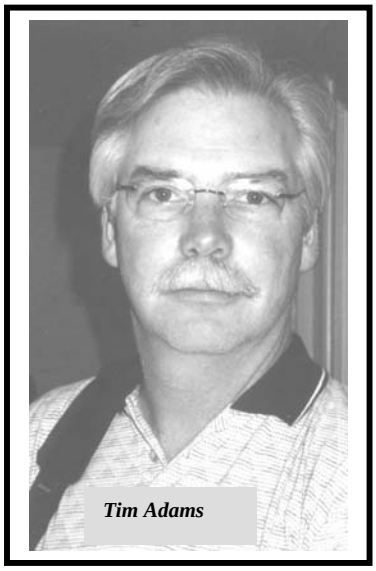
Ricky Lee and Anthony Chan, two volunteer leaders in CPMT

Board Meets in New Orleans Jazz Bistro

Right after the successful ECTC, your hardworking Board of Governors spent all day Saturday planning and executing Society business. The Board now meets twice a year: at ECTC in June and at paper selection in Dallas in November. The officers also meet in winter in either Europe or Asia.


President Rao Tummala

President Rao Tummala started the meeting by introducing the new volunteers. **Tim Adams** of Dow Corning is an appointed Member at Large who has taken on upgrading of the CPMT web pages as his focus. **Ricky Lee** of Hong Kong is a new Member at Large as well as being an associate editor of our transactions. **David Whalley** a Senior Lecturer Loughborough University in the United Kingdom. **Li Li** of Motorola is another new Member at Large. The new Chair of TC-14, System Packaging, was also present at the meeting**, Dr. Yoshitaka Fukuoka.**

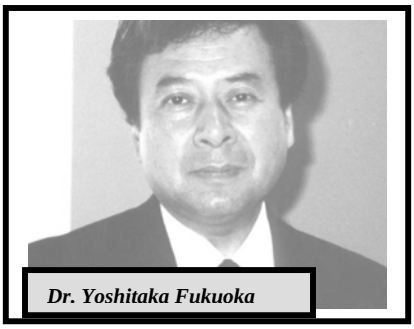

Tim Adams

Representing the ECTC were current chair Donna Noctor and next year Chair Steve Bezuk. Potomac Communications were represented by **Ellen Leeper, Kristine Martin, and Bob Conrad**. **Kimberly Newman** of University of Denver was also visiting the board meeting.

Rao and **Marsha Tickman** had reviewed the state of CPMT to the TAB. This IEEE committee saw CPMT as a small dynamic Society with excellent management. In particular, they liked the way each part of CPMT focused on their regional membership. They wanted to document CPMT "best practices" so that other societies could more easily adopt them. One note of cautions was that as CPMT accepted new volunteers we should advise them as to the amount of time each task is expecting to take. The Board congratulated Rao and Marsha for the successful presentation.

Rao indicated that many issues had to be addressed at this meeting but two were critical: the updating of the CPMT and ECA agreement to run ECTC and the influence of debt ridden IEEE on CPMT finances.

Bob Willis, the President of ECA, explained the up-date of the controlling document for running the ECTC meeting. Now all the roles are well defined so that there is no confusion by the many players that come and go. The governing document discusses the "jointly and equally" run ECTC. In particular it defines the ECTC Governing Council that is responsible for all financial concerns of the meeting. This six person council has both the ECA and the CPMT President and main members. In practice the operations group, the ECTC Executive Committee, will suggest the solutions to each business concern and the Council will review and concur. The responsibilities include:

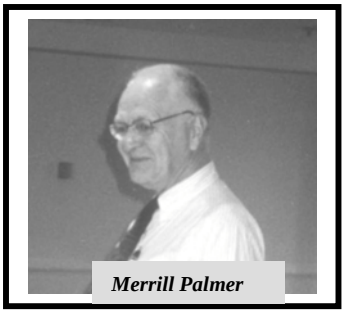

Dr. Yoshitaka Fukuoka

1. Manage all fiduciary responsibilities
2. Define all fixed costs
3. Define expected revenues
4. Approve the financial chair nomination
5. Approve the ECTC Vice Chair

These steps bring the needed transparency without putting hurdles in the way of an historically efficient operations. The Board approved this agreement in Principal.

Merrill Palmer sat in for the Treasurer since he is so good at keeping the Board from overspending. He pointed out that the bill for our Society from IEEE TAB + taxes have been on a roller coaster but is coming down to a low level by 2005.

1997 -- $29.7K
1998 -- $48.7K
1999 -- $39.3K
2000 -- $461.5K (the IEEE reserves go to zero)
2001 -- $1039.4K
2002 -- $383.7
2003 -- $535.9 IEEE expects at least $6.18 M in red ink this year.

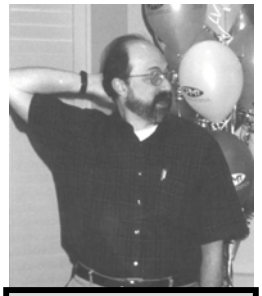

Merrill Palmer

Merrill expects the cost of services from TAB for the CPMT to run about $100K/year in the future. In addition to these IEEE bills we also saw CPMT reserves go down simply because our investments decreased in value for the last few years. The proposed Society budget does not balance in 2004 but goes a long way toward balance and must balance in 2005 as per our pledge to TAB. We will manage the deficit to $60K in 2004. The Board voted not to raise the members dues or Transaction fees despite the looming red ink.

Merrill points out that the Transactions bring in $802K with expenses of 365K for a surplus of $437K for Society operation expenses. About 1200 transactions go to libraries and 1800 go to our members (many members now use IEEExplore to read the transactions, not paper copies). Our Book Broker income has grown in 14 years from $8K to $215K. Our new CD-ROM with Transaction index and 2000-2002 is priced at $60 and should make a profit after the $26K of manufacturing has been recovered. We trust members will buy this CD-ROM to speed up searches of the packaging, component, and manufacturing references.

Vice President **Phil Garrou** summarized the technical activities in our Society:

19 active TCs
9 new Chairs in last 2 years, lots of turn over as people get overloaded
Nano-technology Packaging committee started
Assembly TC-3 is looking for new Chair
Our TC web site has been updated (But 6 TCs need to update their pages)



Phil Garrou, Tech VP

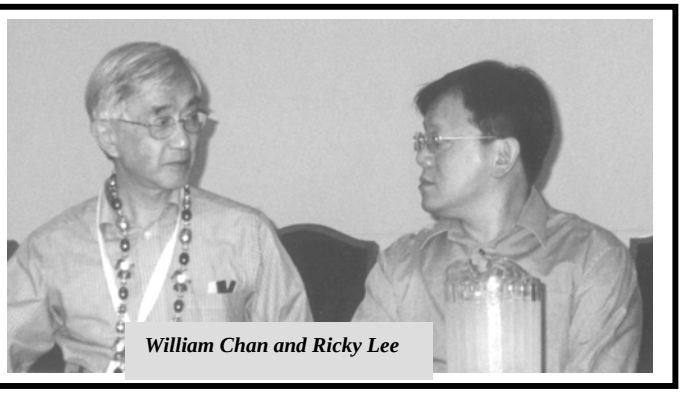
Walt Trybula talked of the IEEE/CPMT presentation to the senate staffers on Nano-technology. He mentioned Deb Newberry on the team, the author of "The Next Big Thing Is Really Small: How Nanotechnology Will Change the Future of Your Business." This helped the deposition of the $2B bill in front of the U.S. congress. Large efforts were also mentioned in Japan, Europe, and China. There is a yet to be defined "Nano path" for everything CPMT does now on the micro level including: boards, systems in packages, systems on chips.

Tim Adams talked about upgrading the CPMT websites. His team wants to use the site as a strategic tool not just a bulletin board. The information presentation should lead to increased Society revenue by making services more available to members and non-members. Perhaps some of web information would be available to members to keep volunteer participation high. His plan includes:

1. Develop a unified web plan
2. Enhance the current search engine on our web pages
3. Develop a business model to allow Web sponsorship revenue
4. Update volunteer resources on the existing site - possibly senior, student, and fellow pages
5. Benchmark our sites with equivalent organizations

Vice President **Anthony Chan** mentioned the balance we have in the Society with strong reserves, diverse services, stable operations, and continual strategic planning. We are maturing in our global participation , professional in many related fields, and have had hundred of volunteers at any one time. However, the world technology economy is at the lowest profit margins ever. This provides CPMT with the opportunity to take leadership including training in this time of fast technology changes.

International relations. **Bill Chan and Ricky Lee** handle the Asian interactions. Bill pointed out that there is a transition underway from focus on Manufacturing to also doing product development and R&D in Asia. However, Asia was hit harder by the recent downturn with the possible exception of China. ASE has a large Asian presence and thinks CPMT is a premier organization. In all cases our Society must show how our meeting and journals can help industry increase their revenue. The regional meetings have been very successful. The Leadership Workshop held at EMAP was very successful.



William Chan and Ricky Lee

Rolf Aschenbrenner and Johan Liu represent European activities. The European Leadership meeting was highly successful due to the heroic organization. Attendees included 25 from European CPMT chapters, 3 from the U. S. , and 6 IMAPS- Europe. The associated emerging technology workshop attracted 80 participants. The conclusion was that CPMT and IMAPS must cooperate in Europe for member benefits. In particular, we must coordinate meeting dates (there are too many meetings), mailing lists, and consider putting on one dual European conference. The agreement is in principle and will be worked out by volunteers in both groups.

Rolf Aschenbrenner

C. P. Wong reported that the CPMT Fellows committee has 11 complete nomination packages that reach all of the IEEE criteria. This is the most every to be generated within the Society. This shows a high degree of activity by individual nominators and a team assembled by **Jack Balde** to achieve higher participation. Rao Tummala notes that there are still many potential candidates we have not focused on including many in the regions CPMT is growing membership. C. P. suggested that we continue to push Senior Ranking for our members since only about 8% have reached that rank and this is where the fellows come from. Once the CPMT committee adds comments and ranks the nomination packages they go for evaluation by the 30 members of the IEEE Committee. Announcements will be made in November.

Johan Liu (standing), Anthony Chan (rt) and C. P. Wong discussing Board issue.

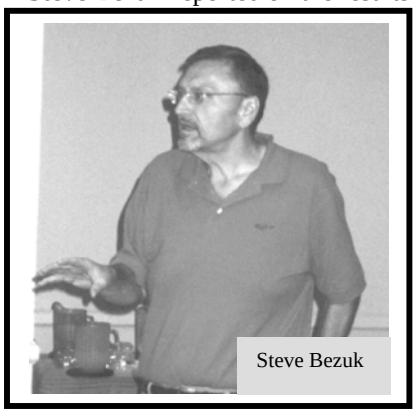
A request was made for what it takes to be an "IEEE Life Member." The rules are that a members age plus years of IEEE membership must total 95. This membership level used to be left unbothered by IEEE renewal packages, but this year they were included and about half did not respond dropping the IEEE membership by 2%. For years our system forgot about an imperative even for engineers…we don't live forever.

Marsha pointed out that of the Board members on the last 6 months of there 3 year term, 4 are eligible to serve again. Nominations for these 6 Member at Large positions are due by July 18th. The slate will be posted by August 1.

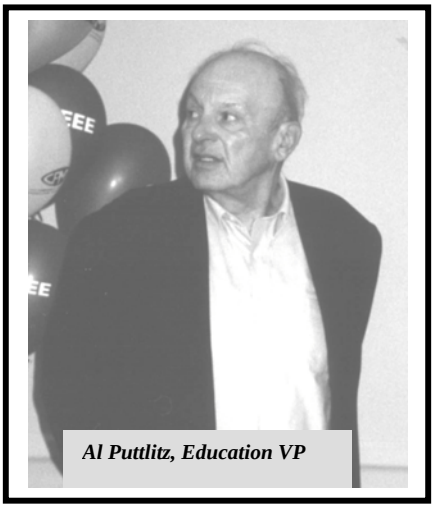
Ralph Russell reported (by telephone). There are now 33 CPMT chapters all over the globe. Durham North Carolina has a new joint chapter approved by IEEE. The president of the Chapter is Dev Palmer. There were few submittals to "Chapter of the Year" award partly because it is a complex process. Ralph said the process is being simplified for next year. The Romanian Student Chapter is winning this year's award.

Our current membership at the end of April is 3,103 that is about equal to our membership in 1999. This is about 400 lower than our all time April membership. The loss is pretty much all around the globe and is probably related to the shrinking job market. Ralph also suggested that we encourage upgrading to senior status for more of our members since this level of membership usually is engaged so they automatically renew. In fact, senior members usually last until they become life members. Marsha pointed out that eight new members joined at the CPMT table during ECTC.

Steve Bezuk reported on the results of ECTC. With 726 attendees this was about the normal number and down from the all time record of 1000. Attendees were 46% from industry, 44% from universities, and 10% from research labs. The 14 professional development courses attracted 261 engineers and should make a surplus. There were 42 new exhibits compared with 70 last year. The academy workshop attracted 22 professors and should become a standard feature of the ECTC week. 474 abstracts were submitted up from 425 last year. 65% were university related, the university presence is rising which represents the increase of packaging/components taught in graduate school. There were 311 technical papers with 252 oral presentations (with 7 each session) and 59 posters. The mix of sessions is changing. Connectors and contacts have been phased out to be featured at the Holm conference of TC-1.

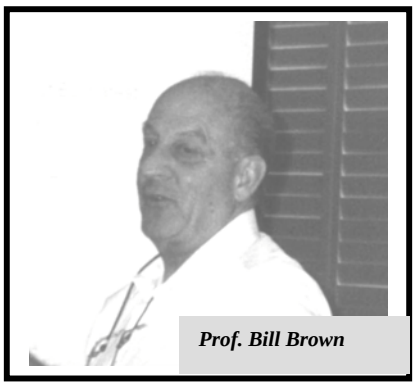

Steve Bezuk

Vice President **Al Puttlitz** described the Motorola Fellowship. There were 13 applicants that met all the requirements. A down-selection was made to 7 finalists to present at ECTC. Five gave oral presentations and two poster sessions. The winner this year was Young-Doo Jeon from KAIST.


Al Puttlitz, Education VP

In addition, the CPMT list has been updated to 20. In 2003 Rao Tummala, Paul Wesling, C. P. Wong, and Paul Totta have used the travel budget. The next year Professional Development courses will include a (1) nano overview, (2) nano packaging, (3) MEMS.

Prof. **Bill Brown** described progress in student chapters. There are now 5 official chapters: Georgia Tech, Romania Polytechnic of Bucharest University, Hong Kong Science and Technology, University of Arkansas, and Sweden. Next year we will try to have a tech corner booth for student chapters.

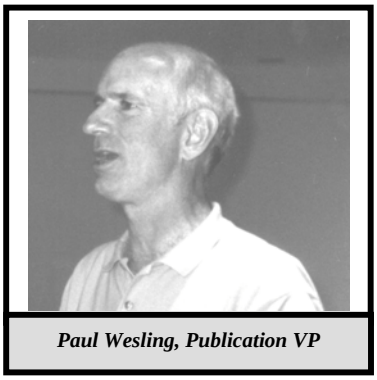

Prof. Bill Brown

Vice President **Jim Morris** described the trend to get CPMT being a financial partner in all conferences we support. If we can't provide value we should not dilute our volunteer efforts. When we do provide value we should get some added to the CPMT surplus. We are making progress in negotiations with all conferences where we have long term commitments. Jim indicated the Packaging Materials Conference would start up again in 2004 in Atlanta. In 2005 the conference will go to Irvine California.

Rao Bonda discussed the successful CPMT awards this year. Next year we must find a way to get many nominations with minimum effort. In particular, the IEEE Field award that CPMT Society is initiating must have several nomination packages prepared from our membership.

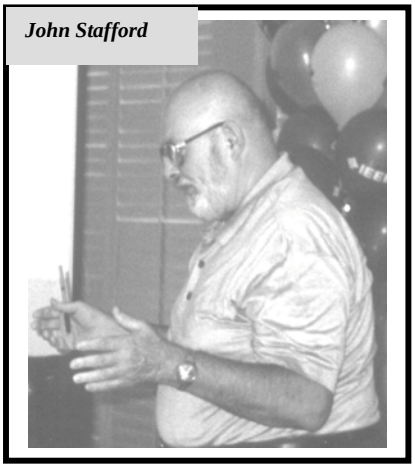

Rao Bonda

Vice President **Paul Wesling** gave more updates on the Society publications. First we have to show that our publications have high impact. Since we have split and changed the name of our transactions a number of times the ISI reference tracking system hasn't been able to validate our journals. ISI does not want to combine references from our previous named transactions. Perhaps we should calculate our own citation index. A second service we will provide is lists of possible references (onlogies) for authors and editors since our articles do not have lots of references. A third effort is to solicit more papers from our membership. For example, we typically get 25 good papers from ECTC if session chairs follow up.


Paul Wesling, Publication VP

Paul also reported that the new CD for transactions from 2000-2002 is on sale for $60 and one can get all the transactions from 1954 on 10 CDs for $260.

John Stafford discussed the changing affiliation of our members. More packaging and assembly manufacturing and development are in the EMS companies. Traditionally these companies are not supporters of professional societies although their engineers often attend meetings and use publications on an individual basis. Here is an opportunity for CPMT to influence the culture of these growing part of the industry.



John Stafford

CALL For BOARD CANDIDATES

The CPMT Society is governed by a Board of Governors composed of officers, 18 elected members-at-large, and various committee chairs and representatives (see inside cover of paper Newsletter for details.)

Annually, Society members are asked to elect six members-at-large for a three-year term of office. Candidates for member-at-large are selected in two ways -- either by the Society Nominating Committee, or by petition.

If you are an IEEE and CPMT Society member in good standing and are interested in serving on the Board of Governors, you can automatically become a candidate via petition by following the procedures below. The term of office for this election is 1 January 2004 through 31 December 2006.

This volunteer position requires two Board meetings each year: usually meeting the day after ECTC in May and in Dallas the day after ECTC paper selection in November. In addition, most Members-at-Large spend a few hundred hours a year volunteering for Board or Committee activities. IEEE advises that volunteers make sure they can fit these demands in their busy schedule before running for election.

****Prepare a petition that contains your name, member number, and statement of your qualifications for office.**
**** Provide lines for signatories. Each line should include space for a printed name, member number, and signature.**
**** Have the petition signed by a MINIMUM of 25 CPMT Society members in good standing (Student grade members are not eligible to sign.)**

Membership status of all signatories will be validated. It is suggested that you gather more than 25 signatures in order to assure meeting the minimum required number of valid signatures. Submit your petition by no later than Friday, July 25, 2003 to:

CPMT Society Nominations Committee
c/o Marsha Tickman
IEEE CPMT Society Executive Office
445 Hoes Lane, PO Box 1331
Piscataway, NJ 08855-1331 USA

or FAX to +1 732-981-1769 --- questions to phone +1 732-562-5529 or email m.tickman@ieee.org .

Why Are You Waiting?

Why are you waiting to become an IEEE Senior Member? There are many misconceptions about becoming a Senior Member. Some believe that you have to be a Nobel Prize winner to qualify, that you have to be published or that you have to be ancient. These beliefs are all myths! You can become a Senior Member with just 10 years of professional practice and education counts. Five years of significant performance is needed within the ten-year period. References are needed from three Senior Member or Fellow Members.

Senior Membership provides professional recognition of your peers for technical and professional excellence. IEEE Senior Membership is recognized throughout the world. You can file for Senior Membership electronically or download forms for mailing. Visit www.ieee.org for forms and detailed information.

Please contact me if you have any questions concerning Senior Membership.
Ralph W. Russell, II
CPMT Society Strategic Director for Membership and Chapter Development,
cpmt-membership@ieee.org

Editor's Turn

This is the Newsletter issue that both summarizes the many results of the big ECTC events and also announces the upcoming IEMT activities. This Newsletter shows how active your Society is in many ways. Unfortunately it is also the hardest issue to put out since all volunteers are exhausted from all the preparation and execution of the ECTC and must catch up on their paying jobs.

The ECTC has been optimized for conversations at coffee breaks, breakfast meetings, lunches, and evening get togethers. This is great, and allows all attendees to meet many people from many different companies and countries. With this "networking" format it is easy to catch the feeling of industry. This year many of the engineers felt the assembly/packaging market was beginning to rebound after more than a year of doldrums. Those engineers that still felt depressed were at companies that were making negative news on the business page. Students still felt that it was a hard push to get a job; that the job market has not yet turned around. Some of the Universities have lost one of their long term government funders and have not been able to find a new line of support in this tight market. Also, industry does not seem to be in the mood for long term support of university efforts although there are lots of short term equipment gifts. Some of the university and company development facilities are clearly underutilized.

What was different at this ECTC? Two things stood out very strongly. First, almost everyone brought their presentation on their lap top and just plugged into the room projector (this editor was one of the few throw backs that used transparencies much to the amazement of the students in the audience...this will probably be illegal by next year). The second trend is that every SARS fearing one of us was really washing their hands in the rest rooms despite the lines at the sink. generated.

REGION 10 CHAPTER ACTIVITY ROUND - UP

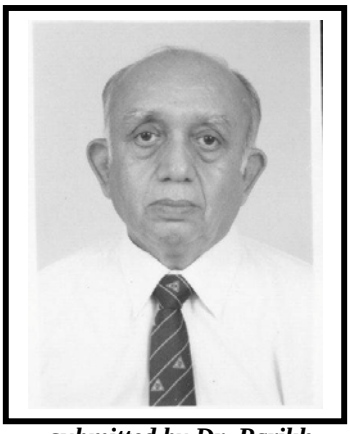
Daejon (Korea) Chapter organized MicroElectronic Packaging Conference at Seoul KOEX as a joint activity of IEEE-CPMT and IMAPS-Korea. As reported by Prof. K.W.Paik, the conference was well attended with 150 delegates and covered latest developments on related technologies as per presentations from leading experts (including 4 invited speakers in Japan and 5 presentations from various universities/industries in Korea). Another jointly sponsored similar structured event is being planned for March 2004 at Seoul.

Hong Kong Chapter Chairman Dr.Cheung reported a successful workshop organized on "BGA Solder Joint Reliability - Failure Modes and Test Methods" by Prof. Keith Newman on 17th March 2003. The workshop was appreciated by about 70 delegates who attended the event. The Chapter plans to organize one more workshop on "Clean-room Technology" by Dr. Ken Goldstein in the coming months.

Taipei Chapter secretary Prof. Lih-Shan Chen, has reported a one-day co-sponsored symposium for Electrical and Information Engineering Symposium as organized on May 30 at I-Shou University, Kaohsiung. This well attended event was structured with 14 technical sessions to include 56 state-of-the art technical presentations on major topics covering materials characterization, opto-electronics technology, modeling and simulation, testing and measurements, image processing, automatic control, and wireless communication.

Prof. K M Seetharamu of **Malaysia Chapter** has reported his participation at the International Workshop on Electronic Packaging Education organized by IEEE-CPMT at New Orleans on May 27, 2003 where he presented a paper on "Electronic Packaging Education in University of Science Malaysia". He would be visiting Georgia Tech Packaging Centre and plans to take up further active work at his Chapter thereafter.

India Council Chapter organized two well-attended technical lectures during this period (in April and May 2003). The Chapter Execom has agreed to participate in the forthcoming 7th Annual convention of Surface Mount Technology Association India Chapter (SMTA-IC) as a joint activity at New Delhi on 16th to 18th July 2003. The 3 day event is being organized by DR. PARIKH as convener. Invited speakers including Prof. Manian Ramkumar of Rochester Institute of Technology, U.S.A, Mr. Aaron Saxton and Mr. Stanley Chen both of Universal Instruments Corp., U.S.A and Mr. William Tan of Dage Prestigious Industries, U.K. have agreed for keynote presentations at the convention and also conduct full day/ half day tutorials.



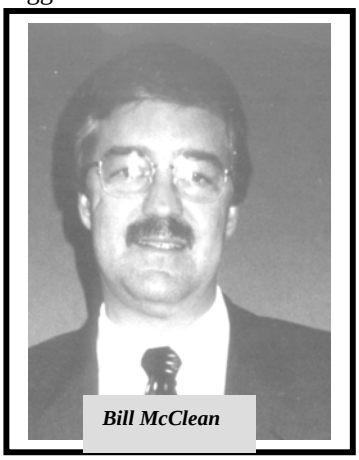
-- submitted by Dr. Parikh

Bill McClean Sees Clearly

Bill McClean gave a lunch time presentation at the New Orleans ECTC during which he discussed the economic metrics of the Semiconductor Product industry. Compared to the good old days Bill's predictions were unexcitingly flat, but compared to last year, things are looking up, maybe even beginning to take off.

He did mention that there is deflation taking place in wafer and system prices due to China coming on strong in those areas.

History: In 2001 the Gross Electronic Product was greater than $800 B. In 2002 it dropped to about $750B but we expect a 5% increase in 2003 to about $790B. The semiconductor production (IC count) actually never went down. It increased 1% last year and is looking like 15% this year ($162B) and a prediction of 25% in 2004. This is big unit growth that some day will lead to a healthy growth in margin (and investment in manufacturing). Equipment represents about $25B with materials having grown slightly bigger than this.



Bill McClean

Perspective: Just in case the audience was getting a little too happy, he mentioned that WalMart sales were bigger than all semiconductor markets added together. He mentioned that the new U.S. tax program that gives $100K write-offs for small companies will have an immediate effect on our business, because everyone will want to upgrade their PCs -- still a driver for the IC business. It will take a partial recovery in both computers and communication. Over time the IC content of electronics system has grown to 20% of the value. It will probably not grow much more now so the economy must pick up as a whole for the IC business to recover.

Cycles: Bill showed that there is a long history of highs and lows in our business. The lows typically come in lengths 2-4 years. We are in a world wide slowdown for 3 years now so the end is probably near. We must wait for the world economy to recover a bit more before we can start negotiating around for a better salary. Years 2001 and 2002 saw the shrinkage in electronics system sales the first time in history.

Prediction: Many companies are back to the revenue of 5 years ago. We can expect an average growth of 8% in the future. Already the IC demand is growing with higher unit sales, but the average selling price is down to levels of 10 years ago despite the vastly increase functionality.

All at the luncheon were smiling, so there must have been some truth in his presentation.

THANKS TO VOLUNTEERS:

These many News Bytes were sent by Jan Vardaman, Marsha Tickman, Paul Wesling, Dr. Parikh, Rao Tummala, Ralph Russell, James Morris, Rajen Chanchani, Craig Gaw, Al Puttlitz, Merrill Palmer, Rao Bonda, Kristine Martin, Angie Wong, and Alina Deutsch.

In addition, we must thank all those at the ECTC that let their picture be taken even when they were yawning or cramming food in their mouth. We are engineers, after all.

TC-5 Meets At ECTC in New Orleans

We had good ECTC conference. The attendance at our breakfast TC-5 meeting was better than expected in spite of the economic conditions. The minutes of the TC-5 meeting is given below.

1. The meeting was held on May 28, 2003 -- 7:00 to 8:00 AM.
2. The following members attended the meeting:
Richard Benson, William Brown, Rajen Chanchani, Charles Lee, Chris C. Lee, Jim Morris, Kyung K. Paik, Dave Palmer, Eric Perfecto, and Paul Wesling
3. I presented the status of TC-5 Committee.
4. There was a discussion on the conferences that TC-5 is co-sponsoring. In the recent past, TC-5 has been sponsoring three conferences every year:
a) Materials Conference in Atlanta
b) Polytronic in Europe
c) Electronic Materials & Packaging (EMAP) Conference in Asia
5. According to Jim Morris, **Materials Conference** traditionally held in Atlanta every year, did not have any compelling reason to be held there. His recommendation was to have this conference rotate every year between a city on east coast and on west coast. This meeting should probably tied to a university with strong packaging program. The committee decided that:
a) Next year (2004) meeting should continue to be held in Atlanta right after nano Workshop organized by Rao at GaTech. The advantage will be that the conference attendance will be favorably affected by this arrangement. Also, there is already a contract in place with the hotel and if it is violated then there could be a severe penalty to IEEE-CPMT. The conflict of interest between the workshop and conference does not arise because both meetings are co-sponsored by the same organizations, namely IEEE-CPMT and Ga Tech. The committee suggestion was to give significant discount in registration fees to the attendees attending both workshop and conference. For example, registration fees will be $300 if meeting is attended or $400 if both are attended. To save cost, the food (lunch) should not be served. Since next year meeting is in uptown Atlanta next to several good restaurants, this should not be a big problem for the attendees. However, whether to serve food or not will depend on the hotel contract that is in place.
b) Materials conference in 2005 should move to Irvine, CA, a west coast city. The conference will be tied to packaging group at U of Cal, Irvine. C. C. lee representing U of Cal, Irvine agreed with the arrangement.
6. **Polytronic Conference** in 2003 will be held in Montreaux, France. In 2004, it will be held in Portland , OR provided Polytronics Steering Committee approves it.
7. **EMAP** will be held in Singapore in 2003 without IEEE-CPMT sponsorship.
8. Rajen will renew the dialogue with Purdue to see if they would like to market their **CINDAS Materials Database** for a low price of around $200 or so.
9. We applaud **Sridhar Canumalla's** help in keeping the web page up-to-date. Due to recent change in his computer hardware, Sridhar's password to our web page does not work. He will call Paul Wesling (408) 252-9051 to work out the password issues with TC-5 web page. Subsequently, he will update the web page.

-- submitted by Rajen Chanchani, Chair TC-5

TC-5 breakfast meeting (from left): Chair Rajen Chanchani (Sandia Labs), C. C. Lee (U. of California,Irvine), and Eric Perfecto (IBM)

TC-5 breakfast meeting (from right counterclockwise): Dick Benson (Johns Hopkins), Charles Lee (Infineon-Singapore), Bill Brown, Eric Perfecto, C. C. Lee, Rajen Chanchani.

TC -18, Wafer Level Packaging, had a breakfast meeting at ECTC. Pictured from left to right: Tom Chung, Paul Wesling, Luu Nguyen, and Chair Michael Toepper

Bill Moody (Technology Corner) and Mike McShane (Past General Chair) are two of the shakers that make ECTC happen.

TC-16 RF and Wireless

Dragging ourselves out of bed after 2 action packed ECTC days, the Wireless and RF TC meet at 7am. Chair Craig Gaw of Motorola fled the >100 degree Phoenix weather to lead the Committee in planning for the next year. First he reviewed the success of this year's RF contribution to ECTC. Sixty papers were submitted to the ECTC committee. About 1/4 ended up in the two RF sessions and another 1/4 went in the high speed circuit modeling or embedded component sessions.

The key to this success was in picking RF topics that emphasized components, module packaging, and modeling. Then getting the work out to a carefully assembled list of experts in these areas. The decision was to repeat this process again adding a bit more to the subject lists and the colleague lists. Each TC-16 member will try to submit a list of 10 more names to the mailing list.

In addition, we will try to get the word out in more newsletters. If you want to be added to the TC mailing list contact Craig Gaw at [c.a.gaw@ieee.org]. In particular, if you find that much of your output does not fit into the IEEE MTT annual meeting, please join this effort to spotlight RF components, microsystems, and manufacturing by submitting a 2 page summary for the next ECTC (deadline is October).

The TC decided to choose the topics of "modules/microsystems with RF functionality" which can include RF embedded components and require RF computer modeling. RFIDs looked at as rugged components and as low cost manufacturing challenges will also be considered. If the turn-out of papers continues to increase it is possible to get a third session at ECTC or a plenary session. In addition, manufacturing papers could be presented at IEMT symposium held with the Semi Technology Symposium.

It was also pointed out that we should tell the presenters at ECTC that they should consider submitting a formal version of their paper to the IEEE/CPMT transactions since the new electronic editing process makes the time to publishing a matter of months. CPMT has become the publisher of choice for this part of the RF/wireless business.

Figure 1 Breakfast meeting of TC-16: Len Schaper, Dennis Olsen, Rama Ramakrishna ?, Li Li, Manos Tentzeris

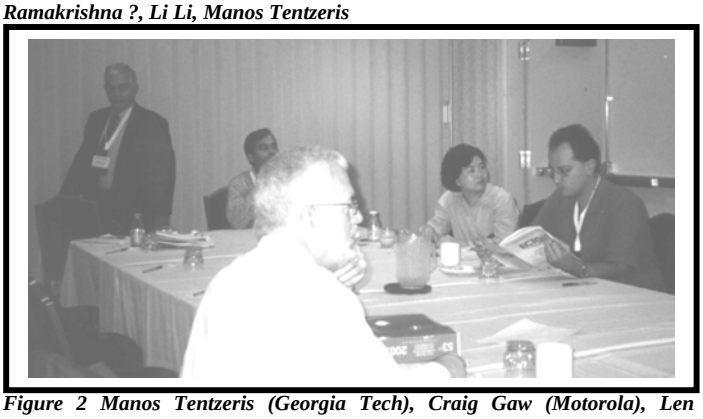
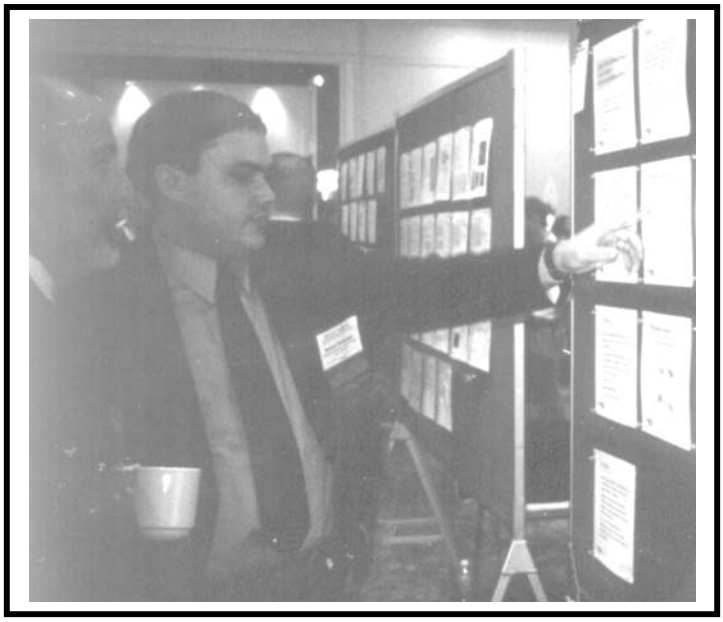
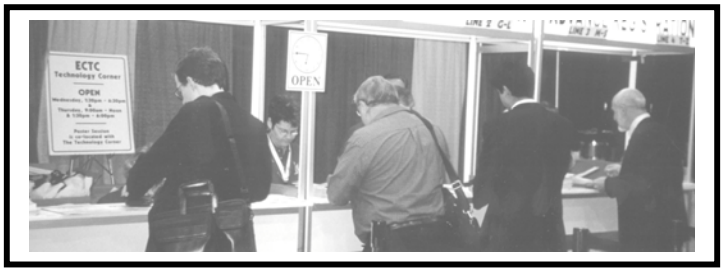


Figure 2 Manos Tentzeris (Georgia Tech), Craig Gaw (Motorola), Len Schaper (University of Arkansas)

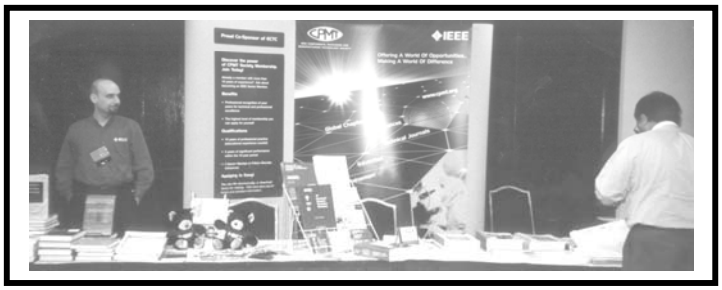
Technology Corner booth of TechSearch with Becky Travelstead



Lots of interaction at the excellent posters



Registration for ECTC proved an efficient process



CPMT Society's display tempted many to buy

Our Future Technologies?

On the first night of this year's ECTC before attendees found out the hotel was walking distance from the jazz clubs of the French Quarter, a well attended panel session was held on Trends in Advanced Packaging and Manufacturing Development.

Dr. Shluh-Kao Chiang of Prismark talked of "subcontract leadership". He mentioned that everyone wants to be the technology leader but no one wants to pay the price--Particularly in today's market of low margins on most products. We need more leadership today in the past since we have been living "disintegration" over the last decade. That is, the system design, the foundries, and the testing are often done by separate companies in separate countries. He asked "who will carry the future since packaging is very complex."

He identified the system innovators as (1) Intel and IBM for CPUs, (2) TI for DSP, and (3) RFMD and Conexant in SiP. This innovation requires a sustained specific product focus in technical and commercial development.

Tom Gregerich (Qualcomm Wireless) and Shluh-Kao Chiang (Prismark)

A few years ago IC revenue was $121B. Of this 13.7% represented packaging/assembly/test. Of this 31% was outsourced and 69% captive. By the year 2007 he saw the market growing to $225B with $30B in packaging of which 38% is performed by merchant services. Currently the big three (Amkor, ASE, and SPIL) perform more than 50% of the merchant business. But the tough market recently has only a 12% margin so these companies can only apply 2% of their flow to R&D. This leads to clever evolutionary change making our industry look like mature.

In contrast, the historic IBM had a longer term perspective and could think about the manufacturing technologies needed 5 years down the road. However, today with the realities of the marketplace, vertically integrated manufacturers like IBM and Agere only spend about 0.4% of revenue on long range packaging development. Companies that have some captive ability but rely on sub-contracting (AMD, Intel, TI) spend about 0.3%. In contrast the subcontract assemblers spend 1.5 - 2.5 %. Fabless companies such as Altera, VIA spend less than 1% today but may put more in the future.

John Nickelsen, VP Sales of ASE, made it clear that their R&D was driven by the immediate needs of their customers. He pointed out that using this approach the advances made were dramatic. For example, in 1991 their operation could be typified by 208 lead QFPs. However, by 2005 the complexity will have increased by a factor of 15 through the use of 3000 lead SiP. In addition flip chip has increased in use by a factor of 4 in the last few years. The lead frame solution is giving way to the flip chip and wafer level packaging. He sees the single chip solution in certain key markets but other products will need SiP development.

His shopping list included: embedded components in substrates, Pb-free bumping, Pb-free BGA flip chips, stacked die for SiP, Chip on Flex, ultra thin BGAs (3mil thinning of 8" wafers), and low strain opto/MEMS. He saw KGD as key to SiP and more development needed there. He noticed a trend for WLP to replace low pin cout packages.

Their business goal must be to shrink the cost of packaging as a percentage of final product price. Electronics moved into the realm of commodity but still has much room for targeted R&D to give the market edge.

Mario Bolanos, director of TI semiconductor packaging, maintained that TI still supports a strong internal packaging development but could not try to do everything themselves. They focus on R&D for their Key Markets. One challenge is to protect the fragile copper/low-K interconnections on advanced ICs. TI develops test die that minimize the development cycle times once the final product die is ready. He sees TI concentration on high performance die: 20 mm, >100W, 10,000 bumps, pitch of 150 micron, ultra-low alpha emitter underfill material, bump current density >100,000, wireless output, and possible stacked chips.

In general, Mario suggested to the audience that real systems houses develop the chip, package, and board simultaneously…not just with view graphs but with manufacturing development. TI is currently doing 20% inside and 30% external. They try to achieve 10% impedance control by computer modeling.

Tom Gregerich, Qualcomm Wireless, listed "Contemporary Issues in IC Packaging Engineering for Wireless Products:" (1) rate of technology introduction, (2) increase in level of product complexity, (3) unpredictable market and less development time, and (4) tech focused but cost driven.

He sees customers using discrete solution when ever it is cheaper. This is particularly true since time to market is usually the dominate force and integration takes more time.

Mario Bolanos (TI) and John Nickelsen (ASE)

He sees Intellectual Property as become a more important issue since fewer centers are developing the new packaging/manufacturing technologies. However, since the technologies are getting more complex it has become harder to prove that someone is copying your IP and not just an example of Darwinian parallel development. He sees room for both SOC and SIP in the future. The audience believed that in general the materials companies would continue to develop the packaging materials since the market will continue to expand. However, it was pointed out that no material makes real money for about 10 years and then only if it spins out many other daughter materials along the way.

ECTC Planery Session Looks to Future

Two potentially disruptive technologies were presented and another was loud in its absence.

Strained Silicon

E. A. Gene Fitzgerald of MIT (and Amberwave Inc) discussed the 13 year history of strained silicon. By placing traces of Ge and other elements in thin films of silicon on wafers, or other growth substrates, very high mobility transistor channels can be demonstrated. This faster mobility can result in faster transistors that may keep industry on the Moore's Law curve without having to go to yet finer channel lengths by lithography. This could be very economical in that the existing foundries could go for a few more generations with the same equipment, just different starting wafers.

He explained that there are only four big IC products that are surfing the advances of Moore's Law: FPGA, DSP, microprocessors, and memory. It was also pointed out that it is not clear that increasing the number of transistors to 400 million is really helping the already beleaguered system designers. Thus by making existing sized designs by faster transistors will have more impact than simply stuffing more transistors on the same chip size. Another manifestation of this problem is that most of the problem in layout of large ICs is the interconnections between transistors not the performance of the transistors.

In addition, Gene Fitzgerald looks at future microsystems as wanting to combine three vastly different functions: the digital, the fast analog, and the interface with E&M waves. Currently the last two functions are forming the bottle neck for today's microsystems since they are made of compound semiconductors which have not been obeying the same manufacturing history curves as silicon. He finds that by adding enough layers and enough Ge to some of these layers that all functions can be made on the same chip using existing manufacturing equipment. One such layering system has strains silicon on top, next Si(80%)Ge(20%), graded SiGe layer to reduce lattice mismatch with Si substrate on bottom.

Using variations of these strained layers gives electron mobility of 80% with another Ge rich layer which eventually increases hole mobility by 800%. The low temperature formation of some of these layers are currently being addressed. If one of the layers has Ge >70% one could add opto sources to the chip. One could also lower voltages evern further with increased Ge.

In summary, Prof Gene Fitzgerald considers that there is still room for 1000% performance improvements by making "designer" strained wafers for existing foundries. That message seemed to satisfy everyone in the audience that they had enough affordable technology advances to make it to retirement.

Polymer Transistors

Dr. Henning Sirringhaus of Plastic Logic Ltd followed with his presentation "Entering the Era of Polymer Transistors." Most of the audience was brought up familiarly fighting with inorganic crystalline semiconductors so this presentation made the first one seem almost possible.

Dr. Sirringhaus basic premise was that printing is a cheap, efficient well known technology. Thus if polymer materials can continue to be refined so that transistors of reasonable characteristics can be "printed" at the same dots-per-inch of the "National Geographic Magazine" there will be many applications that will be performed by polymers rather than silicon.

Most of the work to date has been on "pMOS" with special surface adhesivity pattern treatments to allow short channels to be easily printed. The best mobility have been achieved by vacuum deposition of pentacene (sp?). The mobility is 5 cm2/v.s. If this seems low one must understand that in the last 10 years the mobility in polymers has improved 4 orders of magnitude with no obvious wall in the future.

Dr. Sirringhaus convinced the originally skeptical audience of the viability of polymer electronics.

The Lack of the Barking Dog

Everyone expected to have another presentation on the leading edge of compound semiconductors. The Chair of the session, VP Phil Garrou, explained that several speakers had been lined up only to have their companies decline support. Since compound semiconductors have been the future of the industry for most of the audience engineers' careers, this may mean the beginning of the end of the compound industry (other than for niches like traffic lights). This would be another example of the silicon juggernaut grinding down any competition however promising it appears.

View from Hotel of the ECTC. Mississippi river with paddle wheel steam boats and commercial barges. Below are CPMT Board members taking a break.

ECTC Professional Development

There were 14 half day Courses offered at the beginning of the ECTC week. More than 260 eager engineers attended at least one. Such course work goes into depth in either a fundamental or a cutting edge technology used in the packaging/assembly industry. Each course is packed with information, so the typical student absorbs only a small percentage that their experience has prepared them to learn. This little slice helps make the student a better professional. Continued Education credits can be awarded with these classes as a way to document the accomplishment on your resume.

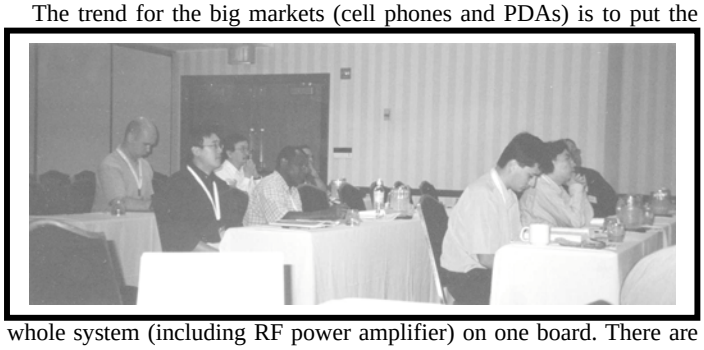
With that in mind a few courses will be reviewed from the perspective of one "old dog" student.

Hassan Hashemi taught a morning course entitled ***"Advanced Organic Substrate Package Design & Manufacturing for RF & Broadband Applications."*** Twenty students listened to and dialogued with his presentation. They came from around the globe and most were from industry. The teacher had much experience in RF board design and manufacture support at Rockwell Science System and now Mind Speed Inc. The student copy of the slides had many hard to find tables of material properties which would aid many design decisions and simulations.

It is the explosion in Wireless and Telecom Industries that have resulted in the drive for integrated, small, cost sensitive RF systems.

There were discussions on relative cost of organic RF boards versus ceramic. For large production runs of commodity product economy of factor of 4 were mentioned. However, as the organic board suppliers are being squeezed by market forces ceramic premiums of 20 - 230% are more typical.

The trend for the big markets (cell phones and PDAs) is to put the



whole system (including RF power amplifier) on one board. There are still some markets where PAs are built on ceramic (Hitachi). Three stages of integration are being pursued. (1) packaged discretes on a hybrid board, (2) bare chips on a MCP, and (3) so super integration like SiP or SoC. Some of the first MCPs were multiple chips on the same leadframe to use manufacturing infrastructure already in place.

In all three cases you need very good CAD tools with excellent libraries. In the case of the new SiP and SoC approaches the tools do not really exist and the NRE cost are $0.6 - 1.0M. As frequency is increased the designs are less tolerant to having plating stubs on the conductor runs so electroless plating is increasing in use.

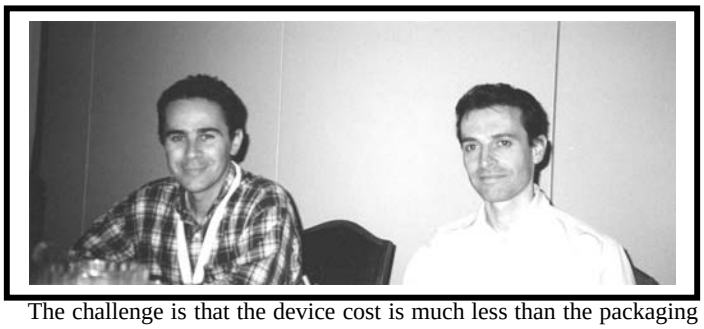
When doing the design, split it up into function modules and simulate and prototype each module to check for EMI/EMC since you will never solve these problems on the system level if you don't have a handle on them at the module level.

There was much discussion of integrating passives in the design. Several rules of thumb were suggested. The first was to look the designer in the eyes and say "you have to be kidding about the number of discretes you want to use…cut it to one third." The second was that using interconnection paths to make inductors often gains in performance, whereas resistor and capacitor chips are often the best way to go. As a designer one must be flexible even during the first build…often the values of discretes must change at the last minute.

Most organic boards have higher RF transmission losses than Ceramic, but some of the latest expensive organic materials (such as PTFE) are slightly better than ceramic. Flex substrates have not been used as much as predicted 10 years ago. This is partly because the frequencies are getting higher and flex gets lossy, and partly because flex companies are not prospering in any of their business lines.

When asked why most of the history of the RF board business is a story of incremental changes, Hassan responded that the market only has room for such improvements. Any breakthrough materials or geometries will need someone with deep pockets outside of the product shipment business…maybe dedicated universities or government labs.

An afternoon course entitled ***"Packaging Challenges for 10 Gb/s and 40 Gb/s ICs"*** was taught **by Roberto Coccioli and Hassan Hashemi**. About 30 engineers attended.



The challenge is that the device cost is much less than the packaging cost for this temperature range. It has become the roadblock for this telecommunication market. Today's limitations for this high bit rate can be listed as (1) packaging capability, (2) fast/efficient devices, (3) integration design, and (4) customer demand (recession).

The designs are dominated by optical communication protocols since this is the first large market to need (or think it needed) this high rate communication. The circuits are made either on ceramic (materials choices good to 40 Gb/s) and organic boards (organic composite polymers). A big process problem for thick film on ceramic is the control of the line width dimension to maintain a design impedance. Another problem is that for good ground planes at these high frequencies a 75% mesh is needed, but 50% mesh are what is typical for trying to prevent layers from delaminated.

Although bump bonding has higher performance, much of the assembly is done with clever implementation of wire bonds. If kept short, signal wires surrounded by ground wires, double wires replacing single, and capacitive pads used to cancel induction of wire…than wire bonding works to 50 Gb/s.

Designers now have the option of SiGe ICs but with x10 the NRE of GaAs designs. At lower frequencies enhanced Si CMOS design is gaining ground, but not yet at this higher bit rate range.

Connectors into and out of the modules must be designed for performance and for reliability since the exacting tolerances can not survive too many matings and temperature cycles.

Signals on the board must be sent along defined impedance paths such as microstrip or ground backed coplanar waveguides. The design needs computer simulation with codes such as HFSS or Cadence's Specter simulator.

With these great challenges to the engineer, perhaps there is a silver lining to the several years of low demand in the market. Perhaps design and process problems can be solved not just worked-around.

Packaging/assembly RoadMap Meeting held at ECTC this year

Academic Conference held just before ECTC starts

INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS

COMPONENTS, PACKAGES AND MANUFACTURING TECHNOLOGY SOCIETY
Components & RF Program Committee
RF & Wireless Technical Committee

ECTC 2004 - June 1-4
Caesar's Palace, Las Vegas, NV

The CPMT RF & Wireless Technical Committee in conjunction with the ECTC Components & RF Program Committee encourages you to submit an abstract to ECTC 2004 in the area of RF & Wireless Technology. In particular, RF papers are solicited for focus sessions on "Component-Like Modules with RF Functionality", as described below. Submissions in other areas of RF technology are also encouraged.

"Component-Like Modules with RF Functionality" (Organizer: Manos Tentzeris)

Emerging high-performance applications, such as personal communication networks, WLAN & RF-optical networks have defined a trend toward more flexible & reconfigurable systems. The RF front-end module is the foundation of these systems & its integration poses a great challenge. In the future, wireless communication will require better performance, lower cost & increasingly smaller RF front-end size. This session solicits papers in the area of "component-like modules with RF functionality" based on ceramic (LTCC), organic or MCM-based technologies. The components could include:

- Embedded passives (inductors, capacitors) & evaluation of their performance in terms of Quality Factor (Q), component value, fabrication challenges & cost
- Subsystem modules, such as filters, baluns
- Antennas that can be integrated in these RF compact modules
- Integrated transceiver architectures

It is strongly recommended that the technology used for each submitted paper should be compared with other technologies & evaluated in terms of advantages & disadvantages for the specific components

SUBMISSIONS:

Please submit abstracts using the ECTC web site: www.ectc.net (available in mid-July)

The ECTC 2004 deadline for abstract submissions is October 15, 2003 (approximate)

Abstracts should comply with the guidelines outlined at the above website.

If you would like to have your paper considered for the focal session outlined above, please do the following:

STEP #1: Submit abstract through the ECTC web site (www.ectc.net) and select "primary" subcommittee preference as "Components & RF"

STEP #2: For "Component-Like Modules with RF Functionality" email abstract copy to: Manos Tentzeris (etentze@ece.gatech.edu)

STEP #3: Also, email copy of abstract for both of above sessions to Craig Gaw at c.a.gaw@ieee.org & Len Schaper at schaper@uark.edu

To receive updates, send your email contact information to Craig Gaw at c.a.gaw@ieee.org .

FIRST CALL FOR PAPERS

54TH ELECTRONIC COMPONENT AND TECHNOLOGY CONFERENCE

www.ectc.net To be held in **Las Vegas, Nevada, USA, June 1-4, 2004**

The ECTC is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. The ECTC is jointly sponsored by the Components, Packaging and Manufacturing Technology Society of the IEEE and the Electronics Industries Association. You are invited to summit abstracts that provide non-commercial information on new developments, technology and knowledge in the following areas:

Advanced Packaging

New packaging technologies, systems packaging, designs, materials and configurations addressing performance density and cooling for single chip, multichip, wafer-level, MEMS and power packages. Special emphasis on flip-chip, fine pitch and high lead count packaging in CSP, BGA, CGA, LGA, SMT packages.

Components and RF

New passive or active component technologies, integrated - embedded components, RF and wireless component applications, component performance, and systems and reliability.

Education:

Education for engineering curricula in the 21st century and collaborative research and engineering programs between universities, government, or industry; development and the use of multimedia for packaging education.

Interconnections:

First level electronic interconnection technologies including, flip chip, 3D interconnect, lead-free, MEMS interconnect, under bump metallurgy, substrate metallurgy and interconnect (HDI and microvia), wire-bonding, TAB, conductive polymers for interconnect (ICA, ACF, ACP, NCP), wafer and device level interconnection, electrical issues of advanced interconnect structures and novel interconnects.

Manufacturing Technology

Processes and equipment for wafer thinning, bumping and stacking, chip packaging, high density and embedded component substrates, test and burn-in. Emphasis on cost, yield, performance and environmental improvements, process characterization, new product introduction and ramp, design for flexible manufacturing and testing.

Materials and Processing

Technology, development and application of adhesives, encapsulants, flip chip underfills, solders and alloys, magnetic and optical materials, ceramics, composites, dielectrics, thin films, thermal materials, bonding and plating processes.

Modeling and Simulation

Electrical, thermal, optical, mechanical modeling, simulation, characterization and packaging solutions, including system-level applications.

Optoelectronics

Packaging for fiber-optic modules, infra-red wireless, consumer optoelectronics, flat-panel, projection and microdisplays, solid state lighting, optical amplifiers, lasers, detectors, OEICs, optical data interconnect, optical backplanes, passive components, and WDMs.

Posters

Papers may be submitted on any of the listed major topics; presentation of papers in a poster format is highly encouraged at ECTC.

Quality and Reliability

Assessment, failure analysis, reliability testing and data analysis, failure and acceleration models, qualification of components and systems, KGD, incremental quality improvement, and TQM

Submittals

You are invited to submit a 750-word abstract that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net. If you have an questions. contact:

Patrick Thompson, Texas Instruments, Inc

PO Box 655012, MS940

Dallas, TX 75265 USA

Email: patrick.thompson@it.com

Phone: +1 972 995 7660; Fax: +1 972 995 2658

Abstracts must be received by October 15, 2003

PhoMat IEEE WESCON 2003 Symposium on "Photonics Materials Reliability"

Symposium: Thursday August 14, San Francisco==**with Short Courses:** Wednesday August 13, San Francisco

(**Organizer and Coordinator:** E. Suhir, University of Illinois, Chicago, IL—**Program Chair:** Dr. Michael Ushinsky

Organizing Committee:

Dr. Lauren Palmateer, Iridigm Corporation, San Francisco, CA

Dr. Annette Teng Cheung, Corwil Technology

Symposium on Thursday August 14, San Francisco

PhoMat is the first comprehensive and multifaceted symposium on Reliability of Photonics Materials, Structures and Systems. The Symposium brings together materials, mechanical, optical, electrical, reliability, industrial and manufacturing engineers, as well as applied physicists and chemists, to discuss and advance experimental and theoretical methods, techniques and approaches aimed at the understanding the materials behavior in, and mechanical (physical) design, packaging, and reliability evaluations and optimization of, optoelectronics and photonics devices and systems.

Objective

The objective of the Symposium is to address the state-of-the-art and the major problems in Photonics Systems Reliability, with an emphasis on the selection, characterization, and short- and long-term performance of photonics and optoelectronics materials. The reliability of optoelectronic and photonic components, devices, packages and structures will also be addressed, as well as their impact on the expected performance of large systems (say, telecommunications systems). Such systems typically contain both hardware and software. The ability to understand, analyze, predict and improve the operational availability of such systems is of substantial importance.

Short Courses on Wednesday August 13, San Francisco

Tutorials given by experts in the field of Reliability of Photonics Materials, Structures and Systems. The individual course offerings are listed on the **PhoMat** website (**www.cpmt.org/phomat/**).

- Short course listings and descriptions are posted. Please sign up early to ensure the course will be given. Without enough attendees the course will need to be cancelled.
- Request for attendance and all communication concerning this event to:

Dr. E. Suhir suhire@aol.com, 650-969-1530 **Dr. M. Ushinsky**, mikeunanotech@yahoo.com 949-653-7621

Dr. Lauren Palmateer, 415-626-8800- ext 137 **Dr. Annette Teng Cheung** Annette@corwil.com

Information and Registration: www.cpmt.org/phomat/

PhoPack™ 2003

PHOTONIC DEVICES & SYSTEMS PACKAGING

August 10-12, 2003------San Francisco, CA USA

This jointly sponsored symposium brings attendees into the forefront of photonic device packaging technology. The technical sessions explore major packaging technology areas and provide a state-of-the-art technical introduction. Technical presenters are leaders in their technology areas. Attendees have free access to the exhibits and programs of **WESCON**, the IEEE's major west coast exposition, which runs concurrently at San Francisco's Moscone Convention Center.

Professional Development Courses – Sunday, August 10:

- **Photonics Packaging: Critical Component Assembly and Test Processes**
- **How to Make a Photonic Device Into a Product: Role of Accelerated Life Testing**
- **Modeling and Simulations for Photonics Packaging**

PhoPack Symposium – Monday and Tuesday, August 11-12:

Keynote: **A Novel Way of Actively Aligning the Optics as Part of the Device**

Invited: **Wafer Level Packaging of MOEMS: Manufacturability Challenges In Optical Cross Connect**

Thermal Issues in Active and Passive Optoelectronic Devices and Integrated Circuits

Optical Alignment **The Photonics of Pulse Oximetry** **Monolithic Integration Technology**

New Hybrid Assembly Technology

Fluxless Wafer-Level Packaging of MEMS and Photonic Integration

Design Requirements for Passive Attachment of a Lensed Cap on a TO header for Laser Coaxial Packaging

Reducing Packaging Costs Through Automation of Fiber Pigtails

Optical Modeling of Channelized MEMS Equalization Filter/Blocker

Optical Nanocomposite Materials for Photonic Packaging **MEMS Reliability Testing in Optical Switching Applications**

Overview of Optical Medical Sensors **Design of a Uniform Scattering Element for Biomedical Applications**

Adhesives and Adhesion Reliability **New Evanescent Coupling Technology with Flip-chip Passive Assembly**

New "Optical Processor" Amplifier/Repeater Scheme for Gigabit Optics

Resource-Saving Optoelectronic Micro System Integration Process-Photolithographic Packaging with Selectively Occupied Repeated Transfer (PL-Pack with SORT) **The Effects of CTE Mismatch on Optical Performance of Packaged Planar Lightwave Circuit** ***Plan to attend!*** www.cpmt.org/phopack/

International IEEE Conference on Asian Green Electronics (AGEC)

January 5-6, 2004, City University of Hong Kong, Hong Kong, China
January 7-9, 2004, Mission Hills Resort, Shenzhen, China

CALL FOR PAPERS

You are cordially invited to submit papers to the International IEEE Conference on Asian Green Electronics (AGEC). The conference will be held in Hong Kong and Shenzhen, China (transportation to Shenzhen will be provided). The purpose of the conference is to present the latest advancements in environmentally compatible electronics design, manufacturing and packaging technology. The goal is to help electronics companies design and manufacture green electronics products for the global market.

Theme & Purpose of the Conference

The purpose of the conference is to present the latest advancements in environmentally compatible electronics design, manufacturing and packaging technology. The goal is to help electronics companies design and manufacture green electronics products for the global market.

Hong Kong & Shenzhen's Electronics Industries

A global trend in today's electronics industry is the relocation of advanced production plants and processes to the Guangdong province in China and specifically to the city of Shenzhen bordering Hong Kong. Today, Shenzhen is the major electronic manufacturing hub of the world. Shenzhen provides the electronics industry with an abundant supply of inexpensive land, subsidized state-of-the-art factory leases and labor. China's World Trade Organization membership should further enable Shenzhen to continue providing electronics manufacturing services, as well as to move to the top of the electronics industrial product chain in all aspects of product development.

With 35% of total export in electronics, Hong Kong is a strong supporter of Shenzhen. In fact, Hong Kong provides design and analysis support to China's manufacturing. In addition, half of Hong Kong's electronics exports come from the electronic parts and components industry, of which the largest export item is electronic parts and accessories for computers, telecommunications and consumer products.

Abstracts and Papers

Papers are now invited from other industry participants as well as researchers from academic and government organizations on the following topics:

- Design for green electronics
- Green manufacturing technologies including lead-free solders, conductive adhesives and other green technologies
- Halogen free substrates
- Environmentally Friendly Packaging and Design Technologies
- Life Cycle Analysis and Assessment
- Life Cycle Cost Analysis
- Life Cycle Data Management

An electronic form of a one-page, 300 word abstract with name, address, phone and fax numbers, and email address must be submitted to the technical committee by email at **wywong@ee.cityu.edu.hk** on/before September 01, 2003. Instructions for preparing the full paper will be sent to authors whose abstracts are accepted after review. Accepted papers will be published in a formal IEEE Conference Proceedings with an ISBN number. Participants will be required to register for the conference upon notification of acceptance of their full papers

Important Dates

September 01, 2003	Abstract Submission
September 10, 2003	Abstract Acceptance
October 13, 2003	Full Paper Due

Conference Correspondence and Inquiries

Ms. Angie Wong
Secretariat of International IEEE Conference (AGEC)
EPA Centre,
Department of Electronic Engineering,
City University of HK,
83 Tat Chee Avenue, Hong Kong
Tel: (852) 2788 7379
Fax: (852) 2788 7579
Email: wywong@ee.cityu.edu.hk
Website: http://www.ee.cityu.edu.hk/~agec/

49th IEEE HOLM Conference on Electrical Contacts 2003

September 8-10, 2003

Omni Shoreham Hotel, Washington, DC

Sponsored By The Components, Packaging, and Manufacturing Technology Society of the IEEE

Web Info http://www.ewh.ieee.org/soc/cpmt/tc1/

PURPOSE: To provide a forum for the presentation and discussion of the latest developments in the field of electric contacts and the application of recent advances in materials and processes in electric, electronic and telecommunications.

FOR WHOM: Practicing designers, engineers, physicists and research scientists – those new to the field and those experienced.

The 2003 Holm Conference will include excellent papers authored by some of the outstanding technical people in this field. The international contributors come from USA, China, Japan, United Kingdom, Canada, Germany, Austria, France, Russia, Ukraine, Norway, Singapore, and Switzerland. These papers, as a group, will provide the attendees with up-to-date information on a wide range of subjects that makes this conference so attractive to the practicing engineer. Additionally, the 2003 Holm Conference will have special speakers for the Ragnar Holm Scientific Achievement Award and the Mort Antler Lecturer.

TECHNICAL PAPERS & WORKSHOPS ON THE MOST RECENT WORK ON ELECTRICAL CONTACTS

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- High Frequency, High-Speed Data, Telecommunications, Degradation Effects

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- Crimp Terminals, Busbar, Lubricants, Glowing Contacts

CONTACT MATERIALS for Relays, Switches, Power Distribution Equipment

- High Frequency Relays, Ultra Miniature Relays, Reed Relays
- Air and Vacuum Materials, Carbon Fiber, Degradation Mechanisms
- Material Development, Switching Performance

ARC INTERRUPTION

- Circuit Breakers, Vacuum Interrupters, Hybrid Switches, High-Speed Film/Video, Micro-Arcing, Super-Conducting Limiters

MODELING

- 3D FEA, Dielectric Breakdown, Arc Motion, Dynamic Welding

MICRO MACHINED DEVICES

- Micro Switches, MEMS, NanoProbes, Field Emission

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445 Hoes Lane
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Email: holm2003info@ieee.org

Call for Abstracts

Send title and abstract (300 words), electronically, to wlp@ee.gatech.edu, by
October 1, 2003

Grand Hyatt Hotel
Atlanta, Georgia, USA
March 22-23, 2004

First International Workshop in

Nano Bio-Packaging

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