



IEEE COMPONENTS, PACKAGING AND
MANUFACTURING TECHNOLOGY SOCIETY



*PhoPack*TM 2003

PHOTONIC DEVICES & SYSTEMS PACKAGING

August 10-12, 2003

San Francisco, CA USA

This jointly sponsored symposium brings attendees into the forefront of photonic device packaging technology. The technical sessions explore major packaging technology areas and provide a state-of-the-art technical introduction. Technical presenters are leaders in their technology areas. Attendees have free access to the exhibits and programs of WESCON, the IEEE's major west coast exposition, which runs concurrently at San Francisco's Moscone Convention Center.

Professional Development Courses – Sunday, August 10:

- **Photonics Packaging: Critical Component Assembly and Test Processes**
- **How to Make a Photonic Device Into a Product: Role of Accelerated Life Testing**
- **Modeling and Simulations for Photonics Packaging**

PhoPack Symposium – Monday and Tuesday, August 11-12:

Keynote: A Novel Way of Actively Aligning the Optics as Part of the Device

Invited: Wafer Level Packaging of MOEMS: Manufacturability Challenges In Optical Cross Connect

Thermal Issues in Active and Passive Optoelectronic Devices and Integrated Circuits

Optical Alignment

The Photonics of Pulse Oximetry

Monolithic Integration Technology

New Hybrid Assembly Technology

Fluxless Wafer-Level Packaging of MEMS and Photonic Integration

Design Requirements for Passive Attachment of a Lensed Cap on a TO header for Laser Coaxial Packaging

Reducing Packaging Costs Through Automation of Fiber Pigtailed

Optical Modeling of Channelized MEMS Equalization Filter/Blocker

Optical Nanocomposite Materials for Photonic Packaging

MEMS Reliability Testing in Optical Switching Applications

Overview of Optical Medical Sensors

Design of a Uniform Scattering Element for Biomedical Applications

Adhesives and Adhesion Reliability

New Evanescent Coupling Technology with Flip-chip Passive Assembly

New "Optical Processor" Amplifier/Repeater Scheme for Gigabit Optics

Resource-Saving Optoelectronic Micro System Integration Process-Photolithographic Packaging

with Selectively Occupied Repeated Transfer (PL-Pack with SORT)

The Effects of CTE Mismatch on Optical Performance of Packaged Planar Lightwave Circuit

Plan to attend!

Additional information and registration
forms may be found at
www.cpmt.org/phopack/

More information: email
phopack@ieee.org