



Institute of Electrical and Electronic Engineers, Inc. Phoenix Section

Components, Packaging and Manufacturing Technology Society Chapter
&
Waves and Devices Chapter

PRESENT AN ALL DAY WORKSHOP ON

Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications

Date: Thursday, November 20, 2003 **Time:** 7:00 A.M. - 6:00 P.M.
Location: Arizona State University, Tempe, Arizona - Ventana Room - Memorial Union

Abstract

The one-day workshop will emphasize device, interconnect and packaging challenges to meet the next generation computing and communication applications. Participants will hear from leading contributors from the industry, academia and national labs. Long-range technology roadmaps will be reviewed. State-of-the art processor, memory, and mixed-signal technologies will be addressed. Chip, package, and board level interconnect issues will be discussed. Materials, process, and performance aspects of physically realizing the required interconnects and packaging will be presented. Market trends in computing and communications will be discussed. Panel discussion on the “future of computing and communications” will bring a closure to the day’s workshop. Vendors in the entire supply chain of chip, package, and board will display their products and services.

Topics

- ? Keynote Presentation – Technology Roadmaps
- ? State of the Art CMOS Technologies and Limitations
- ? Current and Future Memory Technologies
- ? Mixed – Signal Technologies
- ? Chip Level Interconnects
- ? Component Level Interconnects and Packaging Technologies
- ? Board and System Level Interconnects and Packaging Technologies
- ? Failure Analysis for Devices, Interconnects, and Packages
- ? Market Trends
- ? Vision of Next Generation Computing and Communication World
- ? Panel Discussion: Future of Computing and Communications

Vendor Display of Products and Services

For General Information
<http://www.ieee.org/phoenix>

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