Advance Program and Registration

ECTC 2004

The 54th Electronic Components and Technology Conference

June 1 – 4, 2004

Caesars Palace

Las Vegas, Nevada USA

Don't miss out on the industry's premier event.
For more information, visit:

www.ectc.net

ECA Electronic Components, Assemblies & Materials Association
CPMT
IEEE
EIA Electronic Industries Alliance

Introduction from the 54th ECTC Program Chair Patrick Thompson

The 54th Electronic Components and Technology Conference (ECTC)
Caesars Palace, Las Vegas, Nevada, June 1-4, 2004

The Executive and Program Committees of the Electronic Components and Technology Conference (ECTC) welcome you to our 54th meeting at Caesars Palace in Las Vegas.

This premier international conference continues to bring together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. The technical sessions focus on leading-edge developments and technical innovations in several areas, including: optoelectronics, advanced packaging technologies, high-performance package design, simulation and manufacturing interconnections and reliability.

The 54th ECTC provides a wealth of opportunities for education, discussion and networking. In 2004, we will provide 16 professional development courses, taught by leaders from industry and academia. This year's conference has more than 325 papers organized into 39 oral presentation sessions, plus two poster sessions, which provide the opportunity to exchange ideas and information with today's packaging technology leaders. This year, we are especially pleased to highlight papers in two special topic areas – MEMS and nanotechnology – as part of our ongoing effort to bring emerging technologies that have great future potential together with key established packaging technologies. Formal sessions are complemented by informal evening sessions on a variety of topics of interest to packaging technologists. These sessions allow for extensive interaction with presenters and other attendees. The Technology Corner offers companies the opportunity to exhibit their products and services in an environment that fosters discussion and interactions with engineers and managers attending the ECTC.

The ECTC depends on literally hundreds of skilled and dedicated persons each year for continued success. We extend our sincerest thanks to ECTC authors, speakers, instructors and exhibitors for your contributions and participation. We are most grateful to the Program Committee, Session Chairs and Co-chairs, those who made the conference arrangements and handled the publicity and publications. We thank the corporate coffee break and reception sponsors for their generous contributions which allow us to offer a high-quality technical program.

Finally we offer this conference program with pride and anticipation to all conference attendees. You are the reason for the ECTC, and we look forward to your comments on what we've done well and where we can improve to raise the quality and value of future conferences.

Patrick Thompson
54th ECTC Program Chair

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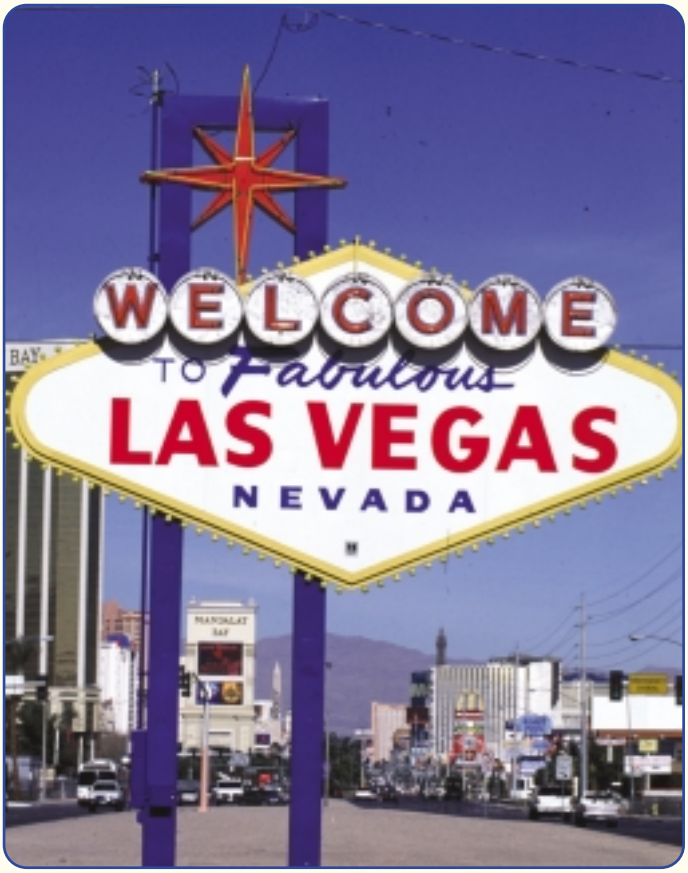

Photograph courtesy of Las Vegas News Bureau

54th ECTC Advance Registration

Advance Registration

To register in advance for the 54th ECTC, your application and payment check/credit card information must be received no later than May 15, 2004. Complete and submit the online registration form (preferred registration) at: www.ectc.net/reg.htm, mail to the address on the Advance Registration Form on page 31, or fax your form with payment information to (703) 875-8908.

Register early … save $100. All applications received after May 15, 2004 will be considered Door Registrations. Those who register in advance can pick up their registration packets at the ECTC Registration Desk in the Prefunction Area, 4th Floor at Caesars Palace. Additional Advance Programs are available from:

Jim Bruorton, Publicity Chairman
54th Electronic Components & Technology Conference
c/o KEMET Electronics Corporation
P.O. Box 5928
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Phone: (864) 963-6621 Fax: (864) 963-6444
Email: margieballinger@kemet.com

DO NOT SEND ADVANCE REGISTRATIONS TO THE ABOVE ADDRESS. SEE REGISTRATION FORM ON PAGE 29.

Registration Fees

Advance Registration with proceedings (CD or printed), CTC, CPMT and Program Chair Luncheons *$600
Door Registration with proceedings (CD or printed), ECTC, CPMT and Program Chair Luncheons *$700
One Day Registration $375
Speaker/Session Chair (Door Rate $500) $400
Speaker/One Day $250
Student Speaker $150
Student (1) $150
Tuesday Single AM or PM Courses with Luncheon . .#$350
Tuesday AM & PM Courses with Luncheon . . . . . .#$550
Student Tuesday All-Day Courses $75
Joint ECTC/ITHERM Advance $750
Joint ECTC/ITHERM Door $800
NEMI Workshop $75
Proceedings only, U.S. Postpaid $300
Foreign $350

* IEEE Member - Advance/$500, Door/$600
# Door rate will be an additional $50
(1) Students receive CD Rom.

Note: There will be no refunds on cancellations made after May 15, 2004.

At Door Registration Schedule

Registration will be held at the Prefunction Area (4th Floor) as follows:

Monday, May 31, 2004 – 3:00 to 5:00 PM (PD Courses & Conference)
Tuesday, June 1, 2004 – 6:45 to 8:00 AM (AM PD Courses Only)
Tuesday, June 1, 2004 – 11:00 AM to 1:15 PM (PM PD Courses Only)
Tuesday, June 1, 2004 – 1:15 to 5:00 PM (Conference)
Wednesday, June 2, 2004 – 6:45 AM to 4:00 PM
Thursday, June 3, 2004 – 7:30 AM to 4:00 PM
Friday, June 4, 2004 – 7:30 AM to 12:00 PM

The above schedule for Tuesday will be rigorously enforced to prevent students from being late for their courses.

General Information

Conference organizers reserve the right to cancel or change the program without prior notice.

Loss Due to Theft

Conference management is not responsible for loss or theft of personal belongings. Security for each individual's belongings is the individual's responsibility.

Coffee Break Sponsors

Sponsorships are available for companies that would like to participate in the 2004 Electronic Components and Technology Conference by assisting in sponsoring the conference breaks. Your company's name will be included in the conference final program and will be displayed on a sign in the refreshments area. A table will be provided nearby to display ***limited*** promotional/informational material about the companies sponsoring breaks. To sign up to sponsor a coffee break, simply indicate your interest on the Conference Advance Registration form (page 29) and enclose the $350 sponsorship fee, payable to the 54th Electronic Components and Technology Conference.

Please note: Sponsorships must be prepaid, and must be received at least four weeks before the conference in order to be listed in the Final Program. For further information, call EIA (703) 907-8027.

55th Electronic Components and Technology Conference

Wyndham Palace
Lake Buena Vista, Florida
May 31 - June 3, 2005
Make plans now to join us!

Technology Corner Exhibits

Although the current economic climate in the electronics industry is improving, companies are still being selective in choosing the conference and trade shows where they will exhibit their products and services. Each year more companies have determined that ECTC provides them the opportunity to identify superior prospects. The primary reason is that the engineers and managers who attend ECTC hold decision-making positions at the world's leading electronics industry's equipment and components manufacturers. The attendees are attracted by ECTC's strong technical program. Authors in the field believe that ECTC offers the best forum for presenting their work.

Exhibit hours will be from 1:30 to 6:30 PM on Wednesday, June 2 and 9:00 AM to Noon and 1:30 to 6:00 PM on Thursday, June 3. Exhibit spaces are still available. Following is a list of exhibitors as of February 2, 2004. The exhibit application, a current exhibitor list and the booth layout showing the available booths can be found on the ECTC web site at www.ectc.net under Technology Corner Exhibits. If you need additional information or have questions, call Bill Moody at (302) 478-4143, or email b.o.moody@ieee.org.

3M Electronics Markets Materials Div.
3M Microinterconnect Systems Div.
Advanced Packaging Magazine
Ansoft Corporation
ANSYS, Inc.
Asymtek
Bergquist Company (The)
Ceramics Process Systems Corp.
Chip Scale Review
Chip Supply, Inc.
Dow Chemical Co., (The)
Dow Corning Corporation
Electronics Cooling Magazine
Emerson & Cuming
Enerdyne Solutions
ENGENT, Inc.
Epoxy Technology, Inc.
ESPEC Corporation
Fluent Inc.
HD Microsystems
Henkel Loctite Corporation
Hitachi Cable America, Inc.
Indium Corporation of America
Innovative Research, Inc.
Interconnect Systems Inc.
KEMET Electronics Corporation
Kyocera America, Inc.
Matec Micro Electronics
Mini-Systems, Inc.
Mitsui Chemicals America, Inc.
NAMICS Technologies, Inc.
National Semiconductor Die Products
Optimal Corporation
Pac Tech Gmbh
PRC (Georgia Tech)
Rotys, Inc.
Semi Dice, Inc.
Semiconductor International
SIGRITY, Inc.
Sony Chemical Corp. of America
SUSS MicroTec
TechSearch International, Inc.
Temptronic Corporation
Thermagon, Inc.
Toray Engineering Co., Ltd.
Unitive, Inc.
Vishay Intertechnology, Inc.
Zymet, Inc.

ECTC Plenary Session

High-Density Interconnection
Wednesday, June 2, 2004 – 7:00 - 9:00 PM

Chair: **Yoshitake Fukuoka – Weisti**
Cochair: **Kishio Yokouchi – Fujitsu Laboratories of America, Inc.**

1. ***Recent Advances in Materials, Processes and High-Density Structures at GT-PRC***
   Venky Sundaram and Rao R. Tummala – Georgia Institute of Technology
2. ***Dielectric Materials for High-Density Interconnect Technology***
   Masahiro Ito and Shunsuke Yokotsuka – Asahi Glass Co., Ltd.
3. ***Recent Advances in Materials, Processes and High-Density Structures at GT-PRC***
   Venky Sundaram and Rao R. Tummala – Georgia Institute of Technology
4. ***Advanced Technology for High-Density Substrate and Boards***
   Yasuhito Takahashi – Fujitsu Microelectronics America, Inc.
5. ***High-Density and High-Frequency Silicon Substrate Technology for SiP***
   Atsushi Takano – Dai Nippon and Yoshitake Fukuoka – Weisti
6. ***Passive and Active Components Embedding Technology for High-Density Substrate***
   Masaaski Katsumata – Matsushita Electronic Components Co., Ltd.
7. ***A consideration for Total Mechanical Stress in Flip-Chip Packaging Utilizing Buildup Substrate Technology***
   Yutaka Tsukada – Kyocera SLC Technologies Corporation

ECTC NEMI Tin Whisker Workshop

Tuesday, June 1, 2004 –8:30AM - 5:00PM
Course Director: Ron Gedney

With the move toward Pb-free electronics, a popular finish for component terminations is 100% tin (Sn). However, pure Sn coatings have a tendency to grow small filaments, popularly called "whiskers," that can bridge adjacent terminals, causing system failures. The National Electronics Manufacturing Initiative (NEMI) formed three projects to work on this phenomenon: Accelerated Test (to develop accelerated tests to predict tin whiskers); Modeling (to understand basic cause of whiskers); and User Group (to determine how high-reliability, long-life systems can be protected with today's knowledge). This workshop will provide an overview of more than three years' work investigating all aspects of tin whiskers from all three projects. Attendees will get a good overview of tin whiskers, a set of tests recommended to JEDEC, basic theories behind whisker formation, and how to protect system reliability given what we know today.

Photograph courtesy of Las Vegas News Bureau

Luncheons

Professional Development Course and NEMI Workshop Luncheon

The Electronic Components and Technology Conference will sponsor a luncheon on Tuesday, June 1st, for all Professional Development and NEMI Workshop attendees.

ECTC Luncheon

The Electronic Components and Technology Conference will sponsor a luncheon on Wednesday, June 2nd, for conference attendees.

CPMT Luncheon

The IEEE Components, Packaging and Manufacturing Technology Society will sponsor a luncheon for conference attendees on Thursday, June 3rd.

Program Chair Luncheon

On Friday, June 4th, the Program Chair will sponsor a luncheon for conference attendees.

54th ECTC Gala Reception

All badged attendees and guests are invited to attend a reception hosted by AVX Corporation, KEMET Electronics Corporation, KOA Speer Electronics, Inc., Murata Electronics North America, ROHM Electronics USA, and Vishay Intertechnology, Inc. on Thursday, June 3rd at 6:30 PM.

General Chair's Speakers Reception

Tuesday, June 1, 2004
6:00 PM - 7:00 PM
(by invitation only)

Hotel Accommodations

Rooms for ECTC attendees have been reserved at Caesars Palace. The special conference rate is $165 for Run of House and $199 for Palace Tower Rooms. There are 2,500 rooms and suites, three spacious casinos, four lounges, nineteen restaurants, a health spa, a fitness center, three swimming pools, an Omnimax theatre, and the Appian Way and Forum Shops available to you for greater luxury and comfort during your stay.

Room reservations must be made directly with the hotel by April 29, 2004 to ensure special convention rates. If you need to change or cancel your reservation, please do so prior to three (3) days or 72 hours before arrival date to avoid forfeiture of deposit. Check-in time is 3:00 PM and check-out time is 12:00 PM. Most major credit cards are accepted. Call for booking assistance today at (702) 731-7222 or 800-634-6661 and mention ECTC for discounted rates or fax (702) 731-7172.

Photograph courtesy of Caesars Palace

Area Attractions

There is plenty to see and do in Las Vegas. You can start at one end of the strip and stop at every hotel to do something different. Adventuredome Theme Park is located at Circus Circus offering 21 rides and attractions. Free circus acts are performed daily inside. The Eiffel Tower located at the Paris Hotel offers the 50-story tower to take a panoramic view of the Las Vegas Valley. Shopping has not been forgotten either. The Forum Shops and the Appian Way are located at Caesars Palace along with the famous Roman statues that come to life at the Festival Fountains. The Bellagio Hotel is the place to see dancing fountains that are choreographed to music by artists such as Frank Sinatra, Elton John, Henry Mancini and more. If you want to go to the beach in the middle of the desert, stop at Mandalay Bay. Enjoy a swim, then visit the aquarium. Treasure Island and the pirates are great fun for everyone. The Mirage's 54-foot volcano eruption every 15 minutes from dusk to midnight is always exciting.

Just 30 miles from Las Vegas on Highway 93 is the Hoover Dam and Power Plant that was built in 1937. The Visitor Center is open from 9:00AM to 5:00PM. Close to 1,000,000 visitors a year visit this National Historic Landmark. Tickets are $10 each for adults ($8 Seniors), children 7 - 16 are $5 and children 6 and under are free. What a great family trip!

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Professional Development Courses June 1, 2004

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MORNING COURSES 8:15 AM – 12:00 PM

1. OPTOELECTRONICS COMPONENTS AND MODULES FOR COMMUNICATION NETWORKS

Instructor: Bill Ring
Tyco Electronics

Course Objectives:
Optoelectronics components and modules for the communications industry and networks are continuously advancing in terms of speed, lower cost and design for high volume manufacture. The objectives of this course are to provide a background on the current industry active components and packaging approaches and review the direction of active devices and packaging technology for discrete components and data network modules. The course will cover the fundamentals of active III-V devices, manufacturing of components and transceivers for the communications industry.

Course Outline:
- Overview of communication requirements
- Brief overview of semiconductor devices for active communications devices
- FP and DFB directly moduled lasers
- VCSEL device for datacommunications
- Packaging technology for communication components
- Low-cost plastic optics based packaging
- TO-style packaging & high-speed RF packaging
- Reliability of components
- Silicon optical bench technology
- Modules for datacom
- SFF and SFP datacom modules
- 10 Gigabit ethernet transceivers
- Parallel module technology

Who Should Attend:
This course is intended for engineers and managers who are involved in the design of components and modules for communication networks. It will be beneficial for those who require a fundamental understanding and broad perspective on active components for LAN, SAN OI connection and telecom modules, specifically technology, and manufacturing issues.

2. ADVANCED ORGANIC SUBSTRATE PACKAGE DESIGN & MANUFACTURING FOR RF AND BROADBAND

Instructor: Hassan Hashemi
Mindspeed Technologies, Inc.

Course Objectives:
The objectives of this course are to review design and manufacturing practices and tradeoffs affecting current and next-generation wireless and broadband IC packaging using laminate substrate technologies in single or multiple die format. The course material is based upon the instructor's experience in current micro-modules designed for GHz IC packaging for wireless and wireline communication and storage area networking applications.

Course Outline:
- Review design and manufacturing practices and tradeoffs
- Ceramic versus laminate substrate-based packaging
  - Micro-module design features with chip-on-board and surface mount technologies
  - Design tradeoffs for high volume manufacturing
  - Laminate module electrical, thermal, and mechanical design features
  - Laminate package materials
- Example package design considering performance, cost & manufacturing
  - Embedded passives in laminate substrates
- Organic substrate package assembly overview
  - Die attach, wire bond, overmold, saw & singulation
  - Process tolerances and their effects on performance
- Conclusions

Who Should Attend:
Engineers and technical managers who are involved in the design and manufacturing of electronic components and modules for wireless and broadband networking or storage applications. Attendees will learn about materials, processes, and design practices used for wirebond ICs, SMDs, and organic substrate modules used in high volume RF/GHz IC and system packaging.

3. INTEGRATED PASSIVE TECHNOLOGY AND COMMERCIALIZATION

Instructor: Richard Ulrich
University of Arkansas

Course Objectives:
This course will be a comprehensive review of potential applications, commercialized technology, and possible future directions in integrated passive components and processing for organic boards. The organization of the course centers on the benefits and problems with their implementation in order to help potential users make decisions about their applicability in a given situation. Considerable time will also be spent on the candidate materials and processes for integrated resistors, capacitors and inductors in order to help the potential user decide what processes can provide the needed electrical performance while being compatible with their existing substrates and fabrication technology. Emphasis will also be placed on electrical testing, since users of integrated passives will find themselves in the business of producing passive components, not just buying them, since the electrical performance characteristics of integrated passives can be very different from their surface-mount counterparts, possibly providing significant competitive advantages. Several current potential applications will be described, with particular emphasis on decoupling. The course emphasizes applicability to manufactured microelectronic systems and includes theoretical material necessary to support that purpose.

Course Outline:
- Why use IPs?
- Substrates of interest
- Integrated resistors
- Integrated capacitors
- Integrated inductors
- Electrical measurement of integrated passives
- Applications favorable for integrated passives
- Economics of IPs
- Tolerance, repeatability and yield issues
- Commercialized systems
- Where are integrated passives going?

Who Should Attend:
Engineers and scientists involved in electronics packaging, circuit board manufacture, electrical design and passive component technologies.

4. POLYMERS FOR ELECTRONIC PACKAGING

Instructor: C. P. Wong
Georgia Institute of Technology

Course Objectives:
Polymers are widely used in electronic packaging as adhesives, encapsulants, insulators, dielectrics, molding compounds and conducting elements for interconnects. These materials also play a critical role in the recent advances of low-cost, high performance novel no flow underfills, reworkable underfills for ball grid array (BGA), chip scale packaging (CSP), system on a package (SOP), direct chip attach (DCA), flip chip (FC), paper-thin IC and 3D packaging, conductive adhesives (both ICA and ACA), embedded passives and nano-functional materials. It is imperative that material suppliers, formulators and their users have a thorough understanding of polymeric materials and their importance in the advances of the electronic packaging and interconnect technologies.

Course Outline:
- Overview of semiconductor packaging technology
- Next generation of electronic packaging
- Common electronic packaging materials: conformal coating, glob-top, potting and casting
- Novel no-flow, advanced and reworkable underfills for flip-chip applications
- Conductive adhesives for lead-free interconnects – fundamentals and recent advances
- Low-cost high-performance embedded passives materials and processes
- Recent advances on nano photonic and low dielectric (k) materials and nano-functional materials

Who Should Attend:
Engineers, scientists and managers involved in the design, process and manufacturing of IC electronic components and hybrid packaging, electronic material suppliers involved in materials manufacturing and research and development.

5. SYSTEM-ON-PACKAGE (SOP) VS. SYSTEM-IN-PACKAGE (SIP), AND SYSTEM-ON-CHIP (SOC)

New Paradigms in Electronics
Instructor: Rao Tummala
Georgia Institute of Technology - Packaging Research Center

Course Objectives:
This course presents an overview of the Georgia Tech Packaging Research Center's SOP (System-on-Package) vision for highly integrated and microminiaturized convergent systems with consumer, computer, communication and bio-medical functions implementing an integrated approach to digital, analog, RF, optical and sensing technologies. The SOP paradigm changes the current chip-centric SOC methodology to a cheaper, faster-to-market IC-package co-design-centric microsystems packaging design and technology flow. The advantages of the SOP paradigm over SOC appear overwhelming due to SOP's design simplicity, lower cost, and higher electrical performance, and without the intellectual property issues that dominate SOC. To realize these enormous advantages, new SOP sub-technology paradigms are required. These include mixed-signal design, ultra high-density embedded digital, embedded optoelectronics and embedded RF component integration as well as wafer level packaging (WLP) and assembly, test and burn-in, thermal management and system reliability. A key technology paradigm, which Georgia Tech has been developing with the National University of Singapore, is the concept of nanoscale WLP, testing and burn-in, which promises ultimate size miniaturization, and virtually unlimited interconnections by means of nanoscale interconnections. This course makes a compelling case for and presents the status of SOP R&D around the world and compares and contrasts with SOC, SIP and MCM.

Course Outline:
- System trends to convergent systems
- Semiconductor trends to SOC
- IC and systems packaging evolution
- Five approaches to convergent systems
- What is SOP, and why?
- Global developments of SOP
- Comparison of SOC, SIP, MCM and SOP
- Status of SOP technologies
- What next after SOP?

Who Should Attend:
This course is an overview course and is suitable for all levels of R&D management, senior engineers and executives involved in technical strategy, R&D, design, manufacturing, process and product development of electronic packaging and systems in automotive, consumer, communication, computer, biomedical, and aerospace industries.

6. "NANO" - THE NEXT TECHNOLOGY?

Overview of Nano-Technology
Instructors: Walter Trybula
International SEMATECH and
Deb Newberry
Newberry Technologies

Course Objectives:
Nano is the catchall phrase that is used to imply some super advanced technology. Everyone has a different idea of what it means. This introduction to nano-technology will provide an overview of various aspects of nano including bio-tech and electronics. Nano-technology started with the carbon Buckyballs, which consist of 60 carbon atoms formed in a sphere. Stretching the Buckyballs creates carbon nanotubes. Nanotubes have low resistance, which has given rise to some predictions of grids of nanotubes for carrying electrical signals. Starting with the Buckyballs more than 20 years ago, the technology has grown exponentially. The explosion of new applications has occurred in the last few years and has become the center of businesses' attention in a search for new areas of expansion. There is a need to understand what this new technology really is. This course provides an explanation of basics of nano-technology. The purpose is to give the attendees an overview of potential applications and an understanding of some of the complexities of developing nano-technology products.

Course Outline:
- Introduction to nano (including what is nano?)
- An overview of nano-bio
- Specific benefits
- Business requirements
- Packaging potential
- Economics and world competition
- The future and the challenges
- Where do we go from here?

Who Should Attend:
This introductory course is focused on people who desire a better understanding of the developing field of nano-technology. It will also be of interest to people who need to become involved in business dealing with nano-technology.

7. MICROELECTRONIC AND MEMS SENSORS

Instructors: Gábor Harsányi and Zsolt Illyefalvi-Vitez
Budapest University of Technology and Economics

Course Objectives:
The course provides participants with an overview of microsensors, i.e. miniature devices for measuring physical and chemical quantities such as pressure, acceleration, speed, chemical concentration, etc. Microsensors fabricated by solid-state and MEMS technology, from ceramics, thin and thick films, polymer films, as well as by optical fiber technology are described and characterized. The different sensor structures in use, the most important sensing effects, as well as the principles of sensing various parameters are presented. The overview of application fields includes industrial process control, automotive

and household case studies, with a special focus on environmental monitoring and biomedical applications. Advances in sensor packaging, modeling, design and fabrication are also described shortly. The presentation will use the magnificent virtual tools of SensEdu and MEMSEdu, which are tools developed as a CPMT initiative in the frame of IEEE/NSF faculty fellowship program.

Course Outline:

- Sensor technologies and materials:
  - Solid-state semiconductor and ceramic technologies
  - Thin and thick film, polymer film, and optical fiber based sensor technologies
- Sensor structures, basic models of sensor operations:
  - Impedance type sensors, semi-conductor devices, calorimetric sensors, electrochemical cells
  - Sensors based on acoustic wave propagation, sensors with optical waveguides
- Sensing effects, basic principles of microsensors:
  - Thermoresistive, thermoelectric, piezoelectric, pyroelectric, piezoresistive, Hall effect
  - The principle of adsorption and the absorption of chemical species; selective molecular receptors
  - Permeation through membranes, ion-selective membranes, chemical-optical transduction effects
- Sensing various parameters:
  - Sensors for mechanical parameters, such as pressure, force, acceleration, angular displacement
  - Thermal, acoustic, radiation, magnetic field, chemical sensors and biosensors
- Application fields: overview and case studies
  - Industrial process control, automotive, household
  - Environmental monitoring and biomedical applications

Who Should Attend:

The course is designed for electrical, mechanical and chemical engineers, physicists, technical managers, salesmen and students who wish to get a comprehensive overview of microsensors' operation principles and characteristics, and to learn more about their applications. The course focuses on practical aspects and addresses field engineers and technicians from companies as well.

8. MICROELECTRONICS PACKAGING AND INTERCONNECTION - A WORLDWIDE PERSPECTIVE

Instructor: E. Jan Vardaman
TechSearch International Inc.

Course Objectives:

This course will cover developments and trends in area array packages. Ball grid array (BGA) packages are increasingly found in products including personal computers, portable communications devices, workstations/servers, mid-range and high-end computers, network and telecommunications systems, and even automotive applications. Package trends and new developments are described. Driven by the demand for smaller, lighter, thinner portable products has come the development of chip scale packages (CSPs). Discussed are the various types of CSPs in volume production and new developments such as wafer level packages. Flip chip's advantage over wire bond interconnection includes higher density mounting, improved electrical performance, and improved reliability for many applications. New applications for flip chip are described. Also included are trends, such as bump pitch, bump metallurgy, and substrate feature sizes.

Course Outline:

- Overview and trends in micro-electronics packaging and interconnect technology
- BGA - definition, package constructions, major volume applications by package type, new developments by package type, and new developments especially in high-performance packaging
- CSP - definition, package constructions, major volume applications by package type, new developments by package type, and new developments including wafer-level packages
- Flip chip related technologies - definition, flip chip in-package (FCIP) and flip chip on board (FCOB) applications, drivers for expansion, and future trends
- In addition, samples of packages/substrates/modules will be used during this course to illustrate the topics described above. Photos of products using advanced packages will also be included in this course.

Who Should Attend:

This course will be beneficial to all managers and individual contributors from the electronics industry who need fundamental understanding and broad perspective on microelectronics packaging and interconnect technology, especially in technology trends and key developmental areas such as BGA, CSP, and flip chip.

AFTERNOON COURSES
1:15 – 5:00 PM

9. RF/WIRELESS PACKAGING

Instructors: Joy Laskar and Emmanouil (Manos) M. Tentzeris
Georgia Institute of Technology

Course Objectives:

Review the latest developments in the area of next-generation RF/ microwave packaging. Investigate different materials and topologies. Present integrated solutions for wireless transceivers incorporating packaging adaptive antennas. Discuss possible solutions for RF-MEMS packaging problems. Provide easy-to-use design rules using CAD tools. Present integrated modules for WiFi and 60 GHz broadband communication/sensor applications.

Course Outline:

- Vertical interconnects (flip chip, BGA, PGA)
- Embedded components in organics and ceramics (LTCC) and LCP materials
- Integrated inductors, filters, duplexers in 3D configurations
- Packaging adaptive ultracompact and multiband antennas
- Integrated wireless transceivers for WiFi and mm-wave applications
- RF-MEMS
- Practical designs using modeling CAD tools
- Discussion of the challenges for the extension of designs in UWB

Who Should Attend:

Engineers and technical managers who would like to get familiar with the challenges and problems encountered in RF/Wireless packaging.

10. WAFER LEVEL - CHIP SCALE PACKAGING

Instructor: Luu T. Nguyen
National Semiconductor Corporation

Course Objectives:

Wafer level-chip scale packaging (WL-CSP) has gained momentum in the small chip arena lately, driven by needs for cost reduction, form factor shrinkage, and enhanced performance. This course will provide an overview of the WL-CSP technology. The market drivers, benefits, and challenges facing industry-wide adoption will be discussed. The current WL-CSP configurations

IMPORTANT NOTICE

It is extremely important to register in advance to prevent delays at door registration. Course sizes are limited.

will be reviewed in terms of their construction, manufacturing process and published electrical/thermal performance, together with package and board level reliability. Since the technology marks the convergence of fab, assembly and test, discussion will also address some fundamental issues such as: Where would it fit best (front end or back end)? Will it be applicable and cost-effective for complex devices such as microprocessors? Are current standards (design rules, outline, reliability, etc.) applicable?

Course Outline:

- Wafer level-chip scale packaging (WL-CSP) - definition
- Market drivers for WL-CSPs
- Benefits of WL-CSPs
- Barriers and challenges for WL-CSPs
- Review of current WL-CSPs in the industry
- Wafer level testing - status and challenges
- Infrastructure service providers
- Future trends: lead-free, large die size, wafer level underfill

Who Should Attend:

The course will be useful to the following three groups of engineers and scientists:
1. Newcomers to the field who would like to obtain a general overview of WL-CSP; 2. Those who are already practicing research and development of IC packaging and would like to learn new methods for solving CSP problems; and, 3. Those who are currently considering WL-CSP as a potential CSP alternative for their interconnect systems.

11. MICROVIAS & HIGH-DENSITY INTERCONNECTS FOR ADVANCED PACKAGING

Instructor: Ricky Lee,
Hong Kong University
of Science and Technology

Course Objectives:

This course will introduce the cutting-edge information on the most important development and latest research results in applying microvias and high-density interconnect technologies to advanced packaging. For professionals active in microelectronic packaging research and development, those who wish to master high density interconnect technologies, and those who need to choose a cost-effective design and high-yield manufacturing process for their electronic systems, this is a timely summary of progress in all aspects of this fascinating field. The lecture contents are based on the instructor's books on electronic packaging, his recent research results, and interactions with the packaging and assembly industries. The scope of course covers flip chip and CSP technologies, wafer-level packaging, microvias and build-up substrates, and emerging high-density interconnect technologies. With the information provided in this lecture, the attendees will acquire a practical understanding in the design, materials, processes, analysis, and reliability issues of high-density interconnection technologies.

Course Outline:

- Overview of area array and high-density interconnect technologies
- Solder-bumped flip chip & wafer level chip scale packages
- Formation of microvias on silicon wafer
- Formation of microvias on organic substrate
- Copper-plated and conductive paste/ink-filled microvias
- Special high-density interconnect technologies
- PCB/substrate with sequential build-up layers
- Reliability issues of high-density interconnects

Who Should Attend:

This short course is intended for research scientists, professional engineers and technical managers who are involved in IC packaging, component assembly, materials and processing, contract manufacturing and marketing.

12. INTERCONNECT AND PACKAGING TECHNOLOGIES FOR 10 AND 40GBPS TELECOM AND DATACOM

Protocols, Design, and Case Studies

Instructors: Roberto Coccioli,
Inphi Corporation and
Hassan Hashemi
Mindspeed Technologies, Inc.

Course Objectives:

The objectives of this course are to review challenges in 10G and 40G IC packaging considering requirements posed by mixed IC technologies and system architecture as defined in industry Multi Source Agreements. Moreover, it is intended to review the technologies available to realize package and board interconnects assessing their relative performance and their impact on signal integrity on high-speed digital signaling. The course material is based upon the instructors' experience on current practices used for GHz IC packaging for telecom, storage, and datacom applications.

Course Outline:

- Review of 10G & 40G system features & packaging challenges
- OE systems requirements and protocols
- Standards for 10Gbps and 40Gbps transponders
- Substrate technologies for 10Gpbs and 40Gbps applications
- Ceramic: thick-film, thin-film, HTCC, LTCC, low resistance multilayer alumina
- Organic: high Tg FR4/BT, PTFE glass fiber, PTFE ceramic
- Leadframe based chip-scale packages
- Effects of interconnects on signal integrity
- First level interconnect: wirebonds, ribbons and flip-chip
- Transmission lines: CPW, microstrip, stripline
- Second level interconnect: BGA, LGA, QFP, QFN
- Connectorized packages for 10Gbps and 40Gbps ICs
- Connector types: threaded & push-on
- 10Gbps and 40Gbps IC package design examples
- Manufacturing tolerances and their effects on performance
- Conclusions

Who Should Attend:

The course is designed for engineers or engineering managers who want to understand more about technical challenges of high-speed packaging, trends, and the unique requirements posed on technology selection and design to assure the achievement of stringent electrical and thermal performance in cost-performance efficient manufacturing.

13. PACKAGE FAILURE ANALYSIS - FAILURE MECHANISMS AND ANALYTICAL TOOLS

Instructors: Deepak Goyal
and Rajen Dias
Intel Corporation

Course Objectives:

The seminar will provide an overview of the failure modes and mechanisms observed in the plastic packages. A brief introduction to the methodology of failure analysis of these packages will be described. Emphasis will be paid to the tools and techniques currently used and the future direction for the tools and techniques required for successful and timely failure analysis of next generation package technologies.

Course Outline:

- Package technology; trends, drivers & challenges
- Failure analysis challenges offered by package technology roadmap
- Overview of the failure modes and mechanisms observed in the organic packages
- Introduction to the methodology of failure analysis of organic packages
- Current analytical capabilities for package fault isolation and failure analysis
- Analytical capabilities to support next generation packaging

Who Should Attend:
Engineers and technical managers who are involved in package technology development, reliability assessment of packages and failure analysis.

14. ADVANCED THERMAL MANAGEMENT MATERIALS

Instructor: Carl Zweben
Advanced Thermal Management

Course Objectives:
This PDC presents an in-depth overview of the increasing number of advanced thermal management materials that are continually emerging to solve critical design problems: heat dissipation, thermal stresses, size, weight and electromagnetic emissions. Advantages include: thermal conductivities up to four times that of copper; low, tailorable coefficients of thermal expansion; tailorable electrical conductivity; high strengths and stiffnesses; low densities; net shape fabrication processes. Payoffs include: increased reliability; reduced thermal stresses and warpage; reduced electromagnetic emissions; simplified thermal design; weight savings up to 90%; size reductions up to 65%; increased manufacturing yield; potential cost reductions. Advanced materials are now being used in high-volume commercial and aerospace production applications, including hybrid vehicles, trains, wind turbine generators, servers, cellular telephone base stations, cellular telephones, laptops, high-power radars, spacecraft electronics, avionics, etc. Components include IGBT packages, heat spreaders, heat sinks, microprocessor unit lids, solid and flow-through PCB cold plates, microwave modules, optoelectronic packages, etc. This PDC compares traditional packaging materials with the large and increasing number of advanced thermal management materials, which include: diamond particle-reinforced copper, aluminum, cobalt and silicon carbide; silicon-carbide-particle-reinforced aluminum (Al/SiC) and copper; carbon-fiber-reinforced polymers, aluminum and copper; beryllia-particle-reinforced beryllium; carbon/carbon composites; natural and highly oriented pyrolitic graphite; "ThermalGraph", etc. Topics include properties, processes, applications, costs, increasing manufacturing yield and future directions.

Course Outline:
- Introduction: design drivers; material requirements; example of successful advanced materials - Al/SiC
- Material property and test method issues
- Traditional packaging materials
- Advanced materials overview: monolithic materials; classes of composites
- Monolithic carbonaceous materials
- Reinforcements: carbon fibers; diamond particles; carbon nanotubes
- Metal matrix composites - Part 1
- Metal matrix composites - Part 2
- Metal/metal alloys-composites
- Carbon, polymer matrix and ceramic matrix composites
- Manufacturing processes
- Solving manufacturing problems and increase yield with composites
- Cost issues
- System applications: servers, laptops, avionics, base stations, hybrid vehicles etc.
- Component applications: modules, heat spreaders and sinks, cold plates, enclosures, optoelectronics, etc.
- Future trends

Who Should Attend:
Engineers and managers involved in electronic packaging design, production and R&D. Packaging material suppliers. Since many of the materials covered are new and not widely known, the PDC will benefit both novice and experienced personnel.

15. INTRODUCTION TO NANOSCALE PACKAGING AND SYSTEMS

Instructors: Rao Tummala, Georgia Institute of Technology - Packaging Research Center and Zhong L. 'ZL' Wang, Georgia Institute of Technology - Center for Nanoscience and Nanotechnology

Course Objectives:
This course introduces nanoscale packaging as an important emerging technology. As the semiconductor industry approaches an historic transition toward nanoscales of 100nm, and with more than 10,000 I/Os and 150 watts/chip, it is becoming clear that nano-packaging is necessary. Nano-packaging comes at two levels: IC and systems, together leading to nano-systems in a decade. Wafer-level packaging, with materials such as solders at 20 micron pitch, fail due to poor fatigue resistance. Compliant structures, on the other hand, are expensive and have too high an inductance and electrical resistance. However, nano-interconnections provide an opportunity to have the best of both electrical and mechanical properties, in addition to low cost and at-speed test and burn-in benefits not presently available. Today's systems packaging consists of bulk dielectrics, conductors for multilayer wiring; capacitors, resistors, inductors, filters for RF; and waveguides and detectors for optoelectronics interconnections, high thermal conductivity materials and designs for heat transfer, solders with underfills for assembly. Can these be scaled down to nano-dimensions with improved properties so as to end up with systems paradigms? This course reviews the status of and presents potential opportunities that nanoscience and packaging technology provide in each of the above.

Course Outline:
- Nanotechnology, what is it?
- Nanotechnology, why now?
- What is nano-packaging? Why now?
- Some research directions in nanopackaging:
  - Nano devices
    - CMOS and its nanoroadmap
  - Nanotubes and nanointerconnects
    - Materials growth
    - Self-assembly techniques
    - Property measurements
    - Integration with devices
  - Nano IC packaging
- Nanosensors
  - Quantom dots
  - Bioapplications of quantum dot
  - Wireless and electric signal based sensors
  - Integration of sensors with microsystems
  - Cantilever based sensors
- Nanowires and nanobelts-based devices
  - Field effect transistors
  - Biosensing
  - Piezoelectric nanobelts
  - Resonators
  - Cantilevers
  - Transducers and sensors
- Nanobioelectronics and fluidics
- Summary and outlook

Who Should Attend:
This course is an overview and introductory course and is suitable for all levels of R&D management, senior engineers and executives involved in technical strategy, future R&D investments, assembly manufacturing processes and product development of electronic packaging and systems in automotive, consumer, communication, computer, biomedical, and aerospace industries.

16. LEAD-FREE SOLDERS FOR ROBUST IC ELECTRONIC AND OPTOELECTRONIC PACKAGING

Instructor: John H. Lau
Agilent Technologies, Inc.

Course Objectives:
Since February 13, 2003, lead-free has been a law in EU (European Union). The implementation date is July 1, 2006. That means, after July 1st, all the electronic products (except those with exemptions) cannot be made in and shipped to EU. At the time being, China is considering to adopt this law. Recently, packages such as PBGA (plastic ball grid array), CSP (chip scale package), and especially WLCSP (wafer level chip scale package) have been very popular for consumer, computer, communication, optoelectronic, and

optical MEMS (micro-electro-mechanical system) products. Most of these packages use solders as their interconnects, thus they are affected by the lead-free regulations. In this course, some critical issues of lead-free soldering (such as cost, regulations, definitions, design, materials, forward- and backward-process incompatibility, and reliability of components, PCBs, tin whiskers, and solder joints) will be presented. Also, some critical issues of PBGA, CSP, WLCSP, optoelectronic, and optical MEMS will be discussed. The impacts of lead-free on PBGA, CSP, WLCSP, optoelectronic, and optical MEMS are examined. Most of the materials are based on the instructor's and his co-authors' (C. P. Wong, Ricky Lee, N. C. Lee, John Prince, Yi-Hsin Pao and Wataru Nakayama) recently published textbooks, "Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies", "Electronics Packaging", "Chip Scale Packages", "Low-Cost Flip Chip Technologies for DCA, WLCSP, and PBGA Assemblies", "Microvias for Low-Cost High-Density Inter-connects", and "Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive Adhesive Materials". (McGraw-Hill publishes all these books.) Each participant will receive a comprehensive set of handout notes. After completing this course, you will be able to: Understand all important aspects and critical issues of lead-free soldering; Have a head-start of lead-free soldering for your green products; Understand all important aspects of BGA, WLCSP, and flip chip technologies; Understand all important aspects of optoelectronic and MEMS technologies; Understand the real meaning of reliability; Identify key parameters that impact the lead-free solder joint reliability of your products; Avoid potential reliability problems due to lead-free soldering of your high-density products; Choose a cost-effective design of your high-density electronic and optoelectronic assemblies; Establish a high-yield manufacturing process.

Course Outline:

- Introduction
- IC trends and IC packaging technology update
- Optoelectronic and optical MEMS packaging
- Lead-free soldering
- Printed Circuit Boards (PCBs)
- Wave soldering technology
- Surface mount technology
- Flip-chip WLCSP technologies with solders
- Flip-chip WLCSP technologies with conductive adhesives
- Optoelectronic with lead-free technology
- Optical MEMS with lead-free technology
- Discussions

Who Should Attend:
If you are involved with any aspect of the electronics industry, you should attend this course. The content is recommended for component, packaging, design, material, process, equipment, reliability, product assurance, quality control, manufacturing, vendor, marketing, and sales engineers and managers. It is equally suited for R&D engineers and scientists.

Continuing Education Units

The IEEE Components, Packaging and Manufacturing Technology Society (CPMT) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Short Courses that will be presented at the 54th ECTC. CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia and workshops. IEEE CPMT CEUs can be applied towards the newly created "IEEE CPMT Professional Development Certificate." Complete details, including voluntary enrollment forms, will be available at the conference. All costs associated with ECTC Professional Development Courses CEUs will be underwritten by the conference, i.e. there are no additional costs for Professional Development Courses attendees to obtain CEU credit.

IMPORTANT NOTICE

AM Short Courses 1 through 8 or PM Short Courses 9 through 16 run concurrently. Make sure you indicate specific course numbers you plan to attend on page 31. The cost of each session (AM or PM) is $350. If you plan to attend both AM and PM courses, registration for all-day is $550. The student all-day course registration fee is $75.

Photograph courtesy of Las Vegas News Bureau

Program Sessions

Wednesday, June 2
Session 1: SIP/SOP
8:00 – 11:40 AM
Committee: Advanced Packaging

Session Co-Chairs:
Jeffrey A. Knight - Endicott Interconnect Technogies, INC.
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High Density and Compliant Wafer-Level Electrical and Optical Polymer Pilar Chip I/O Interconnections
Muhannad Bakir and James Meindl - Georgia Institute of Technology

MAP (Mobile AGP Processor) - A High- Performance Integrated Graphics Module
Raj Pendse, M. Yee, J. S. Yun and Bret Zahn - ChipPAC Inc.; Bob Jafari, Tim Lau, Mihalis Michael, Inderjit Singh and Orion Starr - NVIDIA Corp.

System-on-a-Package (SOP) Substrate and Module with Digital, RF and Optical Integration
Venky Sundaram, Rao Tummala, George White, Kyutae Lim, Lixi Wan, Daniel Guidotti, Fuhan Liu, Ravi Doraiswami, Joy Laskar, G. K. Chang, Manos Tentzeris and Madhavan Swaminathan - Georgia Institute of Technology

Process Development and Reliability for System-in-a-Package Using Liquid Crystal Polymer
Liu Chen and Johan Liu - Chalmers University of Technology; Xinzhong Duo - Royal Institute of Technology

Physical Design of Optoelectronic System-on-a-Package Using Optical Waveguide Interconnects
Chung-Seok (Andy) Seo and Abhijit Chatterjee - Georgia Institute of Technology; Nan M. Jokerst - Duke University

Thermal Limits of Fine Pitch Exposed Pad TQFP SIP for Hard Disc Drive Applications
Tiao Zhou - Texas Instruments; Bill Rugg - Seagate

Physical Layout Automation for System-On-Packages
Ramprasad Ravichandran, Jacob Minz, Mohit Pathak, Siddharth Easwar and Sung Kyu Lim - Georgia Institute of Technology

Wednesday, June 2
Session 2: Pb-Free Flip-Chip Interconnections I
8:00 – 11:40 AM
Committee: Interconnections

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Assembly and Reliability of Flip Chip Solder Joints Using Miniaturized Au/Sn Bumps
Matthias Hutter, Florian Hohnke, Hermann Oppermann, Matthias Klein and Gunter Engelmann - Fraunhofer IZM

A Low-Cost Plated Column Bump Flip Chip Technology for Sub-100um Pitch and WLP Applications
Dev Gupta, C. Holland and M. Fria - APSTL

FCOB (Flip Chip on Board) Reliability Study for Mobile Applications
Se-Young Jang, Soon-Min Hong, Hyun-Wook Nam, Min-Young Park, Sang-Hoon Roh and Young-Joon Moon - Samsung Electronics Co., Ltd.; Dong-Ok Kwak - Samsung Advanced Institute of Technology

Effect of Intermetallic Compounds on Reliability in Sn-Ag-Cu Flip Chip Solder Bumps for Different UBMs and Substrate Pad Finishes
Piyush Gupta, Ravi Doraiswami and Rao Tummala - Georgia Institute of Technology; Kensuke Nakanishi - Harima Chemicals

Study of Spalling Behavior of Intermetallic Compounds During the Reaction between Electroless Ni(P) Metallization and Lead-Free Solders
Yoon-Chul Sohn and Jin Yu - Korea Advanced Institute of Science and Technology; Sung K. Kang and Da-Yuan Shih - IBM T. J. Watson Research Center; Taek-Yeong Lee - Hanbat National University

Reliability of Lead-Free Copper Columns in Comparison with Tin-Lead Solder Column Interconnects
Rahul Joshi and Seungbae Park - State University of New York, Binghamton; Lewis Goldmann - IBM Corporation

Experimental Characterization and Mechanical Behavior Analysis on Intermetallic Compounds of 96.5Sn-3.5Ag and 63Sn-37Pb Solder Bump with Ti-Cu-Ni UBM on Copper Chip
Chih-Tang Peng, Chia-Tai Kuo and Kuo-Ning Chiang - National Tsing Hua University; Terry Ku and Kenny Chang - VIA Technology Corporation

Wednesday, June 2
Session 3: Innovative Testing Methods
8:00 – 11:40 AM
Committee: Quality & Reliability

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Prediction of Process-Induced Warpage of IC Packages Encapsulated with Thermosetting Polymers
D. G. Yang, K. M. B. Jansen and L. J. Ernst - Delft University of Technology; G. Q. Zhang - Philips-CFT; W. D. van Driel and H. J. L. Bressers - Philips Semiconductors; X. J. Fan - Philips

Towards a Predictive Behavior of Non-Conductive Adhesive Interconnects in Moisture Environment
Jo Caers, Xiujuan Zhao and Hansen G. Sy - Philips Electronics Singapore; Ee Hua Wong - Institute of Microelectronics (IME), Singapore; Subodh Mhaisalkar - NTU, Singapore

Detection of Flip Chip Solder Joint Cracks Using Correlation Coefficient Analysis of Laser Ultrasound Signals
Lizheng Zhang and I. Charles Ume - Georgia Institute of Technology; Juergen Gamalski and Klaus-Peter Galuschki - Siemens AG

Mechanical Characterization of Sn-Ag-Based Lead Free Solders
Masazumi Amagai - Texas Instruments, Inc.

Microstructural and Micromechanical Characterisation of Sn-Ag-Cu Solder FCOB Interconnects at Ambient and Elevated Temperatures
Changqing Liu, Dezhi Li and Paul Conway - Loughborough University

In-Process Measurement of the Interfacial Fracture Toughness for a Sub-Micron Titanium Thin Film and Silicon Interface Using a Single Strip Decohesion Test
Jiantao Zheng and Suresh K. Sitaraman - Georgia Institute of Technology

Determination of Fracture Toughness of Underfill/Chip Interface with Digital Image Speckle Correlation Technique
Zhang Yanlie and Zhou Wei - Nanyang Technological University; Shi Xunqing - Singapore Institute of Manufacturing Technology

Wednesday, June 2
Session 4: Adhesives and Encapsulants
8:00 – 11:40 AM
Committee: Materials & Processing

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Electrical and Thermal Conductivities of Polymer Composites Containing Nano-Sized Particles
Lianhua Fan, Bin Su, Jianmin Qu and C. P. Wong - Georgia Institute of Technology

Development on Wafer Level Anisotropic Conductive Film for Flip-Chip Interconnection
Jean-Charles Souriau, Jean Brun, Remi Franiatte and Gasse Adrien - CEA-Grenoble-LETI

Anisotropic Conductive Adhesives with Enhanced Thermal Conductivity for Flip-Chip Applications
Myung Jin Yim, Jin Sang Hwang and Jin Gu Kim - Telephus, Inc.; Woonseong Kwon, Kyung Woon Jang and Kyung-Wook Paik - Korea Advanced Institute of Science and Technology

Reliability Enhancement of Electrically Conductive Adhesives in Thermal Shock Environment
Haiying Li, Kyoung-Sik Moon, Yi Li and C. P. Wong - Georgia Institute of Technology

Integration of Low Stress Photopatternable Silicones into a Wafer Level Package
Geoff Gardner, Brian Harkness and Herman Meynen - Dow Corning; Mario Gonzales, Mathieu Vanden Bulcke, Bart Vandevelde and Eric Beyne - IMEC

Emerging Challenges of Underfill for Flip-Chip Application
Tim Chen - Intel Corp.

Hygro-Thermo-Mechanical Behavior of Mold Compound Materials at Elevated Environment
Sung Yi and Zeyan Yu - Portland State University; Raynard Neo - Micron; Yeong Lee - Dow Corning

Wednesday, June 2
Session 5: Low Cost Optoelectronic Packaging Technology
8:00 – 11:40 AM
Committee: Optoelectronics

Session Co-Chairs:
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Reliability Concerns and Packaging Issues of Non-Hermetic VCSEL- and LED-Based Transceivers for the Enterprise Market
William Ring, Peter Thambinayagam, Wayne Hobson, Henry Meehan, Ming Liang and Peter Silbermann - Tyco Electronics, Inc.

Optical SMT-Packaging for Highly Efficient and Reliable Fiber Optic Components Including 1300nm VCSELs
Hans L. Althaus, Marco Melinde, Gunther Steinle, Martin Weigert and Helmut Wietschorke - Infineon Technologies AG

A Low-Cost Plastic Package for 2.5Gbps Optical Transceiver Modules with High Electromagnetic Shielding
Tzong-Lin Wu, Wen-Chi Hung, Chien-Hui Lee, Cheng-Wei Lin and Wood-Hi Cheng - National Sun Yat-sen University; Wern-Shiarng Jou - National Kaohsiung University of Applied Sciences

Low-Cost Optical Subassemblies for Metro Access Applications
William Hogan, Robert Wolf, Anand Shulka and Phil Deane - JDS Uniphase Corp.

Unique 1 TO Structure Low-Cost Optical Subassembly
Masahiko Tsumori, Sun Hyoung Pyo, Joong Hee Lee, Young kwon Yoon and Taeil Kim - Samsung Electronics Co., Ltd.

Packaging of a High-Speed Optical Modulator Using Flip-Chip Interconnects
Yuvaraja Visagathilagar, Wayne Rowe and Arnan Mitchell - RMIT University

Ultra Compact Optical Subassembly Using Integrated Laser Diode and Silicon Microlens for Low-Cost Optical Components
Daisuke Shimura, Masahiro Uekawa, Ryo Sekikawa, Kyoko Kotani, Yoshinori Maeno, Hironori Sasaki and Takeshi Takamori - Oki Electric Industry Co., Ltd.

Wednesday, June 2
Session 6: Electrical Modeling
8:00 – 11:40 AM
Committee: Modeling & Simulation

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A Fast Full-Wave Modeling Methodology for Stripline Structures with Vertical Interconnects in Multi-Layer Dielectrics
Konstantinos Nikellis - Helic S.A. - National Technical University of Athens; Yorgos Koutsoyannopoulos and Sotiris Bantas - Helic S.A.; Nikolaos Uzunoglu - National Technical University of Athens

An Efficient Finite Element-Based Electromagnetic Field Modeling Methodology for Interconnect Structures Including Lumped Circuit Elements
Hong Wu and Andreas Cangellaris - University of Illinois at Urbana-Champaign

An Efficient Full-Wave Layered Interconnect Simulator (UA-FWLIS)
Xing Wang, Zhaohui Zhu, Steven Dvorak and John Prince - University of Arizona

Very High-Frequency Characterization of High-Density 3-D Module
Matti Mäntysalo, Jarmo Tanskanen and Eero O. Ristolainen - Tampere University of Technology

Modeling and Optimization of Multilayer LTCC Inductors for RF/Wireless Applications Using Neural Networks and Genetic Algorithms
Rana Pratap, Saikat Sarkar, Stephane Pinel, Joy Laskar and Gary May - Georgia Institute of Technology

A Simplified Cross Coupling Model for Multiple Balanced Transmission Lines
David Quint, Karl Bois and Yong Wang - Hewlett Packard Company

Characterization of Discrete Decoupling Capacitors for High-Speed Digital Systems
Joong-Ho Kim, Dan Jiao, Jiangqi He, Kaladhar Radhakrishnan and Changhong Dai - Intel Corporation

Wednesday, June 2
Session 7: Integrated Capacitor and Resistor Technology
8:00 – 11:40 AM
Committee: Components & RF

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Advanced Decoupling in High-Performance IC Packaging
Deepa Mannath, Leonard Schaper and Richard Ulrich - University of Arkansas

Novel Flexible and Thin Capacitors with Mn-Doped SrTiO3 Thin Films on Polyimide Films
Shintaro Yamamichi and Akinobu Shibuya - NEC Corporation

Thin-Film Low Inductance Decoupling Device for High Speed Digital Circuits
Junya Takafuji, Shigeo Konushi, Hisashi Nakashima, Seiji Ueda, Fumio Fukumaru and Shinji Nambu - Kyocera Corporation

Simultaneous Switching Noise Suppression Using Hydrothermal Barium Titanate Thin- Film Embedded Capacitors
Devarajan Balaraman, Vijay Patel, P. Markondeya Raj, Lixi Wan, Michael Sacks, Isaac R. Abothu, Madhavan Swaminathan and Rao Tummala - Georgia Institute of Technology

Design and Performance of Polymeric Ultra-Thin Substrates for Use as Embedded Capacitors
John Andresakis, Takuya Yamamoto and Pranbes Pramanik - Oak-Mitsui Technologies; Nicholas Biunno - Sanmina-SCI

Thin-Film Integration of Passives - Single Components, Filters, Integrated Passive Devices
Kai Zoschke, M. Jürgen Wolf, Oswin Ehrmann, Thomas Fritzsch, Katrin Scherpinski, Michael Töpper and Herbert Reichl - Fraunhofer IZM; Franz-Josef Schmückle - Ferdinand-Braun-Institut (FBH)

Design and Fabrication of an Automotive Engine Controller Using Embedded Passive Technology for PWB
John Myers and Jiming Zhou - Delphi Electronics and Safety

Wednesday, June 2
Session 8: Flip-Chip Packaging
1:30 – 5:10 PM
Committee: Advanced Packaging

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IXP2400 NPU Package Development
Andreh Janian, Altaf Hasan, Adam Barrett and Upendra Sheth - Intel Corporation

High Speed DDR Performance in 4 vs. 6 Layer FCBGA Package Design
Edward Chan, Huabo Chen and Chee Yee Chung - NVIDIA Corporation

NanoLinks: Lithography-Based Wafer-Level Compliant Chip-to-Substrate Interconnects
Suresh Sitaraman and George Lo - Georgia Institute of Technology

BGA Ball Field Interaction with Manufacturing and Design
Altaf Hasan and Daryl Sato - Intel Corporation

Gbps High-Speed Electrical Characteristics of Flip-Chip BGA Package Exceeding 2,000pin Counts
Kazuyuki Nakagawa, Masaki Watanabe, Shinji Baba and Michitaka Kimura - Renesas Technology Corp.; Keitaro Yamagishi, Yuuichi Sasaki, Tomoyuki Kamiyama and Masaaki Namatame - Mitsubishi Electric Corporation

Wednesday, June 2
Session 9: Wirebond
1:30 – 5:10 PM
Committee: Interconnections

Session Co-Chairs:
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Rajen Dias - Intel Corporation
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Manufacturability and Reliability of Different Size Wirebonds on Different Al Pad Structures
Wolfgang Sauter and Kevin Ostrowski - IBM Corporation; Toyohiro Aoki and Takashi Hisada - IBM Japan, Ltd.; Frederic Beaulieu and Stephanie Allard - IBM Canada, Ltd.

Wire Bonding on a Novel Immersion Gold-Capped Copper-Metallized Integrated Circuit
Ganesh Vetrivel Periasamy, Kripesh Vaidyanathan and Chih Hang Tung - Institute of Microelectronics; Loon Aik Lim - ASM Singapore

Assembly Process Development of 50um Fine Pitch Wire Bonded Devices
Yufeng Yao, Zhengpeng Xiong, Xin Gu and Simon Chua - Agere Systems Singapore Pte Ltd.; Tingyu Lin - Motorola Electronics Pte Ltd. Singapore

Changes in Wirebond Integrity and Reliability as Wirebond Pitch Decreases
Toyohiro Aoki and Takashi Hisada - IBM Japan, Ltd.; Wolfgang Sauter - IBM Corporation

A Study on the Reliability and Thermo-Mechanical Properties of The Gold Ribbon Wire Bonding
Chee Wei Tan and Yan Cheong Chan - City University of Hong Kong; Hong Du Liu and Bernard N.W. Leung - Photonic Manufacturing Service Ltd.

Thermosonic Wire Bonding Process Simulation and Bond Pad over Active (BPOA) Stress Analysis
Yong Liu, Scott Irving and Timwah Luk - Fairchild Semiconductor Corporation

Radio Frequency Characterization of Bonding Wire Interconnections in a Molded Chip
Jun Yi Chuang, Sung Pi Tseng and J. Andrew Yeh - National Tsing Hua University

Wednesday, June 2
Session 10: Characterization of Failure Mechanisms in Advanced Packagaing
1:30 – 5:10 PM
Committee: Quality & Reliability

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Gold Embrittlement of Solder Joints in Wafer-Level Chip Scale Package on Printed Circuit Board with Ni/Au Surface Finishing
S.W. Ricky Lee - Hong Kong University of Science and Technology; Xingjia Huang - Foxconn Inc.; Ming Li - Chinese University of Hong Kong; William Chen - ASE Technologies Inc.

Development of BGA Solution for the IBM PowerPC 970 Module in Apple's G5 System
David Edwards, Mukta Farooq and Lewis Goldmann - IBM Corporation; Hope Chambers and Amir Salehi - Apple Computer

Failure Analysis and Virtual Qualification of PBGA Under Multiple Environmental Loadings
Haiyu Qi, Chris Wilkinison, Michael Osterman and Michael Pecht - University of Maryland

Modeling Thermo-Mechanical Reliability of Bumpless Flip-Chip Package
John H. L. Pang and T. H. Low - Nanyang Technological University; Charles Lin and Andrew Yang - Bridge Semiconductor

Thermo-Mechanical Reliability of Power Flip-Chip Cooling Concepts
Bernhard Wunderle, Rainer Dudek and Michel Bernd - Fraunhofer IZM; Reichl Herbert - Technical University of Berlin

Continuous Operation at 200C Device Junction Temperature: The Final Frontier for RF Power Semiconductor Plastic Packaging
Mali Mahalingam, Dave Abdo, Frank Danaher and Alex Elliott - Motorola, Inc.

Calculation of Critical Delamination Size for Failure of the Pad/Encapsulant Interface of Plastic IC Packages Undergoing Solder Reflow
Andrew Tay - National University of Singapore; Yiyi Ma - Institute of Microelectronics; Toshio Nakamura - State University of New York, Stony Brook; Soon Huat Ong - National Semiconductor Manufacturing, Singapore

Wednesday, June 2
Session 11: Nanoscale and Emerging Technologies
1:30 – 5:10 PM
Committee: Special Topics

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Low-Cost and Repairable Nano IC-Package Interconnections by Solution Synthesis
Ankur Aggarwal, Pulugurtha Raj, Isaac Abothu, Michael Sacks and Rao Tummala - Georgia Institute of Technology; Andrew Tay - National University of Singapore

Metallic Fullerene and MWCNTs Composite Solutions for Microelectronics Subsystem Electrical Interconnection Enhancement
Randy Pike, Russell Dellmo, J. Anthony Wade, Scott Newland, Gregory Hyland and Charles M. Newton - Harris Corporation

Z-Axis Interconnects Using Fine Pitch, Nanoscale Through Silicon Vias: Process Development
Silke Spiesshoefer, Leonard Schaper, Susan Burkett, Gowtham Vangara, Parthiban Arunasalam and Ziaur Rahman - University of Arkansas

Power and Reliability Improvement of an Electro-Thermal Microactuator Using Ni-Diamond Nanocomposite
Li-Nuan Tsai - National Chiao Tung University

Study and Characterization on the Nano-Composite Underfill for Flip-Chip Applications
Yangyang Sun and C. P. Wong - Georgia Institute of Technology

Combined Process for Wafer-Direct Bonding by Means of the Surface Activation Method
Tadatomo Suga, Tae Hyun Kim and Matiar Howlader - University of Tokyo

A New Approach in Measuring Cu-EMC Adhesion Strength by AFM
Cell K. Y. Wong, Hongwei Gu, Bing Xu and Matthew M. F. Yuen - Hong Kong University of Science and Technology

Wednesday, June 2
Session 12: Materials for Embedded Passives
1:30 – 5:10 PM
Committee: Materials & Processing

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Effects of the Low-Loss Polymers on the Dielectric Behavior of Novel Aluminum-Filled High-K Nanocomposites
Jianwen Xu and C. P. Wong - Georgia Institute of Technology

Development of a Novel Polymer-Metal Nanocomposite Obtained through the Route of In-Situ Reduction and Its Dielectric Properties
Yi Li, Suresh Pothukuchi and C. P. Wong - Georgia Institute of Technology

Development of High-K Embedded Capacitors on Printed Wiring Board
Isaac Robin Abothu, Markondeya Raj Pulugurtha, Balaraman Devarajan, Swapan Bhattacharya, Michael Sacks and Rao Tummala - Georgia Institute of Technology

Development of Low-K Interlayer Dielectric Film for Embedded Passives and Actives Integral Substrates
Kazuki Uwada and Hotta Yuuji - Nitto Denko Corporation

Development of High-K Inorganic/Organic Composite Material for Embedded Capacitor
Manabu Kawasaki, Yoshitake Hara, Yuka Yamashiki, Noboru Asahi, Ryo Nagase, Takenori Ueoka and Masahiro Yoshioka - Toray Industries, Inc.

Low-Temperature Embedded Capacitor Fabrication
Albert Chee W. Lu, Boon K. Lok, Lai L. Wai and Fan Wei - Singapore Institute of Manufacturing Technology; Kim Huat Wong and Mok C. Neo - Pentex Schweizer Circuits, Ltd.

Super High Dielectric Constant Carbon Black-Filled Polymer Composites as Integral Capacitor Dielectrics
Jianwen Xu and C. P. Wong - Georgia Institute of Technology

Wednesday, June 2
Session 13: Power Delivery
1:30 – 5:10 PM
Committee: Modeling & Simulation

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Design Methodology for Multiple Domain Power Distribution Systems
Nam Pham, Moises Cases, Daniel de Araujo and Erdem Matoglu - IBM Corporation

New Methods for Power Distribution System Design and Analysis
Joel Auernheimer - Intel Corporation

The Effects of On-Chip and Package Decoupling Capacitors and an Efficient ASIC Decoupling Methodology
Nanju Na, Tim Budell, Charles Chiu, Eric Tremble and Ivan Wemple - IBM Corporation

Coupling of Simultaneous Switching Noise to Interconnecting Lines in High-Speed Systems
Jingook Kim, Jongbae Park and Joungho Kim - Korea Advanced Institute of Science and Technology; Mihai Dragos Rotaru, Kok Chin Chong and Mahadevan K. Iyer - Institute of Microelectronics

Analysis of Coupling Suppression Methods on Split Power/Ground Planes
Youchul Jeong and Joungho Kim - Korea Advanced Institute of Science and Technology; Albert Chee Wai Lu, Lai L. Wai, Wei Fan and Boon Keng Lok - Singapore Institute of Manufacturing Technology

Power Delivery System Performance Optimization of a Printed Circuit Board with Multiple Microprocessors
Om Mandhana - Motorola, Inc.; Jin Zhao - Sigrity, Inc.

Power Delivery Validation Methodology and Analysis for Network Processors
Mahadevan Suryakumar, Wei Cui, Christopher Carlson, Morgan John, Bruce Fishbein and Prashant Parmar - Intel Corporation

Thursday, June 3
Session 14: 3D Packaging
8:00 – 11:40 AM
Committee: Advanced Packaging

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Advanced Warpage Prediction Methodology for Matrix Stacked Die BGA During Assembly Processes
Xueren Zhang and Tong Yan Tee - STMicroelectronics

Process Integration of 3D Chip Stack with Vertical Interconnection
Kenji Takahashi, Yuichi Taguchi, Masataka Hoshino, Yoshihiko Nemoto, Mitsuo Ueno, Koji Marusaki, Yasuhiro Yamaji and Hiroshi Terao - Association of Super-Advanced Electronics Technologies (ASET); Toshihiro Yonezawa and Kazuo Kondo - Okayama University

System Design Issues for 3D System-in-Package (SiP)
Jani Miettinen, Matti Mäntysalo, Kimmo Kaija and Eero O. Ristolainen - Tampere University of Technology

High-Performance Vertical Interconnection for High-Density 3D Chip Stacking Package
Mitsuo Umemoto, Kazumasa Tanida, Yoshihiko Nemoto, Masataka Hoshino, Kazumi Kojima, Yuji Shirai and Kenji Takahashi - Association of Super-Advanced Electronics Technologies (ASET)

Board-Level Reliability Study on Three-Dimensional Thin Stacked Package
JinYoung Kim, WonJoon Kang, YoonHyun Ka, YongJoon Kim, EunSook Sohn, SungSu Park, JaeDong Kim and ChoonHeung Lee - Amkor Technology Korea, Inc.; Akito Yoshida and Ahmer Syed - Amkor Technology, Inc.

Ultra-Wide Bandwidth Performance of High-Density Wiring Interposer for 3D Packaging
Katsuya Kikuchi, Eun-Sil Jung, Hiroshi Nakagawa, Kazuhiko Tokoro and Masahiro Aoyagi - National Institute of Advanced Industrial Science and Technology (AIST); Shigemasa Segawa - PI Research and Development Co., Ltd.; Yoshihiko Nemoto and Mitsuo Umemot

Development and Characterisation of Ultra- Thin Autonomous Modules for Ambient System Applications Using 3D Packaging Techniques
John Barton, Kieran Delaney, Kevin Dwane, Bivragh Majeed, Ken Rodgers, Stephen Bellis and Sean C. O'Mathuna - NMRC

Thursday, June 3
Session 15: Pb-Free Flip-Chip II
8:00 – 11:40 AM
Committee: Interconnections

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Lead-Free Flip Chip Interconnect Reliability in DCA and PBGA Packages
Jong-Kai Lin, Jin-Wook Jang, Scott Hayes and Darrel Frear - Motorola, Inc.

Injection Molded Solder Technology for Pb-Free Wafer Bumping
Peter Gruber and Da-Yuan Shih - IBM Research; Luc Belanger and Guy Brouillette - IBM Canada; Valerie Oberson, Michel Turgeon and David Danovitch - IBM Canada, Ltd.; Hideo Kimura - IBM Japan, Ltd.

Pb-Free Bumping for High-Performance SoCs
Hirokazu Ezawa, Masaharu Seto and Hiroshi Katsumata - Toshiba

Evaluation of Thermal Fatigue Life and Failure Mechanisms of Sn-Ag-Cu Solder Joints with Reduced Ag Contents
Sung K. Kang, Paul Lauro and Da-Yuan Shih - IBM T. J. Watson Research Center; Donald Henderson, Timothy Gosselin, Jay Bartelo, Steve Cain, Charles Goldsmith and Karl Puttlitz - IBM Corporation; Tae-Kyung Hwang - Korea Advanced Institute of Science and Technology

Impact Reliability of Flip Chip Solder Joints
Masayoshi Date - Hitachi Metals America, Ltd.; Tatsuya Shoji, Masaru Fujiyoshi and Koji Sato - Hitachi Metals, Ltd.; King-Ning Tu - University of California, Los Angeles

Interfacial Reactions and Bump Reliability of Various Pb-Free Solder Bumps on Electroless Ni-P UBMs
Kyung-Wook Paik, Young-Doo Jeon and Moon-Gi Cho - Korea Advanced Institute of Science and Technology

Qualification of SnAg Solder Bumps for Lead-Free Flip-Chip Applications
Bernd Ebersberger, Robert Bauer and Lars Alexa - Infineon Technologies AG

Thursday, June 3
Session 16: Pb-Containing and Pb-Free Solder Joint Reliability
8:00 – 11:40 AM
Committee: Quality & Reliability

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Effect of Compression Loads on the Thermal Cycle Performance of Flip-Chip BGA Packages
Luke Garner, Keh Shin Beh, Yew Lip Tan, Charles Zhang and Chris Peterson - Intel Corporation

Board-Level Thermal Cycle Reliability and Solder Joint Fatigue Life Predictions of Multiple Stacked Die Chip Scale Package Configuration
Bret Zahn, Dianne Mitchell and Flynn Carson - ChipPAC, Inc.

Damage Mechanics of Electronics on Metal-Backed Substrates in Harsh Environments
Pradeep Lall, Nokibul Islam, Jeff Suhling, John Evans, Tushar Shete and Hecham Abdel-Hady - Auburn University

Reliability Assessment and Failure Analysis of Fine Pitch Pb-Free Flip Chip on Build-Up Laminate
T. C. Chai, Poi-Siong Teo, Navas Khan, S. F. Choy, Vanissa Lim, S. N. Priya and A. Trigg - Institute of Microelectronics

Lead-Free Solder-Joint Reliability and Failure Analysis of High-Density Packages
John Lau, Walter Dauksher and Ed Ott - Agilent Technologies, Inc.; Dongkai Shangguan - Flextronics; Joe Smetana - Alcatel; Rob Horsley - Celestica; Dave Love - Sun Microsystems, Inc.; Irn Menis - IBM Corporation; Bob Sullivan - HDPUG

Intermetallic Morphology and Attendant Damage Evolution Under Thermomechanical Fatigue of Sn-Ag-Cu Solder Interconnections
Steven Dunford, Sridhar Canumalla and Puligandla Viswanadham - Nokia Corporation

A Thermal Fatigue Life Prediction Model for SnAgCu Solder Joints
Ahmer Syed - Amkor Technology, Inc.

Thursday, June 3
Session 17: Flip-Chip Underfill
8:00 – 11:40 AM
Committee: Materials & Processing

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Four-Laser Bending Beam Measurements and FEM Modeling of Underfill Induced Wafer Warpage
Zhuqing Zhang, Lianhua Fan, Suresh S. Sitaraman and C. P. Wong - Georgia Institute of Technology

Fundamental Research on Surface Modification of Nano-Size Silica for Underfill Applications
Yangyang Sun and C. P. Wong - Georgia Institute of Technology

The Effect of Flow Properties on Filler Settling of Underfill in Flip-Chip Package
Jinlin Wang and Tim Chen - Intel Corporation

Underfill Characterization for Low-K Dielectric / Cu Interconnect IC Flip-Chip Package Reliability
Pei-Haw Tsao, Chender Huang, Mirng-Ji Lii, Bob Su and Nun-Sian Tsai - Taiwan Semiconductor Manufacturing Co., Ltd.

Investigation of Different Options of Pre-Applied CSP Underfill for Mechanical Reliability Enhancements
Nael Hannan and Arni Kujala - Nokia Corp.; Vinod Mohan, Paul Morganelli, Jayesh Shah and Doug Katze - Emerson & Cuming

Stencil Printing on Bumped Wafer for Preapplied Underfill Application
Hao Tang, Gray Shi, Larry Crane, George Carson and Michael Todd - Henkel Loctite Corporation

Void-Free Process Development and Reliability for No-Flow Underfills
Michael Colella and Daniel Baldwin - Georgia Institute of Technology

Thursday, June 3
Session 18: Optoeletronics Manufacturing Technology
8:00 – 11:40 AM
Committee: Optoelectronics

Session Co-Chairs:
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Infrared Light Induced Degradation of Polymeric Materials
John Osenbach - Agere Systems; Christopher Theis and Curt Jack - Triquint Optoelectronics

Design and Implementation of a Metallization Structure for High-Power Semiconductor Lasers for Improved Thermal Management and Reliability
Xingsheng Liu, Kechang Song, Ronald Davis, Martin Hu and Chung-En Zah - Corning, Inc.

Thermal Impedance Measurements of Junction-Down Mounted Singe-Side Contact Laser Diodes
Guy Cohen, Dan Kuchta, Bruce Furman, Joanna Rosner and Jean Trewhella - IBM Corp.; Y. Tatsuoka, S. Shira, K. Takagi, T. Aoyagi and E. Omura - Mitsubishi Electric Corporation

Fast Active Alignment in Photonics Device Packaging
Jingyan Guo and Randy Heyler - Newport Corporation

Thermally-Tuned External Cavity Laser with Micromachined Silicon Etalons: Design, Process and Reliability
Marc Finot, Mark McDonald, John Sell, Brad Bettman, Andrew Daiber, William B. Chapman and William J. Kozlovsky - Intel Corporation

Development of Super High-Density Optical Circuit Using Downsized Fibers and Flame-Retardant Fiber Tape and Multi-Fiber Optical Connector
Kenichiro Ohtsuka, Kousuke Tanaka, Shinji Ishikawa and Toshifumi Hosoya - Sumitomo Electric Industries, Ltd.

Modified Passive Alignment of Optical Fibers with Low Viscosity Epoxy Flow Running in V-Grooves
Jeffery Lo and Ricky Lee - Hong Kong University of Science and Technology

Thursday, June 3
Session 19: MEMS Packaging
8:00 – 11:40 AM
Committee: Special Topics

Session Co-Chairs:
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Wafer-Level Vacuum Packaging of MEMS Sensors
Joseph Soucy, Thomas Marinis, James Lawrence and Megan Owens - Draper Laboratory

New Wafer-Level-Packaging Technology Using Silicon-Via-Contacts for Optical and Other Sensor Applications
Jürgen Leib - SCHOTT Electronic Packaging GmbH; Michael Toepper - Fraunhofer IZM, Berlin

Novel MEMS CSP to Bridge the Gap Between Development and Manufacturing
Erik Jung and Rolf Aschenbrenner - Fraunhofer IZM; Maik Wiemer - Fraunhofer IZM, Chemnitz; Alexander Färber - ZEMI Branchlab Microsystem Engineering, Berlin

Packaging of Disposable Chips for Bioanalytical Applications
Matthias Schuenemann - Industrial Research Institute Swinburne; David Thomson, Sebastiaan Garst, Paul Miller, Matthew Solomon and Jason Hayes - CRC for Microtechnology; Micah Atkin - OzMicrofluidics & CRC for Microtechnology; Erol Harvey - MiniFab

Packaging Considerations for Microelectromechanical Microwave Switches
Samara Firebaugh - United States Naval Academy; Harry Charles, Richard Edwards and Allen Keeney - The Johns Hopkins University

Chip Scale Packaging of MEMS Accelerometers
Larry Felton, William A. Webster, Nicole Hablutzel and Kieran P. Harney - Analog Devices, Inc.

A Class of Distributed-Mass Micromachined Gyroscopes
Cenk Acar and Andrei Shkel - University of California, Irvine

Thursday, June 3
Session 20: Thermal and Thermo-Mechanical Modeling of Packaging Polymer and Low-K Dielectrics
8:00 – 11:40 AM
Committee: Modeling & Simulation

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Experimental Validation of Hygro/Thermo-Mechanical Simulations for Multi-Material Polymer Structures
Joshua Kirk, Joshua Tor, Ibrahim Guven and Erdogan Madenci - University of Arizona; Atila Mertol and Zafer Kutlu - LSI Logic Corporation

Constitutive Modeling of Moulding Compounds
Leo Ernst, Cornelis van 't Hof, Kaspar Jansen and Daoguo Yang - Delft University of Technology; Kouchi Zhang - Philips-CFT; Rik Bressers - Philips Semiconductors

Warpage Investigation of a PWB Assembly Under Thermal Loading: Modeling and Experimental Validation
Reinhard Powell, Carl Hanna and I. Charles Ume - Georgia Institute of Technology; Hai Ding - Intel Shanghai

Simultaneously Determining Young Modulus, Coefficient of Thermal Expansion, Poisson Ratio and Thickness of Multi-Layered Thin Films on Silicon Wafer
Enboa Wu and Albert J. D. Yang - National Taiwan University

FEM Study of Deformation and Stresses in Copper Wire Bonds on Cu Low-K Structures During Processing and Testing
Dominiek Degryse, Bart Vandevelde, Serguei Stoukatch and Eric Beyne - IMEC

The Effect of Material Properties and Initial Defects on the Thermo-Mechanical Behavior of a Dual-Damascene Module
Viktor Gonda and Leo Ernst - Delft University of Technology; Jaap den Toonder - Philips Research Laboratories; Johan Beijer and Kouchi Zhang - Philips Center for Industrial Technology

Thermal Modeling of an Extreme Power Density Macro on a High-Power Density Microprocessor Chip in the Presence of Realistic Packaging and Interconnect Structures
Kai Xiu - IBM Corporation; Mark Ketchen - IBM T. J. Watson Research Center

Thursday, June 3
Session 21: Special Topics: MEMS Processing and Applications
1:30 – 5:10 PM
Committee: Advanced Packaging

Session Co-Chairs:
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Wafer Bonding Using Microwave Heating of Parylene for MEMS Packaging
Hong-Seok Noh, Kyoung-Sik Moon, Andrew Cannon, Peter Hesketh and C. P. Wong - Georgia Institute of Technology

Enabling Technologies for Wafer-Level Bonding of 3D MEMS and Integrated Circuit Structures
Anna Topol, Bruce K. Furman, Kathryn W. Guarini, Leathen Shi and Guy M. Cohen - IBM Corporation

Novel Microstructuring Technology for Glass on Silicon and Glass-Substrates
Dietrich Mund and Jürgen Leib - SCHOTT Electronic Packaging GmbH

Lotus Effect Coating and Its Application for Microelectromechanical Systems Stiction Prevention
Jun Li, Jianwen Xu, Lianhua Fan and C. P. Wong - Georgia Institute of Technology

A Wafer-Level Packaging Solution for a Piezoresistive MEMS Pressure Sensor for Harsh Oceanic Environmental Conditions
Ajay Malshe and Ashwin Mohan - University of Arkansas; Shyam Aravamudhan and Shekhar Bhansali - University of South Florida

Vacuum Packaging Development and Testing for an Uncooled IR Bolometer Device
C. S. Premachandran, Choong Ser Chong, Chai Tai Chong and Mahadevan K. Iyer - Institute of Microelectronics

Location and Sensitivity Comparison of MEMS Accelerometers in Signal Identification for Ambulatory Monitoring
Teck Hong Koh, Myo Naing Nyan and Francis Eng Hock Tay - National University of Singapore; Yih Yiow Sitoh - Tan Tock Seng Hospital; Kwong Luck Tan - Institute Bioengineering & Nanotechnology

Thursday, June 3
Session 22: Bump Reliability and Electromigration
1:30 – 5:10 PM
Committees: Interconnections / Quality & Reliability

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Electromigration Reliability of SnAgxCuy Flip-Chip Interconnects
Jenq-Dah Wu and C.W. Lee - Advanced Semiconductor Engineering, Inc.

Electromigration Study of High-Lead Solders in Flip-Chip Packages by Wheatstone Bridge Method
Min Ding, Guotao Wang and Paul S. Ho - University of Texas at Austin; Hideki Matsuhashi - PDF Solutions, Inc.; Amit Marathe, Raj Master and Van Pham - Advanced Micro Devices Inc.

Electromigration in Pb-Free Solder Bumps
Glenn Rinne - Unitive Electronics

Electromigration Failure Mechanism of Sn96.5Ag3.5 Flip-Chip Solder Bumps
T. L. Shao - AU Optronics Corp.

Flip-Chip Electromigration: Impact of Test Conditions in Product Life Predictions
Haluk Balkan - Kulicke & Soffa Industries, Inc. - Flip-Chip Division

Thursday, June 3
Session 23: High-Speed and Parallel Optical Modules
1:30 – 5:10 PM
Committee: Optoelectronics

Session Co-Chairs:
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120Gb/s VCSEL-Based Parallel Optical Link and Custom 120Gb/s Testing Station
Dan Kuchta, Young Kwark, Christian Schuster, Christian Baks, Chuck Haymes, Jeremy Schaub, Petar Pepeljugoski, Lei Shan, Richard John, Daniel Kucharski, Dennis Rogers, Mark Ritter, Jack Jewell and Luke Graham - IBM T. J. Watson Research Center; Karl Schrodinger - Infineon Technologies AG; Alexander Schild and Hans-Rein - Ruhr-University Bochum

Integration of Micro-Optics with a Fiber Array Connector Using Passive Alignment Technique for Parallel Optics Applications
Hongtao Han, Jim Morris, Adam Fedor, Eden Chen, Bingzhi Su and Holly Weathersbee - Digital Optics Corporation

Parallel Optical Interconnect at 10 Gb/s per Channel
Lisa Buckman Windover, Jonathan Simon, Steven Rosenau, Kirk Giboney, Benjamin Law, Graham Flower, Laura Mirkarimi, Annette Grot, Chaokun Lin, Ashish Tandon, Glenn Rankin, Russell Gruhlke and David Dolfi - Agilent Technologies, Inc.

4 Channel x 10 Gbit/s Optical Module for CWDM Links
Takeshi Sakamoto, Nobuo Sato, Shinji Koike, Koichi Hadama and Naoya Kukutsu - NTT

Silicon Optical Bench for Robust, High-Speed Receiver Optical Subassemblies
Christian Baks, Jeremy Schaub and Fuad Doany - IBM Corporation

Transmitter Component for 10.5 Gbps at 1310 nm with Receptacle and 50 Ohm Flexboard
Oliver Stier, Daniel Reznik, Frank Meyer-Güldner, Robert Scholz, Gundolf Wenger, Nicola Iwanowski and Martin Weigert - Infineon Technologies AG

An Opto-Electronic Hybrid Integration Platform with a Polymer Optical Waveguide for High Performance and Low-Cost Modules
Takanori Shimizu, Yuji Akimoto and Kazuhiko Kurata - NEC Corporation

Thursday, June 3
Session 24: Shock and Vibration Modeling
1:30 – 5:10 PM
Committee: Modeling & Simulation

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Mechanical Shock Testing and Modeling of PC Motherboards
Brian Roggeman, Satish Chaparala and Priyank Jain - Binghamton University; Phil Geng - Intel Corporation

Vibration Fatigue Analysis for FCOB Solder Joints
John H. L. Pang, F. X. Che and T. H. Low - Nanyang Technological University

Free Drop Test Simulation for Portable IC Package by Implicit Transient Dynamics FEM
Scott Irving and Yong Liu - Fairchild Semiconductor Corporation

Ball-Grid Array Failure Envelope Development for Dynamic Loading
Ketan Shah and Michael Mello - Intel Corporation

Dynamic Materials Testing and Modeling of Solder Interconnects
Kai Chuan Ong, Vincent Tan and Chwee Teck Lim - National University of Singapore; Ee Hua Wong and Xiaowu Zhang - Institute of Microelectronics

Vibration and Thermo-Mechanical Durability Assessments in Advanced Electronic Package Interconnects
Tse Wong and Harold Fenger - Raytheon Space and Airborne Systems

Advanced Experimental and Simulation Techniques for Analysis of Dynamic Responses During Drop Impact
Tong Yan Tee and Jing-en Luan - STMicroelectronics; Eric Pek and Chwee Teck Lim - National University of Singapore; Zhaowei Zhong - Nanyang Technological University

Thursday, June 3
Session 25: Integrated Inductors
1:30 – 5:10 PM
Committee: Components & RF

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Flip-Chip Based 3D High-Q Integrated Inductors
Jing-Feng Gong and Philip Chan - Hong Kong University of Science and Technology

Fully Embedded LTCC Spiral Inductors Incorporating Air Cavity for High Q-Factor and SRF
Kichan Eun, Myungsun Song and Jaewook Lee - Electronics and Telecommunications Research Institute; Youngchul Lee and Chulsoon Park - Information and Communications University

Super Broadband Lumped Models for Embedded Passives
Chih T. Chiu, Jason T.S. Horng and Anderson H.L. Ma - National Sun Yat-sen University; Sung M. Wu and Chih P. Hing - Advanced Semiconductor Engineering, Inc.

Experiments on Embedded Planar Spiral Inductor Design Optimization for Fabrication
C. K. Liu, P. L. Cheng, S. Y. Y. Leung and D. C. C. Lam - Hong Kong University of Science and Technology

On-Wafer Inductors for SOS-Based RF IC's
Päivi Karjalainen and Eero O. Ristolainen - Tampere University of Technology

High-Q Above-IC Inductors and Transmission Lines - Comparison to Cu Back-End Performance
Geert Carchon and Walter De Raedt - IMEC; Xiao Sun - IMEC, div. MCP-MaRS

Tunable Wideband High-Absorption Bandstop Filter and Low-Absorption Phase Shifter Using Ultrathin Fe-GaAs Layer Structures
Boh-Shun Chiu, Hui-Jae Yoo and Chen S. Tsai - University of California, Irvine

Thursday, June 3
Session 26: Leading Edge Design and Manufacturing in Electronic Applications
1:30 – 5:10 PM
Committee: Manufacturing Technology

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Design and Process Optimization for Reliable Resistor Pack Solder Joints for Microprocessor Packages
S. Sidharth, Ranjit Gannamani, Charlie Zhai, Richard Blish and Raj Master - Advanced Micro Devices Inc.

Improvement of the Adhesion of New Memory Packages by Surface Engineering
Thomas Herzog, Markus Köhler and Klaus-Jürgen Wolter - Technische Universität Dresden

Development of a High-Reliability and Large Volume Manufacturing Assembly Process for a Stacked Memory Package
R. Scott Priore and Anthony Burton - Cisco Systems, Inc.

Impact of Component Technologies and Physical Design Methodologies on High-Density Wireless Products
Tom Swirbel - Motorola, Inc.

Router Flip-Chip Packaging Solution and Reliability
Eric Tosaya - Procket Networks, Inc.; Sylvain Ouimet and Robert Martel - IBM Canada Ltd.

Development and Evaluation of a High-Performance Fine Pitch SODIMM® Socket Package
Phillip Li, Jorge Martinez, Jennifer Tang, Scott Priore, Ken Hubbard and Jie Xue - Cisco Systems, Inc.; Mason Hu - Cisco; Edmund Poh, MeiLin Ong and KengYin Chok - Molex; Dave Mendez - Solectron

Integration of Sea of Leads (SoL) Chip-to-Module I/O Interconnections with an Intel Chip and Results
Muhannad Bakir, Bing Dang and James Meindl - Georgia Institute of Technology; Ric Emery and Gilroy Vandentop - Intel Corporation

Friday, June 4
Session 27: BGA/CSP Packaging
8:00 – 11:40 AM
Committee: Advanced Packaging

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Development of a New Improved High- Performance Flip-Chip BGA Package
Desmond Y. R. Chong, Beng Kuan Lim, Kenneth J. Rebibis, Shujun Pan, Krishnamoorthi Sivalingam, Rahul Kapoor, Anthony Y. S. Sun and Hien Boon Tan - United Test & Assembly Center, Ltd.

Investigation of Cu Stud Bumping for Single Chip Flip-Chip Assembly
Matthias Klein, Erik Busse, Hermann Oppermann and Karin Kaschlun - Fraunhofer IZM

Qualification and Assembly of an Enhanced BGA Package Using Build-Up Layers on Heat Spreader
Liyu Yang, Carl King and Ralph Doe - Intel Corporation

Cavity-Down Thermally-Enhanced Package Reliability Evaluation for Low-K Dielectric / Cu Interconnects ICs
Chender Huang, Pei-Haw Tsao, Allan Lin, Mirng-Ji Lii, D. J. Perng and Nun-Sian Tsai - Taiwan Semiconductor Manufacturing Co., Ltd.

Four Layer BGA Design Optimization for Improved Thermal Performance and Lower Cost
Tiao Zhou - Texas Instruments; Arianna Morelli and Claudio Villa - STMicroelectronics

High-Performance, Four-Layer, Wire-Bonded, Plastic Ball Grid Array Package for a 10 Gbps per Lane Backplane SerDes Transceiver
Don Draper, Ravi Kollipara, Ming Li and Don Mullen - Rambus, Inc.; Scott McMorrow - Teraspeed Consulting Group LLC

A Novel Joint-in-Via, Flip-Chip CSP
Teck Kheng Lee and Ah Chin Tan - Micron Semiconductor Asia Pte, Ltd.; Sam Zhang and Chee Cheong Wong - Nanyang Technological University

Friday, June 4
Session 28: Novel Interconnections
8:00 – 11:40 AM
Committee: Interconnections

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Innovative Packaging Techniques for Wearable Applications Using Flexible Silicon Fibres
Thomas Healy, Julie Donnelly, John Alderman, Brendan O'Neill, Kieran Delaney, Kevin Dwane, John Barton and Alan Mathewson - NMRC, Ireland

Improving Signal Integrity of System Packaging by Back-Drilling Plated Through Holes in Assembly Board
Sergio Camerlo, Bilal Ahmad, Yida Zou, Lekhanh Dang, Mason Hu and Scott Priore - Cisco Systems, Inc.

Integrated Module Board (IMB); An Advanced Manufacturing Technology for Embedding Active Components Inside Organic Substrate
Petteri Palm and Risto Tuominen - Imbera Electronics Oy; Antti Kivikero - Helsinki University of Technology

An Integrated Substrate Technology
Rajen Chanchani, Don Bethke, Denise Webb, Charlie Sandoval and Gregg Wouters - Sandia National Labs

Compliant Die-Package Interconnects at High Frequencies
Henning Braunisch, Kyu-Pyung Hwang and Richard D. Emery - Intel Corporation

Ultrathin Soldered Flip-Chip Interconnections on Flexible Substrates
Barbara Pahl and Thomas Loeher - Technical University of Berlin; Christine Kallmayer, Rolf Aschenbrenner and Herbert Reichl - Fraunhofer IZM

Fabrication and Parametric Study of Wafer-Level Multiple-Copper-Column Interconnect
Ebin Liao and Andrew Tay - National University of Singapore; Simon Ang - University of Arkansas; Han Hua Feng, Nagarajan Ranganathan and Kripesh Vaidyanathan - Institute of Microelectronics

Friday, June 4
Session 29: Portable Product Reliability: Drop, Vibration and Bending
8:00 – 11:40 AM
Committee: Quality & Reliability

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Effect of Thermal Aging on Board-Level Drop Reliability for Pb-Free BGA Packages
Tz-Cheng Chiu, Kejun Zeng, Roger Stierman and Darvin Edwards - Texas Instruments, Inc.; Kazuaki Ano - Texas Instruments Japan, Ltd.

Package to Board Interconnection Shear Strength (PBISS) Behavior at High Strain Rates Approaching Mechanical Drop
Murali Hanabe and Sridhar Canumalla - Nokia Corporation

Experimental and Numerical Reliability Assessment of CCGA Solder Joints Under High-Frequency Vibration
Andy Perkins and Suresh K. Sitaraman - Georgia Institute of Technology

Use-Condition-Based Cyclic Bend Test Development for Handheld Components
Lei Mercado, Joe Paul Sedillo, David Bray, Shubhada Sahasrabudhe and Eric Monroe - Intel Corp.; George Lo and Kang Joon Lee - George Technological University

Effect of Intermetallic Phases on Performance in a Mechanical Drop Environment: Sn3.5Ag Solder on Cu and Ni/Au Pad Finishes
Sambit Saha, Sesil Mathew and Sridhar Canumalla - Nokia Corporation

Models for Reliability Prediction of Fine-Pitch BGAs and CSPs in Shock and Drop-Impact
Pradeep Lall, Dhananjay Panchagade, Yueli Liu, Wayne Johnson and Jeff Suhling - Auburn University

High Drop Test Reliability: Lead-Free Solders
Yoshitaka Toyoda and Takeshi Tashima - Senjyu Industry Inc.

Friday, June 4
Session 30: Pb-Free Solders
8:00 – 11:40 AM
Committee: Materials & Processing

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Wetting Interaction Between Pb-Free Sn-Zn Series Solders and Cu, Ag Substrates
Kwang-Lung Lin and Pei-Chi Liu - National Cheng Kung University

Lead-Free Packaging and Sn-Whiskers
John Osenbach, Rick Shook, Brian Vaccaro and Brian Pottieger - Agere Systems

Aging and Creep Behavior of Sn3.9Ag0.6Cu Solder Alloy
Qiang Xiao and William D. Armstrong - University of Wyoming; Luu Nguyen - National Semiconductor Corporation

Creep and Fatigue Characterization of Lead-Free 95.5Sn-3.8Ag-0.7Cu Solder
John H. L. Pang, B. S. Xiong and T. H. Low - Nanyang Technological University

Study of Intermetallic Growth on PWBs Soldered with Sn3.0Ag0.5Cu
Mikyoung Lee, Yuchul Hwang and Michael Pecht - University of Maryland, CALCE EPSC; Jaihyun Park and Youngseop Kim - RIST; Weifeng Liu - Hewlett Packard Company

Materials Interfacial Reactions and Intermetallics Characteristics in the Formation of Micro-Joints with Sn-Pb and Pb-Free Solder Alloys
Changqing Liu, Zhiheng Huang, Paul Conway and Rachel Thomson - Loughborough University

Lead-Free TQFP Package Achieved JEDEC Level 1/260°C by Specific Combination of Die Attach Adhesive and Leadframe
Tadashi Takano, Renyi Wang, Richard Kuder, Shirley Lam and Kenji Kuriyama - Ablestik; Kazumitsu Seki, Takashi Yoshi and Ayako Saki - Shinko Electric Industries Co., Ltd.; Gordon Emmerson and Gordon Seeley - ICI Strategic Technology Group

Friday, June 4
Session 31: Emerging Optoelectronic Applications
8:00 – 11:40 AM
Committee: Optoelectronics

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Optical Data Links for Automotive Applications
Eberhard Zeeb and Thomas Kibler - DaimlerChrysler AG

780nm & 850nm VCSELs for Home Networks and Printers
Hideo Nakayama, Takeshi Nakamura and Masao Funada - Fuji Xerox Co., Ltd.; Yuichi Ohashi and Mikihiko Kato - Fuji Photo Film Co., Ltd.

Low-Cost Transceiver Components for Short Distance Optical Interconnects
Flora Ho, Mark Mak, Ben Lui, Edwin Cheung, Allan Hui, Amanda Siu, F.W. Tong, Kin Yau and Torsten Wipiejewski - ASTRI

Design and Simulation of Novel Optoelectronic Interconnect Using Photonic Crystal Virtual Waveguide with Robust Fabrication and Misalignment Tolerances
Tsuyoshi Yamashita and Christopher Summers - Georgia Institute of Technology

Micromachined Double-Side 45° Silicon Reflectors for Dual-Laser DVD Optical Pickup Head Applications
Chun-Wen Chang and Wen-Feng Hsieh - National Chiao Tung University; An-Nong Wen - Neostones Microfabrication Corporation

Development of a Novel and Cost-Effective Bi-Directional Optical Triplexer Based on a Polymer PLC Platform
Junehyeon Ahn, Youngmin Lee, Kyusub Kwak, Dongsung Shin, Sungmin Kim and Taeil Kim - Samsung Electronics Co., Ltd.

Mirror Coating and Packaging for a Horizontal MEMS Optical Switch Array
Ming Li, P. S. Chung, M. T. Yeung, P. S. Chan, T. K. Liang, C. Shu, K. W. C. Lai, W. J. Li, F. Tong and H. K. Tsang - Chinese University of Hong Kong

Friday, June 4
Session 32: Modeling, Measurement and Design Optimization
8:00 – 11:40 AM
Committee: Modeling & Simulation

Session Co-Chairs:
Steve Dvorak - University of Arizona
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Ravi Kaw - Agilent Technologies, Inc.
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Design and Analysis Methodologies of a 6.4 Gb/s Memory Interconnect System Using Conventional Packaging and Board Technologies
Wendem Beyene and Chuck Yuan - Rambus, Inc.

Design and Optimization of 3D RF Modules, Microsystems and Packages Using Electromagnetic and Statistical Tools
Nathan Bushyager, Daniela Staiculescu, Jong-Hoon Lee, Nikolaos Vasiloglou and Manos Tentzeris - Georgia Institute of Technology; Lara Martin - Motorola, Inc.

Evaluation of Frequency-Dependent Transmission Line Model Extraction Methods Based on Laboratory Measurements
Seth Syverson and David Heckmann - University of North Dakota; Trevor Timpane and Paul Dahlen - IBM Corporation

Optimization of RF/Microwave Multichip Module Performance Based on Neural Models of Passives and Interconnects
Mustapha C. E. Yagoub and Prasun Sharma - University of Ottawa

Broadband Via Transition Analysis and Characterization
Albert Chee Wai Lu, Lai L. Wai, Wei Fan and Lin Jin - Singapore Institute of Manufacturing Technology

Calibration of Near-Field Measurements Using Microstrip Line for Noise Predictions
Madhavan Swaminathan, Krishna Srinivasan and Rao Tummala - Georgia Institute of Technology; Hideki Sasaki - NEC Corporation

Electromagnetic Interference Issues for Mixed-Signal System-on-Package (SOP)
Hideki Sasaki - NEC Corp.; Vinu Govind, Krishna Srinivasan, Sidharth Dalmia, Venky Sundaram, Madhavan Swaminathan and Rao Tummala - Georgia Institute of Technology

Friday, June 4
Session 33: Manufacturing Advances for Next Generation Technologies
8:00 – 11:40 AM
Committee: Manufacturing Technology

Session Co-Chairs:
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High Reliability Second-Level Interconnects Using Polymer Core BGAs
Sashidhar Movva - Kyocera America, Inc.

Effect of Organic Package Core Via Pitch Reduction on Power Distribution Performance
Jean Audet - IBM Canada Ltd.; Michael Grinberg, Daniel O'Connor and Jim Libous - IBM Corporation

Process and Design Analysis of Ultra Fine-Pitched Wiresweep Elimination for Advanced Copper Heat Spreader BGA Package
Surasit Chungpaiboonpatatana - Conexant (Mindspeed) Corporation; Frank Shi - University of California, Irvine

High-Frequency Thermosonic Flip-Chip Bonding for Gold to Gold Interconnection
Charles C. H. Pang and Kin-Yik Hung - ASM Assembly Automation Ltd.; Man-Lung Sham - Hong Kong University of Science and Technology

Comparison of Via-Fabrication Techniques for Through-Wafer Electrical Interconnect Applications
Alexander Polyakov, Ines Eidner, Marian Bartek and Joachim N. Burghartz - Delft University of Technology; Timon Grob, Ron A. Hovenkamp, Henk J. Kettelarij and Marc A. de Samber - Philips CFT Eindhoven

Innovative Solutions to Enable Smaller Substrate Bump Pad Size for Flip-Chip Technology
Seaw Lai Cheah, Chee Koang Chen, Kuljeet Singh, Toon Yoon Ang, C. C. Loke, Mun Lin Lai and Anita Earley - Intel Corporation

A High Throughput Optoelectronic Module Assembly Process
Paul Schwab, Terry Bowen, Richard Perko and Nuri Delen - Tyco Electronics, Inc.; Richard Anderson and Joel Goodrich - MACOM Inc.

Friday, June 4
Session 34: Wafer-Level Packaging
1:30 – 5:10 PM
Committee: Advanced Packaging

Session Co-Chairs:
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Yee L. Low - Lucent Technologies Bell Labs
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Constrained Collapse Solder Joint Formation for Wafer Level-Chip Scale Packages to Achieve Reliability Improvement
Viraj Patwardhan, Hau Nguyen, Nikhil Kelkar and Li Zhang - National Semiconductor Corporation

A Low-Temperature Wafer-Level Hermetic Package Using UV Curable Adhesive
Zhi-Hao Liang, Yu-Ting Cheng and Wensyang Hsu - National Chiao Tung University; Yuh-Wen Lee - Industrial Technology Research Institute

Low-Cost, Wafer Level Underfilling and Reliability Testing of Flip-Chip Devices
Alan Grieve, M. Albert Capote, Howard A. Lenos and Arsenia Soriano - Aguila Technologies, Inc.

Reaching Détente in the Design and Material Selection for Hi Rel WL-CSPs
Glenn Rinne - Unitive Electronics; Craig Schuckert - HD MicroSystems

Effect of Wafer-Level Packaging, Silicon Substrate and Board Material on Gigabit Board-Silicon-Board Data Transmission
Madhavan Swaminathan, R. Madhavan, J. Mao, D. Ravi, Z. Zhang, George Lo and C. P. Wong - Georgia Institute of Technology; S. Sitaraman, M. Iyer and M. Rotaru - Institute of Microelectronics; A. Tay - National University of Singapore

Wafer-Level Interconnects for 3D Packaging
Riki Banerjee and Rhonda Drayton - University of Minnesota

Circuit Partitioning and RF Isolation by Through-Substrate Trenches
Saoer M. Sinaga, Alexander Polyakov, Marian Bartek and Joachim N. Burghartz - Delft University of Technology

Friday, June 4
Session 35: Board-Level and Embedded Optical Interconnects
1:30 – 5:10 PM
Committees: Optoelectronics / Interconnections

Session Co-Chairs:
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Embedded Optical Interconnections in Printed Wiring Boards
Takeshi Suzuki - Matsushita Electric Industrial Co., Ltd.; Toshihisa Nonaka - Toray Industries, Inc.; Nobuyuki Ogawa - Hitachi Chemical Co., Ltd.; Sang-Yeon Cho and Sang-Woo Seo - Georgia Institute of Technology; Nan Marie Jokerst - Duke University,

Optical Path Redirected Three-Dimensional Lightguide Connectors for High-Speed Interconnection Modules
Seiki Hiramatsu, Masao Kinoshita, Takashi Mikawa and Osamu Ibaragi - Association of Super-Advanced Electronics Technologies (ASET); Hidetoshi Nanai - Central Glass Co., Ltd.; Takumi Yoshida and Shuji Suzuki - Hirose Electric Co., Ltd.

Heterogeneous Integration of InP/InGaAsP MQW Thin Film Edge Emitting Lasers and Polymer Waveguides
Hung-Fei Kuo, Sang-Yeon Cho and Nan Jokerst - Georgia Institute of Technology

Optical Interconnects on Printed Circuit Board Level - Results Based on the German Funded Project OPTICON
Martin Franke and Frank-Peter Schiefelbein - Siemens AG

High-Efficiency Optical Interconnection Using 45 Degree-Ended Connection Blocks in Fiber- and Waveguide-Embedded PCBs
Byung Sup Rho, Mu Hee Cho, Han Seo Cho and Hyo-Hoon Park - Information and Communications University; Kyoung-Up Shin, Sang-Won Ha and Byoung-Ho Rhee - Samsung Electro-Mechanics Co.; Dong-Su Kim, Sun Tea Jung and Taeil Kim - Samsung Electronics Ltd.

Demonstration of an MT-Compatible Connectorisation of a Laser-Ablated Optical Interconnection on a Printed Circuit Board
Geert Van Steenberge, Peter GeerInc.k, Steven Van Put and Peter Van Daele - Ghent University; Jan Van Koetsem and Danny Morlion - FCI 's-Hertogenbosch

1K-Channel Optical Interconnects of CMOS-PQR Flip-Chip
O'Dae Kwon, Sangkyeom Kim, Moojin Kim, Seungeun Lee, Dongkwon Kim and Junho Yoon - Pohang University of Science and Technology; Kwonsub Lim, Jungyeon Kim and Byunghun Park - Samsung Electronics Co., Ltd.

Friday, June 4
Session 36: Thermo-Mechanical Modeling of Package and Interconnect
1:30 – 5:10 PM
Committee: Modeling & Simulation

Session Co-Chairs:
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Isothermal Fatigue Test of Wafer-Level Chip Scale Package (WLCSP) and Plastic Ball Grid Array (PBGA) Lead-Free Solder Joints on Printed Circuit Board (PCB) with Immersion Silver (ImAg) Surface Finish
John Lau - Agilent Technologies, Inc.; Ricky Lee - Hong Kong University of Science and Technology; Dongkai Shangguan - Flextronics

Leading Indicators of Failure for Prognosis of Electronic and MEMS Packaging
Pradeep Lall, Nokibul Islam, Kaysar Rahim and Jeff Suhling - Auburn University

Accelerated Thermal Cycling: Is It Different for Pb-Free Solder?
Krishna Tunga, Karan Kacker, Raghuram Pucha and Suresh Sitaraman - Georgia Institute of Technology

Fatigue Life Estimation of an Ultra-Fine-Pitch Solder Column Wafer Level Package Using the Macro-Micro Modeling Approach
Audrey Chng, Andrew Tay and Kian Meng Lim - National University of Singapore; Ee Hua Wong - Institute of Microelectronics

Influence of Interfacial Compliance on Thermomechanical Stresses in Multilayered Microelectronics Packaging
Yujun Wen and Cemal Basaran - State University of New York, Buffalo

Applied FEM Techniques in Ceramic Feedthru Package Design
Mark Eblen - Kyocera America, Inc.

Stacked-Chip Packaging: Electrical, Mechanical, and Thermal Challenges
J. J. Maloney, Richard S. Graf, Hanyi Ding, Elie Awad and Geoff Simson - IBM Corporation

Thursday, June 3

Session 37: Substrates and Bumps

1:30 – 5:10 PM

Committee: Materials & Processing

Session Co-Chairs:
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Integrated RF Module Produced by Aerosol Deposition Method
Yoshihiko Imanaka - Fujitsu Laboratories, Ltd.; Jun Akedo - National Institute of Advanced Industrial Science and Technology (AIST)

A Novel Highly Heat Resistant Substrate Material for Halogen-Free Applications
Kenji Shima, Kousuke Hirota, Koutarou Asahina and Takashi Iiyama - Mitsui Chemicals, Inc.

Materials, Process and Reliability of Mixed Signal Microvia Substrates for SOP Technology
Raghuram Pucha, Saketh Mahalingam, Suresh Sitaraman, Venky Sundaram, Fuhan Liu, White George and Rao Tummala - Georgia Institute of Technology

Flip-Chip Bump Integrity with Copper/Ultra Low-K Dielectrics
Vaidyanathan Kripesh, Hong Yu Li, Chao Yong Li, Yong Ji Jeffrey Su and Mahadevan K. Iyer - Institute of Microelectronics

Fluxless Flip-Chip Technique with Electroplated Sn/Au Bumps
Dongwook Kim, Jongsung Kim and Chin C. Lee - University of California, Irvine

Characterization of Nanocrystalline Copper and Nickel for Nanointerconnect Applications
Shubhra Bansal, Ashok Saxena and Rao Tummala - Georgia Institute of Technology

Effect of Substrate Material and Solder Ball Pitch on Reliability
Subhotosh Khan - DuPont - AFS; Mohamed Asaduzzaman, Mark Lamontia and Jay Sloan - DuPont - DuET

Friday, June 4

Session 38: RF Modules

1:30 – 5:10 PM

Committee: Components & RF

Session Co-Chairs:
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Multi-Band RF and mm-Wave Design Solutions for Integrated RF Functions in Liquid Crystal Polymer System-On-Package Technology
Valeria Palazzari - Universita' di Perugia; Dane Thompson, Nikko Papageorgiou, Stephane Pinel, Jong-Hoon Lee, Saikat Sarkar, Rana Pratap, Gerald De Jean, Ramanan Bairavasubramanian, Rong-Lin Li and Manos Tentzeris - Georgia Institute of Technology

A Multiple Frequency Signal Generator for 802.11a/b/g VoWLAN Type Applications Using Organic Packaging Technology
Sidharth Dalmia, Amit Bavisi, Souvik Mukherjee, Vinu Govind, George White, Madhavan Swaminathan and Venkatesh Sundaram - Georgia Institute of Technology

Characterization of Transfer Molding Effects on RF Performance of Power Amplifier Module
Li Li, Anju Kapur and Ken Brice Heames - Motorola, Inc.

Design Consideration for System-in-a-Package with Embedded Passive Circuits
Gye-An Lee and Franco De Flaviis - University of California, Irvine; Mohamed Megahed - Skyworks Solution, Inc.

System-on-Package Based CMOS Voltage Controlled Oscillator
Tae-Je Cho and Se-Yong Oh - Samsung Electronics Co., Ltd.; Sang-Woong Yoon, Kyutae Lim, Stephane Pinel, Joy Laskar, Swapan Batthacharya and Rao Tummala - Georgia Institute of Technology

Chip-Package Co-Design of a Concurrent LNA in System-on-Package for Multi-Band Radio Applications
Tommi Torikka and Esa Tjukanoff - University of Turku; Xinzhong Duo, Li-Rong Zheng and Hannu Tenhunen - Royal Institute of Technology

System-on-a-Package (SOP) Module Development for a Digital, RF and Optical Mixed-Signal Integrated System
Kyutae Lim, Lixi Wan, Daniel Guidotti, Stephane Pinel, Venkatesh Sundaram, George White, Fuhan Liu, Swapan Bhattacharya, Ravi Doraiswami, Manos Tentzeris, Joy Laskar and Rao Tummala - Georgia Institute of Technology

Friday, June 4

Session 39: Educational Initiatives for the 21st Century

1:30 – 5:10 PM

Committee: Education

Session Co-Chairs:
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Leyla Conrad - Georgia Institute of Technology
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Electronics Packaging; A Course for the Rutgers University
Michael Caggiano and Ka-Mun Ho - Rutgers University

Undergraduate Students' Research Activities
Paul Svasta, Virgil Golumbeanu, Ciprian Ionescu, Daniel Victoras Ene, Rocsana Ionescu and Diana Sinzeana Chirileasa - Politehnica University of Bucharest

Development of a Curriculum in Nano and MEMS Packaging and
Ajay P. Malshe - University of Arkansas

Research and Education in MEMS and Optoelectronics Packaging in
Sheng Liu - Wayne State University; Sheng Liu - Huazhong University of Science and Technology

Multi-Level Education Curriculum of Electronics Manufacturing Engineering in GUET
D. G. Yang, Ling Sun and Xiaosong Ma - Guilin University of Electronic Technology

Process Technology of Electronics - A Graduate Textbook
Thomas Zerna, Martin Oppermann, Wilfried Sauer and Klaus-Juergen Wolter - Dresden University of Technology

Distance Learning - How to Use this New Didactic Method in Education of Electronics Engineering
Zsolt Illyefalvi-Vitez and Peter Gordon - Budapest University of Technology and Economics

Wednesday, June 2 and Thursday, June 3

Posters

Committee: Posters

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Active Devices and Wiring Under Chip Bondpads: Stress Simulations and Modeling Methodology
Elie Awad - IBM Corporation

Reliability of Large Organic Flip-Chip Packages for Industrial Temperature Environments
Anurag Bansal and Yuan Li - Altera Corporation

A Thermodynamic Model for Electrical Current Induced Damage in Microelectronics Solder Joints
Cemal Basaran - State University of New York, Buffalo

Development of a Fully Automated Low-Cost High-Throughput Menis Coating Method for Large Format SOP Substrates
Swapan Bhattacharya, Sachin Bhatevara, Gary May and Rao Tummala - Georgia Institute of Technology

Broadband Electrical Characterization of a Flip-Chip Interconnect
Andrew Byers and Laudie Doubrava - Tektronix

High-Frequency Characterization of Differential Signals in Flip-Chip Organic Package
Charles Chiu and Hanyi Ding - IBM Corporation

Study of Assembly Processes for Liquid Crystal on Silicon (LCoS) Microdisplays
Anupam Choubey, Bahgat Sammakia and Frank Andros - State University of New York, Binghamton

Simulation Study of Power Delivery Performance on Flip-Chip Substrate Technologies
Musawir Chowdhury - Agere Systems; Jin Zhao and Raymond Chen - Sigrity, Inc.

Liquid Crystalline Polymer Based RF/Wireless Components for Multi-Band Applications
Sidharth Dalmia, Venkatesh Sundaram, George White and Madhavan Swaminathan - Georgia Institute of Technology

Co-Design Optimization of Laminate Substrates for High Speed Applications
Daniel de Araujo, Moises Cases, Nam Pham and Erdem Matoglu - IBM Corporation

Impediments to Impedance & Coupled Noise
Matt Doyle - IBM Corporation

LTCC and Thick-Film Microresistors
Andrzej Dziedzic and Edward Mis - University of Technology, Wroclaw; Lars Rebenklau and Klaus-Jurgen Wolter - Dresden University of Technology

The Challenge of Ultra-Thin Chip Assembly
Michael Feil, Cliff Adler and Dieter Hemmetzberger - Fraunhofer IZM; Martin König and Karlheinz Bock - Fraunhofer IZM, Munich

Moisture and Temperature Effects on the Reliability of Interfacial Adhesion of a Polymer/Metal Interface
Timothy Ferguson and Jianmin Qu - Georgia Institute of Technology

Design of Multiband Baluns on Liquid Crystalline Polymer (LCP) Based Substrates
Vinu Govind, Sidharth Dalmia, Venky Sundaram and Madhavan Swaminathan - Georgia Institute of Technology; George White - Jacket Micro Devices, Inc.

Test Vehicle to Characterize Silicon to Organic Flip-Chip Package Thermomechanical Failures
Dongming He, Sriram Srinivasan, Sairam Agraharam, Biju Chandran, Mike Mello, Pankaj Sinha and Vasu Atluri - Intel Corporation

Design, Fabrication, and Reliability Testing of Embedded Optical Interconnects on Board
Shashikant Hegde, Suresh Sitaraman, Raghuram Pucha, Daniel Guidotti, Fuhan Liu and Rao Tummala - Georgia Institute of Technology

A Novel Fiber Alignment Shift Measurement Technique Employing an Ultra-High Precision Laser Displacement Meter in Laser-Welded Laser Module Packaging
Yi-Cheng Hsu, Yeh-Lin Ho, Ying-Chien Tsai, Jao-Hwa Kuang and Wood-Hi Cheng - National Sun Yat-sen University; Maw-Tyan Sheen - Yung Ta Institute of Technology and Commerce

A Comparison Study between Eutectic Au-Si and Au-Sn Solders as Die Attach Materials for High Power Devices
Jin-Wook Jang, Scott Hayes, Jong-Kai Lin and Darrel Frear - Motorola, SPS

Computer-Aided Thermal, Mechanical and Optical Simulation for Parallel Optical Subassembly Design
Chih-Ting Kao, Chih-Hsiang Ko, Shu-Jung Yang, Chun-Hsun Tsai, Yii-Tay Chu and Rex Chiou - Industrial Technology Research Institute

Measurement of Deformation and Strain in Flip-Chip on BGA (FC-BGA)
Liam Kehoe, VIncent Guénebaut and Patrice Kelly - Optical Metrology Innovations, Ltd.

Sensitivity Analysis of On-Chip Delta-I Noise Calculation
Bernd Kemmler and Andreas Huber - IBM Deutschland Entwicklung GmbH

Electrical Characteristics of Fine-Pitch Flip-Chip Solder Joints Fabricated Using Low-Temperature Solders
Young-Ho Kim and Un-Byoung Kang - Hanyang University

C-SiC Package /Board Materials Technology for Next Generation Convergent Micro Systems
Nitesh Kumbhat, P. Markondeya Raj, Raghuram Pucha, Shashikant Hegde, Ravi Doraiswami, Swapan Bhattacharya, Suresh Sitaraman and Rao Tummala - Georgia Institute of Technology; Steve Atmur and Susan Hayes - Starfire Systems

The Effect of Tg on Thermo-Mechanical Deformation and Reliability of Adhesive Flip-Chip Assemblies During Temperature Cycling
Woon-Seong Kwon, Se-Young Yang, Soon-Bok Lee and Kyung-Wook Paik - Korea Advanced Institute of Science and Technology

The Solder Joint Characterization in Green WLCSP
Jeffrey C. B. Lee - ASE Corp.; S.W Li - Advanced Semiconductor Engineering, Inc.

Chip-on-Chip 3D Optical Interconnect with Passive Alignment
Ricky Lee and Jeffery Lo - Hong Kong University of Science and Technology

Modeling of Embedded Inductor on Low-Cost Multilayer Laminate MCM Technology and Its Application
Ryan Lee, Jeremy Goodrich and Anil Agarwal - Skyworks Solutions, Inc.

High Manufacturability and Thermal Stability Mini-Flat Transmitter for 10Gb/s Ethernet Applications
Shin-Ge Lee, Chih-Li Chen, Chu-Li Chao, Chun-Hsing Lee, Li-Chun Liao, Chih-Hao Hsu, Fu-Yi Cheng, Cheng-Hung Tsai, Min-Fa Huang and Chiung-Hung Wang - Industrial Technology Research Institute

Photolithography of 3D Topology in Si Optical Bench for Self-Aligned Placement of Laser Dies
Ming Li, H. K. Tsang and C. Shu - Chinese University of Hong Kong; C. W. Law, Y. K. Lau and R. W. M. Kwok - Shipley Asia, Ltd.; X. W. Hu and H. L. Zhu - Institute of Semiconductors

Electrical Property of Anisotropically Conductive Adhesives Joint Modified by Self-Assembled Monolayer
Yi Li, Kyoung-Sik Moon and C. P. Wong - Georgia Institute of Technology

Conductivity Improvement of Isotropic Conductive Adhesives with Short-Chain Dicarboxylic Acids
Yi Li, Kyoung-sik Moon, Haiying Li and C. P. Wong - Georgia Institute of Technology

ShapeTControlled Synthesis of Nanoparticles and Their Incorporation into Polymers
Yi Li, Suresh Pothukuchi and C. P. Wong - Georgia Institute of Technology

Polymeric Waveguides on Rigid and Flexible PCB
Wei-Chung Lo, Li-Cheng Shen, Hsiang-Hung Chang, Huan-Chun Fu, Yu-Chih Chen, Shu-Ming Chang, Yuan-Chang Lee, Wun-Yan Chen and Ming-Chieh Chou - Industrial Technology Research Institute

Optimizing the Output Impedance of a Power Delivery Network for Microprocessor Systems
Om Mandhana - Motorola, Inc.

Wafer-Level Integration of On-Chip Antennas and RF Passives
Paulo Mendes - University of Minho / Delft University of Technology; Saoer Sinaga, Alexander Polyakov, Marian Bartek and Joachim Burghartz - Delft University of Technology; Higino Correia - University of Minho

Nano-Metal Particles for Low-Temperature Interconnect Technology
Kyoung-Sik Moon, Hai Dong, Yi Li, Suresh Pothukuchi and C. P. Wong - Georgia Institute of Technology

Lead-Free Solder Interconnect by Variable Frequency Microwave (VFM)
Kyoung-Sik Moon, Yi Li, Jianwen Xu and C. P. Wong - Georgia Institute of Technology

High Thermal Dissipation Transfer Molded Package for Power Modules
Dai Nakajima, Kazuhiro Tada and Yoshihiro Kashiba - Mitsubishi Electric Corporation; Taishi Sasaki and Takeshi Shikano - Fukuryo Semicon Engineering Corporation Japan

Heat Spreader Impact on Electrical Performances of a 4-Layer PBGA Package
Shujun Pan and Anthony Sun Y.S. - United Test & Assembly Center, Ltd.

An Accurate Electromagnetic Modeling of the Die-to-Die Interconnect Link for Gigabit Systems Applications
Victor Prokofiev, Udy Shrivastava, Lesley Polka and Michael Hill - Intel Corporation

High Aspect Ratio Metal-Polymer Composite MEMS Structures for Tunable Capacitors and Wafer-Level Nano Interconnects
P. Markondeya Raj, Ankur Aggarwal, Kianoush Naeli, Farrokh Ayazi, Swapan Bhattacharya and Rao Tummala - Georgia Institute of Technology

Electromagnetic Noise Mitigation in High-Speed Printed Circuit Boards and Packages Using Electromagnetic Band Gap Structures
Shahrooz Shahparnia, Baharak Mohajeriravani and Omar Ramahi - University of Maryland

LCP Injection Molded Packages-Keys to JEDEC I Performance
Richard Ross - RJR Polymers, Inc.

Modeling and Hardware Correlation of Power Distribution Networks for Multi-Gigabit Designs
Ralf Schmitt, Xuejue Huang, Ling Yang and Chuck Yuan - Rambus, Inc.

FR4 Printed Circuit Board Design for Gigabits Embedded Optical Interconnect Applications
Jaemin Shin, Cheolung Cha, Sang-Yeon Cho and Jaehong Kim - Georgia Institute of Technology; Nan Marie Jokerst and Martin Brooke - Duke University

RF Modeling and Design of Flip-Chip Configurations of Microwave Devices on PCBs
Young Song - University of California, Irvine

Ultrathin Patterned Graphite Nanoelectronics
Zhimin Song, Clair Berger and Walt De Heer - Georgia Institute of Technology

Package-Level Performance Analysis Based on Laser Diode Far Field Distribution
Yakov Soskind, Jeff Perkins and Jack Tomlinson - JDS Uniphase Corporation

A Micromechanics Model for Electrical Conduction in Isotropically Conductive Adhesives During Curing
Bin Su and Jianmin Qu - Georgia Institute of Technology

Process Characterization and Issues in LTCC Assembly
Vasudivan Sunappan, Arulvanan Periannan and Chua Kai Meng - Singapore Institute of Manufacturing Technology

Components' Emisivity Influence in Reflow Soldering Process
Paul Svasta, Daniel Simion-Zanescu and Rocsana Ionescu - Politehnica University of Bucharest; Gabriel Popovici - Micronix Plus

A Leadless Packaging Concept for High-Frequency Applications
Horst Theuss, Jochen Dangelmaier, Mario Engl, Klaus Pressel, Werner Simbürger, Herbert Knapp, Klaus Gnannt, Wolfram Eurskens and Josef Hirtreiter - Infineon Technologies AG

Effect of Spin Coating on the Adhesion of Epoxy Adhesive on Si Substrate for the Fabrication of Polymer Optical Waveguide
M. A. Uddin, H. P. Chan and C. K. Chow - City University of Hong Kong

Time Domain Analysis of the Signal Integrity of a 1Gbps 4-Module Memory Bus with a Broadband Ceramic Directional Coupler Designed in the Frequency Domain.
Yutaka Uematsu, Hideki Osaka, Hiroaki Ikeda and Yasunori Sakisaka - Hitachi

Parametric Study of Warpage of PWB Assemblies and PWB Assembly Warpage Minimization by Component Layout Optimization
I. Charles Ume - Georgia Institute of Technology; Hai Ding - Intel Corporation

Embedded Passives Technology for Bluetooth Application in Multi-Layer Printed Wiring Board
Ching-Liang Weng - Industrial Technology Research Institute; Pel-Shen Wei, Chun-Kun Wu, Chang-Sheng Chen, Uei-Ming Jow and Ying-Jiunn Lai - ERSO,ITRI; Shur-Fen Liu - Materials Research Laboratories,ITRI

Packaging of Thermally Tunable Fiber Bragg Grating Sensor
Ling Xie, D. Pinjala, K. Sudharsanam, Ramana Pamidighantam and Navas Khan - Institute of Microelectronics; Jingbo Zhang, Wanxun He and Baoxi Xu - Data Storage Institute

High Coupling Tapered Hyperbolic Fiber Microlens
Huei-Min Yang, Sun-Yuan Huang, Chao-Wei Lee and Shih-Hung Wang - National Sun Yat-sen University

A Novel Silica Planar Waveguide Structure with High Thermal Efficiency
Enchao Yu and Dawei Zheng - Consultant

Process Considerations and Long Term Thermal Performance of Power Packages with Heat Slug Soldered to PCB
Tiao Zhou - Texas Instruments; Mike Hundt - STMicroelectronics

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Will Arrive: Day _____Date _____Time_____AM/PM
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Special Room Rates

(Based upon availability at check-in)

____ Non-smoking
____ Smoking
____ Other

____ One Bed (King)

Two Beds
____ Run of House (DBL)
____ Palace Tower (QN)

Check-In Time is after 3:00 PM • Check-Out Time is 12:00 PM daily

Name: _____ Share With: _____
Last First Last First

Home Address: _____

City: _____ State: _____ Zip _____

Company Name: _____ Company Address: _____

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Note: Reservations will not be held after 14 days without a deposit. Credit card numbers are taken as a guarantee and will be charged upon receipt. Reservations must be cancelled three (3) days or 72 hours prior to arrival to avoid forfeiture of deposit. Group rates, rooms and dates are subject to availability. Enclosed is my one night's deposit payable by:
(Please check one) _____ Check _____ Credit Card (If you are guaranteeing your deposit with a credit card, please complete the following)

_____ Discover _____ American Express _____ Diner's Club _____ Carte Blanche _____ Visa _____ MC _____

Credit Card Number: _____ Exp. Date _____

Print name as it appears on card: _____ Signature: _____

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How To Register

By Internet: Submit your registration electronically via www.ectc.net/reg.htm. Your registration must be received by the cutoff date, **May 15, 2004**, to qualify for the early registration discounts.

By Mail: Return your completed registration form to EIA/ECA, 2500 Wilson Boulevard, Arlington,VA 22201-3834 with payment by company check, money order or credit card. Your registration must be received by the cutoff date to qualify for the early registration discounts.

By Fax: Fax your completed registration form with credit card payment to (703) 875-8908. Your fax must be received by the cutoff date to qualify for the early registration discounts.

54th Electronic Components & Technology Conference

Advance Registration Form

Send your advance registration to EIA/ECA, 2500 Wilson Boulevard, Arlington, VA 22201-3834, or fax (credit card only) to (703) 875-8908 to be received no later than May 15, 2004. You may call (703) 907-8027 for additional information.

On-line registration is available at www.ectc.net/reg.htm

Last Name _____ Badge First Name _____ First Name _____ Title _____

Company _____ Mail Stop _____

Address _____ City _____ State/Country _____ Zip _____

Telephone _____ Fax # _____ Email _____

ECTC Advance Registration

Check one or more of the following:
Registration includes printed proceedings or CD-ROM (see below) and lunch each day:

- ☐ IEEE Member * No. _____ $500
- ☐ Non-Member* $600
- ☐ One Day (Circle W T F) $375
- ☐ Speaker/Session Chair* Session#_____ $400
- ☐ Speaker/One Day $250
- ☐ Student Speaker Session #_____ $150
- ☐ Student (receives CD) $150

** Door Registration will be an additional $100*

As part of my registration fee, I request:

- ☐ the printed proceedings or
- ☐ the CD-ROM or
- ☐ both ($50.00 additional fee)

If a selection is not made, you will receive a CD.

ECTC/ITHERM Joint Registration

☐ Joint ECTC/ITHERM Advance $750
(Joint Door Registration $800; includes both luncheons and proceedings.)

PRIMARY AREA OF INTEREST (Check One)

___Advanced Packaging	___Interconnections	___Modeling & Simulation
___Components & RF	___Manufacturing Technology	___Optoelectronics
___Connectors & Contacts	___Materials & Processing	___Quality & Reliability

Professional Development Course Registration

- ☐ Single AM or PM PDC includes luncheon *$350
- ☐ AM & PM PDC includes luncheon *$550
- ☐ Student (AM and/or PM PDC) includes luncheon $75

Check course(s) you plan to attend (Pages 8-13)

AM Courses 1___ 2___ 3___ 4___ 5___ 6___ 7___ 8___

PM Courses 9___ 10___ 11___ 12___ 13___ 14___ 15___ 16___

***Door rate will be an additional $50.**

**** See hours of registration on Advance Registration page 3.**

IMPORTANT TO REGISTER IN ADVANCE TO AVOID DELAYS AT REGISTRATION DESK. COURSE SIZES LIMITED.

Printed Proceedings & CD-ROM Only

- ☐ U.S. postpaid $300
- ☐ Foreign via air mail $350

☐ NEMI Tin Whisker Workshop $75

Extra Luncheon Tickets

#_____ Wed. $38 each
#_____ Thur. $38 each

Please indicate how many luncheon tickets are needed.

☐ Coffee Break Sponsor $350

Credit Card and Payment Information

Please make all checks for Advance Registration payable to the ***54th ECTC***. Mail your check together with this form to EIA/ECA, 2500 Wilson Blvd., Arlington, VA 22201-3834. There will be no refunds on cancellations after May 15, 2004. Substitutions can be made at any time. DO NOT MAIL CHECKS AND REGISTRATIONS TO ANY OTHER ADDRESS. You may fax this form and your credit card information to: (703) 875-8908.

Name on Card _____ Credit Card # _____

Signature _____ Exp. Date _____ ☐ MC ☐ Visa ☐ AMX

Join IEEE and the Components, Packaging and Manufacturing Technology Society and Save!

- Non-IEEE members can join IEEE and save $100 on ECTC registration and receive CPMT Society membership free for 2004.
- IEEE members can join the CPMT Society free for the remainder of 2004 with ECTC registration.

A membership application must be completed to obtain an IEEE member number before sending registration form to EIA. For details contact Marsha Tickman, IEEE CPMT Society, phone 732-562-5529, fax 732-981-1769, email: m.tickman@ieee.org or visit the CPMT booth in the ECTC Registration area if registering at the door.

Conference Overview

June 1, 2004
Morning Professional Development Courses
8:15 AM - 12:00 PM

1. Optoelectronics Components and Modules for Communication Networks
2. Advanced Organic Substrate Package Design & Manufacturing for RF and Broadband
3. Integrated Passive Technology and Commercialization
4. Polymers for Electronic Packaging
5. System-On-Package (SOP) vs. System-In-Package (SIP), and System-On-Chip (SOC)
6. "Nano" - The Next Technology?
7. Microelectronic and MEMS Sensors
8. Microelectronics Packaging and Interconnection - A Worldwide Perspective

June 1, 2004
Afternoon Professional Development Courses
1:15 - 5:00 PM

9. RF/Wireless Packaging
10. Wafer Level - Chip Scale Packaging
11. Microvias & High-Density Interconnects for Advanced Packaging
12. Interconnect and Packaging Technologies for 10 and 40GBPS Telecom and Datacom
13. Package Failure Analysis - Failure Mechanisms and Analytical Tools
14. Advanced Thermal Management Materials
15. Introduction to Nanoscale Packaging and Systems
16. Lead-Free Solders for Robust IC Electronic and Optoelectronic Packaging

June 1, 2004
NEMI Tin Whisker Workshop
8:15 AM - 5:00 PM

June 2, 2004
Technical Sessions
8:00 - 11:40 AM

S1 SIP/SOP
S2 Pb-Free Flip-Chip
S3 Innovative Testing Methods
S4 Adhesives and Encapsulants
S5 Optoelectronic Packaging Technology
S6 Electrical Modeling
S7 Integrated Capacitor and Resistor Technology

June 2, 2004
1:30 - 5:10 PM

S8 Flip-Chip Packaging
S9 Wirebond
S10 Characterization of Failure Mechanisms in Advanced Packaging
S11 Nanoscale and Emerging Technologies
S12 Materials for Embedded Passives
S13 Power Delivery

June 3, 2004
8:00 - 11:40 AM

S14 3D Packaging
S15 Pb-Free Flip-Chip II
S16 Pb-Containing and Ob-Free Solder Joint Reliability
S17 Flip-Chip Underfill
S18 Optoelectronics Manufacturing Technology
S19 MEMS Packaging
S20 Thermal and Thermo-Mechanical Modeling of Packaging Polmer and Low-K Dielectrics

June 3, 2004
1:30 - 5:10 PM

S21 Special Topics: MEMS Processing and Applications
S22 Bump Reliability and Electromigration
S23 High-Speed and Parallel Optical Modules
S24 Shock and Vibration Modeling
S25 Integrated Inductors
S26 Leading-Edge Design and Manufacturing in Electronic Applications

June 4, 2004
8:00 - 11:40 AM

S27 BGA/CSP Packaging
S28 Novel Interconnections
S29 Portable Product Reliability: Drop, Vibration and Bending
S30 Pb-Free Solders
S31 Emerging Optoelectronic Applications
S32 Modeling, Measurement and Design Optimization
S33 Manufacturing Advances for Next-Generation Technologies

June 4, 2004
1:30 - 5:10 PM

S34 Wafer-Level Packaging
S35 Board-Level and Embedded Optical Interconnects
S36 Thermo-Mechanical Modeling of Package and Interconnect
S37 Substrates and Bumps
S38 RF Modules
S39 Educational Initiatives for the 21st Century

June 2, 2004
1:30 - 6:00 PM

S40 Poster Session 1

Session Summary by Interest Area

Advanced Packaging
S1, S8, S14, S21, S27, S34

Components & RF
S7, S25, S38

Education
S39

Interconnections
S2, S9, S15, S28, S35

Manufacturing Technology
S26, S33

Materials & Processing
S4, S12, S17, S30, S37

Modeling & Simulation
S6, S13, S20, S24, S32, S36

Optoelectronics
S5, S18, S23, S31, S35

Poster
S40, S41

Quality & Reliability
S3, S10, S16, S22, S29

Special Topics
S11, S19

June 3, 2004
1:30 - 6:00 PM

S41 Poster Session 2

June 2, 2004
1:30 - 6:00 PM

Technology Corner Exhibits

June 3, 2004
9:00 AM - 12:00 PM
1:30 - 6:00 PM

Technology Corner Exhibits

ECTC 2004

The 54th Electronic Components and Technology Conference

Electronic Industries Alliance
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