Components, Packaging, and Manufacturing Technology Society

Newsletter

The Global Society for Microelectronics Systems Packaging

Vol. 27, No. 2, June 2004 (ISSN 1077-2999)

www.cpmt.org
www.ewh.ieee.org/soc/cpmt/newsletter

PRESIDENT'S REPORT

ECTC 2004

I hope everyone had a chance to enjoy the great 54th ECTC conference in Las Vegas, 1-4 June 2004. As you know, this conference is jointly sponsored by the CPMT Society and the Electronic Components, Assemblies and Materials Association (the components sector of the Electronic Industries Alliance). There were more than 1000 of us in attendance. The Technical Program of 39 oral and two poster sessions had over 325 papers. The program covered a wide range of topics, including: embedded optical interconnects, portable product reliability, 3D and high performance package design, flip chip bump reliability and electromigration, Pb-free flip chip interconnections, integrated inductors, wafer-level packaging and manufacturing, RF modules, reliability test methods, and electrical, thermal and mechanical modeling. Sessions were also included on the two new emerging technology areas of MEMS and nanotechnology.

The technical program was complimented by a plenary session featuring presentations on high density substrate technology, coordinated by CPMT High Density Substrates and Board Technical Committee, chaired by Yoshitaka Fukuoka of WEISTI, and a panel discussion featuring several industry perspectives on the emerging use of low-k dielectrics in integrated circuits.

As part of our new cooperative arrangement with NEMI, the National Electronics Manufacturing Initiative (discussed in the last newsletter) a special workshop was held on Tin Whiskers. The well-attended workshop provided the results of three NEMI-formed projects on 100% tin component finishes.

I'm sure you'll all join me in congratulating Pat Thompson, Program Chair; Steve Bezuk, General Chair; Donna Noctor - Vice General Chair; Eric Perfecto, Assistant Program Chair and all of the session chairs, professional development course instructors and speakers for a great week.

Global Representation:

As I shared with you in the last issue, one of my goals is to increase global participation in our Society. At our Board of Governors meeting in Las Vegas, I introduced a motion to implement a process whereby governing board members are nominated and elected on a regional basis. The process will ensure that membership on the Board is proportionate to the geographic make-up of the CPMT membership. So if the Asia/Pacific Region has 30% of the CPMT membership -- it will have 30% of the Board elected positions. Candidates for these positions will come to the CPMT Nominations Committee from the region (chapters and leaders of major conferences) . Only members in a region will vote for the representatives of that region. When this is implemented, it will give us true representative governance.

The motion passed, and the Constitution and Bylaws Committee will draft the required changes (which must be approved by IEEE before they can take effect.) Assuming all things proceed as planned, the new election process will take effect with the election of Board in 2005.

Award Winners

The ECTC conference is also a time to recognize outstanding contributions by individuals. Congratulations go to all the award winners for the year 2004.

David Feldman Outstanding Contribution Award

Ralph W. Wyndrum, Jr. (Wyndrum Associates) for exceptional service to IEEE and the CPMT Society in various leadership roles for over 45 years.

(continued on page 3)

CPMT OFFICERS

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Elected Board Members

2004: Tim Adams, N. Rao Bonda, Rajen Chanchani, Ralph Russell, Connie Swager, Naoaki Yamanaka

2005: William T. Chen Li Li, L. Merrill Palmer, Walter J. Trybula, E. Jan Vardaman, David C. Whalley

2006: William D. Brown, Philip C. H. Chan, Charles Lee, Johan Liu, Thomas G. Reynolds-III, Ephraim Suhir

Standing Committee Chairpeople

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Joint Committee on Semiconductor Manufacturing -- G. C. Cheek

Next News Deadline: September 5, 2004

Members-only Web:

UserName: xxxx (join CPMT to find out)
Password: xxxx (for 3rd quarter)

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TC-GEMP (21) Green Electronics Manufacturing and Packaging, Hansjoerg Griese, Email: griese@izm.fhg.de
TC-NANO Nano Packaging -- Rao Tummala, Georgia Tech, rao.tummala@ee.gatech.edu

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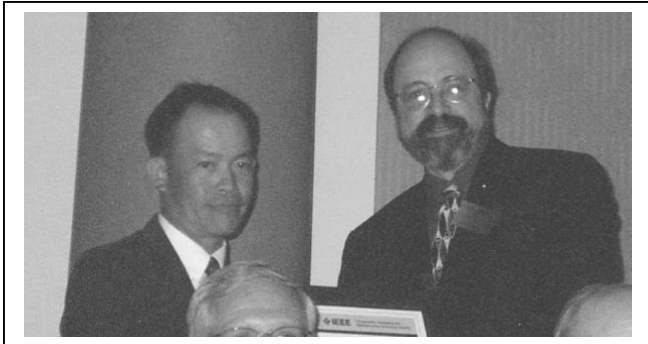
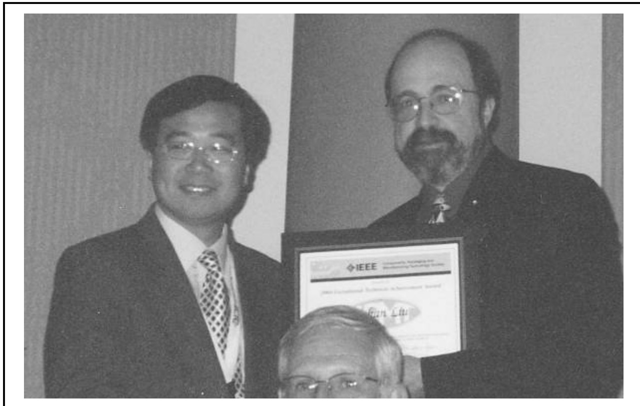
Outstanding Sustained Technical Contribution Award
Luu T. Nguyen (National Semiconductor Corp.) for major contributions to wafer level packaging and lead-free packaging, and for research collaboration and technology transfer in the area of electronic packaging.



Exceptional Technical Achievement Award
Johan Liu (Chalmers University of Technology) for major research contributions in the area of conductive adhesives for electronic interconnect applications for a wide variety of industrial and consumer products.

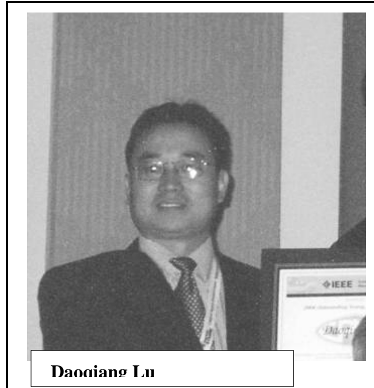


Outstanding Young Engineer Award (in alphabetical order)
Daoqiang Lu (Intel Corporation) for outstanding contributions to electrically conductive adhesives and advanced interconnect technologies and for supporting CPMT Society activities.
Shijian Luo (Micron Technology, Inc.) for outstanding contributions to underfills for flip chip packaging, and materials and processes for wafer level packaging and for supporting CPMT Society activities.
Lei L. Mercado (Intel Corporation) for outstanding contributions to the development of industry standards for electronic package reliability assessment, RF MEMS designs and copper low-k packaging and for supporting CPMT Society activities.
2003 IEEE Transactions on Advanced Packaging Best Paper Award
"High-Density 3D Packaging Technology for CCD Micro-Camera System Module" - published in the May 2003 issue
Hiroshi Yamada, Takashi Togasaki, Masanobu Kimura, Hajime Sudo

2003 IEEE Transactions on Advanced Packaging Honorable Mention Paper Award
"Thermal Analysis of Micromirrors for High-Energy Applications" - published in the August 2003 issue

Jianglong Zhang, Y.C. Lee, Adisorn Tuantranont, Victor M.Bright
2003 IEEE Transactions on Components and Packaging Technologies Best Paper Award
"Thermal Management of BioMEMS: Temperature Control for Ceramic-based PCR and DNA Detection Devices" - published in June 2003 issue
Daniel J Sadler, Rajnish G. Changrani, Peter C. Roberts, Chia-Fu Chou, Frederic Zenhausern
2004 Chapter of the Year Award
Santa Clara Valley Chapter
Tom Tarter - Chapter Chair
2004 Student Chapter of the Year Award (co-winner)
Georgia Institute of Technology
Shashikant Hedge - President
Leyla Conrad - Student Chapter Advisor
2004 Student Chapter of the Year Award (co-winner)
University of Arkansas
Ryan Pooran, President
Fred Barlow, Steve Tung - Student Chapter Advisors

"…Don't leave your career to chance"

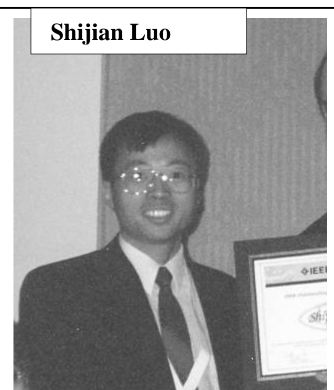


Daoqiang Lu

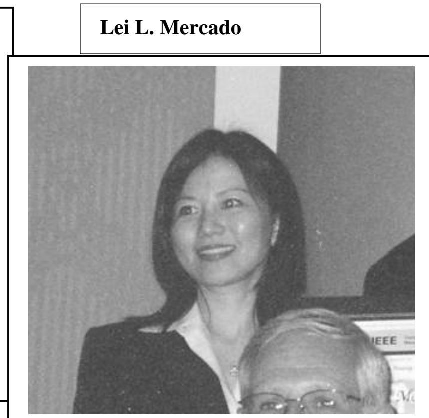
As I mentioned in my ECTC luncheon address, the draw of Las Vegas is gambling, the hope of hitting the long shot…crossing your fingers, closing your eyes and leaving your fate to chance. While this is a great attitude for gambling in Las Vegas, this is not how we should look after our careers. May I suggest that members aggressively seek out the opportunities that CPMT membership affords them, whether it be attending chapter meetings, attending the professional development courses and the technical sessions that are held each year at ECTC and other CPMT sponsored meetings around the world or simply networking with your peers from other companies who someday might think about YOU for that job opening that they have. So I encourage you -- do not become complacent in your career; do not leave it to chance. Leave the slot machine mentality in Las Vegas and invest in yourself. Take advantage of the opportunities your IEEE CPMT, membership affords you . And last but not least - enjoy your careers. These continue to be exciting times in the microelectronics industry.

I look forward to meeting and working with all of you during the next two years and thank you for your continued membership in our Society.

Shijian Luo



Lei L. Mercado



Board of Governors Meeting June 5 in Las Vegas

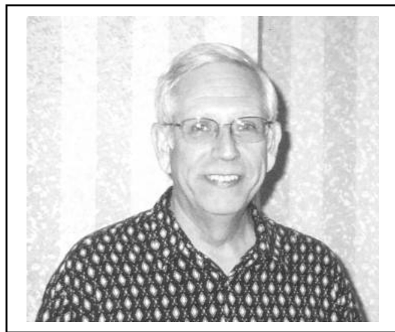
After a long week of ECTC, ITherm, and Las Vegas gaming 32 of your most active volunteers met all day as your Board of Governors.

Stirring up Discussion

President Phil Garrou opened the meeting by proposing reorganization of the officer ranks of the Society in the future due to changes in our structure. First, Phil suggested the elimination of the Secretary position since the function is now part of the Executive Director's functions. Next the treasurer would not balance the budget on a monthly basis (again the executive Director function) but become a VP of finance and worry about long range strategy. Third, consider removing the VP of Administration and Director of Technical Marketing positions. Phil proposed that a committee be appointed to consider making these changes in 2006.

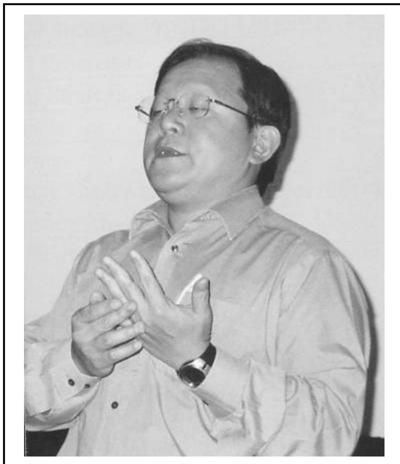
He announced that the Fiber Optics and Photonics TC has a new Chair, Susan Law from Australia.

Budget



John Segelken explained that the CPMT Society reserves went up to $1,919K. This resulted from the surplus of this year being $365.4K instead of the anticipated $171.9K. The main reason for this was that the Stock Markets went up so IEEE organization only taxed the society $99.8K rather than the anticipated $535.9K. Once again the objective in year 2005 is for a budget with balance of $0. The CPMT reserves are still on the thin side. The rule of thumb is that each society should have more than 1 year of operating expenses in reserve so that if necessary to disband, the last 12 months can still be of benefit to all members.

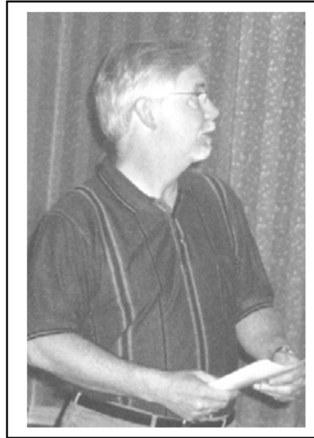
Conferences



Prof. Ricky Lee, Vice President of Conferences, listed the current 20 conferences with active CPMT participation. The agreements to partner with meetings all over the world are slowly evolving to a few easy to implement methods. It is important that all conference committees have independence of action but it is equally important that the value added by partnering with a global CPMT entity be matched in a sustaining way. The two options for conference support is the standard suggested IEEE approach where 15% surplus is planned from the beginning with a percentage of that going to CPMT for the advertisements, the Distinguished Lecturers, any keynote speakers, Proceedings, and technical help in assembling the sessions. The second approach would be agreed upon services from CPMT with fixed fees. This could involve the Proceedings.

The plans for this year's EPTC meeting point to the possibility that it will become the Asian equivalent to the ECTC in the US...currently the biggest CPMT conference. Moving the Packaging Materials conference to University of California - Irvine for this year, holding the 3S (SoC, SiP, SoP) at Georgia Tech, and supporting an Organic Microelectronics workshop with American Chemic Society in April 2005 in NE U.S. were OKed by the Board.

There was discussion initiated by Ephraim Suhir on having a Workshop on Display Materials in spring 2005 in the San Francisco area. Other discussion



concerned coordinating the ECTC and ITherm so one could more easily participate in both. Having one in the Mirage and one at Caesar's Palace did not work out this year.

CPMT Website

Tim Adams went over the massive improvements that have been made in scope and usability of the web pages. Templates are available so Chapters and TC can easily assemble pages with the same general look of the rest of the CPMT home pages. Go look at the CPMT websites if you have not seen them for a year.

Technical V P Report

Vice President Rolf Ashenbrenner updated the technical committee status. There are 18 active committees. The TC Opto, Fiber Optics and Photonics has a new Chair, Susan Law of Australian Photonics/OFTC. The TC of IC and Package Assembly is currently without a Chair possibly because the assembly foundries are still trying to recover from the electronics recession. Some TCs still need to update their web pages.

Conference Activities in Japan

Yoshitaka Fukuoka reported on the year in Japan. In particular ICEP - International Conference on Electronics Packaging, VLSI-PKG-WS VLSI Packaging Workshop, and SP JWS - System Packaging Japan Workshop. The ICEP in April 2004 had 248 attendees to hear 84 papers. About half the papers were from overseas. The SPJWS in February 2004 hosted 78 attendees hearing 24 papers. The VLSI workshop had 100 attendees and 41 papers. About 1/3 of the papers were from overseas.

After much discussion and accommodations in Japan, a proposal on CPMT financial participation in these meetings was presented by Yoshitaka Fukuoka and was immediately accepted by the Board of Governors.

ECTC Report

C. P. Wong explained that new topics are being considered including Bio-nano packaging. Donna Noctor and Pat Thompson are on both the CPMT BOG and on the ECTC organizing committee. Pat Thompson reported that 554 abstracts were received and 326 papers were accepted. 273 were given as view graph presentations in 39 sessions and 53 papers were given as posters in 2 sessions. The papers came from 24 countries. North America provided 56%, 8 countries supplied 30% of the papers from Asia, 12 countries of Europe supply 13%, and 2 other companies provided the rest. The affiliation of the attendees are 49% from Corporation, 47% from Universities, and 4% from R&D institution. There was a total of more than 1000 attendees counting the exhibitors, speakers, and ses-

sion organizers. This was the second highest attendance ever.

The ECTC website has been a great success in advertising and signing people up for the meeting. In addition, the members-only section is used by program volunteers to score abstracts and arrange sessions. This year the professional development courses were asked for on-line. Forty were submitted and 16 selected. Rao Bonda will be the new ECTC website administrator.

They have changed the name of Advanced technology sessions to "Emerging Technology." This will include the MEMs, Bio, and Nano trends. This year the final program that was handed out at registration had every preplanned event clearly listed so no one missed anything they wanted to go to.

This was the first year of the "Intel Best Student Paper Award." In addition, the Motorola Best paper Fellowship was held with the winner to be announced later.

Press Conference

A press conference was held during the conference to get the highlights to the media. Semiconductor International, Chip Scale Magazine, and a technology columnist were represented. This format has become an effective way to get the story of advancing technology to the media.

Publications

Vice President Paul Wesling reported a new faster access server is now hosting many of our Society pages. The TC and Chapter pages can be placed here as can the members-only area. Paul is looking for more webmasters all the time.

He has started a monthly e-Newsletter with late breaking news, reminders, ads. He intends to build up the address list for this e-Newsletter beyond CPMT members to get more draw to our meetings and publications.

In addition to improving submitted paper references by making subject matter "ontologies' available to authors, Paul is also investigating a 3 month path for 2 page papers for the transactions. To this end we need more reviewers for the transactions.

There is a new Transaction on Display Technology which CPMT is a partner. IEEE is using CDs instead of paper copies for most conference proceedings in the future. Papers must be in IEEE PDF specification which is not exactly the same as the PDF on everyone's computer. There are special fonts and symbols used in engineering that must be accommodated. IEEE will make conference papers available through XPLORE to members, paying individuals, and paying companies and universities. In turn CPMT gets $25 per paper (so ECTC could generate $10K for the society)

Membership

Ralph Russell, director of membership and chapters, announced that the Chapter of the year is from Santa Clara. He pointed out that like most of IEEE, the membership of CPMT has dropped in the last year by about 5%. Current total is 2,931. The best thinking indicates this is due to unemployment of U. S. engineers increasing to 6% in this period, increased retirements among packaging and component engineers, IEEE purged non-active life members (-2%), and fewer companies are paying professional society dues for employees.
IEEE has stopped societies from selling "lifetime society memberships" in which a one payment flat fee would make a person a member forever. This had been considered by CPMT over the last few years. Ralph suggested that the future members were the students of today and we must further enhance the student chapters and the ease of getting students to our big meetings and published in our transactions. Ralph discussed the pros and cons of having a CPMT Membership Directory.
The irony was evident that despite the best core of active volunteers ever, the largest set of international meetings, and the most pages published as a Society we continue to slowly lose membership.

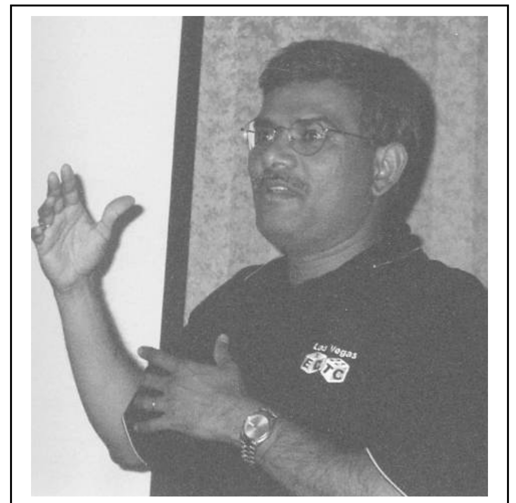
Marketing

Director Connie Swager explained that the CPMT has had 1.3 million media impressions (including print and electronic) over the last year. This is a metric to measure how often CPMT reaches the limelight in engineering media. This metric has probably gone up by a factor of ten due to volunteer efforts led by the Potomac Communication Company. In addition, we now have 6 polished fact sheets that we can distribute on the strengths of our society. How and when this media attention relates to more attendance at meetings, more members, and more references to our publications is not yet clear. Marketing is an experiment not an art for engineers.

Fellow Nominations

C. P. Wong reminded everyone that in 2003 our society generated 10 nominations to the IEEE Fellows Committee. Of these 5 were picked by the committee along with 5 other CPMT Society members nominated by other societies. This year 5 strong nominations were submitted but none were repeat nominations. To increase the number of Fellow nominations (our society size could accommodate at least 15 nominations) we must encourage members to suggest names for nomination. In addition, a team of Walt Trybula, C. P. Wong, Rao Tummala, David Palmer, Anthony Chan, Johan Liu, Luu Nguyen, and others will assemble a list of at least 25 potential nominees. With the nominee's permission a nominator will be appointed and a handful of references will be assigned. Our Society currently has about 100 Fellows so finding 5 knowledgeable fellow references for each nomination should be possible.

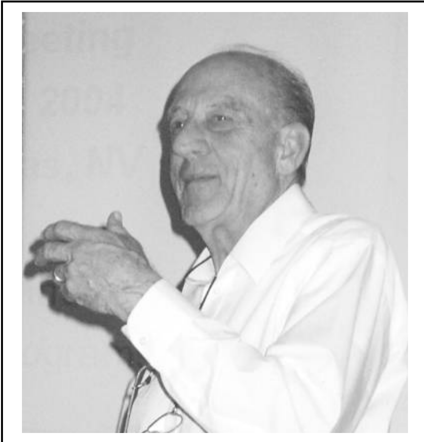
Awards



Rao Bonda reported on the CPMT Award process this year. He was extremely pleased at the quality of those submitted for awards but would hope that more submissions would occur next year. He would like each board member to submit one nomination. (see article elsewhere in Newsletter for award winners)

Industry Program

John Stafford submitted a report showing the growing partnership of CPMT and NEMI. For example, 15 CPMT members are participating in the NEMI roadmaps.



Students

Bill Brown repeated the truism that our society future depended on the students of today. But he also indicated that without a faculty sponsor there could be no student chapter. He reviewed the 5 existing chapters and indicated that 3 had booths at the ECTC (Arkansas, Georgia Tech, and Hong Kong). He suggested starting a contest between chapters to get a little of the competitive student juices flowing.

Region 8

Johan Liu reviewed recent activities in Europe. The Eurosimu'04 in Belgium in May had 100 delegates. The Scandinavian Chapter meeting was held in Denmark with a visit to Delta Denish Technical University. Discussions were held with IMAPS Europe concerning participation in their Belgium 2005 meeting.

The Conference Electronic Goes Green 2004+ is being organized by the Fraunhofer IZM Dept of Environmental Engineering. It will be held September 6-8 in the Estrel Convention Center of Berlin Germany. The main topics will be: Implementation and Legal Compliance, Leading Edge Technologies, Looking Ahead: Technologies, Markets & Sustainability

The annual IEEE workshop on System Packaging is planned for Jan 31 - February 2, 2005. It will take place at the Park Inn Alexander Platz, Berlin, Germany.

Region 10 Activities

Ricky Lee reported briefly that in Asia. there are now 8 chapters in Asia (see report elsewhere in this newsletter). Hong Kong has been very active with 8 meetings during the year and has a very active student chapter. Currently Taiwan's organization is spread a bit thin and refocus is needed. India has a lot of active individuals and companies but does not yet host a CPMT meeting. This appears to be a good opportunity.

EDITOR's TURN

First, my thanks to all those who sent in their news. All those pictured in this newsletter contributed plus: Marsha Tickman, Alina Deutsch, Walt Trybula, Nikita Ryskin, Li Li, Uwe Arz, Evan Davidson, Al Puttlitz, Ron Gedney, Len Schaper, Jan Vardaman, and Vasu Atluri. I apologize for any dim pictures; going to ECTC resulted in 4 x-rays by airport security. Next time I will go digital.

Your Society is “going Internet” just as the world is. On page 2 of this paper newsletter is the password to reach the members-only section of CPMT website. Every week this site is getting richer. In the banner on page 1 is the web link to the Internet manifestation of this Newsletter. It comes out 1 month earlier, is updated often, and is in color. Paper comforts but is second.

Ephraim Suhir Awarded

The ASME Society awarded CPMT Board member Ephraim Suhir the prestigious ASME award - 2004 Worcester Reed Warner Medal for outstanding contribution to permanent literature of engineering. His citation is "for outstanding contributions to the permanent literature of engineering through a series of papers in mechanical, microelectronic, and optoelectronic engineering, which established a new discipline known as the Structural Analysis of Microelectronic and Photonic Systems". Formal presentation of the award is scheduled to take place at the President's Luncheon, Monday, November 15, during the ASME IMEC in Anaheim Hilton.

REGION 10 CHAPTER ACTIVITY ROUND-UP

-- by Dr. P. B. Parikh

· Dr. Lih-Shan Chen of **Taipei CPMT Chapter** has reported the chapter having organized a talk on the "Thermal-Fatigue Life Prediction of Electronic and Optoelectronic Lead-Free Interconnects" at Kaohsiung, Taiwan on June 13, 2004. In addition to the IEEE/CPMT Taipei Chapter members, they expect many non-members at Kaohsiung also to attend this interesting talk. CPMT Taipei Chapter will also co-organize an international symposium and Exhibition on Electronic Packaging at Kaohsiung, Taiwan on April 21-24, 2005.

· As reported by Dr. K N Seetharamu, the **CPMT Malaysia Chapter** has planned two technical lectures in the month of June 2004. The first one will be on 9th June with the title, " MEMS and their Application" and the second one has been scheduled on 23rd June 2004 on "Photonics: A light introduction". Both these technical talks will be delivered by Prof K N Seetharamu, the chapter chair at Seminar Room, Engineering Campus.

· Dr. Cheung Yiu Ming, Ken of **Hong Kong Chapter** has reported that the chapter successfully launched two technical workshops in April 2004. The first one was by Dr. Chuck Bauer on 21st April with "Three Dimensional Packaging, Interconnection & Assembly for Microelectronics Miniaturization" as the topic. The second workshop on "Wire Bonding in Microelectronics" was led by George G. Harman on 30th April 2004.

The chapter has further arranged two technical workshops in June 2004:
(i) Dr. Michael Pecht, "Monitoring the Health (Reliability) of Products" on 9 June 2004.
(ii) Dr. John H. Lau, "Impact of Lead-Free on Electronic and Optoelectronic Packaging and their SMT assembly" on 15 June 2004.

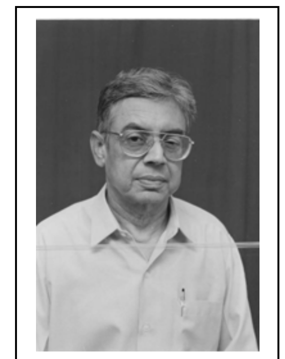
The chapter has also planned a workshop given by Professor Johan Liu from Chalmers University of Technology, Sweden in July and one other given by Professor Kuo-Ning Chiang from ERSO/ITRI and National Tsing Hua University, Taiwan in August.

The student activities for the Hong Kong chapter are:
(i) An exhibit booth from CPMT Hong Kong Student Chapter at ECTC 2004.
(ii) A Student Symposium in June 2004.

· The **India Council CPMT Chapter** had planned to co-organise a technical talk on "Recent Advances in Microelectronics - Packaging" and a half-day workshop on "SMT Production Technologies" with IEEE Bombay section and SMTA- India Chapter in April 2004. The same had to be postponed because of preoccupation of the faculty and also the student members because of the academic year ending examinations. These programs are now planned for June 2004. The executive committee for CPMT India Council Chapter for the year 2004:

Dr. P. B. Parikh - Chapter Chairman
Dr. Shankara Prasad - Chapter Vice-Chairman
Prof M. M. Shah - Chapter Secretary/Treasurer
Members - Dr. Maneesh Guru Dhingra
Dr. J. N. Roy
Mr. I. M. Rao

Meanwhile, our Chapter Vice-Chairman, Dr. Shankara Prasad, and Our executive committee members, Dr. Maneesh Dhingra and Mr. I. M. Rao have expressed active interest in the chapter's activity and we look forward to a spurt in the CPMT India Chapter.



CPMT Society and NEMI Join Forces with New Partnership

The CPMT Society and the National Electronics Manufacturing Initiative (NEMI), an industry-led consortium focused on strengthening the global electronics supply chain, recently entered into a formal agreement outlining key areas of collaboration between the two organizations.

One of the primary collaborations under this new agreement will be roadmap development, beginning with the 2004 NEMI roadmap. The roadmaps, created every two years, map the future manufacturing needs of the electronics industry and identify key technology and infrastructure developments required to assure leadership of the global supply chain over the next decade. It helps companies anticipate shifts in product requirements and provides an early warning of changes in technology or infrastructure.

Both the Society and NEMI realized that many of our own members' fields of expertise complement and substantially overlap. In fact, many CPMT Society members have already represented their respective employers in the development of previous NEMI roadmaps. It made sense that the two organizations should collaborate on a more formal basis.

"NEMI has been involved with deriving roadmaps for important cutting-edge technologies and we are excited to partner with this prestigious organization," said Phil Garrou, CPMT Society President. "CPMT's partnering with NEMI in the roadmapping activity will hopefully produce an even better forecast of future technology directions," he adds.

NEMI is also embracing a more global perspective. With more than 40 percent of the Society's members outside the United States, the CPMT Society is offering experienced professionals from Europe, Asia and North America to many of the NEMI roadmap chapter committees. Involvement of this broad-based group will help NEMI in its efforts to globalize the scope of the 2004 roadmap. Conversely, NEMI plans to participate in our activities by collaborating on CPMT Society-sponsored conferences, workshops and refereed publications. The CPMT Society will also coordinate with the NEMI Technical Committee to develop R&D priorities.

Rolf Aschenbrenner, Vice President of Technical Activities for the CPMT Society notes, "We look forward to NEMI members presenting their work at CPMT Society workshops and conferences as well as soliciting papers for IEEE CPMT Transactions journals. In fact, we are already coordinating a NEMI tin whisker workshop as part of our Electronic Components and Technology Conference (ECTC) in Las Vegas this June."

CPMT President Phil Garrou with NEMI CEO Jim McElroy

NEMI sees this partnership as a win-win situation as well. "We have worked informally with the CPMT Society for many years, but wanted to form a more structured relationship with planned activities that would allow us to work together rather than just doing things on an opportunistic basis," said Jim McElroy, Executive Director and CEO of NEMI. "The two organizations share many areas of focus and activity, and we feel there are a number of synergies to be gained by collaborating."

The two organizations launched the partnership at NEMI's 2004 roadmap kick-off meeting, 24-25 March in Newark, California USA. For more information about NEMI, visit www.nemi.org.

Call for Candidates CPMT Board

The CPMT Society is governed by a Board of Governors composed of officers, 18 elected members-at-large, and various committee chairs and representatives (see inside cover of this Newsletter for details.) Annually, Society members are asked to elect six members-at-large for a three-year term of office. Candidates for member-at-large are selected in two ways -- either by the Society Nominating Committee, or by petition. If you are an IEEE and CPMT Society member in good standing and are interested in serving on the Board of Governors, you can automatically become a candidate via petition by following the procedures below. The term of office for this election is 1 January 2005 through 31 December 2007.

- Prepare a petition that contains your name, member number, and statement of your qualifications for office.
- Provide lines for signatories. Each line should include space for a printed name, member number, and signature.
- Have the petition signed by a MINIMUM of 25 CPMT Society members in good standing (Student grade members are not eligible to sign.)

Membership status of all signatories will be validated. It is suggested that you gather more than 25 signatures in order to assure meeting the minimum required number of valid signatures.

- Submit your petition by no later than Friday, 23 July 2004

to: CPMT Society Nominations Committee
c/o Marsha Tickman
IEEE CPMT Society Executive Office
445 Hoes Lane, PO Box 1331
Piscataway, NJ 08855-1331 USA
or FAX to 732-981-1769.

If you have questions or need additional information, contact Marsha Tickman at the above address, by phone at 732-562-5529, or by e-mail at m.tickman@ieee.org.

ECTC Professional Development

On June 1 at Caesars Palace Las Vegas 292 students took part in 16 professional development courses offered just before the ECTC began. These courses result from the volunteer work of Albert Puttlitz, Rao Bonda, Ronald Scotti and all the instructors. These courses produce about one third of the budget surplus for this meeting, thus providing services for all members. The most popular courses were "Interconnect and Packaging Technologies for 10 and 40 Gbps Telecom and Datacom" taught by Roberto Coccioli and Hassan Hashemi, "Introduction to Nanoscale Packaging and Systems" given by semi-professional golfer Rao Tummala, and "Lead-Free Solders for Robust IC Electronic and Optoelectronic Packaging" with Instructor John Lau.

The CPMT Society is authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET). CEUs are recognized by employers as a formal measure of participation in self-study, tutorials, symposia and workshops. In addition, the CPMT CEUs can be applied towards "IEEE CPMT Professional Development Certificates" It takes about 50 hours of Professional Development courses to earn this Society Certificate.

TAB talks to CPMT Board

IEEE TAB member Ralph Wyndrum has talked to most IEEE Societies with these same issues and hopes small societies such as the CPMT Society do not remain introverted but get their great ideas into the mix.

First, Ralph pointed out that despite having 800 Distinguished Lecturers in IEEE there often are none willing to appear at remote chapter meetings. In contrast, there are no end of volunteer speakers for Beijing or Berlin, but mention rural campuses or technology sparse cities and there is only silence.

Second, Ralph discussed the tremendous impact that must be managed by the transfer of IEEE publications to digital rather than paper format. Since IEEE is only the low cost technical publication provider (due to our dedicated volunteer authors and editors) in a large publication market that is already going "electronic" we are not controlling the destination or the rate of change. However we do need a business plan and our own milestones for this transition. We all must remember that in volunteer professional societies at the simplest level only publications and meetings earn revenue that supports all member services.

Charles A. (Bud) Eldon

Interview by Li Li, Newsletter associate editor

(Freescale Semiconductor)

CPMT Society member CHARLES A. (Bud) ELDON is a former President of the IEEE - the only CPMT Member who has served as President. He is also a CPMT Society Past President. He was elected as an IEEE Fellow in 1987 for contributions to the manufacture of high-quality electronics components and systems. As a former IEEE President, the CPMT newsletter team interviewed him to hear about his experiences as an IEEE President, overseeing one of the world's largest and most prestigious technical societies for engineers. He shares his experience, vision, and contributions on IEEE globalization and various other aspects, such as engineering jobs outsourcing, IEEE Fellow standards, and international relations.

Bud also was the organizer of our Santa Clara Valley chapter, now the most active local CPMT chapter and winner of this year's "Chapter of the Year" award. Later he was a founder of CPMT itself within the IEEE. So the Newsletter asked him to share stories of the "old days": What motivated him to start the chapter? And what was the origin of CPMT?

Editor:
Tell us a bit about what it was like to be President of the IEEE.
Bud:
Being IEEE President surely was the greatest honor of my life, as well as an incredible experience. It also was a complete surprise - really a result of fate - because I never sought the position. What happened is that the man elected to be President-Elect in 1984 died early in the year. Under IEEE Bylaws, the Board of Directors is charged by themselves to elect a replacement, subject to subsequent membership approval. As the 1983 Executive VP (a position eliminated several years later), who had been elected by the entire membership, I was an obvious candidate and was chosen. Previously I'd been Director of Region 6, then IEEE Treasurer. Now I became the 1984 IEEE President-elect and thus the 1985 President.

Editor:
How did it get started, and where does "CPMT" come in?
Bud:
It all began with what has now become CPMT. The story: my boss, the VP-Manufacturing of HP, walked down the aisle, sat on my desk, and said, "Bill (Hewlett) wants us to start a chapter of the IRE Professional Group on Product Engineering and Production (PEP), here in the Bay Area, and we agreed that you should do that." To which I innocently replied, "What's IRE?" Explanation: as a physics major (but with mostly electronics courses), I hadn't been a member - didn't even know that Hewlett was a recent Past President. My boss laughed but assured me that joining IRE would be no problem - and a good idea. Need I add that I agreed immediately? I became an IRE member on 2/1/1955.

With the helpful guidance of past IEEE GM, Dick Emberson, I learned what was necessary to form a chapter. Then, after calling production engineers and production managers whom I knew in several Bay Area companies, I recruited enough volunteers to qualify. Is it a surprise that several became close friends, as well as helpful technical counselors? Together we started the San Francisco Chapter of the IRE's PEP Group in 1956. Paul Wesling was an early active member who has been serving the CPMT Society for numerous years, currently as the Society's VP of Publications.

At that time we all were concerned about how to make printed circuits. I was responsible for designing assembly and test systems for them, as well as for entire instruments, and for plastic molding, sheet metal fabrication and precision machining. A major concern was the quality and limited life of tubes (remember those?): transistors had been invented by then, but integrated circuits were not in use. PEP members shared experiences and solutions, just as they do nowadays Then in 1963, when I'd been elected chairman of the PEP Group, and IRE was merging with AIEE, I was asked to consider how to reduce the number of technical units in the eventual IEEE. So I approached the chair of the IRE Components Group, Lew Kahn, about merging our Groups into an IEEE Society. We did it, forming what later came to be called CHMT (Components Hybrids and Manufacturing Technology), then CPMT.

Editor:
So what stands out in your mind about serving as IEEE President?
Bud:
As President in 1985 I was in the right place at the right time to help internationalize IEEE. Ten years earlier, IEEE had broken relations with the Popov Society of the USSR, because of IEEE leaders' opposition to the invasion of Afghanistan. Accepting an invitation to "the President of IEEE" to attend the 40th anniversary of the Popov Society and to discuss renewing relations, I went to Moscow with a plan to negotiate a written agreement that specified terms of quid pro quo: IEEE members from "the West" would receive identical treatment to that received by Popov visitors in our region. Most former exchanges had involved technical tours in the US or Europe by Popov parties, but no technical presentations or tours during IEEE visits to the USSR. The plan worked: a formal agreement was reached within a year; the IEEE Moscow Section was organized; many Russians have become IEEE members; and technical exchanges have continued since.

Negotiating agreements with non-US engineering societies has been a regular task for IEEE presidents, along with installing new Sections around the world. In 1985, a few of us went to Beijing to officiate at the opening of that Section, the first IEEE entity in the PRC. And "showing the flag" (a euphemism for traveling and making speeches) at IEEE Section meetings and conferences all over the world is an equally enjoyable honor - and an obligation.; so there was lots of that in 1985, too.

Editor:
What other IEEE issues involved your time?
Bud:
One issue during that period was the official IEEE-USA position about education of non-US engineers in US universities. IEEE-USA ("USAB" at that time) passed a resolution that all such graduates must "return home" immediately after receiving their degrees. Already approximately 50% of PhDs in engineering were being awarded to non-citizens. In addition, "outsourcing" of manufacturing was beginning to boom in Asia. Believing that their position was unfair, I sought support of past presidents and vice presidents of IEEE for a petition to USAB to change their resolution so that talented graduates would be encouraged to stay in the US, if they wished. They did, and that seems to have been to the ultimate benefit of everyone, although "outsourcing" now includes engineering jobs, too, partly as a result of some US-educated engineers "going home" to India, etc. That issue in 1985 (and until last year) reflected industry's expressed need for more engineers than were available in the US. That need led to a perception among industry leaders in the US that IEEE had different goals. In an effort to resolve that perception, I invited the elected presidents of most US industry associations (AEA, EIA, ERA, SIA, et al) to a meeting. Eric Herz, our GM, invited his counterparts, the various staff directors, to join us. Everyone agreed to form an informal committee (the "No Name Committee") as a forum for sharing concerns and working together to deal with them. That committee was effective for several years, eventually formalized as the US Electronics Industry Forum. But IEEE presidents in the mid-1990s dropped it - an unfortunate mistake, in my opinion, because IEEE's relations with US industry have been an obvious and perplexing problem for many years.

Related to that issue has been my concern about IEEE recognitions, in particular the selection of IEEE Fellows. One of my predecessors as chair of the San Francisco Section in 1970 complained even then that outstanding industry engineers seldom were elected to Fellow Grade - that only professors and industry executives appeared to be anointed. That sad image continued. However, as chair of an ad hoc committee appointed by the past 3 IEEE Presidents, I saw the Board approval of changes in June, 2003 that will encourage explicitly the nomination of "Application Engineer/Practitioner" candidates, as distinct from either industry or academic "Research Engineers" - or "Educators" or "Leaders". That's a change that I believe will be particularly attractive to members of CPMT who are involved in Manufacturing Technology and Packaging, most of them in industry.

As part of my orientation in 1984 I sat in a meeting of the IEEE Long Range Planning Committee and discovered that it was a dumping ground for strategic matters that were either too complex or too controversial for the Board of Directors. That prompted me to introduce "strategic planning" during my term. With help from a Director who was also familiar with that activity from his work in Westinghouse, we wrote Bylaws approved by the Board to replace LRP with Strategic Planning, and I submitted the exact procedures and terminology that are still in use today. I believe it was a real contribution to IEEE.

Otherwise my term as IEEE President, like my previous assignments and my later service on the Board of the IEEE Foundation, was challenging but enormously rewarding. I'm truly grateful for the experiences and for the many friendships I've established.

Charles A. (Bud) Eldon, LF

Facts about Charles Eldon

Charles A. (Bud) Eldon currently lives in Sierra Vista, AZ with his wife Betty, his Stanford University undergraduate classmate. They are proud parents of 4 children (boy, girl, boy, boy) and now 7 grandchildren, the 2 oldest now students at Stanford.

He was raised in Hawaii thru high school. He left high school early to attend Stanford, got drafted into the Navy, and became an electronics technician. After discharge, he returned to Stanford for a BS in physics in 1948, followed by an MBA in 1950. He worked at Hewlett-Packard from January 1951 until April 1990, when he retired and moved from Los Altos, CA to Sierra Vista, AZ.

Charles A. (Bud) Eldon can be reached by email: b.eldon@ieee.org.

2004 IEEE Systems Packaging Japan Workshop

February 2 - 4; Hakone, Japan

The Japan Systems Packaging workshop was held this year in the beautiful mountain resort area of Hakone alongside Lake Ashinoko nearby Mount Fuji. This is the tenth Japanese workshop in a biennial string that began in 1986 as the Japan Computer Packaging Workshop held in Oiso, Japan. At its inception, the workshop encompassed all aspects of advanced electronics packaging. As time evolved more specialized packaging technology meetings began being held all over the world while important packaging applications began to broaden beyond computers and the workshop was renamed to Systems Packaging at the ninth workshop in 2002. Its new focus is on the choices, challenges, interactions and tradeoffs between all aspects of packaging technologies at the systems product level.

There were twenty-four invited presentations at this year's workshop held in seven sessions. In addition there was a most unique opportunity for all of the seventy-eight participants (sixteen from abroad) to visit the world's largest computer at the Earth Simulator Center located at the Japan Marine Sciences and Technology Center at theYokohama Institute for Earth Sciences.

Yuzo Shimada of NEC, the workshop's General Chair, gave opening remarks. His first task was to mourn the recent loss of two of the Japan committee's most active members. Prof. Koji Nihei was retired from Oki Electric and a faculty member at Waseda University. He was a former workshop chair, an IEEE Fellow and a member of CPMT's Board of Governors (BOG). Nihei-san was instrumental in building the bridges that exist today between the packaging societies in Japan and the rest of the world. He was also a renowned contributor to the semiconductor packaging industry. The other loss was Mr. John W. (Jack) Balde. Jack served as the liaison between CPMT and the Japan Systems Packaging Committee. From the beginning in 1986, Jack advised the committee and helped to organize each Japan workshop. He ran his own company (Interconnection Decisions Consulting) for over twenty years after retiring from Western Electric. He was a founding member of the Computer Society's Computer Packaging Technical Committee (now also CPMT's TC-14) in 1971 and remained actively involved with it until his death. Along the way he became an IEEE and IMAPS Fellow, a member of CPMT's BOG, and the winner of the IEEE-CPMT Millennium Medal for all of his contributions to packaging technologies and technical societies throughout the years.

The morning kick-off keynote session consisted of three speakers. Prof. Rao Tummala, past President of CPMT and Director of the Packaging Research Center at Georgia Tech, shared his vision and status of System-on-Package (SOP). He compared it with the less integrated passive component-less System-in-Package (SIP) and the earlier uses of SCMs in the '70s and MCMs in the '80s. Following this talk was one from Bob Guernsey of IBM Research and Development. He spoke about the new packaging needs and opportunities for the 45 nm silicon design node. The last morning presenter, Prof. Yoshiaki Nakano of the University of Tokyo, highlighted the recent progress that has been made in photonic networking devices and he described their recent challenges and solutions.

The afternoon session began with another keynote speech from Prof. Tetsuya Sato of the Earth Simulator Center. He described the knowledge being learned from the Simulator and its impact upon scientists throughout the world. He also talked about plans for improving the Earth Simulator to allow scientists to predict future events such as catastrophic weather phenomena with greater accuracy. Following Prof. Sato's presentation were ones from Hubert Harrer of IBM Germany, Kazunori Nakajima of Hitachi, Shinji Baba of Renesas Technology, Masateru, Koide of Fujitsu and Jun Inasaka of NEC. They gave descriptions of the packaging technologies used in IBM's z990 mainframe, Hitachi's SR11000 supercomputer, high-end flip-chip ball-grid-array substrates (FC-BGA), Fujitsu's high-end server and the Earth Simulator, respectively.

In the evening of the first day, there was a session on optical interconnections for communications systems. Takeshi Sakamoto of NTT, Takashi Mikawa of ASET and Ichiro Hatakeyama of NEC gave presentations on the subjects of packaging parallel optical interconnection modules, optoelectronic packaging technology and packaging techniques for optoelectronic interconnections, respectively. These talks were followed by a lively and interactive banquet.

At the banquet, Hisao Kanai, the 1998 workshop General Chair, reviewed the history of the Japan Computer Packaging Workshops. He also gave his views on the future of LSI packaging. After this talk, Erich Klink of IBM Böeblingen - Germany, the current TC on Systems Packaging (TCSP - TC-14) Chair, presented Yuzo Shimada of NEC, the workshop's General Chair, with a beautiful engraved wooden and brass plaque to thank him for the excellent organization work he and his team contributed to making the workshop a success. Subsequent to this ceremony, one and all enjoyed a wonderful banquet replete with great food, conversation and laughter.

The next morning Tadanori Shimoto of NEC described an ultra-thin high-density packaging technology for chip scale packages (CSP) and SIPs. Rolf Aschenbrenner of Fraunhofer IZM - Berlin illustrated the successful integration of passive and active components into organic built-up layers. A gigahertz SIP using a multi-layer thin film interposer on a silicon substrate was presented by Hirohisa Matsuki of Fujitsu. Following this, Marcos Karnezos of ChipPAC talked about 3-D packaging architectures: their design challenges and applications. To end this session, Yasuhiro Yamaji of ASET described a thermal and reliability design study for 3-D chip-stacked modules with vertical interconnections.

The afternoon of the second day was set aside for the visit to the Earth Simulator Center. During this two and half hour tour, participants were able to look at the technology and interact with the Center's experts. They saw exhibitions of the machine's capabilities and checked out the facilities and air conditioning required for cooling this massive computer. After returning to the hotel, there was a dinner party with local entertainment including "Mame-make" (throwing beans) and "Yudate-Shishimi" (a lion dance performed by a troupe from Miyagino, Hakone). Intermixed with all the fun were a myriad of technical discussions about impressions of the technical tour. (tour group in garden)

On the last day of the workshop, a morning session dealing with cellular phones and mobile information systems was held. Mitsuru Murata of NTT DoCoMo showed the latest trends in cellular handsets. Packaging solutions and system optimization for advanced wireless base-stations was described by Petri Savolainen of Nokia. This was followed by Aroon Tungare of Motorola who presented a packaging technology with embedded capacitors for cellular phones. To end this session, Tamotsu Nishino of Mitsubishi talked about suppressing multi-path coupling in a direct conversion receiver packaged on a low temperature ceramic carrier (LTCC).

Two final talks on advanced packaging were given by Osamu Okada of Casio and Eric Beyne of IMEC - Belgium. Okada-san described a wafer level chip scale package (WL-CSP) for consumer products while Beyne-san revealed a multi-layer thin film technology for systems packaging.

The 2004 Japan workshop was considered a great success by all attendees. They felt it was a great opportunity to see the most advanced work going on in all the different fields that involve semiconductor packaging. It was also a unique chance to get to know and interact with their peers from all over the world. Yuko Shimada gave the closing remarks and the next chair for the 2006 workshop was named. He will be Masakuzu Yamamoto of Hitachi.

The TC on Systems Packaging is currently planning to have a 2004 workshop in Atlanta, Georgia USA and one in Berlin Germany in 2005. The TC's web site can be checked periodically for updates. It's URL is: http://ewh.ieee.org/soc/cpmt/tc14/index.html .

Prepared by: Yuzo Shimada, edited by: Evan Davidson

IEEE/CPMT Technical Committee on Electronics Manufacturing

The focus of the TC-EM is on enhancements in existing manufacturing technologies, tracking and assisting emerging manufacturing technologies, and evaluating opportunities in future manufacturing technologies. TC-EM is the combination of the old CPMT TC-4 (Manufacturing) and CPMT TC-8 (Semiconductor) technical committees.

Due to the changes in technologies and manufacturing requirements, TC-EM is evolving into a multi-focused committee with four primary areas: electronics manufacturing (packaging and assembly level); semiconductor manufacturing; Technology Roadmaps; and interfacing with the nano community to assist in manufacturing issues.

Electronics Manufacturing - the focus is on all aspects of electronics manufacturing. The primary conference is IEMT, which is jointly run with SEMI during the SEMICONWest week. A meeting of this sub-committee is anticipated during IEMT in July 2005.

Semiconductor Manufacturing - the focus is on semiconductor manufacturing. The Litho Workshop (TC-8) focuses on the imaging aspects of the manufacturing processes. The proposed PhotoMask Europa is directed at the manufacturing process for semiconductor masks. There are a couple of other potential meetings that could be co-sponsored which are under consideration. There will be a meeting of this group during the Immersion and 157nm Symposium in Vancouver, B.C. Canada, August 2-5, 2004.

Roadmaps - the focus is on the NEMI technology roadmap. The detailed collaboration and the identification of the people for the next version of the Roadmap has not been identified. The people who will be involved for the next revision (2006) will come from the Electronics Manufacturing Technical Committee. Identification of participants will be at the IEMT Conference in July 2004.

Nano - The emergence of nano technologies will require nano manufacturing efforts. Most nano manufacturing will begin with lithography. This will require a liaison with the nano TC. Interested people are being sought. The activity in this area is starting to develop. There are no meetings planned at this date.

For further information, including participation, on any of these sub-committees, please contact Walt Trybula w.trybula@ieee.org and include "TC-EM" in the subject line.

Report on the Workshop on Signal Propagation on Interconnects

The Workshop on Signal Propagation on Interconnects (SPI) is a traditional mid-May event in Europe. Its 8th edition SPI 2004 was held in Heidelberg, Germany. SPI is now an internationally accepted meeting place for experts in the field of signal integrity, interconnect modeling, simulation, testing and measurement on chips, boards, and packages. The SPI Workshop was initiated in Germany in 1997, moved to Italy in 2001, and came back to Germany in 2004. During the years, this Workshop has gained the recognition of IEEE: the 2004 edition was co-sponsored by the Electrical Design, Modeling and Simulation Technical Committee (TC-12) of the Components, Packaging and Manufacturing Technology Society and by the Test Technology Technical Council of the Computer Society.

The aim of this Workshop is to be a forum of exchange on the latest research results in the field of interconnect modeling, simulation and measurement on chips, boards, and packages. The event is also meant to bring together developers and researchers from industry and academia in order to encourage cooperation. A distinctive organizational element of this Workshop is its residential nature, maximizing the interactions among the attendees in a serene atmosphere.

The number of attendees at SPI 2004 reached a new record high of 91 participants from 14 nations of three continents. The participants had the opportunity to attend ten sessions, where 31 oral presentations were delivered. They had also the possibility to meet the authors of 16 posters that stayed displayed for the entire duration of the Workshop.

The keynote speech "Design Challenges of the 90 nm Pentium 4 Processor" was given by Dr. Greg Taylor of Intel Co. The workshop technical program was complemented by three very well attended tutorial courses held on Sunday May 9, before the Workshop started. The first tutorial, entitled "VLSI Interconnect Characterization: Fundamentals, Modeling, and On-Wafer Measurements", was taught by Hartmut Grabinski, Andreas Weisshaar, and Uwe Arz; the second one, entitled "Signal Integrity and Characterization of Lossy Interconnections", was presented by Alina Deutsch, and the third one, named "Characterization and Macromodeling of 3D Interconnects", was given by Stefano Grivet-Talocia. Before presentation at the SPI Workshop, all three tutorials went through the review process of the IEEE Computer Society's Test Technology Educational Program and received high ratings.

The Workshop Proceedings volume, containing a four-page summary of all presentations was distributed to the participants and is available for sale as an IEEE publication (see the web address www.cpmt.org/proceedings/order.html for the order form). The presentation slides of many contributions are available on the Workshop web site. An invited mini-special issue of IEEE Transactions on Advanced Packaging, based on the presentations held during SPI 2004 is also planned.

The Workshop Standing Committee intends to continue this traditional event, and has decided the 9th edition of SPI Workshop will be held in Garmisch-Partenkirchen, Germany, in May 2005. Information on the past SPI Workshops, and details of the venue and program of the next edition are available on the workshop web site: http://www.spi.uni-hannover.de/

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E-mail: Uwe.Arz@PTB.de.

New CPMT Senior Members

Charles Bauer -- Denver
Yoshitaka Fukuoka -- Tokyo
Kirk S Giboney -- Phoenix
Jang-Hi (Jay) Im -- Michigan
Beth Keser -- Phoenix
Kupdapur R. Kini -- Madras
Tien-Yu (Tom) Lee -- Phoenix
Ronald J. Lucas -- Baltimore
Lakshmi N. Ramanathan -- Phoenix
Kannan Ray -- Phoeniz
Thomas G. Reynolds III -- Florida
Jan Vardaman -- Texas 2004
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JOHN W. BALDE wins IEEE CPMT Field Award

Jack (John) Balde, a Senior Consultant of Interconnection Decision Consulting -- Flemington, NJ won the IEEE CPMT Field Award in May 2004.

"For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing."

This IEEE CPMT Award was established in 2002. The award is presented for meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies. The technical field for this award includes all aspects of device and systems packaging including packaging of microelectronics, optoelectronics, RF and wireless and micro-electro-mechanical systems (MEMS).

Prof. Leonard Schaper of the University of Arkansas, a long time colleague of Jack Balde, accepted the award at the June 3rd Society Luncheon held at the ECTC conference. This setting was appropriate for the many years that Jack enriched this conference with his session and panel organization, his questioning of speakers, and his assembling of the right people to address the most important issues facing components and assembly. Prof. Schaper stressed in his acceptance speech that beyond the many individual technical contributions that Jack is given credit, his biggest mark on industry was his natural ability to be the catalyst applied to the looming problems. He would handpick expert speakers that had part of the solution and manufacturers in search of a complete solution and get them to fully engage at some remotely located workshop. He could keep the discussion going at a high pitch without a breakdown in civility. For example, much of the quick progress of surface mount and Multi-chip Modules can be traced to rump sessions guided by Jack Balde.

The following is the text given out at the CPMT luncheon describing Jack Balde's life of contribution:

During his almost 40-year tenure at Bell Telephone Laboratories and Western Electric company in both the Princeton, New Jersey and Winston-Salem, North Carolina facilities, John W. (Jack) Balde contributed significantly in the areas of tantalum film hybrids, under-carpet cable technology, and the introduction of advanced interconnect technology to the Bell System. Under-carpet cable technology later became a major product line for Thomas & Betts Corporation in Memphis, Tennessee.

A pioneering promoter of industry synergy, Mr. Balde spearheaded the globalization of multichip module (MCM) and advanced interconnect technology, most notably through founding the annual Denver MCM Conference in 1990, his Advanced Technology Workshops for the International Microelectronics and Packaging Society (IMAPS), his leadership of the IEEE computer and the IEEE Components, Packaging and Manufacturing Technology (CPMT) Societies' joint Technical Committee on Systems Packaging (TCCP), and numerous publications. As surface mount technology began to emerge, Mr. Balde initiated a multi-company task group effort that was instrumental in the adoption of compliant lead packaging. His work with regard to non-hermetic packaged semiconductor devices resulted in the "use COTS (commercial-off-the-shelf) not custom parts" drives by the U.S. Departments of Defense and Energy; cost savings at Sandia National Laboratories alone are estimated at $1 million per year.

Born on 4 March 1923 in Brooklyn, New York, John W. Balde earned a bachelor of electrical engineering degree from Rensselaer Polytechnic Institute in Troy, New York, in 1943. He joined Western Electric in 1943 and served as research leader at Bell Laboratories and Western Electric from 1946 to 1980. In 1981, he founded Interconnection Decision Consulting in Flemington, New Jersey, where he was a senior consultant at the time of his passing on 8 September 2003.

An IEEE Life Fellow and a Fellow and Life Member of IMAPS, Mr. Balde wrote 130 technical articles, published a number of IEEE and IMAPS books--including the IEEE bestseller Multichip Modules--and held 16 patents. His awards include the IEEE Third Millennium Medal, the International Packaging Consortium's President's Award, the IMAPS Hughes Award for excellence in electronic packaging, and the IMAPS/IEEE Founders joint award for establishing the Denver MCM Conference. Mr. Balde was the chairman of several task forces on chip carriers and corrosion protection of silicon circuits. During his tenure on the TCCP, he led the establishment of international workshops that remain a cornerstone of both the IEEE Computer and IEEE CPMT Societies' technical activities.

Professor C. P. Wong

Prof. C. P. Wong, a Regents' professor at Georgia Tech, is the recipient of the Georgia Tech (GT) 2004 Class of 1934 Distinguished Professor Award (the Highest Honor bestowed by Georgia Institute of Technology to any GT faculty) for sustained contributions to Teaching, Research, and Services. He will be delivering the GT commencement speech and receive a $20,000 prize from the GT Foundation.

C. P. Wong is a Past President and a long time member of the IEEE CPMT Board.

News from Saratov/Penza joint AP03/ED15/MTT17/CPMT21 Chapter

Chapter Officers:
In December 2003 new Chapter Officers were elected:

Chair: Dr. Nikita M. Ryskin, Associate Professor, Dept. of Nonlinear Physics, Saratov State University.
Mail address (office): Moskovskaya str. 155, Saratov 410012, Russia.
Tel. (office): 7 8452 514311
Fax: 7 8452 523864
E-mail: RyskinNM@info.sgu.ru

Vice-Chair: Prof. Michael V. Davidovich, Saratov State University
Mail address (office): Moskovskaya str. 155, Saratov 410012, Russia.
E-mail: DavidovichMV@info.sgu.ru

Secretary: Dr. Artem A. Gubenkov, Associate Professor, Saratov State Technical University.
Mail address (home): Radishcheva str., 74-76, Saratov 41003, Russia.
E-mail: agubenkov@ieee.org

Conference information

The conference "Radio Engineering And Telecommunications" devoted to the 15th anniversary of Radio Engineering Department of Saratov State Technical University (SSTU) took part in April 12–17, 2004 in Saratov. Saratov/Penza Chapter participated in organization of the conference. Professor Vladimir A. Kolomeytsev, IEEE and CPMT Society member and Head of the Radio Engineering Department at SSTU, was the conference Chairman. At the conference, 46 papers were presented by the scientists and engineers from academia and industry in 4 sections: Information receiving, transmission and processing, Telecommunication systems, Electrodynamics and propagation of electromagnetic waves, and Radio engineering and electronics. Among the topics of presentations there were design of digital signal processing systems, finite element simulation of complex resonant and waveguide structures, design of microwave heating systems, etc. The conference proceedings was published and distributed among the participants.

Meeting Reviews

During January — May 2004, our chapter has held four technical meetings:

1). Date: 01/27/2004, 7 members and 18 guests attended.
Two papers have been presented:
1: Virtual cathode oscillators, Speaker: Prof. Dmitry I. Trubetskov, IEEE Member.
2: Influence of two-dimensional effects on dynamics of a varactor, Speaker: Dr. Alexander E. Hramov.

2) Date: 02/24/2004, 12 members and 16 guests attended.
Two papers have been presented:
1: Nonstationary phenomena in a relativistic backward wave oscillator, Speaker: Dr. Nikita M. Ryskin, IEEE member.
2: MAGIC-2D simulation of self modulation and chaos in a relativistic BWO, Speaker: Dr. Vladimir N. Titov.

3) Date: 03/16/2004, 9 members and 17 guests attended.
One paper has been presented: Modern methods of modelling of electromagnetic wave propagation in dielectric waveguides, Speaker: Maxim V. Eliseev.

Our plans for the nearest future are:

- Technical and financial co-sponsorship of the International Conference on Actual Problems of Electron Devices Engineering (APEDE'2004), Saratov, Saratov State Technical University, September 15-16, 2004. More information can be found at http://www.sstu.ru/sstu/win/konf/apede2004.html
- Organizing the 2004 Chapter workshop "Electromagnetics of Microwaves, Submillimeter and Optical Waves" within in the framework of Saratov Fall Meeting 2004, Saratov State University, September 21-24, 2004. More information can be found at: http://optics.sgu.ru/SFM/2004/electrodynamics
- Technical and financial co-sponsorship of the 7th International School on Chaotic Oscillations and Pattern Formation (Chaos-2004), Saratov, October 1-6, 2004. More information: http://cas.ssu.runnet.ru/chaos04.htm
- Technical and financial co-sponsorship of the annual School "Nonlinear Days in Saratov" for postgraduate, undergraduate and pre-college students. Saratov, Russia in October 8-13, 2004.

Submitted by
Dr. Nikita M. Ryskin
Saratov/Penza Chapter Chair
Saratov State University, Dept. of Nonlinear Physics.

Technical Committees Meet at ECTC

MEMs and Sensor Packaging

On Wednesday morning the MEMs & Sensor Packaging TC-17 had a nine member meeting chaired by Eric Jung. One action item was the restarting of the TC Newsletter. One function would be to send out each quarter a list of conferences and meetings that would be of interest to members. There was some discussion of linking the electronic Newsletter to the "MEMS clearing house" Internet site.

In addition to lists of upcoming meetings, it would benefit members if there were reviews of recent meetings and recent articles in the Newsletter. Most engineers miss most meetings and articles in a fast moving field so having brief summaries could be a real service to members.

There was much discussion on whether the ECTC was the right conference for MEMs/ Sensor packaging. The international participation and breadth of companies present was encouraging. In addition ECTC has been the telecommunications opto-electronics packaging meeting for almost 10 years. Since industry is beginning to embrace many MEMs products, this may be the right time to solicit a session at next year's ECTC. However, as always, as the component becomes the system the specialization reaches the point where presentation at any meeting may be difficult.

An annual special IEEE CPMT transaction on MEMs packaging seems possible. Last year the special issue stemmed mostly from papers given at an ASME conference. The TC home page must be redone in the new software. Rolf Aschenbrenner reminded the group that often the solution to MEMs packaging was Wafer level packaging and we should coordinate with the WLP TC for sessions and transactions. This led to a suggestion that we create a list of all MEMs devices that need packaging so we can categorize the packaging to better balance sessions and transactions.

Thermal

On Wednesday (June 2) evening Tony Mak chaired the Thermal Management and Thermal Mechanical Design TC (from left: Goran Matijasevic, Kouchi Zhanag, and Tony Mak). Because of the ongoing activities at the ITherm meeting that was being held about a kilometer away at the Mirage Hotel, attendance was limited to ECTC participants.

It was mentioned that the European thermal conference received 140 papers and ITherm was having a healthy attendance. Another transaction special issue was planned so this TC must pick about 7 papers to represent advances across the Thermal front. The TC home pages are currently on a server computer at Vanderbilt University and a graduate student in thermal studies was recommended as the new web master. A new editor for the TC Newsletter is needed and several suggestions were made.

Editors

Vice President Paul Wesling believed that he would get a turn out of editors if he had the earliest meeting of the conference. His breakfast meeting started at 6:30am. He was right; at least 13 showed up. There was much discussion of the citation index and how our CPMT grade can be improved by: (1) not changing the name of the publications again, (2) turning the articles around faster since only articles sited within 2 years of their publication really count, (3) growing

stronger as the place active engineers in the area want to publish, and (4) presenting authors with a list of previously published articles from which their work flowed so their references would be more complete. Being volunteer-run puts

our transactions in a disadvantage in editing turn around time.

Paul gave a description of the method he would use to start creating "ontologies." These lists of publications in each area of interest to CPMT would allow an author quick access to the original references for each of the chains of technology used in their article.

Avram Bar-Cohen then gave a presentation on converting the existing ISI index rating to one that would have happened had we not changed the transaction title and lost the trail in ISI software.

There was much discussion of the good and bad of manuscript central. Apparently it is possible for a paper reviewer to not realize there are articles waiting for review. It is also possible for editors to not find the right reviewer for a subject based on the way Manuscript Central bins reviewers. Paul agreed to address these issues.

Materials TC

Also on Thursday Morning Rajen Chanchani held the Materials Technical Committee meeting. About 13 members were able to awaken after the previous late night session. Rajen held discussions on lining up papers for next years ECTC and for the annual Packaging Materials conference, this year to be held in Irvine California.

There was also a long animated discussion on the long time it could take to get something published in a CPMT transactions. It was decided that one person should be responsible for following a paper all the way though the system since the problem seems to be once it stops no one is responsible for finding it and getting it moving. Because of this universities have not submitted many papers to CPMT recently. They need publications to prove their worth in academia.

Rajen ended the meeting just before they lit torches and marched down to the editors' meeting.

RF and Wireless TC

Chair Craig Gaw of Free Scale Inc held a breakfast meeting on Thursday morning. Rolf Aschenbrenner, M. Iyer, Tom Reynolds, Len Schaper, Al Puttlitz, Manos Tentzeris, Li Li, and Dave Palmer attended. Craig reported that for this year's ECTC 70 abstracts were submitted which had RF or Wireless content. To make a bigger impact in this growing area we must attract even more papers.

To this end Craig requested that all members of the TC come up with a list of 5 other engineers in this area with a particular subject that they should submit a paper for next year's meeting. Each member should solicit one definite abstract that they submit in addition to many that they encourage. Tom Reynolds has agreed to make a mailing list of all those that have recently submitted RF papers to ECTC so we can encourage the most likely group to continue their support. Craig also will pen a special RF/Wireless ECTC solicitation like we did last year and Dave Palmer will place it in the CPMT Newsletter and Paul Wesling will place it in the Bay Area IEEE regional newsletter. We still need to fill in our key contacts in Companies and countries though our representation is growing it is still spotty.

Themes for next year's sessions were listed and voted on. The dominant ones appeared to be Integrated Passives for RF microsystems and component -like modules with RF fuctionality.

Low K dielectric Panel at ECTC

A panel of experts in the evolution of Low K dielectric spoke on Tuesday Night June 1. After a brief introduction by David McCann of Amkor Tech Ken MacWilliams of Applied Materials spoke.

Ken talked of Black Diamond (SiCOH) that is now 6 years after introduction and proving its worth in manufacture. Ken stressed that the adaptation of low K has more impact on the industry than the switch to copper. However, the road to Low K has proved much more difficult than to Cu and he showed how the roadmap has been pushed out many years with the goal being K-2.9 in the next few years rather than originally thinking about approaching 1.0 at the end of the last century. One of the original problems of the film not being hard enough has been addressed so that hardness of 3GPa is achievable (SiO2 ~ 6 GPa). Because of the success of this CVD deposited film, the spin-on materials are no longer viable in Ken's mind (think SiLK). On the packaging front, Ken saw a good path to Pb-free flip-chip on organic.

Next Tom Ivers of IBM stated that classic scaling was over. Now many materials must change not just improvements in photo patterning. In particular Low-K on die was needed to get the most from either 130nm or 90nm. This need is because the passive power dissipation (conductive lines) has become equal to active power dissipation (transistors). One problem with Black diamond is the brittleness that results in cracking. It was important to limit the size of any initial crack made in processing. One way to do this was to design the edge of the die so that any cracking caused by sawing is minimized. Because of the losses in long conductive lines (1) die size is saturating despite scaling, (2) diagonal routing is being tried despite the much more complex software tools needed in design, and (3) design where most routing is in local islands of functional significance is being revisited.

K. H. Lee of TSMC next set the perspective in reminding everyone that low K was in production for 90nm at TSMC (several panel members nodded in agreement). They use the CVD low-K process. The results show a 10% power reduction compared to the same circuits in the previous best dielectric FSG (fluorinated silica glass). Like any scaling technology there were/are difficulties but none are a "wall". For example, integration with Cu was a challenge. In addition, proving reliability robustness to customers was necessary and is taking time. As an example of package reliability, some chip product of 2 cm on a side is now shipped in BGAs. Stress in vias was one hurdle for TSMC. However, he concedes that being reliable does not mean that some trade off in margins has not taken place. With each new technologies all the margins are re-optimized and the fact that one margin goes down has never meant the net result must be worse.

Mario Bolanes of Texas Instruments directly listed the challenges of this technology to TI. First the adhesion between Low-K and metals (Cu) is not as strong as Al- SiO2/N so that when there is a failure it is often at the metal to low-K interface. For example, probing tips can often damage the interface as can wire bonding which is not adjusted to the smaller windows now available. Flip-chp now often give more CTE mismatch than before. Sawing the wafers requires a more exacting process to make sure no damage is done to the edge protection. In

Mario Bolanes, Tom Ivers, Ivor Barber, K.H.Lee, Ken MacWilliams

general more moisture control is needed during processing with low-K wafers. Ivor Barber of LSI Logic concurred with many of the points made by the IC experts but indicated that none-the-less by the end of next year LSI will only be

using the Cu/Low-K fabrication for their deliverables. He did point out that the porosity of low-K has necessitated certain packaging changes on LSI's part.

David McCann indicated the packaging challenge was to develop materials / processes in packaging that can handle any Low-K solution the wafer industry sends. If separate packaging was needed for each foundry's wafers the expense would drive us back to "high-K". He summarized the low-K problems discussed by the panel:

1. Delamination under low-K because of traditional underfill. Industry must moderate the "Tg" underfill to allow a little more relaxation during temperature cycling.
2. More development of the saw process parameters and with saw blades and optimization of a good wafer seal
3. Do not require backgrinding. This is a WaterLoo for Low-K.
4. Expand wafer before die placement so you don't hit die edges when picking up another die from the tape.
5. keep metal in streets 150 microns from die corners since it gums up the saw

He summarized that Low-K is here but packaging has changed to accommodate. In bumping this means that things are moving from eutectic to high Pb bumps. Also he said don't try Pb-free and low-K in the same system. It is way to soon to make this transition.

In answer to audience questions, the panel predicted that the 65nm technology will start with the same Low-K materials and the same packaging methods perfected for 90nm. There is enormous energy behind Low-K CVD processing so it will be a while before there is another pretender to the throne. However, he cautioned against wringing our hands worrying about the lost world of robust packaging. There are inherent weaknesses in Low-K wafers but every past step of scaling presented apparent weaknesses to the packaging community and slowly they were overcome and soon just accepted as normal business and considered the new definition of "robustness."

CALL FOR PAPERS

Abstract Submission: Please send your title and 300-word abstract, electronically, to wlp@ee.gatech.edu by October 15, 2004. For further info, please visit
www.prc.gatech.edu/nanobiopack

Second International Workshop on March 22-23, 2005
Nano & Bio-Electronic Packaging General Chairs

General Chairs

Prof. Rao Tummala (rao.tummala@ee.gatech.edu), Director, Packaging Research Center - Georgia Institute of Technology

Prof. Z. L. Wang (zhong.wang@mse.gatech.edu), Director, Center for Nanoscience & Nanotechnology - Georgia Institute of Technology

LOCATION
Atlanta, Georgia

PLENARY SESSION
To be announced

TECHNICAL SESSIONS
Nano Package Design
Nano Bio-Packaging
Nano Photonics
Nano Manufacturing
Nano Packaging Materials
Nano Dielectrics
Nano Interconnects and Wiring
NEMS & Fluidics

SEMICON West 2004 International Electronics Manufacturing Technology

July 13 – 16, 2004
San Jose Marriott Hotel

IEMT is an international forum on electronic components and systems manufacturing technology. The conference is a joint effort of SEMI and the IEEE CPMT Society and offers a unique venue for engineers and scientists for original work.

You will Learn: Practical solutions to current production problems, progress on 90 nm process challenges, advanced packaging, latest trends in final manufacturing technology, what's new in advanced packaging/ reliability/ materials/ design for test.

For detailed keynote, program, and event information visit www.semi.org/semiconwest

July 13 Professional Development courses

**Introduction to Flip chip Technology—A User's Guide
**Advanced Packaging Technology Solutions for Today's Leading Edge
**Materials, Processes and Defect Recognition for Hybrids, Microcircuits and MMICs
**Lead-Free Soldering
**Failure Mode Analysis of Flip Chip
**Nano-The Next Technology

July 14 Technical Presentation Sessions

**Assembly with Low-k Dielectrics
**Reliability and Lead-Free
**Green Manufacturing
**Integration Packaging Technology: Stacked Die and 3-D
**Characterization and Modeling
**Emerging Trends in Electronics Manufacturing

July 15 Technical Presentation Sessions

**Advances in Wire Bonding Technology
**Advanced Methods for SoC Testing
**Wafer Level Packaging/Manufacturing
**New Advances in DFM and DFT
**SiP/Sub-System Advance Processes
**MEMS Packaging and Test

INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS

COMPONENTS, PACKAGES AND
MANUFACTURING TECHNOLOGY SOCIETY
Components & RF Program Committee
RF & Wireless Technical Committee

ECTC 2005 – May 31 - June 3
Wyndham Palace Resort & Spa
Lake Buena Vista, FL

The CPMT RF & Wireless Technical Committee in conjunction with the ECTC Components & RF Program Committee encourages you to submit an abstract to ECTC 2005 in the area of RF & microwave component & packaging technology. In particular, RF & microwave papers are solicited for focus sessions on "RF & Microwave Component-Like Modules", as described below. Submissions in other areas of RF & microwave component & packaging technology are encouraged.

"RF & Microwave Component-Like Modules"

Emerging high-performance applications, such as WLAN, RF-optical networks & automotive radar have defined a trend toward flexible & reconfigurable systems. RF & microwave front-end modules are the foundation of these systems & their integration poses a great challenge. These components & modules require better performance, lower cost & increasingly smaller front-end size. Abstracts for papers are solicited in the area of "RF & Microwave Component-like Modules". Topics may include:

- Auto radar, adaptive phased array antennas, filters, baluns, UWB (ultra wide band) modules
- High power & high efficiency RF/microwave power amplifiers & packaging
- Integrated de-coupling for RF/microwave, analog, digital & mixed signal applications
- Embedded passives (inductors, capacitors) for RF/microwave applications & evaluation of their performance in terms of Quality Factor (Q), component value, fabrication challenges & cost
- Antennas integrated in compact RF/microwave modules
- Integrated transceivers for Zigbee, Bluetooth, …

We recommend that the technology used for each submitted paper be compared with other technologies & evaluated in terms of advantages & disadvantages for the specific components

SUBMISSIONS:

Please submit abstracts using the ECTC web site: www.ectc.net by October 15, 2004.
Abstracts should comply with the guidelines outlined at the website.

To have your paper be a part of the RF & microwave oriented sessions & be considered for the above focus session, you must select **"Components & RF" committee as your PRIMARY subcommittee** preference when you submit your abstract at the ECTC web site. Again, to have your paper considered for the RF & microwave components sessions, please do the following:

STEP #1: Submit abstract through the ECTC web site (www.ectc.net) and select **"Components & RF" as PRIMARY subcommittee** preference

STEP #2: Email abstract copy to:
Craig Gaw at c.a.gaw@ieee.org ,
Manos Tentzeris at etentze@ece.gatech.edu , &
Eric Michelson at Eric.Michelson@Vishay.com

To receive updates, send your email contact information to Craig Gaw at c.a.gaw@ieee.org .

EGG 2004+ -- Driving Forces for Future Electronics

September 6-8, 2004, Berlin, Germany

http://egg2004.izm.fraunhofer.de

Electronic products have to be developed with a long-term perspective on technical and environmental issues. In co-operation with IEEE's CPMT the "Electronics Goes Green 2004+" conference will address a wide range of technological and environmental aspects with respect to design, manufacturing, and end-of-life of electronics. As the electronics industry matures, we notice a progressive change in micro-system technology and the upstream business environment. Customers however are looking beyond technology issues, demanding complete solutions in quality and for a good price. Despite such challenges the electronics industry recognizes new tasks which derive from globalization and the need for a more balanced – sustainable – development. Environmental regulations like the European directives WEEE/ RoHS as well as similar activities in some US States or China requires now lead-free technology. In the near future manufacturers will be required to share detailed material content data and provide an eco-profile of a product.

Dr. Robert C. Pfahl , Vice President of Operations, NEMI

The EGG 2004 bringing together leading corporations, research institutions and international organizations to explore tomorrow's developments in electronics design, manufacturing and usage. By addressing environmental and sustainability needs and opportunities, it is a must for product developers, marketers and business leaders. ***See you in Berlin!***

What topics will the conference EGG 2004+ cover?

Legal Compliance to WEEE/ RoHS

- **Lead-free** and Halogen-free technologies – from components to processes
- Design for ReUse, Recycling and Reliability
- Greening the global production network – green procurement, labeling and data management

Leading Edge Technologies

- Eco-Design in practice – corporate concepts
- New materials and technologies – the paradigm of being mobile and low cost
- Green electronic manufacturing – looking beyond technology
- Novel energy supply systems

Looking Ahead

- Technology roadmaps – new approaches with products and prcesses
- Long-term orientation – defining sustainability in the electronics sector
- Emerging legal requirements – the EU directive proposal EuP and REACH

We have to focus our research in micro-lectronics on tech-ology solutions, that maintain a balance of technical excellence as well as economical, social and environmental comatibility over the next decades.

Rolf Aschenbrenner, Technical Vice President CPMT, Deputy Director of Fraunhofer IZM, Berlin

The International congress and exhibition **"Electronics Goes Green 2004+"** is the place were more than 130 experts of international leading electronic companies and research facilities

- from the US, like Hewlett Packard, Texas Instruments, Intel, AMD, NEMI as well as the MIT or University of Wisconsin
- from all over the world, like Siemens, Philips, ST Miccroelectronics, LG Electronics, Sony or Hitachi as well as the University of Tokyo or Fraunhofer Society

will present and discuss latest results from corporate or academic work.

Contact:
Fraunhofer IZM, Berlin, Germany
Email: EGG2004@IZM.FhG.de

4th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics

DOUBLETREE HOTEL LLOYD CENTER – PORTLAND, OREGON, USA

12-15 September 2004

Incorporating POLY, PEP & Adhesives in Electronics

IEEE

IEEE CPMT SOCIETY and the OREGON CPMT CHAPTER

Materials:
Thermosetting/thermoplastic systems; inorganic adhesives; composites; filler materials; isotropic conductive adhesives; anisotropic conductive adhesives; pastes and films; heat seal connectors; thermally conductive adhesives; polymers with adapted refractive index; photosensitive polymers; high temperature materials; PCB materials, polymer thick and thin films, low and high dielectric materials.

Processing and Manufacturing:
Lamination; printing; dispensing; spraying; transfer techniques; injection and transfer molding; potting; adhesion improvement; curing; equipment; statistical process control; economic analyses.

Design and CAD:
Design, modeling, simulation, CAD of materials and systems; thermo-mechanical behavior.

Reliability and Testing:
Degradation mechanisms; adhesion; hermeticity; accelerated testing; humidity and environmental sensitivities; non-destructive testing methods; stress behavior.

Functional Polymers for Microelectronics:
Conductivity of polymers; electronic transport; self-assembly; photoactivity; polymeric materials for molecular electronics.

Applications:
Polymer optical fibers; polymer wave guides; polymer electronic devices; organic displays; polymer batteries; e-paper; flexible electronics.

Environmental Issues:
Ecology and toxicology; life cycle analyses.

The conference provides a unique opportunity for the meeting of polymer developers to meet with polymer users from the electronics and photonics industries.

Tutorials (short courses) on Sunday 12th September

Exhibition: A technical exhibition will be included, with vendor displays of CAD software, materials, process equipment, analytical instruments, services, etc. If you plan to exhibit, please contact Jim Currier at jrc@jrca.com

Event Sponsors: If you wish to sponsor a reception, a luncheon, refreshment breaks, etc, please contact the General Chair at j.e.morris@ieee.org

On-line Paper Presentations: The oral presentations will be posted on-line within 12 hours of delivery, and will be accessible by password. Attendees can access papers they missed, or wish to see again, for a period of one month after the conference. The on-line availability of paper presentations permits remote “attendance” by registrants who cannot attend in person. The Poster Session will run entirely on-line, and offers students world-wide the opportunity to publish at the conference, and to participate in on-line discussion of their work.

Abstracts: Electronic submission only

Dates

Submission of abstracts: **15 June 2004**
Notification of acceptance: **30 June 2004**
Final papers due: **31 July 2004**
Pre-registration: **15 August 2004**
Hotel registration: **31 August 2004**

See www.polytronic2004.org for more information

22nd International Conference on Electrical Contacts

together with

50th IEEE Holm Conference on Electrical Contacts 2004

September 20-24, 2004

Sheraton Hotel, Seattle, U.S.A.

Sponsored By The Components, Packaging, and Manufacturing Technology Society of the IEEE

Web Info http://www.ewh.ieee.org/soc/cpmt/tc1/

PURPOSE: To provide a forum for the presentation and discussion of the latest developments in the field of electric contacts and the application of recent advances in materials and processes in electric, electronic and telecommunications.

FOR WHOM: Practicing designers, engineers, physicists and research scientists – those new to the field and those experienced.

The International Conference on Electrical Contacts is a bi-annual conference hosted by North America, Europe and Asia. The 22nd conference will be held jointly with the 50th IEEE Holm Conference this year in Seattle. This year will include 83 excellent papers authored by some of the outstanding technical people in this field. The international contributors come from USA, China, Japan, United Kingdom, Canada, Germany, Austria, France, Russia, Ukraine, Norway, Singapore, and Switzerland. These papers, as a group, will provide the attendees with up-to-date information on a wide range of subjects that makes this conference so attractive to the practicing engineer. Additionally, the 2004 Holm Conference will have special speakers for the Ragnar Holm Scientific Achievement Award and the Mort Antler Lecturer.

TECHNICAL PAPERS & WORKSHOPS ON THE MOST RECENT WORK ON ELECTRICAL CONTACTS

AUTOMOTIVE

- 42 V Power Net, Series Arc Faults, Lead Free, Environmental Effects, Hot Plugging, Electroplating

COMMUNICATIONS

- High Frequency, High-Speed Data, Telecommunications, Degradation Effects

POWER

- Crimp Terminals, Busbar, Lubricants, Glowing Contacts

CONTACT MATERIALS for Relays, Switches, Power Distribution Equipment

- High Frequency Relays, Ultra Miniature Relays, Reed Relays
- Air and Vacuum Materials, Carbon Fiber, Degradation Mechanisms
- Material Development, Switching Performance

ARC INTERRUPTION

- Circuit Breakers, Vacuum Interrupters, Hybrid Switches, High-Speed Film/Video, Micro-Arcing, Super-Conducting Limiters

MODELING

- 3D FEA, Dielectric Breakdown, Arc Motion, Dynamic Welding, Thermal simulations.

MICRO MACHINED DEVICES

- Micro Switches, MEMS, NanoProbes

IEEE Holm Conference Administrator:
445 Hoes Lane
Piscataway, NJ 08854 USA
Phone: +1 732 562 5350 Fax: +1 732 981 1203
Email: holm2004info@ieee.org

Organizers:

Hungarian & Romanian Joint Chapter

Sponsors:

Ministry of Education Research and Youth

ARIES

Romanian Association for Electronic and Software Industry

Romania Section

Association for Promoting Electronic Technology

The 10th International Symposium for Design and Technology of Electronic Packages

Bucharest, Romania, September 23-26, 2004

You are cordially invited to submit papers to the **International Symposium for Design and Technology of Electronic Packages** (SIITME). The conference is a high scientific event focused on **electronic packaging**, an annual event in Central and Eastern Europe since 1995. In September 23-26, 2004 we will celebrate the **10th jubilee edition** at the University Politehnica of Bucharest, Romania, in conjunction with BINARY 2004, the **7th Romanian Electronic and Software Fair,** September 24-26, organized by ARIES at the Conference Center ROMEXPO, Bucharest, Romania.

The conference is dedicated to debating the role of Universities as Research and Development Centers in today's Industrial and Economical Environment. The conference continues on meeting tradition of specialists in the electronics technology field and it is focused on dissemination of information and scientific results relating to education, research development and manufacturing of electronic packages in the following topics:

- CAE - CAD - CAM for electronic packages and modules; modeling and simulation;
- electromagnetic compatibility and signal integrity analysis; electrostatic discharge;
- printing wiring board - new materials, processing, process simulation and application;
- thermal management, reliability and life time prediction;
- quality management: Q- assurance, Q- control, Q- inspection;
- concurrent engineering and project management on electronic packages;
- electronic components and packaging (SMD, BGA, CSP, FC);
- electronic and optoelectronic modules manufacturing (SMT/PCB/ MCM);
- reliability of new packaging concepts interconnection technology;
- design for environment and environmentally conscious manufacturing;
- clean technologies;
- technology and testing of electronics equipments;
- optical investigation in circuit-test systems;
- fault tolerant digital design;

The conference will include regular technical sessions, plenary sessions and tutorials. Regular sessions will include poster and oral sessions. Prospective authors are invited to submit their manuscripts reporting work, as well as proposals for special sessions, tutorials and areas presented above. The abstract shall be half page of text (200 - 250 words), using no smaller than 12-point type font. They will receive manuscript format and layout instructions for paper submission. Please use E-mail to siitme2004@cetti.ro for any correspondence, submission of abstract and paper.

Planned joint Events:

- IEEE - CPMT Hungary - Romanian Joint Chapter Meeting
- IEEE- CPMT Student Branch Meeting

Organized by:

- **Hungarian & Romanian Joint Chapter**
- Politehnica" University of Bucharest
- Center of Technological Electronics and Interconnection Techniques
- IEEE-CPMT Student Branch Chapter of "Politehnica" University of Bucharest

Chairman: Prof. Paul Mugur Svasta , Ph.D, UPB-CETTI, Romania

Important dates:

Submission of Abstracts	**May 7, 2004**
Notification of Acceptance	**June 1, 2004**
Submission of Manuscripts	**September 3 , 2004**

Organizing Secretariat SIITME 2004:

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Future Directions in IC and Package Design Workshop, FDIP'04

sponsored by:

organized by:

CPMT Technical Committee on Electrical Design, Modeling, and Simulation (TC-EDMS)

October 24, 2004

Portland, Oregon

The goal of this workshop is to provide a forum to address the future needs associated with the design of next generation ICs and packages. The Technical Program Committee will solicit invited presentations from experts in the university and industrial communities. The workshop will be held in conjunction with the **IEEE Topical Meeting on Electrical Performance of Electronic Packaging** in order to enhance this conference with presentations that give directions for future requirements and developments in the area of electrical analysis and design. The workshop will foster active participation and discussions from all the speakers and attendees during the meeting.

The following talks are planned:

- ***Gigascale Integration – Design Challenges and Opportunities, Shekhar Borkar, Intel Corporation***
- ***Emerging Trends in High-Speed Interconnects and Packaging Engineering, Sergio Camerlo, Cisco Systems***
- ***Analog RF CMOS and Optical Design Techniques for 10+ Gbps Datacom, Martin Schmatz, IBM Corporation***
- ***Power Distribution: Status and Challenges, Madhavan Swaminathan, Georgia Institute of Technology***
- ***Signal Integrity Modeling and Simulation for IC/Package Co-Design, Ching-Chao Huang, Optimal Corporation***
- ***Current and Future Directions in Simulator Development, Sani Nassif and Jaijeet Roychowdhury from IBM Corporation and University of Minnesota***

Workshop Chairs:

Alina Deutsch
IBM Watson Research Center

Madhavan Swaminathan
Georgia Institute of Technology

Technical Program Committee:

Tawfik Arabi – Intel Oregon
Andreas Cangellaris - University of Illinois
Moises Cases - IBM Austin
Chi-Shih Chang – Consultant
Paul Franzon - North Carolina State University
Hartmut Grabinski - University of Hanover, Germany
Harold Hosack - Semiconductor Res. Corp.
Lewis Terman – IBM Watson Research
Mahadevan Iyer - IME, Singapore
George Katopis - IBM Poughkeepsie
Istvan Novak - SUN
Toshio Sudo - Toshiba, Japan
Gregory Taylor - Intel Oregon
John Prince – University of Arizona
Ryszard Vogel - Nokia, Finland

Workshop will be held at the Hilton Portland and Executive Tower, 921 SW Sixth Ave., Portland, OR 97204, 503-226-1611. The hotel is holding a block of rooms at $99.00 (no tax). Reservations must be made by September 30, 2004 in order to guarantee this rate. Be sure to mention that you are attending the EPEP conference in order to secure this rate. For more information on the hotel go to http://www.portland.hilton.com

Additional information may be obtained from the workshop chairs:

Alina Deutsch
deutsch@ieee.org
phone: (914) 945-2858, fax: (914)945-2141

Madhavan Swaminathan
madhavan.swaminathan@ece.gatech.edu
phone: (404) 894-3340

Attendees interested in the workshop will be charged a $60.0 fee that will cover afternoon refreshments, digest of abstracts, and posting of the foils on the CPMT Society TC-EDMS web site. All attendees must register by September 13, 2004 using the EPEP'04 website at www.epep.org in order to assure that the workshop is being held. On-site registrants will be admitted depending on availability of seating.

13th Topical Meeting on Electrical Performance of Electronic Packaging

EPEP 2004

October 25-27, 2004
Portland, Oregon

Sponsors

The IEEE Components, Packaging and Manufacturing Technology Society

IEEE Microwave Theory and Techniques Society

Call for Papers

The **general subject of the meeting** is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. Authors are invited to submit papers describing new technical contributions in the areas broadly covered below:

- Current and future issues related to on-chip interconnections
- Router friendly models and modeling tools: accuracy & efficiency
- Modeling and design of high speed digital IO circuits: signal propagation and reception
- On-chip power delivery and regulation
- Advances in modeling core switching noise, and design of novel solutions
- On-chip measurement techniques
- Package analysis, including numerical methods
- Electromagnetic analysis tools
- Advances in transmission-line techniques
- Power distribution and package resonance
- Long distance propagation in large switching complexes
- Switching noise in multi-layered systems
- Optoelectronic packaging; structure and system applications
- Electrical issues in MEMS packaging
- New and innovative interconnect packaging structures and their electrical performance
- RF/microwave packaging structures and their electrical performance
- MMIC modules and high density packaging
- Experimental characterization techniques
- EMC/EMI sources & effects
- Prediction/measurement of radiation from on-chip sources, interconnect structures and packages
- Electrical design implications for low cost, high volume packaging
- Packaging concerns for wireless communication: design and modeling
- Packaging solutions for one chip radios: design and modeling
- Performance of packaging for automotive radar systems

Conference Co-chairs: Tawfik Arabi, Intel Corp.; Robert W. Jackson, University of Massachusetts

Conference Web Page: Detailed and updated information can be found at http://www.epep.org

Paper Submission: Detailed information for authors can be found on the conference web page. Electronic submissions of no more than four pages must be received no later than **July 10, 2004.**

Student Paper Award: Two awards will be presented to the best two papers submitted by students

Short Courses/Workshops: On Sunday, October 24, 2004, a workshop entitled "Future Directions in Packaging" will be presented and short courses/tutorials will be offered.

Institute of Electrical and Electronic Engineers, Inc.

Phoenix Section

Components, Packages, and Manufacturing Technology Society
&
Waves and Devices Chapters

PRESENT AN ALL DAY WORKSHOP ON

Devices and Packaging For Wireless Communications

Date:	Friday, November 12, 2004	**Time:**	7:00 A.M. - 6:00 P.M.
Location:	Arizona State University, Tempe, Arizona – Arizona Room - Memorial Union		

ABSTRACT

This one-day workshop will emphasize RF semiconductor device and packaging technologies to meet the needs of next generation wireless applications. Participants will hear from leading contributors in industry, academia and national labs. Current status and future directions of wireless communications will be reviewed. State-of-the-art silicon/alternative technologies, system architectures, RF characterization/modeling, packaging and applications will be addressed. Panel discussion will bring a closure to the day's workshop. Vendors in the entire supply chain of chip, package, and board will display their products and services.

TOPICS

- Keynote Presentation – Wireless Communication: Current and Future
- System Architecture and Design Challenges
- Si Technologies for Wireless Communication
- Alternate and Novel technologies
- Characterization and Modeling
- Wireless Communication Standards
- Wireless Applications
- RF Modules
- Low Cost RF Packaging
- High Power RF Packaging
- Wafer Scale Packaging
- Board and System Level Packaging
- Reliability of RF Packages
- Vision of Wireless Communication in Future
- Panel Discussion: Future Market Opportunities in Wireless Communications

- Vendor Display of Products and Services

For General Information
http://www.ieee.org/phoenix

Vasu Atluri	(480) 554-0360	Steve Goodnick	(480) 965-6410	Mali Mahalingam	(480) 413-5368
Rao Bonda	(480) 413-6121	Olin Hartin	(480) 413-3831	Sujit Sharan	(480) 552-8073
Chuck Weitzel	(480) 413-5906	Dragan Zupac	(480) 413-3964		

For Workshop Registration Forms
http://www.ieee.org/phoenixcpmt
Victor Prokofiev
(480) 552-0228

For Vendor Registration Forms
http://www.eas.asu.edu/~wadweb/
Ellen Lan
(480) 413-4128

6th International Conference on Electronics Materials and Packaging (EMAP 2004)
5-7 December 2004, Penang, Malaysia

FIRST ANNOUNCEMENT AND CALL FOR PAPERS

About EMAP

The 6th Electronics Material and Packaging Conference (EMAP 2004) is an international event organized by the School of Mechanical Engineering, Universiti Sains Malaysia, and IEEE CPMT Chapter with joint technical co-sponsorship from CPMT society of IEEE.

EMAP 2004 will feature short courses, technical sessions, and exhibition. It aims to provide good coverage of developments in all areas of electronics materials and packaging, from design to manufacturing and operation. EMAP 2004 is a major forum, providing opportunities to network and meet leading experts in addition to exchange of up to date knowledge in the field. Since 1999, EMAP has gained a reputation as a premier electronics materials and packaging conference in Asia Pacific where the bulk of the packaging activities are taking place.

Conference Topics

The topics of interests are specific to micro systems/MEMS, their packaging, electronics materials and reliability issues. Extended abstracts are being sought from, but not limited to, the following areas:

- **Automotive Electronics**
- **Chip-Scale Packaging/Flip Chip**
- **Electrical Modeling & Signal Integrity**
- **Green Materials**
- **High Density Displays**
- **High Density Packaging**
- **Interconnection Technologies**
- **Low Cost Packaging Methods**
- **Manufacturing Technologies**
- **Mechanical Modeling and Structural Integrity**
- **MEMS Packaging and Applications**
- **Microelectronic Materials & Processes**
- **No Flow Underfilling Process**
- **Optoelectronics/Photonics**
- **Polymer Materials & Microelectronic Applications**
- **Printed Wiring and Flex Boards**
- **Quality & Reliability**
- **Thermal Design, Analysis, and Characterization**
- **Electronic Inspection**
- **Thick & Thin Film Materials**
- **Wafer Scale Packaging**
- **Wireless Sensor Packaging & Applications**
- **Vibration on Electronic Devices**

Important Dates:

Submission of Abstract	**31 May 2004**
Notification of Acceptance	**15 July 2004**
Submission of Manuscript	**31 August 2004**

Extended Abstract and Paper Submission

Extended abstracts are invited to describe original and unpublished work. The extended abstract should be about 500 words stating clearly the purpose, methodology, results, and conclusions of the work. Key references to prior publications and how the work enhances the existing knowledge should be included in the extended abstract. Authors are requested to designate appropriate areas for the purpose of abstract review. All submissions must be in English and should be made via electronic mail to **abstract_emap2004@eng.usm.my**. The required file format is either MS Word or Adobe Acrobat© PDF with only one single file for each submission.

The abstracts must be received by 31 May 2004. Authors are requested to include their affiliation, mailing address, telephone and fax numbers, and e-mail address. Authors will be notified of paper acceptance and instruction for preparing final papers by 15 July 2004. The final manuscript for publication in the conference proceedings is due by 31 August 2004.

Short Courses:

The conference program includes short courses, which will be conducted by leading experts in the field. Details will be provided in the conference website and available in subsequent mailings.

Exhibition:

A tabletop exhibition from suppliers of materials, equipment, components, software, and service providers of electronics industries will be held at the venue of the conference

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Conference Information and Contacts: **Website:** http://www.eng.usm.my/mekanik/emap2004.html

General Chair	Technical Program Chairs	
Dr. Zaidi Mohd Ripin mezaidi@eng.usm.my Tel: 60-4-593-7788 (ext: 6300) Fax: 60-4-594-1025	**Prof. K. N. Seetharamu** knramu@eng.usm.my Tel: 60-4-593-7788 (ext: 6309) Fax: 60-4-594-1025	**Mr. Teck Joo Goh** teck.joo.goh@intel.com Tel: 60-4-253-1236 Fax: 60-4-253-1028
Secretariat		
School of Mechanical Engineering, Engineering Campus, Universiti Sains Malaysia **14300 Nibong Tebal, Seberang Perai Selatan, Pulau Pinang** jaa@eng.usm.my Tel: 60-4-593 7788 (ext. 6301) Fax: 60-4-594 1025		

6th Electronics Packaging Technology Conference (EPTC 2004)

8 - 10 December 2004, Pan Pacific Hotel, Singapore

CALL FOR PAPERS

About EPTC

The 6th Electronics Packaging Technology Conference (EPTC 2004) is an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter with joint technical co-sponsorship from the CPMT Society of IEEE and IMAPS.

EPTC 2004 will feature technical sessions, short courses and exhibition. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Inaugurated in 1997, the EPTC has gained a reputation as a premier electronics packaging conference in South East Asia where the bulk of the world's packaging activities are taking place. Since 2002, it has been held annually in December, due to the growth in the number, scope and quality of its presentations.

Conference Topics

You are invited to submit an abstract presenting new development in the following categories:

- Advanced Packaging: Single chip and multi chip packaging, wafer level thinning, bumping, packaging and 3D integration, Embedded Passives & actives on substrates, high power, high frequency / RF packaging, SiP and other system integration technologies
- Interconnection Technologies: gold and copper wire bonding and flip chip (eutectic/lead-free solders) on standard and copper low k wafers, solder replacement flip chip (ICP, ACP, ACF, NCP), under bump metallurgy, microvia and build-up technologies, nano interconnects.
- Manufacturing Technologies: Process characterization, yield improvement, cost and cycle time reduction, environmental improvements, Statistical process control.
- Materials & Processes: Advancements in adhesives, encapsulants, underfills, solder alloys, halogen-free materials, dielectrics, ceramics, composites, thin film processes on laminates, nano-materials and processes for packaging.
- MEMS Packaging: Packaging solutions for Inertial MEMS - Pressure sensors, actuators, microrelays Bio-MEMS, RF MEMS – Resonators, Switches and Optical MEMS- Switches, Crossconnects etc
- Electrical Modeling & Signal Integrity: Modeling simulation & measurement for coupling, reflection & switching noise, EMI/EMC analysis on package & subsystems, Time & frequency domain measurements for advanced modules.
- Thermal Characterization & Cooling solutions: Modeling & simulation methodology for thermal characterization of advanced packaging, modules & systems. Novel thermal management solutions. Enhanced air & liquid cooling techniques.
- Mechanical Modeling & Structural Integrity: Structural analysis, modeling and simulation of modules, sub-assemblies and systems. Failure mechanics and damage modeling. Thermo-mechanics. Multi-physics modeling. Moisture effects. Impact and dynamic effects. Experimental techniques and model validation. Numerical methods. Design optimization..
- Optoelectronics: Passive components (waveguides, splitters etc), Photonic interconnects, Design, Modeling & Measurements for Gb/sec & Tb/sec modules and Optical backplanes.
- Quality & Reliability: Component, board and system level reliability assessment, failure analysis, interfacial adhesion, accelerated testing and models, component and systems

Important Dates

31 July 2004	**Submission of abstract**
31 August 2004	**Notification of Acceptance**
9 October 2004	**Submission of manuscript**

Extended Abstract and Paper Submission

Extended abstracts are solicited to describe original and unpublished work. The abstract should be about 500 words and it must clearly state the purpose, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications and how the work enhances existing knowledge should be included in the abstract as well.

Authors must designate two appropriate categories for abstract review. All submissions must be in English and should be made either online at www.eptc-ieee.net or via electronic mail to abstract@eptc-ieee.net . The required file format is **Adobe Acrobat® PDF** with only one single pdf file for each submission. Please limit the file size to a maximum of 2MB.

The abstracts must be received by **31 July 2004**. Authors must include their affiliation, mailing address, telephone and fax numbers, and email address. Authors will be notified of paper acceptance and publication instruction by 31 August 2004. The final manuscript for publication in the conference proceedings is due by 9 October 2004.

Outstanding Technical Papers

The conference proceedings will be an official IEEE publication. Top quality papers will be submitted to IEEE/CPMT Transactions to be considered for publication. Author(s) of Outstanding Technical Paper(s) will receive an award at the next conference.

Short Courses

The conference program includes full-day short courses that will be conducted by leading experts in the field. Details will be updated in the conference website and available in subsequent mailings.

Exhibition

A tabletop exhibition featuring suppliers of materials, equipment, components, software and service providers of the microelectronics and electronic assembly industries will be held during the conference.

For latest conference information & contacts: Website: http://www.eptc-ieee.net

General Chair	**Technical Program Chairs**		**Secretariat**
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Call for Papers

The 7th ***VLSI PACKAGING WORKSHOP of JAPAN***

Nov. 30 - Dec. 2, 2004

Kyoto, Japan

Sponsored by the IEEE CPMT Society and National Institute for Standards and Technology

The VLSI Packaging Workshop of Japan has been held every other year since 1992 in the best season of Kyoto, the ancient capital of Japan, and it has become a well-known international workshop for advanced packaging technologies. The committee strongly encourages you to attend this workshop and participate in the discussion, in order to understand technology trends and find the proper target for technology development. Bring your latest research results and share with the participants who are experts from industry and the grove of Academe, and discuss with them. Anybody contributing to human progress through electronics is very welcome at this workshop. The following areas of technology are primarily of interest to the participants:

+ Advanced Fine Pitch Packaging
+ 3D Packaging & COC (Chip on Chip)
+ Micro Bumping Technology
+ Laminated Materials & Processing
+ RF Components & Modules
+ Integrated Passives
+ Packaging for Optoelectronics
+ Failure Mechanisms & Reliability Improvement
+ Electrical Performance & Thermal Management
+ Wafer Level CSP
+ Manufacturing Technology
+ Pb Free Interconnections
+ Materials for High Speed Application & Wafer Process
+ RFID tags
+ System in Package (SIP)
+ MEMS Packaging Technologies
+ Assembly and Packaging Challenges for Cu/Low-k Chips
+ Wafer Level Burn-in

The official language of this workshop is English. 30 minutes is allocated for each presentation, and it should include 5 - 10 minutes for Q&A. Authors who give outstanding papers will receive official recommendations for paper submission to the IEEE Transactions by the Japan Chapter and the Workshop Committee. This workshop will be held at Kyoto Research Park where the 6th Workshop was held in 2002.

Submission of abstracts:

Those who wish to contribute to the workshop should send a two-page summary of their paper (including figures) to the Program Chair **by May 28th, 2004**. The title of the paper as well as the names and affiliations of all authors must appear on the summary. If the paper is accepted, the summary shall be written to fit in a four-page format for the workshop's Proceedings **by September 3rd, 2004**. Notification of acceptance will be given **by July 9th, 2004**.

Program Chair:

Michitaka Kimura, Renesas Technology Corp.
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Email: mkohno@dow.com

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George Harman, NIST

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