



Announcement and Call for Papers
The Sixth IEEE CPMT Symposium on High Density Microsystem Design and Packaging and Component Failure Analysis (HDP'04)

Date: June 30 – July 3, 2004

Venue: Bao Long Hotel, No 180, Ye Xian Road

Co-sponsored by

Shanghai Science and Technology Commission, Shanghai Government

IEEE CPMT Society, USA

DaimlerChrysler SIM TECH, Shanghai, China.

Chalmers University of Technology, Sweden

IVF Industrial Research and Development Corporation, Sweden

IEEE CPMT Scandinavian Chapter

IEEE CPMT China Chapter

Shanghai Institute of Microsystems and Information Technology, China

Jiaotong University, China

SMIT Centre, Shanghai University, China

Microsystem manufacturing, assembly and packaging technology is playing a key technology for the progress of the microsystems and microelectronics industry in the world. China is not an exception. Therefore, many multi-national companies are establishing new facilities in China for expanding their global business and interest. Following the successful previous conferences, we are proud to announce the sixth International IEEE CPMT Symposium on High Density Microsystem Design and Packaging and Component Failure Analysis in Electronics Manufacturing (HDP'04).

Scope for the Symposium: The Symposium will cover the following areas and subjects:

- High density design and packaging including micro- and nanosystems, microelectronics and opto-electronics design and packaging, CSP, BGA, Flip-chip, Chip on Board, Surface Mount Technology and other novel emerging technology
- High density substrate including integrated passives and active devices
- MEMS and MOEMS design, packaging and assembly
- Microsystems manufacturing issues including cleaning issues, quality control, logistics, repair, process optimization, statistic process controls, ISO compliance, tooling or equipment, early manufacturing involvement initiatives and yield and test innovations used to enhance manufacturing processes or products related to high density substrates, single chip and multichip packaging, chip bumping and integrated component technologies
- Component failure analysis techniques including non-destructive X-ray, ultrasonic microscopy, IR-microscopy etc
- Simulation and modelling for packaging and microsystems and microelectronics manufacturing processes
- Thermal management
- Environmental design and materials development including life cycle analysis and end of life strategy etc
- Cost reengineering, improvements and analysis for electronics packaging processes and products

Documentation: The documentation from the Symposium will be published in a proceeding with CD ROM with a full length papers (max 12 A4 pages) in English.

Journal publication: In addition, high quality papers will be selected for consideration to be published as special editions of the IEEE CPMT Transactions.

Languages: English will be used.

You are welcome to submit an abstract with max 300 words that cover the topic, experimental approach, results and conclusions for the paper by April 30, 2004. Notification of abstracts will be made by May 10, 2004, Final paper is requested by May 25, 2004.

We are also interested to have exhibitors from materials, equipment suppliers to exhibit their products.

For further information please contact Professor Johan Liu at johan.liu@me.chalmers.se or Dr Jiang Hua Zhang at jhzhang@mail.shu.edu.cn.