

SEMICON[®]
West2004



**SEMI[®] Technology Symposium: International Electronics
Manufacturing Technology (STS: IEMT)**

Tuesday, July 13–Friday, July 16, 2004
San Jose Marriott Hotel

Executive Committee:

Martin Goetz, IBM, **General Conference Chair**
Thomas S. Tarter, Neophotonics, **Program Chair**
Brian Toleno, Henkel Technologies, **Vice Program Chair**

Description:

The STS: IEMT is an international forum on electronic components and systems manufacturing technology. The conference is a joint effort of SEMI and the IEEE CPMT society and offers a unique venue for engineers and scientists to present and publish their original work. The conference features technical papers on research, development, and applications of manufacturing technology for electronic components, assemblies, and systems selected by a committee of experts. Individual sessions will deal with reliability, green manufacturing, MEMS packaging, design for manufacturing, the effects of using low-k materials, wafer level and stacked die packaging and testing.

You will learn:

- Practical solutions to current production problems
- How to meet the process challenges of the 90 nm node
- The latest trends in final manufacturing technology from recognized experts
- What is new in advanced packaging, reliability, materials, and design for test

Who should attend:

- Process, equipment and materials engineers associated with assembly, packaging and test
- Customers, process and product development managers

SEMICON[®] West 2004—Where People Define Tomorrow

SEMICON West gives you free access to the full spectrum of quality suppliers (more than 1,500 companies), exposure to a thought-provoking Technology Innovation Showcase (TIS) highlighting emerging technology breakthroughs, and FREE entrance to hear “The Voices of the Industry”—SEMICON West Keynote Addresses. Don’t miss the largest and most comprehensive industry event of the year. For detailed keynote, program, and event information visit www.semi.org/semiconwest.

Co-produced by IEEE's CPMT



For more information or to register, visit: www.semi.org/semiconwest/stsiemt

STS: IEMT Professional Development Courses

Introduction to Flip Chip Technology—A User's Guide

Description:

Dev Gupta, Ph.D., APSTL presents both an overview and a detailed look at flip chip technology by presenting the application, design, reliability, infrastructure, materials and processing aspects of various flip chip technologies.

You will learn:

- The needs of the user community—the primary focus of this course
- Motivations, niche technologies, emerging WLPs, electrical performance and stress/thermal aspects that will be defined
- The outline of the assembly process, the typical qualification process for high and medium reliability applications, the details of key bump/interconnect structures, substrate design, failure mechanisms and diagnostics, package and system design using mixed technologies, infrastructure and future options

Who should attend:

- Product Development Engineers
- Managers
- R&D Engineers
- Scientists

Advanced Packaging Technology Solutions for Today's Leading Edge Microelectronics

Description:

This presentation will explore advanced packaging solutions for next generation microelectronics by looking at three key applications areas that are driving the packaging and interconnection developments. We will look at technology trends, market segments, application requirements, packaging approaches and electronic material developments.

You will learn:

The strong historical background of the microelectronics industry; and show the audience where packaging and interconnection are today and where they are going.

Who should attend:

- New entrants into the packaging and interconnection field
- Suppliers of materials, components and equipment to the microelectronics fabrication and assembly industry
- Users of electronics

Materials, Processes and Defect Recognition for Hybrids, Microcircuits and RF/MMIC Modules

Description:

The intent of this course is to give the student a good overview of the materials and processes needed to assemble Hybrids, Microcircuits and RF/MMIC Modules. Taught by Tom Green, National Training Center for Microelectronics, the emphasis is on understanding defects in relationship to the process and in conjunction with customer expectations and end use environment.

You will learn:

- Advance your understanding of the basic materials and processing steps used in the assembly of Hybrids, Microcircuits and RF/MMIC Modules
- Know what you're looking at and what constitutes a "reject" in the production flow along with the technical rationale to support the decision
- Be able to explain to others visual defects that result from the basic manufacturing processes, i.e. wire-bond, component attach, thick and thin film processing
- Understand the industry "lessons learned" and tap into the corporate knowledge base

Who should attend:

- A must for design and process engineers, manufacturing engineers and senior technicians looking to broaden their understanding of the materials and processes used in manufacturing and the associated visual defects that result from out of control conditions
- Newly assigned engineers, management and QA personnel looking to learn the basic terminology and key concepts vital to manufacturing flow

Registration for STS: IEMT Professional Development Courses:

Pre-registration for Members by June 25: \$350

Pre-registration for Non-members by June 25: \$450

Registration for Member or Non-members after June 25 or onsite: \$600

Student rate: \$100

Special Discount: Sign up for two courses and receive a 25% discount

To register, visit: www.semi.org/semiconwest/stsiemt

STS: IEMT Professional Development Courses

Lead-Free Soldering—Metallurgical Fundamentals, Reflow Applications, and Challenges

Description:

This course is designed to provide a thorough understanding of the fundamental design considerations of lead-free alloys, with an emphasis on metallurgical properties analysis. The course attendees will also receive the textbook, "Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive-Adhesive Materials" authored by John Lau, C.P. Wong, Ning Cheng Lee (course instructor), and Ricky Lee.

You will learn:

- Understand the design consideration of lead-free alloys
- Comprehend the metallurgical aspects of lead-free alloys
- Review the options of lead-free replacement
- Realize the strengths and limitations of each option
- Recognize the compatibility with reflow applications
- Analyze the challenges in implementing lead-free soldering
- Understand the defect mechanisms encountered at lead-free soldering
- Determine the proper move toward lead-free soldering

Who should attend:

- Engineers, supervisors, managers, directors, safety staff, scientists, technologists, and technicians who are involved in implementing lead-free solder selection and soldering process work

Failure Mode Analysis of Flip Chip in Package and Board Assemblies

Description:

Daniel F. Baldwin, Ph.D., Georgia Institute of Technology teaches this course on reliability test procedures and common failure modes that occur in advanced area array packages and board assemblies.

You will learn:

- Reliability test standards
- Destructive and non-destructive failure analysis
- Process defects and effects on failure and reliability
- Reliability modeling
- Failure modes and reliability implications
- Design factors
- In situ stress analysis of flip chip assemblies

Who should attend:

- Managers and engineers associated with low-cost surface mount assembly and low-cost electronics packaging

Nano—The Next Technology

Description:

Deb Newberry and Walt Trybula provide an explanation of the basics of nano-technology. The purpose is to give the attendees an overview of potential applications and an understanding of some of the complexities of developing nano-technology products.

You will learn:

- Introduction to nano
- An overview of nano-bio
- Specific benefits
- Business requirements
- Packaging potential
- Economics and world competition
- The future and challenges

Who should attend:

- People who desire a better understanding of the developing field of nano-technology
- People who need to become involved in business dealing with nano-technology

STS: IEMT and Henkel Presents:

Future Trends in Semiconductor Packaging

Since the birth of semiconductor packaging, the industry has seen many changes and shifts in technology. These shifts have resulted in ever increasing sophistication in materials and processes, which in turn drives the research and development groups to innovate. Keeping track of the many advances and new technologies is a daunting task. The purpose of this seminar is to bring together industry leaders such as Intel, Amkor, Henkel Technologies, Sun, Asymtek and Techsearch International to highlight the emerging challenges and how our industry as a whole is addressing this host of issues:

- Low-k devices/Cu interconnect
- Lead-free material set
- Need for "green" packages
- 3D architectures for packaging
- Thermal management
- High speed dispensing

Following the seminar there will be a networking social where you can talk with the speakers and fellow attendees.

Registration:

Pre-registration for Members by June 25: \$25
 Pre-registration for Non-members by June 25: \$25
 Registration for Member or Non-members after June 25 or onsite: \$25
 To register, visit: www.semi.org/semiconwest/stsiemt

Sponsored by:



Technologies

Keynote Session: "Macro, Micro, Nano, and Beyond"

Walt Trybula, International SEMATECH

Chair: Martin Goetz, IBM

See how the semiconductor industry will transition from micro to nanotechnology. Hear an expert describe the complexities involved in implementing the technology. Learn about the exciting possibilities presented by these new products and applications and how they will change our lives.

Biography:

Walt Trybula is a senior fellow in the Lithography Division of International SEMATECH. He is responsible for developing strategies for future technologies, tracking emerging technologies, and evaluating the impact of new technology on the lithography segment of the semiconductor industry.

Session 201: Assembly with Low-k Dielectrics

Chair: Jan Vardaman, TechSearch International, Inc.

Description:

The introduction of low-k dielectric materials on the inner layers of the die requires changes in package assembly materials and processes for both flip chip and wire bond. This session focuses on the development and characterization of new packaging methods needed to accommodate critical device changes.

Papers:

Featured Paper: Flip Chip Underfill Technology Development for Next Generation Silicon Technologies
Sarathy Rajagopalan, LSI Logic

Featured Paper: Bonding Copper Low-k Die with Bond Pads over Active Circuitry (Pads on I/O)
Q.H. Low, LSI Logic Corporation

Considerations for Using Low Dielectric Constant Material as Re-passivation Layer on 300 mm Wafer Bump Process and Manufacturing Benefits of Flip Chip Package
Rick Yu, Advanced Semiconductor Engineering, Inc.

Toward Determining Optimal Mechanical Properties in Adhesives for Flip Chip and Wire Bonded Low-k Die
George Carson, Henkel Loctite

Gold Wire bonding on Low-k Material a New Challenge for Interconnection Technology
Ralph Binner, ESEC AP

Session 202: Reliability and Lead-Free

Chairs: Reza Ghaffarian, JPL and Annette Teng Cheung, Corwil Technology

Description:

Reliability issues for advanced flip chip devices, BGA/CSP/WLP packages and PCB assemblies become more critical as the industry moves to lead-free solder. Presentations in this session describe how these new reliability issues have been addressed by APSTL, Intel, ASE and Flextronics.

Papers:

Evaluation of a Low-Cost Column Bump Technology for Fine Pitch Flip Chip and WLP
Dev Gupta, APSTL

High Reliability Solutions for Center Bond Lead mBGA Packages
Henry Liu, Intel Corp.

Correlation Between Power Cycling and Thermal Cycling Fatigue Reliabilities of Chip-Scale Packages
Tong Hong Wang, ASE, Inc.

Lead-Free Solder Flip Chips on FR-4 Substrates with Different PCB Surface Finishes and Underfills
Dongkai Shanguan, Ph.D., Flextronics

Session 203: Green Manufacturing

Chairs: Luu Nguyen, National Semiconductor and Ning-Cheng Lee, Indium Corporation of America

Description:

By July 1, 2006 the majority of electronic products sold in Europe must be lead-free. In this session learn how companies are preparing to meet this deadline. Presentations address the issues related to implementing the changes required for the processing and assembly of lead-free components.

Papers:

Novel Technology to Prevent Component Overheating During Processing
Alan Rae, Cookson Electronics Inc.

PPF (Pre-Plated Frame) Technology Using Pure Sn and Sn-Bi Electro-Deposition on Alloy 42 Lead Frame for Semiconductor Package Corresponding to Lead-Free Movement
J.D. Kim, Precision Instruments R&D Center

Effect of SAC Composition on Soldering Performance
Ning-Cheng Lee, Indium Corporation of America

Comparative Study of the Wetting Dynamics of Tin Lead Eutectic and Tin Silver Copper Lead-Free Solder Alloys on Various PCB Surface Finishes
Daniel F. Baldwin, Ph.D., Georgia Institute of Technology

**Session 204:
Integration Packaging
Technology: Stacked Die and
3-D Packaging**

Chairs: Joe Lippincott, ESEC and Marc Papageorge, Semiconductor Outsourcing Solutions

Description:
Stacked die and 3-D packaging integrate a variety of technologies in a single package to provide maximum performance from minimal space. The packaging engineer can significantly reduce the time to market by combining known processes. This session will help develop a good understanding of the dynamics of the assembly process, which is vital to the success of the integration when to use 3-D packaging.

Papers:

Featured Paper: 3-D Packaging: Where All Technologies Come Together
Marcos Karnezos, ChipPAC Inc.

Thin Die Bonding Techniques
Jonathan Medding, ESEC SA

**Wafer Sawing Process
Characterization for Stacked Thin Die (75 micron and below)
Applications**
Chetan Paydenkar, National Semiconductor Corporation

Die Attach Quality Control of 3-D Stacked Dies
Marta Rencz, Budapest University of Technology and Economics

**Advanced Wire Bond Looping
Technology for Emerging Packages**
Bob Chylak, Kulicke & Soffa

The Development of a Novel Stacked Package: Package in Package
Flynn Carson, ChipPAC Inc.

**Session 205: Characterization
and Modeling**

Chairs: Atila Mertol, LSI Logic and Bret Zahn, Amkor

Description:
Accurate electrical, mechanical and thermal modeling and characterization are important elements of the product development process, leading to improved performance, greater reliability, reduced costs, and faster time to market. The papers in this session show examples of how these techniques have been utilized.

Papers:

Testing Next Generation CSPs with Next Generation Micro-Spring Probes
Eric Bogatin, IDI Corporation

O/E Characteristics of 40-Gbps InGaAs Side-Illuminated Waveguide Photodiodes for Optical Receivers
Su Chang Jeon, Yonsei University

Evaluation of Simplified and Complex Thermal Finite Element Models for a 3-Die Stacked Chip Scale Ball Grid Array Package
Bret Zahn, Amkor

Package Design Optimization and Materials Selection for Stack Die BGA Package
Rahul Kapoor, United Test and Assembly Center Ltd.

Development of Novel Packaging Structures, Encapsulation Process, Materials and Reliability for Matrix Array Over-Molded Flip Chip CSP
Hsun-Tien Li, Industrial Technology Research Institute

Modeling Reliability of Flip Chip on Board Assemblies Implementing a Correction Function Approach Comparing Analytical and Finite Element Techniques
Daniel F. Baldwin, Ph.D., Georgia Institute of Technology

**Session 206:
Emerging Trends in Electronics
Manufacturing Poster Session**

Chairs: Ismail Fidan, Tennessee Tech University and Jerry Bartley, IBM

Description:

This Poster Session is an effective means of promoting research activities and the application of new technologies to a broad viewing audience. Each author will give a short presentation of his work. After all the posters have been presented, attendees can hold in depth individual discussions on how the work applies to their own specific applications.

Papers:

Sensitivity Analysis and Optimization of Excimer Laser Ablation for Microvia Formation using Neural Networks and Genetic Algorithms
Robert Setia, Georgia Institute of Technology

New Design-to-Test Software Strategies to Accelerate Time-to-Market
Hau Lam, Credence Systems Corporation

Latest Development in Chip Scale Package Laser Marking and Micro Laser Marking
Bo Gu, Ph.D., GSI Lumonics

The MicroDot Dabbing Process
Brian P. Prescott, Speedline Technologies

A New Approach to Chemical Analysis of Packaging/Assembly Materials: SARISTM Laser Ablation ICP Mass Spectrometry
Fuhe Li, Air Liquide-Balazs Analytical Services

Low Temperature Curing of Polyimide Wafer Coatings
Robert L. Hubbard, Ph.D., Lambda Technologies

Peculiarities of Measuring the Alpha Particle Activity of Flat Samples of Metal, Alloys, and Powders using Gas Flow Proportional Counters
Robert Gerber, Pure Technologies, LLC

A New Route for Cost-Effective Multi-Process Assembly of an Optical Silicon Bench at the Sub-Micron Accuracy
Gilbert Lecarpentier, SUSS MicroTec

Numerical Analysis of Mold Compound using Lagrange Formula
Jose Felizco, Amkor Technology Philippines

Intelligent Simulation Environment for Electronics Remanufacturing Systems
Ismail Fidan, Tennessee Tech University

New Flip Chip Technology Utilizing Non-Conductive Adhesive for Chip Card Module Production
Joachim Pajonk, Datacon Technology AG

Using Manufacturing Execution Systems (MES) to Track Complex Manufacturing Processes
Mark J. Gonia, Camstar, Inc.

Thursday, July 15

9:00am-12:00pm

Session 207: Advances in Wire Bonding Technology

Chairs: Jeff Demmin, Tessera and Jeff Kennedy, Celestica

Description:

Wire bonding will continue to be the dominant chip interconnect technology well past 2007, far outliving its projected life span. The success of wire bonding is due to advances in materials technology that support finer pitches with higher reliability and at lower cost. Learn how the process has kept pace with other developments in device packaging.

Papers:

Guidelines for Improving Intermetallic Reliability

Lee Levine, Sr., Kulicke & Soffa Ind. Inc.

Realizing Low Cost and High Reliability in CSP Packages with Surface Treatment and Material Technology

Ryota Furukawa, Panasonic Factory Automation Company

Effect of Chromium—Gold and Titanium—Titanium Nitride—Platinum—Gold Metallization on Wire/Ribbon Bondability

Jianbiao Pan, Ph.D., California Polytechnic State University

The Emergence of High Volume Copper Ball Bonding

Lee Levine, Sr., Kulicke & Soffa Industries Inc.

Plasma Processing for Improved Wire Bonding Yield and Strength

James Getty, March Plasma Systems

Session 208: Advanced Methods for SoC Testing

Chairs: Allan Calamoneri, Test Spectrum and Mouli Chandramouli, Virage Logic

Description:

The challenges facing today's test professional continue to involve the dynamics associated with increasing clock and bus speeds, as well as, the incorporation of analog and RF cells to SoC designs. This session's papers will address the specific tester resources and software methodologies currently being deployed to solve these emerging challenges.

Papers:

Using a Digital Channel of a Test System as an Analog Reference for Wireless SOC Testing

Joe Kelly, Agilent Technologies

How to Employ Multi-GHz Analog and RF Modules in Open Architecture ATE

Rochit Rajsuman, Advantest America R&D Center

Test and Debug Techniques for Multiple Clock Domain SoC Devices

Ross Youngblood, Credence Systems Corporation

A Comparison of Structural Test Approaches

Stephen Pateras, LogicVision

Serial ATA Testing with Analog Tester Resources

Hideo Okawara, Agilent Technologies International Japan, Ltd.

High-Speed Bus Debug and Validation Test Challenges

Mark Hosman, Credence Systems Corporation

Thursday, July 15

2:00pm-5:00pm

Session 209: Wafer Level Packaging/Manufacturing

Chairs: Bill Chen, ASE and Erik Jung, Fraunhofer IZM

Description:

Wafer Level Packaging has been very important to the development of miniaturized products with a higher functionality. This session will focus on metallization and patterning processes done at the wafer level to support this low cost, high performance packaging method.

Papers:

Near Void Free Hybrid No-Flow Underfill Flip Chip Process Technology

Daniel Baldwin, Ph.D., Georgia Institute of Technology

Solder Paste Printing and Stencil Design Considerations for Wafer Bumping

Rick Lathrop, Heraeus CMD

Photo-Imageable Auto-Catalytic Resin Metallization as an Alternative to Sputtering

Masaki Kondoh, Rohm and Haas

A Non-Cyanide Pure Gold Electroplating Process for Wafer Applications

Kai Wang, Rohm and Haas Electronic Materials

A Low-Cost, Robust Method to Vertical Sidewalls for Thick Resist Processing

Clif Hamel, SUSS MicroTec

Photolithography for Wafer Bumping

Elvino da Silveira, AZORES CORP

Session 210: New Advances in DFM and DFT

Chairs: Allan Calamoneri, Test Spectrum and Mouli Chandramouli, Virage Logic

Description:

Enormous cost and time to market advantages can be achieved by moving process development improvements earlier in a product's life cycle. This session's papers will address the evolving DFT, DFM and process improvement tools available from the industry's leading suppliers.

Papers:

Featured Speaker: Optimize Manufacturability by Designing for Yield

Yervant Zorian, Virage Logic

Low-Cost Test Requires More than a Cheap Tester!

Jochen Rivoir, Agilent Technologies

How Can Design for Manufacturability Improve Mask Costs and Yields

Philippe Hurat, Ph.D., Synopsys

Silicon Debug: Avoid Needless Respins

Wilco de Boer, Philips Research Laboratories, ED&T

Optimizing the Whole Test System to Achieve Optimal Yields and Lowest Test Costs

Jeffrey Sherry, Johnstech International

Session 212: MEMS Packaging and Test

Chairs: Erik Jung, Fraunhofer IZM and Daniel Baldwin, ENGENT, Inc.

Description:

MEMS devices continue to play an important role in modern devices by providing them with capabilities beyond what is possible solely with electronics. Packaging and testing of these sensitive devices still pose a major challenge to the development of a successful product. This session features presentations by those who have successfully met these challenges.

Papers:

Non-Contact Fast Wafer Metrology for Ultra-Thin Patterned Wafers Mounted on Grinding and Dicing Tapes

Wojciech Walecki, FSM

Optical Leak Detection for Wafer Level Hermeticity Testing of MEMS and Optoelectronic Sub-Assemblies

Gordon Elger, Hymite GmbH

Leveraging Mainstream Design and Analysis Tools for MEMS

Ilya Mirman, SolidWorks Corporation

Spray Coating—A Solution for Resist Film Deposition across Severe Topography

Ralf Suss, SUSS MicroTec AG

Chip Level Packaging for MEMS Using Silicon Cap

Xianfeng DU, Peking University

"Low Ball" BGA—A New Concept in Thermoplastic Packaging

Kenneth Burton Gilleo, Ph.D., ET-Trends LLC

Session 211: SiP/Sub-System Advance Processes

Chairs: Leo Higgins, ASAT, Inc. and Frank Juskey, Sawtek

Description:

System in Package (SiP) and Sub-System Assembly continue to drive IC packaging integration. The use of passive components with traditional chip and wire technology has opened new opportunities to improve the cost and performance of packaged devices. The key to these advanced processes is the implementation of new materials and methods into production.

Papers:

Development of High Power QFN Package

Francis Poh Koon Seong, United Test and Assembly Center Ltd.

Performance Evaluations of Stacked CSP Memory Modules

Vern Solberg, Tessera Technologies, Inc.

A Vertical Surface Mount Package Optimized for DC/DC Power Conversion Applications

MP Divakar, Power One

Area Array Contacts to Assemble a 3D Transformer for a Miniaturized Voltage Converter

Erik Jung, Fraunhofer IZM

Advanced Manufacturing: New Challenges in the Rework of 0201 Passives

Neil O'Brien, Finetech

An Alternative Printing Solution to Sphere Placement for Second Level Interconnect Assembly

Gerald Pham-Van-Diep, Speedline Technology

Registration for STS: IEMT Sessions

Complete Package

with proceedings book (Event Code: IEP1)

OR with proceedings CD (Event Code: IEP2)

Pre-registration for Members by June 25: \$395

Pre-registration for Non-members by June 25: \$520

Registration for Member or Non-members after June 25 or onsite: \$650

To receive both the proceedings book and CD (Event Code: IEP3), add \$50 more to the prices above.

Complete Package (Student Discount)

with proceedings book (Event Code: IES1)

OR with proceedings CD (Event Code: IES2):

Pre-registration for Members by June 25: \$100

Pre-registration for Non-members by June 25: \$100

Registration for Member or Non-members after June 25 or onsite: \$100

To receive both the proceedings book and CD (Event Code: IES3), add \$50 more to the prices above.

Complete Package (Speaker/Committee Discount)

with proceedings book (Event Code: EIC1)

OR with proceedings CD (Event Code: IEC2)

Pre-registration for Members by June 25: \$195

Pre-registration for Non-members by June 25: \$195

(No registration is available for speakers/committee after June 25 or onsite.)

To receive both the proceedings book and CD (Event Code: IEC3), add \$50 more to the prices above.

Wednesday Only (All Attendees)

with proceedings book (Event Code: IEW1)

OR with proceedings CD (Event Code: IEW2)

Pre-registration for Members by June 25: \$295

Pre-registration for Non-members by June 25: \$390

Registration for Member or Non-members after June 25 or onsite: \$450

To receive both the proceedings book and CD (Event Code: IEW3), add \$50 more to the prices above.

Thursday Only (All Attendees)

with proceedings book (Event Code: IET1)

OR with proceedings CD (Event Code: IET2)

Pre-registration for Members by June 25: \$295

Pre-registration for Non-members by June 25: \$390

Registration for Member or Non-members after June 25 or onsite: \$450

To receive both the proceedings book and CD (Event Code: IET3), add \$50 more to the prices above.

Friday Only (All Attendees)

with Proceedings Book (Event Code: IEF1)

OR with Proceedings CD (Event Code: IEF2)

Pre-registration for Members by June 25: \$195

Pre-registration for Non-members by June 25: \$260

Registration for Member or Non-members after June 25 or onsite: \$300

To receive both the proceedings book and CD (Event Code: IEF3), add \$50 more to the prices above.

To register, visit: www.semi.org/semiconwest/stsiemt