

Components, Packaging,  
and Manufacturing  
Technology Society



IEEE



Newsletter



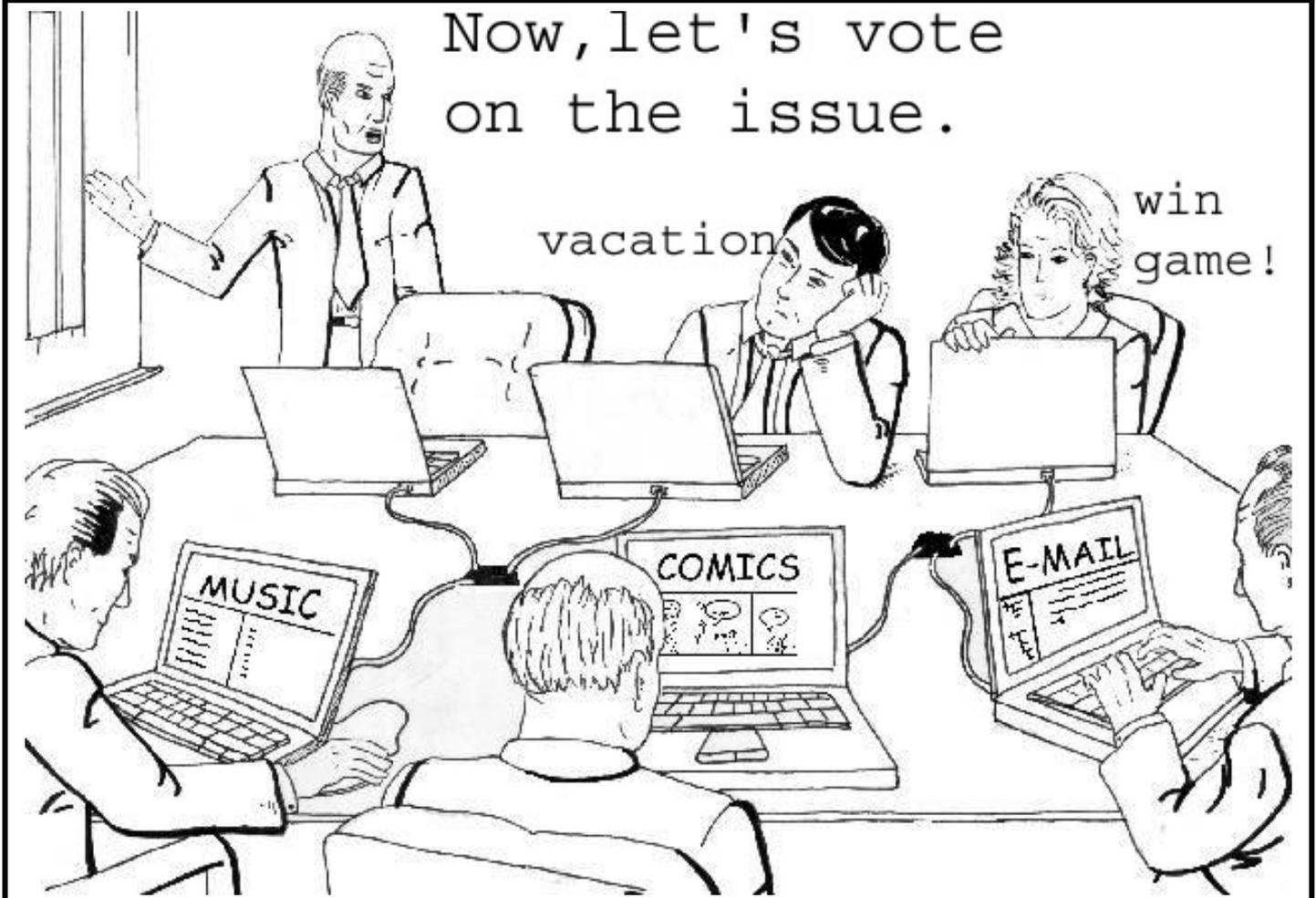
The Global Society for Microelectronics Systems Packaging

Vol. 27, No. 4, December 2004 (ISSN 1077-2999)

[www.cpmt.org](http://www.cpmt.org)

[www.ewh.ieee.org/soc/cpmt/newsletter](http://www.ewh.ieee.org/soc/cpmt/newsletter)

## What hath our components, packaging, and manufacturing wrought?



Why the laptop computer has not quite  
doubled the productivity of committee meetings

## CPMT OFFICERS

President -- Phil Garrou, +1 919 248 9261  
Technical VP -- Rolf Aschenbrenner, +4930-46403164  
Administration VP -- H. Anthony Chan  
Treasurer -- John Segelken, +1 732 920 3023  
VP Publications -- Paul B. Wesling, +1 408 331 0114  
VP Conferences -- Ricky Lee, +852 2358 7203  
VP Education -- Albert Puttlitz, FAX +1 802 879 0466  
Senior Past President -- John Stafford, +1 602 413 5509  
Junior Past President -- Rao Tummala, +1 404 894 9097  
Secretary -- Ron Gedney, +1 703 834 2084  
Executive Director -- Marsha Tickman, +1 732 562 5529  
IEEE VP TAB -- Ralph Wyndrum, +1 732 219 0005

## Elected Board Members

**2007:** Eric O. Beyne, Steve J. Bezuk, N. Rao Bonda, Rajen Chanchani, Kitty Pearsall, CP Wong

**2005:** William T. Chen Li Li, L. Merrill Palmer, Walter J. Trybula, E. Jan Vardaman, David C. Whalley

**2006:** William D. Brown, Philip C. H. Chan, Charles Lee, Johan Liu, Thomas G. Reynolds-III, Ephraim Suhir

## Standing Committee Chairpeople

Student Chapter Development -- William D. Brown, wdb@engr.uark.edu  
Distinguished Speakers -- A. F. Puttlitz, FAX +1 802 879 0466  
Fellows Search--Rao Tummala-rao.tummala@ee.gatech.edu & David Palmer-d.palmer@ieee.org  
Fellows -- C. P. Wong, cp.wong@ieee.org  
Constitution & Bylaws -- Tony Mak, +1 972 371 4364,  
Finance -- Ralph Wyndrum, Jr., r.wyndrum@ieee.org  
Long Range Planning -- Dennis Olsen, d.olsen@ieee.org  
Standards --  
IEEE Books & C and D Magazine Editor, Joe Brewer, +1 386 445 2593, j.brewer@ieee.org  
Membership -- Ralph Russell, cpmt-membership@ieee.org  
Chapter Development -- Ralph Russell, II, see membership  
Nominations -- John Segelken, +1 732 920 3023  
International Relations -- Leo Feinstein, +1 508 870 0051; Europe -  
- Ephraim Suhir, +1 908 582 5301; Far East -- W. T. Chen, +65 874 8110  
Joint Committee on Semiconductor Manufacturing -- G. C. Cheek

**Next News Deadline: March 5, 2005**

**Members-only Web:**

**UserName: xxxx (don't tell non-members)**

**Password: xxx xxx (for 1st quarter) 2**

## CPMT SOCIETY NEWSLETTER

**Editor:** David W. Palmer, email: d.palmer@ieee.org,  
FAX +1 505 844 7011, Tel: +1 505 844 2138  
**Composition:** Alina Deutsch: deutsch@us.ibm.com  
**Associate Editor:** Li Li, Free Scale Inc, li.li@ieee.org  
**Proofreading:** Janice Washington, jewashi@sandia.gov

## CPMT Archival Publications

**Publications VP:** Paul Wesling, email: p.wesling@ieee.org,  
Tel: +1 408 331 0114.  
**Transactions-CPT editor,** Avram Bar-Cohen, Univ. of Maryland,  
2181B Martin Hall, College Park, MD 20742 USA,  
Tel: +1 301 405 3173; email barcohen@eng.umd.edu  
**Transactions-AdvP editor;** G. Subbarayan, Purdue University, ME  
Department, Tel: +1 765 494 9770; email ganeshs@ecn.purdue.edu  
**Transactions EPM editor;** R.Wayne Johnson, Tel: +1 334 8441880,  
johnson@eng.auburn.edu

## Technical Committee Chairpeople

**TC-ECCC (1) Electrical Contacts,** Connectors and Cables--  
Gerald Witter, Chugai, +1 708 244 6025  
**TC-DIP (2) Discrete and Integral Passive Components--**  
Leonard Schaper, Univ. of Arkansas, schaper@uark.edu  
**TC-Assy (3) IC and Package Assembly --** Michele Berry, Intel  
michele.j.berry@intel.com  
**TC-EM (4) Manufacturing Design & Process--**Walt Trybula,  
SEMATECH, +1 512 356 3306  
**TC-M (5) Materials--**Rajen Chanchani, Sandia Labs,  
+1 505 844 3482, r.chanchani@ieee.org  
**TC-HDSB (6) High Density PWB packaging --** Yoshitaka Fukuoka,  
weisti.fukuoka@rose.zero.ad.jp  
**TC-ASTR (7) Environmental Stress & Reliability Test--**Kirk Gray,  
k.a.gray@ieee.org  
**TC-Therm (9) Thermal Management & Thermomechanical  
Design--** Tony Mak, Dallas Semi, +1 972 371 4364  
**TC-Opto (10) Fiber Optics & Photonics--**Susan Law -- Fax: +612 9351 1911,  
Email: s.law@ofc.usyd.edu.au  
**TC-Test (11) Electrical Test --** Bruce Kim, Bruce.Kim@asu.edu,  
Tel: +1 480 965 3749  
**TC-EDMS (12) Electrical Design, Modeling and Simulation--**  
Madhavan Swaminathan, G Tech, +1 404 894 3340  
**TC-PEP (13) Power Electronics Packaging--**Doug Hopkins, SUNY  
Buffalo, +1 607 729 9949, d.hopkins@ieee.org  
**TC-SP (14) Systems Packaging--** Erich Klink, eklink@de.ibm.com  
**TC-RF+W (16) RF and Wireless--** Craig Gaw, Motorola,  
+1 480 413 5920, c.a.gaw@ieee.org  
**TC-MEMS (17) MEMS and Sensor Packaging--**Eric Jung, IZM  
Berlin email: erju@izm.fhg.de  
**TC-WLP (18) Wafer Level Packaging--**Michael Toepper, IZM  
Berline toepper@izm.fhg.de  
**TC-Ed (19) Education--**Rao Tummala, G Tech, +1 404 894 9097  
**TC-GEMP (21) Green Electronics Manufacturing and Packaging,**  
Hansjoerg Griese, Email: griese@izm.fhg.de  
**TC-NANO Nano Packaging --** Rao Tummala, Georgia Tech,  
rao.tummala@ee.gatech.edu

\*\*\*\*\*IEEE Components, Packaging, and Manufacturing Technology Society Newsletter is published quarterly by the Components, Packaging, and Manufacturing Technology Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17<sup>th</sup> Floor, New York, NY 10016-5997. \$1.00 per member per year (included in Society fee) for each member of the Components, Packaging, and Manufacturing Technology Society. Printed in U.S.A. periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE CPMT Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved, copyright (c) 2004 by the CPMT Society of IEEE. Authors and Artists given full permission for further use of their contributions. This Newsletter was printed in the U.S. of America. For circulation information call IEEE customer Service 908 981 1393, or FAX 9667.

## Results of Election for IEEE CPMT Society Board

On behalf of Nominating Committee Chair John Segelken, I am pleased to report that the votes have been tallied for the election of six Members-at-Large to the CPMT Society Board of Governors. The following individuals (in alphabetical order) have been elected to serve for a three-year term -- 1 January 2005 to 31 December 2007:

**Eric O. Beyne**  
**Steve J. Bezuk**  
**N. Rao Bonda**  
**Rajen Chanchani**  
**Kitty Pearsall**  
**CP Wong**

We thank all candidates for their interest and willingness to serve.

-- Marsha S. Tickman, CPMT Executive Director

## WILLIAM D. BROWN

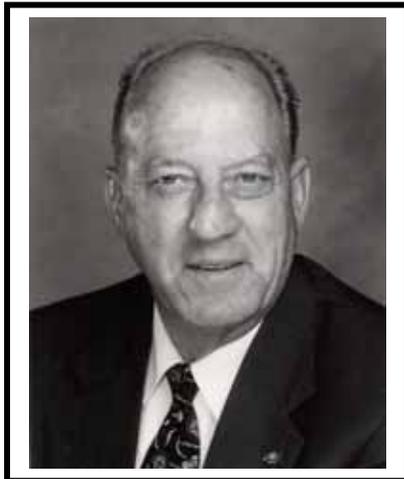
Received the IEEE Fellow of Institute in 2004 for leadership in furthering education of high density electronics.

William D. Brown received the B.S. degree in Electrical Engineering from the University of Arkansas, Fayetteville, in 1969, the M.S. degree from Pennsylvania State University, University Park, in 1970; and the Ph.D. degree from the University of New Mexico, Albuquerque, in 1975.

From 1969 to 1977, he was a Member of the Technical Staff at Sandia National Laboratories in Albuquerque, NM. In 1977, he joined the faculty of the Electrical Engineering Department at the University of Arkansas where he presently holds the rank of Distinguished Professor. From 1983 to 1998, he served as the Head of the Department of Electrical Engineering. Since January 1999, he has served as the Associate Dean for Research in the College of Engineering. His research interests include microelectronic materials and devices, solid-state and semiconductor physics, and electronic packaging.

Bill's research has resulted in over 300 conference presentations, over 300 technical journal/proceedings publications, and 10 U.S. patents. He has contributed to the book, *Electronic Manufacturing Processes* published by Prentice Hall, and has contributed to and edited the books *Nonvolatile Semiconductor Memory Technology* and *Advanced Electronic Packaging: With Emphasis On Multichip Modules*, both published by the IEEE PRESS.

Bill is a registered Professional Engineer in the State of Arkansas and holds memberships in the Institute of Electrical and Electronics Engineers (he serves on the Board of Governors of the Components, Packaging, and Manufacturing Technologies Society), the International Microelectronics and Packaging Society, the Materials Research Society, the American Vacuum Society, the Arkansas Academy of Science, and the American Society of Engineering Educators (ASEE). He is a Fellow of the Electrochemical Society.

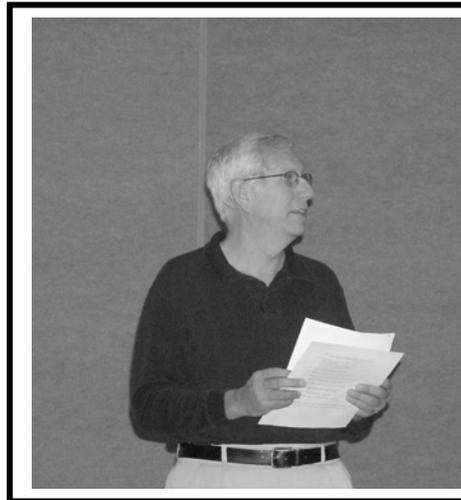


## IEEE CPMT Treasurer's Report

As a result of our recent financial performance, we can now celebrate that CPMT has made a recognized turnaround and we have been removed from the IEEE TAB's "Watch List". We established a 2005 budget that projects a \$76.6K surplus for 2005 (Revenue of \$1.8133M). In 2003 we had a surplus of \$349.4K (Revenue of \$1.3862M) and added to our CPMT reserves that surplus to bring the reserves to ~ \$2M at the end of 2003.

We currently expect to end 2004 on or close to budget (Revenue of \$1.4753M) with a surplus of \$36K. The CPMT Leadership and the BOG continues to enhance our financial stewardship and look for opportunities to increase revenues and reduce our expenses and bring about increasing global value to the CPMT membership.

--John M. Segelken, CPMT Treasurer



John also mentioned that the Las Vegas ECTC with more than 1000 in attendance resulted in a revenue input to CPMT activities of \$88K. This is the best example of how the CPMT volunteer effort results in more resources to help members even more.

### Web Content - ONLY for CPMT Members!

Your membership in the IEEE and the CPMT Society just got more valuable! Beginning last January, all CPMT members were enabled to use our Members-Only webspace to access full-text papers or presentations, in PDF format, from several recent conferences:

- \*\*IEEE Photonic Devices & Systems Packaging (PhoPack) Symposium '02 and '03
- \*\*EuroSimE'03: 4th Int'l Conference on Thermal Simulation in Micro-Electronics and Micro-Systems (France)
- \*\*Phoenix Chapter Fall'03 Workshop on Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications
- \*\*IEEE Photonics Materials Reliability (PhoMat) Symposium '03
- \*\*NEMI Tin Whisker Workshop, Las Vegas '04

These are papers and presentations that cannot be found on IEEE's XPLORE. For someone who is not a CPMT member, they can only be purchased on CD-ROM. If you have a need to learn the latest in any of the fields above, check out the Tables of Contents and read some of the fine papers presented there.

Accessing our Members-Only area is very simple:

Point your Browser to: [www.cpmt.org/mem/](http://www.cpmt.org/mem/)

When you are asked, enter:

Username: xxxx Password: xxxxxx

(all lower-case, notice to know what to put in for the xxxx's you must look at page 2 of this latest CPMT printed newsletter, a newsletter that is mailed only to members)

## New Senior Members in Our Society

Robert Darveaux -- Phoenix  
Michael D. Evans -- Boston  
Vivek Gupta -- Phoenix  
Daoqiang Lu -- Phoenix  
Arthur S. Morris -- North Carolina  
Ben Jemaaa Nouredine -- France  
Ravi S. Prasher -- Phoenix  
Raghuram V. Pucha -- Atlanta  
Charles E. Volk -- Winston Salem  
Charles K. Williams -- North Carolina

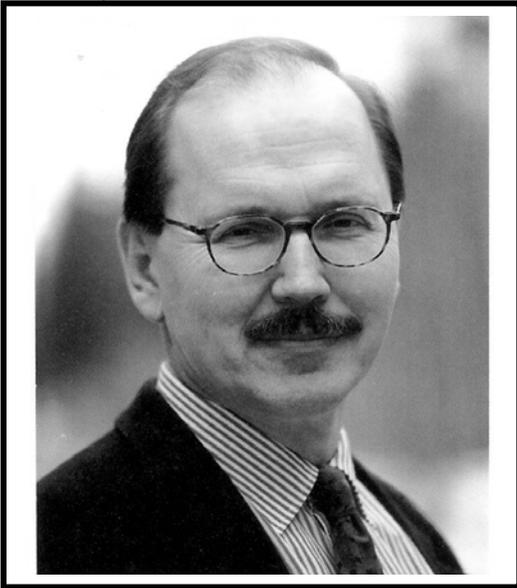
"... a candidate shall be an engineer, scientist, educator, technical executive or originator in IEEE-designated fields. The candidate shall have been in professional practice for at least ten years and shall have shown significant performance over a period of at least five of those years."

Less than 10% of CPMT Society members have applied for the senior member status even though about 50% meet the requirements. See the following website for your path to this deserved honor.

<http://www.ieee.org/organizations/rab/md/smprogram.html>

### Prof. Jorma Kalevi Kivilahti

Received the IEEE Fellow award for contributions to the reliability of lead-free electronics.



Prof. Kivilahti's key technical contributions have been in the areas of thermodynamic and kinetic modeling of electronic materials such as lead-free solders, their compatible metallization and diffusion barrier layers, and the modeling of

multi-phase diagrams. Prof. Kivilahti has published over 200 scientific and technical papers and four book chapters in his career, given over 30 keynotes and invited lectures and tutorials, and received best paper awards in the areas of materials and manufacturing technologies. He has served as an Advanced Research Fellow of the Academy of Finland, a member and Chair of committees of international conferences, and a reviewer for a number of international research journals. He received the Order of Merit: The White Rose of Finland (Knight, I Class) in 1998 for his contribution to the Finnish electronics society. He served as the first Chairman of the CPMT Finnish Chapter from 1998 to 2001, advising students and holding meetings to promote CPMT activities within the student body and professionals within the Helsinki area. As an educator, he has graduated over 100 MS and over two dozen PhD students over his career. 4

## IEEE-CPMT Society Awards for Year 2005

(Nomination Due Date: January 31, 2005)

Your CPMT Society offers the following awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and CPMT Society.

**David Feldman Outstanding Contribution Award:** To recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.

Prize: \$2,500 and Certificate

**Basis for Judging:** Contributions to the organization or enterprises connected with the field, to CPMT Chapter, Section or Board of Governors activities, and to the fields encompassed by the CPMT Society.

**Eligibility:** Recipient must have been a member of IEEE and CPMT for the past five (5) years, including 2004.

**Outstanding Sustained Technical Contributions Award:** To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society.

Prize: \$2,500 and Certificate

**Basis for Judging:** Technical contributions must be sustained and continuing over a period of at least five (5) and preferably 10 years. One major contribution will not qualify. Must be documented by open literature publications such as papers, patents, books and reports (available to the public).

**Eligibility:** Must have been a member of the IEEE and CPMT Society for the past three (3) years, including 2004.

**Electronics Manufacturing Technology Award:** To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society.

Prize: \$2,500 and Certificate

**Basis for Judging:** Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Work in the management of CPMT conferences or its BoG may be contributory but not sufficient to receive the award.

**Eligibility:** No need to be a member of IEEE and CPMT Society.

**Exceptional Technical Achievement Award:** To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the CPMT Society.

Prize: \$2,500 and a Certificate.

**Basis for Judging:** Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in CPMT's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.

**Eligibility:** Recipient(s) must have been a member of IEEE and CPMT for the past three (3) years, including 2004. There are no requirements for service to the IEEE or CPMT Society.

**Outstanding Young Engineer Award:** To recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.

Prize: \$1,500 and Certificate plus one year free membership in CPMT with all CPMT Transactions.

**Basis for Judging:** Technical contributions through patent invention, contributions to technology or product development within the CPMT Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.

**Eligibility:** Must have been a member of the IEEE and CPMT (member grade or above) for the past three (3) years, including 2004, and must be 35 years of age, or younger, on December 31, 2004.

#### Guidelines for Nominators:

Ø Past recipients of an award are not eligible to receive that same award. For list of past awardees, see the CPMT Society Home page (<http://www.cpmt.org/awards/>).

Ø An individual may submit only one nomination per award but may submit nominations for more than one award.

Ø It is the responsibility of the nominator to provide quality documentation to assist the Awards Committee in evaluating the candidate.

Ø Please send nominations to CPMT Society Awards Committee Chair by e-mail, fax or mail:

**Rao Bonda, Ph.D.**

Freescale Semiconductor, Inc.  
2100 East Elliot Road,  
Mail Drop: EL725  
Tempe, AZ 85284,  
USA

Ph: +1-480-413-6121

Fax: +1-480-413-4511

#### Email address:

r.bonda@ieee.org or  
rao.bonda@freescale.com



Winners will be notified by 28 February 2005, and the awards will be presented at the 55th Electronic Components and Technology Conference, May 31- June 3, 2005, in Orlando, Florida, USA.

*poster session at IEMT San Jose July 04 -->*

## Paul B. Wesling

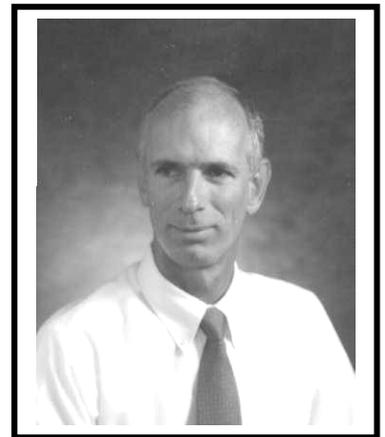
**Received the IEEE Fellow award in 2004 for contributions to multimedia education development within the IC packaging.**

Paul Wesling led the CPMT Society Santa Clara Valley Chapter to prominence as one of the leading chapters in the world. He served as treasurer, Chair, and Chapter Advisor; instituted and ran a short course program beginning in 1970 that has consistently been financially successful, with over \$100K/year in gross revenues and \$15K in surplus each year; organized leading edge topics such as disk drive design, microprocessor programming, reliability, and project management, with attendances up to 700, at low Member pricing; recruited and trained instructors; taught other Sections/Chapters how to replicate these at an IEEE Sections Congress and at local Section Officer Training sessions. He

served as CPMT Society Secretary and Newsletter Editor before assuming the position of Vice President of Publications (1985-present; grew the CPMT Transactions from 450 pages into three journals with over 1,800 pages and a net revenue contribution of over \$350K/year; developed Society conference publications to a revenue contribution of over

\$200K/year; and brought the Society from <\$250K reserves to over \$3M in 10 years. He founded the International Electronics Manufacturing Technology (IEMT) Symposium, and produced its Proceedings for many years; served as General Chair and host of for the VLSI Packaging Workshop.

He published a series of papers on multimedia education, presented keynote talks worldwide as an IEEE Distinguished Lecturer on this topic, managed a NSF grant for the creation of multimedia training modules and virtual labs in the discipline of electronics packaging and manufacturing for worldwide use. He helped plan the Sloan Foundation-funded IEEE USA video on college-student career advising, and appeared in it. He is the Chair of the Packaging Education program subcommittee for the ECTC. He was awarded the IEEE Centennial Award (1984), Chapter Man of the Year (1985), CPMT Contribution Award (1986), Board of Governors Distinguished Service Award (1991), and the IEEE Third Millenium Medal (2000).



## In Memorium: Vijai K. Tripathi

Vijai K. Tripathi, Professor Emeritus and former Department Head of Electrical and Computer Engineering at Oregon State University, died on May 1, 2004, after a seven-year struggle with ALS, better known as "Lou Gehrig's disease."

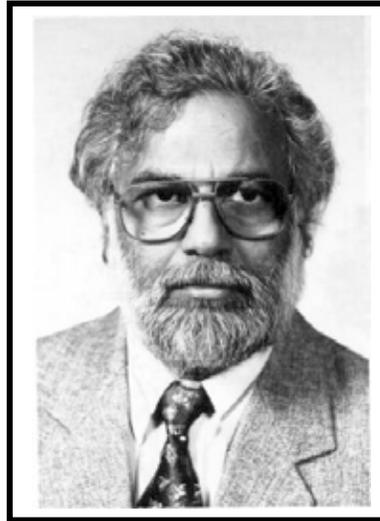
He was born in Kanpur, India, in December 1942. He received the bachelor of science degree at a young age of 15 from Agra University in 1958, and a master's degree in electronics and radio engineering from Allahabad University in 1961. He worked as a senior research assistant at the Indian Institute of Technology in Bombay from 1961 to 1963. He immigrated to the United States in 1963 to attend the University of Michigan at Ann Arbor, where he received the master's and doctoral degrees in electrical engineering in 1964 and 1968, respectively. He started his professorial career at the University of Oklahoma. He moved to Oregon State University in 1974 and was on the faculty for more than 25 years. He became a full professor in 1985 and served as Head of the Department of Electrical and Computer Engineering from 1994 to 1997. He continued to serve as Professor Emeritus after retiring due to his illness in 1999.

Professor Tripathi was a dedicated educator and a distinguished scholar. He developed an innovative, integrated research and teaching program of international recognition in the areas of microwave electronics and electromagnetics at Oregon State University. He was a visionary and leading authority in the field of signal integrity in high-frequency analog and high-speed digital electronics, with his pioneering contributions serving as the cornerstone for its foundation and the springboard for its future growth.

Early on Prof. Tripathi recognized the significance that electromagnetic interactions due to the signal and power distribution network in packaged electronic systems will have on electrical system performance. In response to the escalating demand for comprehending the signal integrity and EMI issues and developing the knowledge and expertise for their effective resolution through noise-aware design, he established a unique educational program, one of the first of its kind worldwide, that helped set the norm for university-based education and training in high-frequency/high-speed signal integrity.

His educational activities were complemented by a prolific research program that led to seminal contributions in the general areas of RF and microwave circuits, electronic packaging, interconnects, and computational electromagnetics and its applications for the development of methodologies and tools for the computer-aided design (CAD) of microwave and high-speed electronic circuits. More specifically, his seminal research work on SPICE-based modeling of coupled and lossy transmission lines, as well as the electromagnetic analysis of multilevel interconnect structures, has found wide application in the electrical characterization and modeling of the high-density interconnections and packaging structures in state-of-the-art packaged electronic systems.

In parallel to his theoretical work, his research contributions in the area of experimental characterization of interconnects and packaging structures led to significant breakthroughs in the development of novel probing techniques and sophisticated de-embedding methodologies for accurate characterization and modeling of interconnections in microwave and high-speed electronic circuits, including the TDR measurement-based interconnect model extraction and signal integrity analysis algorithms first commercialized by Tektronix and later productized by TDA Systems.



His prolific educational and research work was complemented by an unselfish dedication to professional service. Prof. Tripathi held various leadership positions in the professional societies including the co-chair of the IEEE Topical meeting on Electrical Performance of Electronic Packaging during 1994-1997, chair of the MTT-12 technical committee, several guest editorial appointments for the IEEE Transactions on

Microwave Theory and Techniques, an Associate Editor appointment for the IEEE Transactions on Circuits and Systems II, member of the editorial boards of several journals, and member of the technical program committee of the International Microwave Symposium and several other international conferences. As chairman of the IEEE ED/MTT-S Oregon chapter he organized many technical meetings that brought together students and engineers working in industry. He organized and taught numerous, well-attended short courses and workshops locally, at IEEE sponsored conferences including the IEEE International Microwave Symposium, and at several locations in Asia and Europe.

He received numerous recognitions for his contributions in research and education, most notably his election to IEEE Fellow in 1993 for "contributions to microwave and millimeter-wave circuits and to coupled transmission-line techniques." He was also the first recipient of the Alumni Professor Award of the College of Engineering at OSU in 1991-92 for his excellence in teaching, inspirational and dedicated guidance of his graduate students and distinction in scholarship. He was a sought-after consultant to many high-tech companies and held visiting appointments at renowned academic and research organizations including Chalmers University of Technology in Gothenburg, Sweden, Duisburg University in Germany, and the Naval Research Laboratory in Washington, D.C.

Prof. Tripathi was an exceptional and inspirational teacher and advisor to numerous master's and doctoral students as well as post-doctoral fellows. Many of his students and faculty moved on to distinguished careers in industry and in academia. As an indication of his devotion, he continued to mentor his graduate students and young faculty long after being confined to his bed and losing his ability to breathe on his own and speak during his illness.

Prof. Tripathi was deeply appreciative of the shared travel and other fun activities, and later, the support of numerous friends throughout his long illness. He has inspired many students and colleagues through his intellect, his dedication, and his foresight. He will be missed by the many who knew him personally or through his research contributions.

Memorial contributions can be made to the Vijai Tripathi Graduate Student Fellowship Fund through the non-profit Oregon State University Foundation at 850 SW 35th Street, Corvallis, OR 97333 ([osufoundation.org](http://osufoundation.org)).

--submitted by officers of TC-EDMS

# Your Board Meets behind Closed Doors in Dallas

A hearty group of about 30 volunteers spent Saturday November 6th near the Dallas Fort Worth airport making sure your Society remains running smooth and efficiently. President Phil Garrou set the tone by introducing many proposed changes to the Board Members at large process to make sure the Board reflects the global weighting of the members. He also proposed changes in the officer structure to make the constitution reflect better how the leadership has evolved over the last 15 years. He gave an upbeat status for the Society and turned the meeting over to each officer and their accomplishments.



## Membership

Chair of membership, **Ralph Russell**, reported that our Society is seeing approximately the same decrease in numbers that the majority of IEEE societies are experiencing. For example, the 6 societies in IEEE Division I has had a 10.3% decrease during the last year compared to the CPMT loss of 6.9%. Our current membership is 3,092 which is about the level in 1998.

Ralph encouraged all members to apply for Senior Membership and then help their colleagues achieve this goal (do search on "senior member" on [www.ieee.org](http://www.ieee.org)). Ralph indicated that the decision to go senior is a large step toward a member engaging fully in IEEE. In addition, Ralph requests that Board members stay active in our Professional marketing efforts to grow "CPMT" as the brand name in packaging/ components/ manufacturing. He lead a brief discussion of our membership support efforts in Eastern Europe, possibility of making a membership directory as a benefit of belonging, and the December region 10 conference in Asia.

In his alternate roll as Chapter Development Chair, Ralph discussed last year's "Chapter of the Year Award" that went to the Santa Clara Chapter. Ralph was developing a web tool that would enhance the communication ease among our global Chapter leaders. One initiative is to have an "Electronic Distinguished Lecturer Program" which would allow the Chapters to receive a polished lecture and question period at their meeting over the web. This would eliminate the high hurdle of travel time and travel expenses for the Distinguished Lecturers. In addition, Ralph is updating the Volunteer Recruiting Tool Kit that chapters use.

## Awards

Rao Bonda of Freescale Semiconductor requested nominations for this year's IEEE CPMT awards. The nomination due date is January 31, 2005. In addition, C. P. Wong mentioned that



CPMT had submitted five excellent IEEE Fellow nominations last June and would find out by early December (see articles elsewhere in newsletter). Co-chair of the Fellows Nomination Committee, Dave Palmer, indicated that the Board was encouraging and assisting in about a dozen Fellow nomination efforts which are due by March 1, 2005. Our Society has about 110 Fellows; our Fellows should expect requests for "Letters of Recommendation" for this new group of Fellow nominations since at least 5 letters are needed for each candidate.

## ECTC

**C. P. Wong** reported that by extending the due date for presentation summaries by a few days, the ECTC organizing committee received 506 suggested papers. Approximately 350 will be selected for presentation at the meeting in June. There will be a total of 16 Professional Development classes at ECTC. Approximately half of the class attendees are new to ECTC each year. The organizing committee has set aside at least one exhibition booth for Student Chapters but how it is manned (series or parallel) has still not been resolved. C. P. Reported that there remains a good synergetic relationship between ECTC and CPMT.

The 13th Motorola IEEE Graduate Student Fellowship competition will be held between seven student presentations. This ECTC will also hold the 2nd Intel Corp. best student paper contest. IBM will sponsor the ECTC Student Reception on Tuesday night of the conference. There will be a special room set aside for a student poster session to enhance exchanges between students.

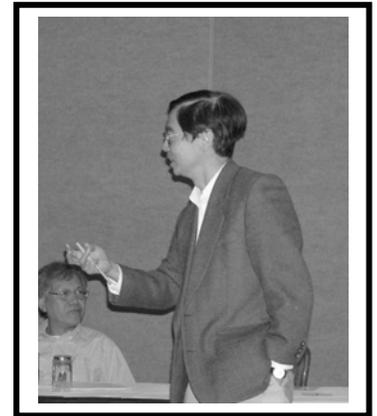
New rules were applied to paper selection. For example, session chairs could not be co-authors of papers in their sessions. In general, only one paper in each session could come from each institution. An abstract can only be considered by two subcommittees. These changes are intended to broaden the scope of presentations in each session and to lessen the appearance of "insider" advantage.

Discussions of the nature of the IEEE/NEMI Whisker Workshop and the Advanced Flexible Circuit Board Technology TC meeting are still underway.

## Changes in Board

A small team of CPMT leaders proposed the following changes to the structure of the CPMT Board: Elimination of the Secretary position, elevation of Treasurer to a Vice President of Finance position, elimination of Administrative Vice President position, and elimination of Director of Technical Marketing. Changes in the Constitution and ByLaws will soon be published to reflect these approved proposals.

**Anthony Chen**, VP Administration, proposed



that by the next Board meeting members could have wireless LAN connections between their laptop computers or even complete Internet connectivity. One advantage would be the sharing of files, ability for those not at meeting to see presentations, and ability to download from the CPMT home pages. However, several members pointed out that their companies had begun holding "no computer" meetings because the presence of laptops often resulted in meetings up to twice as long because everyone was preoccupied with catching up with email, surfing the web, or playing games. So one engineer's productivity enhancer has become another's window to distraction.

**Marketing**

Connie Swager, Director of Marketing, announced that 2 million CPMT media impressions (print and electronic) had occurred since June. Another 2 million are expected by the end of 2004. Articles have appeared in Advanced Packaging, Chip Scale Review, Semiconductor International, SMT, Solid State Technology, and Global SMT & Packaging. A Tin Whisker story should soon appear in Fortune Magazine including interviews of Phil Garrou and Ron Gedney. Kristine Martin of Potomac Communications will be interfacing our EPTC Asia meeting with the media. This is part of the Globalization emphasis on CPMT Marketing. Many plans are being made for the upcoming ECTC meeting in Orlando. First steps have been taken to market the Intellectual Property collection of data that CPMT controls.

**Ralph Wyndrum**

Ralph called in his TAB report concentrating on the issues of Publications, Conferences, and Membership.

In **Publication**, the whole industry is being shaken by the "expectation" of a lot of users that past papers should be available



at no expense on the Internet to everyone. Since publications result in about \$20M of income for IEEE our future handling of technical publications is important. Typical expense of each IEEE paper from submission to publication is \$900 plus a lot of volunteer editing. It is believed that the peer and professional editing is an important value added. In other subject matter where everyone just posts their own "papers" it has become

impossible to separate the few good papers from the many misleading ones. But who and how will future editorial efforts be paid for? Even getting volunteer reviewers is becoming difficult as workers are being overwhelmed by their jobs. However, IEEE has the built-in advantage of established conferences and transactions that entice good papers from good engineers.

**Conferences** result in about \$10M in immediate IEEE income and \$10M in further income from the Proceedings rights. The Goal is always to help members in face-to-face technology exchanges. The IEEE is deciding which services to centralize and which to decentralize in the global vision. There is growing conference competition from for-profit groups and other non-profit professional societies. Where the IEEE has been the standard for up to 50 years, we will maintain our strength. However, in new subject matter and in new locations the best answer for membership is often jointly sponsored meetings.

Recently IEEE has addressed the Visa problem many members have in applying to attend USA hosted IEEE meetings. Some societies have attempted to meet in several wonderful Canadian cities to avoid this issue but confronted difficulty with US non-citizens trying to quickly cross the border.

75% of conference attendees attend the 25 largest IEEE meetings. Depending on what you include on the IEEE technical meeting list, there are 325-1000 annual IEEE events. The presentations at these meetings are 35% research oriented and 20% describe advanced development. In contrast, our membership is only 11% research occupied with greater than 50% doing product development. Although much of the off-line discussion at IEEE meetings concerns product development, only 3% of our papers address this topic. One membership enticement might be increased product development papers. Historically companies have been hesitant to release such papers although many trade magazines have this flavor.

TAB held a workshop on **membership** to develop a new model more in keeping with the "age of the Internet." Downside pressure due to the changing "value proposition" to members is added to the lack of investment in the future by IEEE societies in lowering membership. This society near-sightedness is a result of resource restrictions caused by high IEEE overhead charges and negative stock market performance over the last 4 years. There is some concern that IEEE volunteerism may be threatened by inadvertently walking into the perfect "tipping point." However, the financial markets are recovering and the IEEE overhead tax was just reduced by \$2 million.

Ralph notes that there are approximately 1 million engineers in the US that would qualify for IEEE membership, but only 225,000 are members. In addition, the expanding health care and broadcasting industries have many workers who would mix well with IEEE activities.

Ralph is now the IEEE-USA President-Elect. His perspective will continue to be excellent on Institute issues.

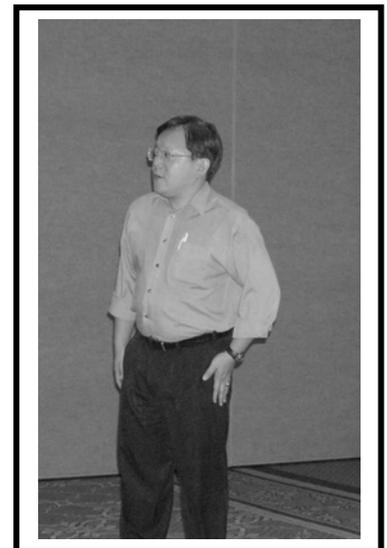
**Conferences**

Vice President **Ricky Lee** reported on the health of CPMT Global Conferences. Board approval was given for our 50% support of a large European pan-CPMT conference beginning every second year. In addition, joint support with ACS and MRS for an Organic Microelectronics Workshop was approved.

Ricky reviewed our 20 major meetings in 2004: 4 in Europe, 6 in Asia, and 10 in USA. Only a few of these fell short on income. For example, Polytronics advertisements went out a bit too late for most members to reserve calendar time. In addition, for 204 most companies and universities restricted conference attendance to minimize expenses.

V. P. Lee noted the 6th EPTC meeting held in December has been established as a major Asia conference covering many

CPMT Society topics. In a similar fashion he requested Board support for Region 8 to accomplish a similar goal. The ICEP,



SPJWS, and the VLSI packaging Workshop had a good 2004 in Japan. Japan will host EMAP in 2005 and perhaps Polytronics in 2006.

### Technical Committees

Vice President **Rolf Aschenbrenner** reviewed the current status and history of the 18 active Technical Committees. He noted that Dr. Sue Law of Australian Photonics was now the chair of TC-Opto Fiber Optics and Photonics. He also pointed out that the focus of TC- IC and Package Assembly was little studied in Universities anymore. The main developers are now in the EM Service companies who historically sit quietly at CPMT meetings. The chair of TC-Discrete and Integral Passives, Len Schaper, has suggested that the industry push is over and it is time to retire this TC. In addition TC-Systems packaging is thriving under the new chair, Eric Klink.

Rolf suggested that as new topics come up he will assign a task force with short-term goals. Only if long-term interest grows will he initiate a new Technical Committee. The Board agreed that as Vice President he already had the authority to carry out that approach.

Rolf noted that our members have been active for a very long time on NEMI Committees particularly roadmap efforts. He wanted to make sure that more synergy existed such as the Tin Whisker workshop so that our members had more direct benefit.

### Publication

Vice President Paul Wesling submitted his report in writing. Paul reports that the artificially low citation Index numbers caused by changing the name of our Transactions five years ago have been recalculated by Thompson ISI, the keepers of the index. Thanks to editor Avi Bar-Cohen for calculating the index as if the name had not changed and officers in CPMT, IEEE, and Thompson for reaching a conclusion that is fair and practical for our members' career advancement. Paul has a team that is also supplying training and web aids for transaction authors to easily find correct references for their publications.

Paul announced that Rick Ulrich's book "Integrated Passives" was published by Wiley/IEEE Press and is selling well. Paul also presented a motion that Prof. Wayne Johnson as Editor of the Transactions on Electronic Packaging Manufacturing, replacing Walt Trybula having served 8 years.

### Student Programs

Prof. Bill Brown updated the BOG on activities of the five official student Chapters: Georgia Tech, Romania, Hong Kong, Sweden, and University of Arkansas. Three more Chapters are somewhere along the petition process. Bill presented a motion to provide a financial award for the student chapter of the year; motion passed.

### Distinguished Lecturer Activities

**Bill Chen**, Member at Large of the Board, nominated Ho-Ming Tong for the CPMT Distinguished Lecturer position. Ho-Ming has a long history in Flip-chip and assembly ranging from R&D to Manufacturing and Management. Approval was quick, making Ho-Ming the 21st Distinguished Lecturer for CPMT.

**Albert Puttlitz** reminded everyone of the availability of Lecturers for both conferences and chapter meetings. And reviewed and updated the requirements to remain a distinguished lecturer and to receive travel assistance from CPMT for lecturing. Next Board Meeting is on the Weekend after ECTC in Orlando Florida (perhaps in the haunted house)

## Editor's Turn

There is good news and bad news in the recent strong CPMT Board meeting. The good was obvious as one great report after another jumped out in an efficient manner. The bad news was that about 60% of the attendees also attended Board meetings 20 years ago. In contrast, approximately 30% of all IEEE society members do not even renew membership each year. However, about 1000 of our CPMT members have belonged for more than 10 years. Yet only about 50 of these long-term members plus 50 rotating new members are making all the directional decisions for the Society (this is an estimate since no one really has the time or money to pin such data down). So, this is an issue of leadership balance and every member can decide for themselves what fraction of the seasoned volunteers are best to mix with the newer volunteers. This member has decided that after 25 years of CPMT Newsletter involvement, it is time to turn the editorial cutting and pasting to another (new) volunteer. Below is a job description so that any of the 3000 CPMT members can rush to apply for this opening.

### CPMT Newsletter Editor position:

#### Tasks

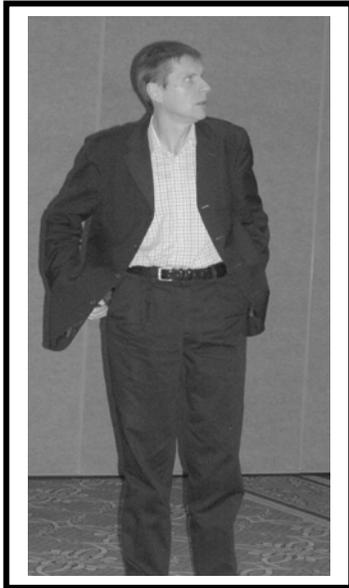
- \*\*Send out news request to email list of 100 most active volunteers 4 times a year (1 hour/issue)
- \*\*Attend for each issue either a Board meeting, a Chapter meeting, or a CPMT conference so you take pictures and report first hand on the activities (10 hours)
- \*\*Receive many emails from volunteers and edit their rushed engineering language into informal English (5 hours). However, this material represents probably 100 hours by our many volunteers (thanks to you all).
- \*\*Paste this news and photographs into a simple frame based web format (15 hours)
- \*\*Download this copy to the IEEE/CPMT website and regularly update for late news (4 hours)
- \*\*Reformat everything into the "standard" 24 page paper PDF format for the mailed Newsletter (20 hours, and you should know how to swear for this part.)
- \*\*Fight with your computer that can't stand these big files and keeps trying to change all your perfect pages after you add just one little last picture on page 24. (5 hours)
- \*\*Listen to the almost complete silence after the issue is done (unless you spelled someone's name wrong, used an old telephone number wrong, or gored someone's ox with your cartoon) ( 0 hours)

#### Rewards

- \*\*Four times a year you don't have to ask "what will I do in the evenings and over the weekend?"
- \*\*You get to interact with a lot of great technology leaders -- build a great professional network and feel like Benjamin Franklin must have when he ran a newspaper single handedly. You feel satisfaction in providing a large part of the glue and communication that helps volunteers accomplish their goals and maximize their impact on the members and the larger profession. In contrast, if we let this job to the many professional Newsletter providers it would quickly become another artistic masterpiece that will be quickly discarded by our already overwhelmed members.

#### Contact

Now that you are motivated, please contact Paul Wesling, Vice President of CPMT Publications, email: p.wesling@ieee.org, Tel: +1 408 331 0114 with your interest. Thanks.



## Networking the "CPMT" World

The motto of IEEE is "Networking the World". Members of the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society are Networking the "CPMT" World. CPMT members have the opportunity to network with other professionals, and the chance to participate in technical and educational activities for professional development at over 30 chapters around the world. The CPMT Society through a subsidy program for local technical, educational and membership activities, and a Distinguished Lecturers Program, support the global CPMT Chapters.

Additional networking opportunities exist at over 30 technical meetings the CPMT Society sponsors or co-sponsors annually. Global leaders in their fields of expertise share the newest technologies, providing the most up-to-date information. Topics include: Foundation Technologies, Components and Devices, Packaging, and Process and Manufacturing. Members are eligible for discounts on conference registration.

The CPMT Society values its global members. Thanks for being a CPMT Society member.

--Ralph W. Russell, II --CPMT Society Strategic Director for Global Membership and Chapter Development

## Upcoming Conferences

### 2005

\***European System Packaging Workshop**, January 31 - February 2, 2005, Berlin, Germany, [www.ewh.ieee.org/soc/cpmt/tc14](http://www.ewh.ieee.org/soc/cpmt/tc14)

\***21st Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM'05)**, March 15-17, 2005, San Jose, California -- contact Bonnie Crystall, [cscomm@earthlink.net](mailto:cscomm@earthlink.net)

\***2nd International Workshop on Nano & Bio-Electronics Packaging**, March 22-23, 2005, Atlanta Georgia, [www.prc.gatech.edu/nanobiopack](http://www.prc.gatech.edu/nanobiopack)

\***6th Quality Electronic Design (ISQED)**, March 28 - 30, 2005, San Jose, California, [www.isqed.org](http://www.isqed.org)

\***EuroSime2005**, April 17 - 20, Berlin Germany, [www.eurosime.com](http://www.eurosime.com)

\***Workshop on Signal Propagation on Interconnects (SPI'05)**, May 10-13, 2005 -- Garmisch-Partenkirchen, Germany Contact: Hartmut Grabinski, Laboratorium fur Informationstechnologie, Hannover, Germany - Ph +49-511-762-5030; Fax +49-511-762-5051; [grabinski@lfi.uni-hannover.de](mailto:grabinski@lfi.uni-hannover.de)

\***55th Electronic Components and Technology Conference (ECTC'05)**, May 31 - June 3, 2005, Orlando, Florida -- Contact: Donna Noctor, [noctor@ectc.net](mailto:noctor@ectc.net)

\***30th International Electronics Manufacturing Technology Symposium (IEMT'05)**, July 11 - 13, 2005, San Francisco, California -- Contact: Sheri Mukai, [smukai@semi.org](mailto:smukai@semi.org)



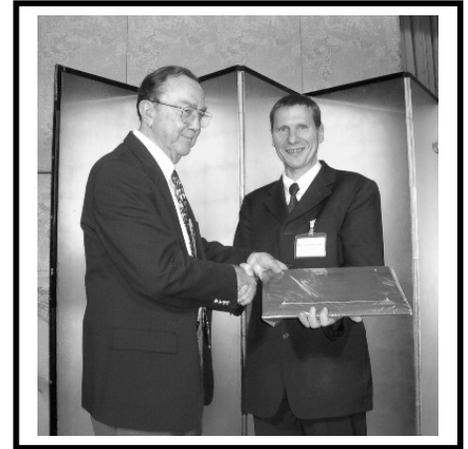
**Walt Trybula**  
making point as  
keynote speaker at  
IEMT San Jose,  
July 2004

10

## 7th VLSI Packaging Workshop Awards Volunteers

The 7th VLSI Packaging Workshop of Japan was successfully held in Kyoto, Japan, from November 30 through December 2, 2004.

At an award ceremony, Conference Committee Chair Rolf Aschenbrenner recognized with award plaques George Harman for establishing the workshop, and Kanji Otsuka for establishing a permanent home for the workshop in Japan.



## Summary of the 7th CPMT HDP'04

The 7th IEEE CPMT HDP'04 Conference, Between June 30 and July 3, 2004 Shanghai, China was successfully held in Bao Long Hotel, Shanghai, China. About 80 papers were presented at the Conference. 9 short courses were made with high class instructors from industry and academia: These are:

- **Torsten Wipiejewski, ASTRI, Hong Kong**
- **Lawrence Wu, City University of Hong Kong**
- **Itsuo Watanabe, Hitachi Chemicals, Japan**
- **Hans Grönqvist, IVE, Sweden**
- **CP Wong, Georgia Tech, USA**
- **James Morris, Portland Sta, USA**
- **Jie Xue, Cisco, USA**
- **Li Li, Freescale, USA**
- **Wei Koh, Kingston, USA**

Professor Tummala, Georgia Tech, Dr William Chen, ASE, Jan Vardman, Techsearch, Itsuo Watanabe, Hitachi Chemicals and Dongkai Shangkuan, Flextronics, gave key-note speeches during the conference. They were well received by the audience.



The SOP Session and 3D packaging session were of high class with good papers from Georgia Tech, USA, China Central South University, China and Royal Institute of Technology, Sweden.

A special section in the IEEE CPMT transaction Part B: Advanced Packaging is being prepared. Due to the interest of this conference in China, it is decided to change this conference series from biannual to annual basis with the IEEE CPMT financial sponsorship and it is going to be the first IEEE CPMT financially sponsored conference in China!



**E. Jan Vardaman giving keynote address**

**Rao Tummala during his keynote address**



**Jim Morris giving short course**



*-- submitted by Johan Liu*

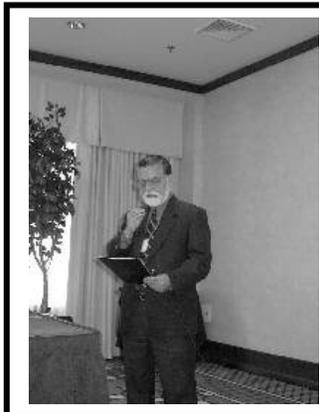
## Bangalore is Newest CPMT Chapter

IEEE has recognized the official formation of the CPMT Bangalore Chapter as of 17 November 2004. When notified of the formation of the CPMT Bangalore Chapter, Mr. Kuppuswamy Raghunathan said: "We want to live up to the standards set by other chapters; given the presence of leading semiconductor companies in India (50+ and growing)." The new CPMT Chapter plans to have its inaugural meeting in the 2nd week of December while Rao Tummala and Madhavan Swaminathan will be visiting Bangalore.

--Ralph W. Russell, II -- Director for Chapter Development **11**

## Review of Future Directions in IC and Package Design Workshop (FDIP'04)

The fourth FDIP workshop had record attendance of 80 participants on Sunday, Oct. 24, 2004, in Portland, OR. This matched the very well attended EPEP'04 conference that followed for the three days, on Oct. 25-27, namely 190. The very interesting sessions were chaired by **Ravi Kaw** from Agilent Technologies, Prof. **Hartmut Grabinski** from University of



Hannover, and **Zhaoqing Chen** from IBM Corporation. All the presentations were given by experts in the field that were invited to the workshop. The topics that were covered fell in three categories, System Design Challenges, Modeling Challenges, and Simulation Challenges.



The first session was started by **Shekhar Borkar** from Intel Corporation. The title of the talk was Gigascale Integration - Design Challenges and Opportunities. Shekhar outlined all the challenges faced by future chip designers in order to achieve the 1 TIPS goal by 2010 while not exceeding the 100W power limit imposed by the package. Although 1 billion transistors will be available on one die, due to leakage and all the other tolerances, new means need to be devised to utilize all the integration improvements. Such approaches were suggested as low power designs, higher integration of slow devices, tri-gate devices with 10x lower leakage, high-K, metal gate, multiple supply rails, body bias control, sleep transistors, variation-tolerant circuits. Micro-architectural changes are envisioned such as multi-threading, multiple cores, deep pipelining, increased on-chip caches. Heterogeneous systems with optical and RF brought on the same die (SOC) or on the same carrier (SIP) with the CMOS

processors. Processors could have the traditional functions that are augmented by many special purpose CPUs.

The second talk, entitled Emerging Trends in High-Speed Interconnects and Packaging Engineering, was given by **Sergio Camerllo** from Cisco Systems. Sergio addressed the issue of increased design cycles due to signal, power, and timing integrity issues. All aspects of the system design are becoming more complex and yet technological improvements, such as printed circuit material properties, are not keeping up with the higher integration capabilities. Future designs need multi-disciplinary efforts with a convergence of circuit theory, electromagnetics, mathematics, numerical simulation, thermo-mechanical optimization. Sergio saw the need for smart I/O buffers, self-timed and de-skewed circuits, self-diagnostic capability on chip since on-chip testing is no longer possible or adequate, use of communication techniques, statistical designs, chip-package co-design, SIP, MCP, 3D stacking, intelligent power management, on-die temperature sensors, development of new model libraries and CAD tools.



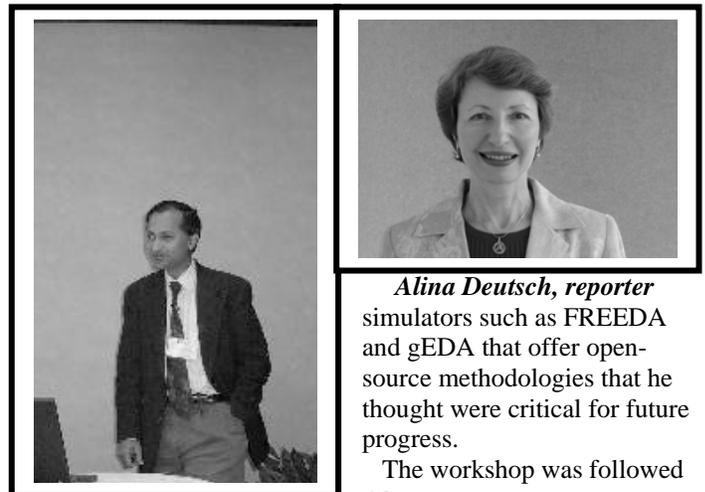
The third talk was presented by **Martin Schmatz** of IBM Corporation and was entitled Analog RFCMOS and Optical Design Techniques for 10+ Gbps Datacom. The main issue that Martin addressed was the fact that in spite of the extremely high integration level on-chip, the I/O technology for communication between chips is lagging behind. His view is that we need Tbyte/sec/inch rates for the 1 TIPS chips in 2010. In order to achieve this, novel technologies have to be developed such as I/O density being pushed to 2-mil pitch and high-speed, small I/O cells interfacing directly with the I/O connections. Such density would drive development of new SIP technologies. Board-level optical interconnects are expected to appear in commercial high-end systems toward the end of the decade through the use of multi-mode waveguides having 30-70 um pitch and wavelength of 850 nm and embedded microlenses to couple to electrical interconnects in the board. Such optical interconnects will need much simpler channel equalization circuits than electrical counterparts and thus higher data-rates.

The second half of the workshop addressed the future modeling and simulation tool development requirements. Power Distribution Status and Challenges was presented by **Prof. Madhavan Swaminathan** of Georgia Institute of Technology. Due to the need to reduce the power distribution effective impedance by a factor of 2x for every product generation, new design tools, new technologies, and new decoupling schemes are needed. Heterogeneous systems lead to a chip-package co-design, time and frequency-domain analysis interchange, new embedded decoupling materials such as BatiO3 in the printed circuit boards, and in laminate-based chip carriers, the use of FDTD,



TMM, device macromodels to include non-linear simulation of interconnect and power distribution noise, novel EBG structures included in large boards to isolate RF and digital circuits. **Ching-Chao Huang** from Optimal Corporation presented the talk entitled Signal Integrity Modeling and Simulation for IC/Package Co-Design. Ching-Chao echoed the message given by all the previous speakers for the need of chip-package co-design and he reviewed the available tools that can be used for modeling and simulation of such complex systems. DC power drops, electromigration, as well as simultaneous switching noise, power plane resonances, and isolation have to be modeled for the chips and the package structures together. Signal and power integrity have to be optimized concurrently and microwave and RF design techniques have to be adopted by the digital circuit designers. Full-chip and full-package CAD tools need to include full-wave effects and still deliver 24 hour turn-around analysis time for the many design iterations. Several tools available from Optimal Corporations were shown as examples.

The last session was shortened by the typhoon and earthquake that was taking place in Japan. Sani Nassif was unable to travel to the US and **Jaijeet Roychowdhury** from University of Minnesota had to deliver the Current and Future Direction in Simulation Development talk alone. His talk was extremely well received and generated very interesting discussions. Jaijeet indicated that simulator development is gaining again momentum and progress due to the increasing demands of high integration levels, speeds, and heterogeneous systems. These new demands can be addressed by using modular approaches to algorithmic development for ease of use, maintenance and interoperability. He traced the evolution of SPICE and gave examples of new



**Alina Deutsch, reporter** simulators such as FREEDA and gEDA that offer open-source methodologies that he thought were critical for future progress.

The workshop was followed

by a very interesting IEEE CPMT Society Technical Committee on Electrical Design, Modeling, and Simulation (TC-EDMS) meeting chaired by Prof. Madhavan Swaminathan from Georgia Institute of Technology. The meeting covered among other topics a discussion led by Ravi Kaw of Agilent Technologies on power-distribution modeling standardization and a discussion led by Prof. Paul Franzon of North Carolina State University on the development of new device macromodels to advance the current IBIS capabilities.

## Boston Chapter Activities

*Boston IEEE/CPMT Meeting Notes for 2004 and 2005*  
by Dan Bauks Chapter Chair (dzbauks@aol.com) (978-692-1559)

The Boston CPMT chapter usually has 6 to 8 meetings a year with meetings held the third Tuesday of the month at the Sun Computer's East Coast Campus complex in Burlington, MA. See ([www.ieeeboston.org](http://www.ieeeboston.org)) for monthly meeting details. For 2003 meetings please see the CPMT December 2003 Newsletter.

### Recent 2004 meetings have included:

2/17/04 "**LCP - Liquid Crystal Polymer Packaging**" by Michael Zimmerman, PhD CTO - Quantum Leap Packaging, Wilmington, MA ([www.qlpkg.com](http://www.qlpkg.com))

3/23/04 "**Laser Micro-Electronic Machining**" by Ron Schaeffer, PhD President, Photomachining Inc., Pelham, NH ([www.photomachining.com](http://www.photomachining.com))

4/20/04 "**Ultra Dense MCM Packaging Technology**" by Tom Marinis, PhD Draper Laboratories, Cambridge, MA ([www.draper.com](http://www.draper.com))

9/21/04 "**Flexible Automation Systems for Optical/Electronic Assembly**" by **Andre By**, Chief Technology Officer, Automation Engineering Inc., Wilmington, MA ([www.aeiboston.com](http://www.aeiboston.com))

11/30/04 "**Laser Diode**



"**Heat Spreaders**" by **Robert Quagan**, President, Ion Beam Milling Inc., Manchester, NH ([www.ionbeammilling.com](http://www.ionbeammilling.com))  
12/21/04 "**Plastic Photovoltaic Solar Cells**" by Daniel McGahn, Executive VP

& Chief Marketing Officer, Konarka, Lowell, MA. ([www.konarka.com](http://www.konarka.com))

The Boston CPMT local chapter will also again be presenting a free "Educational Program" at the **IEEE ELECTRO 2005 Conference** to be held Wednesday May 4th during the Nepecon-East Show at the new Boston Convention & Exhibition Center in South Boston. (See [www.nepeconeast.com](http://www.nepeconeast.com) and click on the free IEEE-Electro Program). The Boston CPMT chapter will also sponsor an Introduction to Flexible Circuitry one day paid course by Ken Gilleo, PhD and one day paid seminar on "POF" (Plastic Optical Fibers) by Paul Polishuk, PhD.

CPMT Educational Program Topics to include Flip-Chip Assembly, Laser Micro-Electronic Machining, LCP Packaging, Laser Diodes, Plastic Solar Cells, & Aero-Flexible Circuit Packaging.

To preview or join any of the IEEE Online Communities visit <https://www.ieeeonline.com>

## CHAPTER NEWS

### REGION 10 CHAPTER ACTIVITY ROUND UP -- by Dr. P. B. Parikh

#### Taipei Chapter

Dr. Lih-Shan Chen Secretary of IEEE CPMT Taipei Chapter has reported having organized IMAPS Taiwan 2004 Technical Symposium in Kaohsiung on October 22, 2004. More than 40 technical papers were presented in the conference. The papers included such topics as advanced packaging, lead-free soldering technology, green materials, testing and reliability of packaging. Dr. Okuno, general manager of Senju Metal Industry Co. Taiwan Branch, was invited to give a speech with "Technical Report in Recent BGA Soldering" as the topic.

#### Hong Kong Chapter

The IEEE CPMT Hongkong Chapter had organized the election of Chair elect and Vice Chair of the year 2005 and 2006. Dr. Ming Li will step up to be the Chairperson of IEEE CPMT Hongkong chapter by 1st January 2005 for the year 2005-2006.

The Chapter successfully elevated three local members from Member grade to Senior Member grade. They are Dr. Torsten Wipiejewski, Dr. Matthew MF Yuen, and Dr. Wing Yiu Cheung.

The **Student Chapter** arranged a Student Booth in ECTC 2004 and a Student Symposium held in HKUST on 15 June 2004. Company visit were arranged, including a visit to Hua Wei in ShenZhen on 30 August, 2004.

In addition Mr. Cheung Yiu-Ming, Ken has also summarized the activities of the Hongkong chapter during the year 2004 below:

#### A. Eight workshops with details as listed-

Ø Three Dimensional Packaging, Interconnection & Assembly for Microelectronics Miniaturization by Dr. Chuck Bauer on April 21 2004 (one day).

Ø Wire Bonding in Microelectronics by George G. Harman on April 30 2004 (one day).

Ø Monitoring the Health (Reliability) of Products by Dr. Michael Pecht on June 9 2004 (half day).

Ø Trends in High Density Packaging and Portable Microelectronics by E. Jan Vardaman on June 29 2004 (half day).

Ø Impact of Lead-Free on Electronic and Optoelectronic Packaging and their SMT Assembly by Dr. John H. Lau on June 15 2004 (half day).

Ø Conductive Adhesive Joining Technology for Electronics Packaging Applications by Prof. Johan Liu on July 26 2004 (one day).

Ø Preparation and Implementation for Lead-Free Soldering by Dr Ning-Cheng Lee on August 20 2004 (one day).

Ø Trend and Design of MEMS and Advanced Packaging by Dr K. N. Chiang on September 3 2004 (half day).

#### B. Two Technical Lectures:

Ø Migration to Lead-Free Microelectronics Assembly & Some Key Technical Issues by Dr. Karl Puttlitz on July 23 2004.

Ø Semiconductor Packaging Industry Trends - Flip Chip & System in Package by Dr. William Chen on September 7 2004.

## Singapore Chapter

Dr. K L Pey of Singapore Chapter has reported the following activities during the quarter:

### **A. Technical Seminars.**

Two IEDM video short courses were arranged in Sep'04. Due to an overwhelming response, three separate viewing sessions were conducted

Ø Sep 19 & 24 and 2 Oct, Course 1 - The Future of Semiconductor Manufacturing

Ø Sep 22, Course 2 - Silicon +: Augmented Silicon Technology.

### **B. Technical talk and short courses**

Ø Oct 11, Dr. Professor Arun N. Chandorkar of Indian Institute of Technology, Bombay, India gave a talk on "Technology scaling and its influence on architecture designs".

Ø A one-day short course on "Integration of Copper with Low-k Dielectrics" by Dr Jeffrey Gambino, IBM, USA was held on 25 October 2004 at the Sheraton Towers, Singapore.

### **C. Conferences/Events Planned**

Ø EPTC'04

The 6th EPTC is scheduled for 8 - 10 December 2004. The Call for Papers has received a good response and close to 200 abstracts were received, topping the submissions in 2003. All the arrangements for a successful conference are being made including the short courses, keynote and invited speeches, table-top exhibition and social events. A new feature will be an executive forum on the trend and directions in key packaging thrusts targeted at technology leaders in the region. With the industry pick-up and the impending lead-free implementation, it is expected that EPTC 2004 will generate even greater interest and participation.

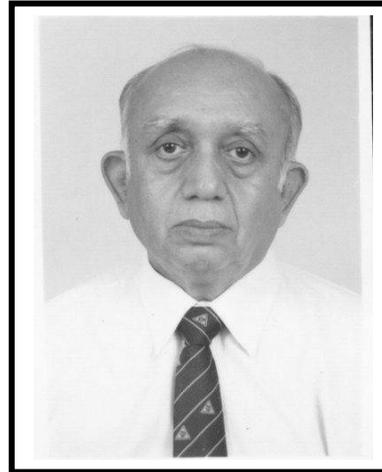
Ø A one-day short course on "Failure Mechanisms and Reliability in Integrated Circuits" by Dr. M.K. Radhakrishnan, NanoRel Consultants will be held on 10 December 2004 at the Sheraton Towers Singapore.

Ø IPFA'05

The 2005 International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA'05), organized by the IEEE Rel/CPMT/ED Singapore Chapter, and technically co-sponsored by the IEEE EDS and Reliability will be held at Shahgri-La's Rasa Sentosa Resort, Singapore, 27 - 31 June 2005. The second call for papers has been announced. For more information, please visit the IPFA'05 website at <http://www.ewh.ieee.org/reg/10/ipfa/html/2005/>.

Ø The Chapter donated S\$500 to the Student Chapter of the Nanyang Technological University branch for a "Back to the Future" competition for post-graduate students.

**India Council** IEEE CPMT India Council chapter organized a co-sponsored one-day technical event (with the Annual Conven-



tion of SMTA-IC) on 26th November 2004 at Bangalore. The theme for this convention was "Managing Profitable Electronic Manufacturing Services". As a sponsoring organization all our members of IEEE CPMT were entitled to free registration at the convention. Accordingly, 5 of our IEEE CPMT members (including 2 **Dr. P.B. Parikh** from CPMT Execom) attended

the convention. Totally 8 review papers (including one on "Lead Free Interconnect Technology" by Mr. R Kaura and one on "Electronic Packaging" by Prof N J Rao of Indian Institute of Science, Bangalore) were presented and discussed in detail. The convention was well attended by about 80 delegates from all over India.

The chapter has planned a technical lecture on "Status of Commercialization of MEMS in Indian Perspective" by Dr. D. N. Singh on 17th December at IIT, Powai, Bombay along with IEEE Bombay section. One more technical lecture on "Advanced Packaging" by Mr. S.Shakar Narayan is also planned in December 2004.

## **IEEE CPMT Shanghai University Student Chapter Inauguration**

The official inauguration ceremony of SMIT-SHU IEEE CPMT Student Chapter was successfully concluded at Shanghai University on 9 Aug. 2004.



Great welcome addresses were delivered both by the leaders of Shanghai University and the distinguished guests coming from companies such as Intel, Hitachi Chemical, Flextronics, TOYO Kohan, Chrysler, etc. as well as some key players such as the Shanghai Institute of Microsystem and Information Technology, etc. An ardent hope is raised by the chapter advisor, Prof. Johan Liu followed by three invited talks given respectively concerning the Future Challenges for Microelectronics Packaging by Mr. Jack Zhong, Intel Products (Shanghai) Ltd.,

Interconnection technology with ACF by Mr. Zhu Jian, Hitachi Chemical Co.,Ltd., and DFM Introduction by Mr. Frank Geng, Flextronics Tech (Shanghai) Co.,Ltd.



Speech given by **Prof. Yu Tao**, the assistant president of Shanghai University.



Speech by **Prof. Johan Liu**



Invited Talk given by **Mr. Jack Zhong**, ATD manager, Intel Products (SH) Ltd.



Invited Talk given by **Mr. Zhu Jian**, Hitachi Chemical Co.,Ltd

"The establishment of this IEEE student chapter must be a very constructive and meaningful event to all the three parties: Shanghai University, Industrial companies and the master &

PhD students." said president of the Chapter, Zhang Qi through the interview afterwards, "It will be a perfect vehicle to enhance the connecting between the high level students in SHU and the industrial and promote R&D collaborations in this field. Based on the full support from those companies and our school, we students are definitely going to have more opportunities to open our horizons and embody or improve the knowledge which could be merely kept in a mnemonic stage. So the only task now is how to stretch out our plans carefully and make it happen with our biggest co-efforts. I believe that this will give rise to fruitful future." The student members present also expressed their resolutions one after another.



--Sent in by Sam (Qi) Zhang, The IEEE CPMT Shanghai University student Chapter Chair

Agenda for Inaugural meeting of SMIT-SHU IEEE CPMT Student Chapter

Introduction of SMIT centre	Johan Liu <i>Director of SMIT</i>
Introduction of the student chapter	Sam Zhang <i>President of SMIT-SHU IEEE CPMT Student Chapter</i>
Welcome Speech	Mr. Wang Ming <i>Vice President of Shanghai University</i>
Welcome Speech	Officer <i>Shanghai Science &amp; Technology Commission</i>
Welcome Speech	Mr. Zhai Qijie <i>Section Chief of SHU Scientific Research Office</i>
Welcome Speech	Mr. Gong Liming <i>Vice Section Chief of SHU Scientific Research Office</i>
Welcome Speech	Mr. Yan Jialin <i>Vice Section Chief of SHU Scientific Research Office</i>

#### Seminar

Invited Talk 1: **Future Challenges for Microelectronics Packaging**  
Mr. Jack Zhong,  
*Department manager of Assembly Technology Development Intel Products (Shanghai) Ltd.*

Invited Talk 2  
**Interconnection technology with using ACF**  
Mr. Kera  
*Hitachi Chemical Co.,Ltd.*

Invited Talk 3  
**DFM Introduction**  
Mr. Frank Geng  
*Engineering Manager Flextronics Tech (Shanghai) Co.,Ltd.*

# Phoenix Section Workshop

## Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications An All Day Workshop, Arizona State University

Submitted by Vasudeva P. Atluri, Ph.D., Workshop Chair

IEEE Phoenix Section Components, Packaging, and Manufacturing Technology Society Chapter, & Waves and Devices Chapter jointly held An All Day Workshop on Friday, December 3rd, 2004, at the Memorial Building located on the campus of Arizona State University, Tempe, Arizona. The workshop was very well attended with about 175 registrants. The breakdown of registrants included 22 organizing committee members, 12 speakers, 40 vendor representatives, 60 IEEE members (included 3 student members), and 41 non-members. The workshop agenda included:

**Introduction** by Dr. Vasudeva P. Atluri, Intel Corporation, Chandler, Arizona.

**Morning Section I:** Chair: Dr. Dragan Zupac, Freescale Semiconductor, Inc., Tempe, Arizona.

"Keynote Presentation: Next Generation of Wireless Devices - Challenges and Issues", Presented by Dr. Sayfe Kiaei, Arizona State University, Tempe, Arizona.

"Research Toward More Flexible Radio Systems", Presented by Dr. Kevin C. Kahn, Intel Corporation, Hillsboro, Oregon.

"Silicon for Millimeter-Wave Wireless Applications", Presented by Dr. Modest M. Oprysko, IBM Research, Yorktown Heights,

**Morning Session II:** Chair: Mr. Steve Rockwell, Motorola, Inc., Tempe, Arizona.

"Nanoelectronics: Near-Term and Long-Term Opportunities", Presented by Dr. Stephen M. Goodnick, Arizona State University, Tempe, Arizona.

"Modeling and Characterization of Noise and Linearity for RFIC Design", Presented by Dr. Guofu Niu, Auburn University, Auburn, Alabama.

"Wireless Communication Standards and Regulations", Presented by Dr. Michael J. Marcus, École Nationale Supérieure des Télécommunications, Paris, France.

**Afternoon Session I:** Chair: Mr. Eric C. Palmer, Intel Corporation, Chandler, Arizona.

"Keynote Presentation: Systems-in-Package: Challenges and Directions for Communications and Wireless Products", Presented by Mr. Ken Brown, Intel Corporation, Chandler, AZ

"Integration of Passives", Presented by Mr. Dean P. Kossives, STATS ChipPAC, Inc., Tempe, Arizona.

"High Power RF Packaging for Wireless Infrastructure", by Dr. Mali Mahalingam, Freescale Semiconductor, Inc., Tempe, AZ

**Afternoon Session II:** Chair: Mr. Sam Karikalan, STATS ChipPAC, Inc., Tempe, Arizona.

"Wafer Level Packaging for Wireless Applications", Presented by Dr. Luu Nguyen, National Semiconductor Corporation, Santa Clara, California.

"System Level Packaging for Wireless Applications", Presented by Dr. Amit Agrawal, Broadcom Corporation, San Jose, CA

"Keynote Presentation: Enabling Mobility: Future Wireless Technologies", Presented by Mr. Behrooz Abdi, Qualcomm Inc., Carlsbad, California.

The morning session with a focus on challenges, issues, research, applications, nanoelectronics, modeling, characterization, standards and regulations was very well received by the workshop audience. Dr. Sayfe Kiaei focused on various RF Front-End Blocks to support Multi-Band Wireless Data Transceivers. Design of High-Q MEM's resonators for front-end RF

band-pass filters will also be discussed. Dr. Kevin C. Kahn talked about research being pursued at Intel Corporation for better understanding the design constraints on creating more flexible radios that can be better integrated with other system elements and provided the motivations that driving this research. He emphasized that the issues of flexibility and integration increase the desirability of building radios more flexibly.

Dr. Modest M. Oprysko suggested that we may be witnessing the birth of an entirely new application space for silicon technologies. He described the progress made at IBM Research in demonstrating some of the key circuit building blocks and functions required for a basic millimeter wave radio using a gigabit per second wireless personal area network operating in the 60 GHz Industrial Scientific Medical (ISM) band as an application driver. The results suggest that the next step of building an entire IQ transmitter on a chip and receiver on a chip are within reach.

Dr. Stephen M. Goodnick gave a review of near-term and long-term opportunities of Nanoelectronic Technologies with emphasis on developments that are undergoing in a variety of fields. These technologies included scaled semiconductor devices approaching the end of the road map in terms of Moore's law, nanodevice technologies that will complement traditional semiconductor CMOS technology for high density memory and processing circuits, ultra-dense sensor arrays, and bio-compatible electronics for applications in biomedicine and bio-threat detection.

Dr. Guofu Niu reviewed the basics of broadband noise, low-frequency noise, phase noise, as well as their modeling and experimental characterization for both high SiGe HBT and CMOS RF technologies. The connections between process level parameters such as base resistance and  $1/f$  noise K factor and system level parameters such as frequency synthesizer phase noise were established to facilitate process evaluation / qualification from a noise perspective. Optimal sizing and biasing for optimum noise and linearity were discussed.

Dr. Michael J. Marcus mentioned that wireless technology differs from other electro-technologies in the large degree of government regulation in all countries which affects the introduction of new technology and the evolution of existing ones. In addition to government regulations, wireless technologies are also governed by many nongovernmental standards in order to assure interoperability. He suggested that in both regulations and standards, national and international levels are involved. He gave an insight into better understanding of the processes that are used for definition of standards and regulations across national and international standards organizations that are very important for many researchers in wireless technology.

The afternoon session focused on packaging, integration, enabling mobility, and panel discussion. Mr. Ken M. Brown described the emerging requirements, the packaging, and the packaging challenges to come for System in Package (SIP). He suggested that communication and wireless semiconductor products are now driving significant requirements for chip packaging. While System on Chip (SOC) has been deployed successfully, it is SIP, or System in Package, that provides the more exciting backdrop for packaging.

Mr. Dean P. Kossives presented the challenges in the SIP package assemblies and the use of imbedded passives in such commercial packages. He also focused on the state of the art of SIP assembly in a typical packaging foundry and briefly dis-

cussed the future directions such as passives on silicon substrates.

Dr. Mali Mahalingam focused on high power RF (Radio Frequency) packaging to support the wireless infrastructure applications. He mentioned that Thermal performance, RF electrical performance and stringent reliability requirements traditionally have played a vital role in influencing the choice of structures, interconnects, materials, and assembly processes practiced in high power RF packaging. He highlighted the challenges faced and how they were overcome at Freescale Semiconductor, Inc., with metal-ceramic and overmolded plastic packages for high power RF applications with continuous operation of device junction to 200°C. Dr. Luu T. Nguyen talked about wafer level-chip scale package growth requiring lower cost, smaller form factor, and increased performance. The talk highlighted the packaging trends and migration path of packages to WL-CSPs, and key issues in test. NSC's WL-CSP, the micro SMD package family, was presented as a case study. New developments in lead-free solders, thinner packages, pre-applied underfill, and wafer/die stacking were also discussed together with the ensuing challenges.

Dr. Amit P. Agrawal reviewed LTCC and organic substrate technology for wireless system/module design. The system-in-package (SiP) technology, including antenna were discussed. The modeling and simulation tools to analyze the performance of RF systems were discussed and the need for future tools was highlighted. Mr. Behrooz Abdi mentioned that enabling mobility is what is needed for future wireless technologies. He suggested that the mobile market continues to evolve rapidly towards the convergence of cellular and WLAN wireless connectivity with computing, and consumer applications. According to him, converged world is however now driving technology convergence, calling for a new paradigm in which multiple technologies interact seamlessly to create an optimized system solution. He predicted that an inflection point in the mobile market will emerge new technology leaders.

The day ended with an hour long panel discussion consisting of ten speakers and moderated by Dr. Charles E. Weitzel. The topic was "Future market Opportunities in Wireless Communications". The panel discussion was interactive between speakers, audience, and moderator. The discussions among panelists and between panelists and audience were lively and interesting. About 40 people were in the audience for the panel discussion.



## Technical Seminar on “Packaging of Biomedical Electronic Devices”-- 22 January 2005

Location: Room 116, UCSD Extension Sorrento Mesa  
Center -- 6925 Lusk Blvd. **San Diego, CA**, 92121

### Technical Program (As of 12/6/04)

8:00am Registration. Coffee and donuts available

8:35am Dr. Darryl D’Lima, Scripps Clinic Center for Orthopaedic Research and Education (SCORE): “Design and Packaging Considerations of the Electronic Knee (‘E-Knee’)”.

9:05am Dr. Christopher Druzgalski, Ph.D, Professor Electrical/BioMedical Engineering, California State University, Long Beach: “Component, Sensor, and Subsystem Technology Issues Related to Biomedical Electronic Device Design and Packaging”.

10:20am James A. Steele Jr., Senior Reliability and Quality Assurance Manager, Medtronic Submicron Wafer Fab: “Introduction to Implantable Medical Devices”

11:00am James A. Steele Jr.: “Medical Integrated Circuits”

11:20am Mark Henschel, Manager, Hybrid Process Development, Medtronic Microelectronics Center: “Medical Microelectronic Packaging”

12:00am Lunch (Provided)

12:45pm James A. Steele Jr.: “Implantable Medical Materials”

1:00pm Clive Groom, Retired; Formerly Sr RQA Manager, Reliability Systems, Medtronic Microelectronics Center: “Medical Device Energy Sources”

2:00pm Clive Groom: “Change Management in the Medical Device Industry”

3:00pm Clive Groom: “Reliability Test Levels/Methodologies”

3:30pm Robert Czajkowski, NexGen: “Medical Application Electronic Device Packaging”

4:30pm Wrap-up and adjourn

Registration form is available at Register by email and  
PayPal:

<http://www.cpmt.org/docs/sd-bio.html>

For additional information see

<http://www.cpmt.org/docs/sd-bio.html> or email  
[BioMedPkg@cox.net](mailto:BioMedPkg@cox.net).



<b><i>International Symposium on Quality Electronic Design</i></b>		
<b>March 21-23, 2005</b>	<b>San Jose, CA, USA</b>	<b><i>www.isqed.org</i></b>
		
<b><i>Design for Quality in the Era of Uncertainty</i></b>		

ISQED is the pioneer and leading international conference dealing with the design for manufacturability and quality issues front-to-back. ISQED spans three days, Monday through Wednesday, in three parallel tracks, hosting near 100 technical presentations, six keynote speakers, two panel discussions, workshops/tutorials and other informal meetings.

**Register now!** The San Jose DoubleTree Hotel is holding rooms through February 19. Save \$100 on fees by registering for the Symposium before March 14th. Visit [www.isqed.org](http://www.isqed.org) for the complete Advance Program and on-line registration.

# ECTC – Orlando

The **55th Electronic Components & Technology Conference** will be held at Wyndham Palace Resort & Spa in Orlando, Florida USA on May 31 – June 3, 2005.

This conference comprises papers covering a wide spectrum of topics, including not only electronic components, but also exciting new developments in all areas of electronics technology (for example, electronics assembly, packaging, systems packaging, optoelectronics, reliability and materials). In 2005, over 350 papers and posters, and 16 Professional Development Courses will be presented by companies, universities and research institutions from around the world. The audience includes representatives from leading universities and companies eager to stay abreast of the rapidly changing and emerging technologies in the electronics field. This is the big annual CPMT Society all technology meeting.

The primary goal of the conference is to offer quality coverage of technological innovations in the areas of packaging design, materials, processes, quality and manufacturing of devices, components and systems. The Program Committee represents a wide variety of disciplines and expertise from the electronics industry. We are committed to assembling the highest quality program for the 55th ECTC, and we need many excellent papers to meet this commitment.

**Registration starts in January at [www.ectc.net](http://www.ectc.net)**

**Major Topics for ECTC: Advanced Packaging, Components & RF, Education, Emerging Technologies: Biomedical Packaging & Nano-Scale Packaging, Interconnections, Manufacturing Technology, Materials & Processing, Modeling & Simulation, OptoElectronics, Quality & Reliability, plus 16 Professional Development Courses and a Tin Whisker workshop.**

**Transportation is provided from the Hotel to all the local entertainment parks so bring the family.**

## Announcement and Call for Papers

The 7th IEEE CPMT International Conference on High Density Microsystem Design and Packaging and Component Failure Analysis (HDP'05)

Date: June 27 – 30, 2005

Venue: Shanghai, China

Co-sponsored by

Shanghai Science and Technology Commission, Shanghai Government

IEEE CPMT Society

DaimlerChrysler SIM TECH, Shanghai, China.

Chalmers University of Technology, Sweden

IVF Industrial Research and Development Corporation, Sweden

IEEE CPMT Scandinavian Chapter

IEEE CPMT China Chapter

Shanghai Institute of Microsystems and Information Technology, China

Jiaotong University, China

SMIT Centre, Shanghai University, China

Microsystem design, manufacturing, assembly and packaging technology is playing a key technology for the progress of the microsystems and microelectronics industry in the world. China is not an exception. Therefore, many multi-national companies are establishing new facilities in China for expanding their global business and interest. Following the successful previous conferences, we are proud to announce the sixth International IEEE CPMT Symposium on High Density Microsystem Design and Packaging and Component Failure Analysis in Electronics Manufacturing (HDP'05).

**Scope for the Symposium:** The Symposium will cover the following areas and subjects:

- High density design and packaging including micro- and nanosystems, microelectronics and opto-electronics design and packaging, SOP, SIP, CSP, BGA, Flip-chip, Chip on Board, Surface Mount Technology and other novel emerging technology
- High density substrate including integrated passives and active devices
- MEMS and MOEMS design, packaging and assembly
- Microsystems manufacturing issues including cleaning issues, quality control, logistics, repair, process optimization, statistic process controls, ISO compliance, tooling or equipment, early manufacturing involvement initiatives and yield and test innovations used to enhance manufacturing processes or products related to high density substrates, single chip and multichip packaging, chip bumping and integrated component technologies
- Component failure analysis techniques including non-destructive X-ray, ultrasonic microscopy, IR-microscopy etc
- Simulation and modelling for packaging and microsystems and microelectronics manufacturing processes
- Thermal management
- Environmental design and materials development including life cycle analysis and end of life strategy etc
- Cost reengineering, improvements and analysis for electronics packaging processes and products

**Documentation:** The documentation from the conference will be published as an IEEE Conference proceedings with CD ROM with full length papers as well as in book form in English.

**Journal publication:** In addition, high quality papers will be selected for consideration to be published as special editions of the IEEE CPMT Transactions.

**Language:** English will be used.

You are welcome to submit an abstract with max 300 words that cover the topic, experimental approach, results and conclusions for the paper by February 28, 2005 Notification of abstracts will be made by March 15, 2005, Final paper is requested by April 30, 2005.

We are also interested to have exhibitors from materials, equipment suppliers to exhibit their products.

**Conference Chair:** Min Ren Fang, Shanghai University, China

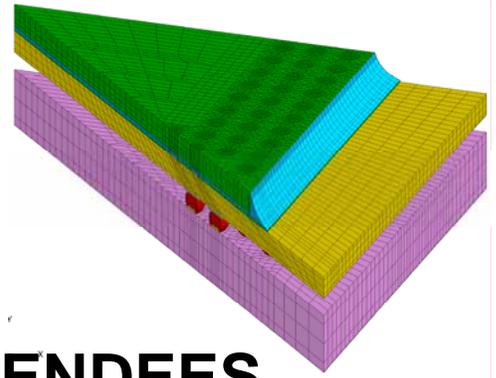
**Conference co-chair:** Johan Liu, SMIT Centre, Shanghai University, China and Chalmers University of Technology, Sweden

**Program committee Chair,** Mark Brinett, , Cisco, USA

**Program committee Co-Chair,** Xiaomin Xie, DaimlerChrysler SIM TECH, China

**Assistant program chair,** Qiao Wang, Ericsson, Sweden

For further information please contact Liqiang Cao at [lqcao@mail.shu.edu.cn](mailto:lqcao@mail.shu.edu.cn) or [johan.liu@mc2.chalmers.se](mailto:johan.liu@mc2.chalmers.se) at SMIT Centre, Shanghai, China and Sweden. Further information will be posted at the website at [www.smit-shu.com](http://www.smit-shu.com)



## CALL FOR ATTENDEES

Thermal, mechanical and multi-physics simulation and experiments in micro-electronics and micro-systems

April 17-20, 2005 -- Berlin, Germany

### **The Conference**

After five successful editions of the EuroSimE conference, a sixth edition is planned in 2005 and will take place in Berlin. This EuroSimE 2005 will address the results of both fundamental research and industrial application for **thermal, mechanical and multiphysics** solutions of (micro)-electronics, focusing on advanced **simulation** and **experiments**. The conference will include keynote presentations and sessions with a wide range of topics including, but not limited to:

#### **Subjects:**

- Mechanical simulation (static & dynamic)
- Thermo-mechanical simulation
- Thermal simulation (steady state & transient)
- Multi-physics simulation (coupled thermo-fluidic problems, coupled electro-mechanics, fluid-structure interactions)
- Validation of simulations by experiments
- Material characterisation, experiments and modelling
- Failure criteria and damage-modelling (fatigue, creep, delamination, cracks, buckling, large deformation, moisture-induced failures, yield)
- Process modelling
- Advanced numerical and analytical simulation methodologies and tools
- Behavioural modelling (HDL-A)
- Thin-film mechanics, interface strengths
- Simulation-based optimisation, virtual prototyping in product and/or process design
- Compact modeling and model order reduction

#### **Applications:**

- Components and packaging (traditional packages, flip-chip, BGA, CSP, Wafer-Level packages, MCM)
- MEMS (pressure, accelerometers, gyroscopes) and MOEMS
- Chip level reliability
- Nanotechnology
- Opto-electronic packages
- High Temperature Packaging
- Piezoelectric components
- Wafer processing and chip design
- PWB design and application
- Packaging for Harsh Environments
- Fluidic Components (microvalves, ink-jet nozzles, ...)
- Infrared sensors and cameras, thermal actuators

Local Organiser: Rainer Dudek

Email : [dudek@che.izm.fhg.de](mailto:dudek@che.izm.fhg.de)

## European System Packaging Workshop – Berlin Germany

January 31 – February 2, 2005

The 9<sup>th</sup> European Workshop of the IEEE CPMT and Computer Societies' Systems Packaging Committee will be held this year in Berlin, Germany, at the Park Inn Hotel, Berlin-Alexanderplatz. General Chair: Rolf Aschenbrenner (ISM Germany), General Co-Chair: Christine Kallmayer (IZM Germany)

### **Program**

**Keynote: "The History of Electronic Packaging" Evan Davidson (IBM US- Ret)**

**Session 1: Ambient Intelligence – Cian Mathuna (NMRC) and Christine Kallmayer (IZM)**

**Session 2: Biotechnology & Biomedical Technologies – Dr. Meyer and Melchholm Wilkinson**

**Session 3: Photonics & Interconnect Technology – Prof. Elmar Griese & Dr. Pdraig Hughes**

**Session 4: High Performance Computing – George Katopis (IBM US) & Paul Callender (Nokia)**

**Keynote: "Current View of Package Technology Opportunities in the 45 nm Silicon Generation" Bob Guernsey (IBM US)**

**Session 5: MNT Heterogeneous System Integration – Christian Val & Rolf Aschenbrenner**

**Keynote: "New Advances in System-in-a-Package" Prof. Rao Tummala (Georgia Tech)**



# CALL FOR PAPERS



9th IEEE WORKSHOP ON

## SIGNAL PROPAGATION ON INTERCONNECTS

Sponsored by the IEEE Computer Society – Test Technology Technical Council (TTTC)  
and by the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society

May 10-13, 2005

“Dorint Sporthotel”, Garmisch-Partenkirchen, Germany

During the last eight years, the IEEE Workshop on Signal Propagation on Interconnects has developed into a forum of exchange on the latest research results in this area. The aim of this ensuing workshop is to report on the most recent developments in the field of interconnect modeling, simulation and measurement on chips, boards, and packages. The event is also meant to bring together developers and researchers from industry and academia in order to encourage cooperation. In view of the last years' success, the committee is looking forward to the 9th IEEE Workshop on Signal Propagation on Interconnects where world class developers and researchers will share and discuss leading edge results in Garmisch-Partenkirchen, Germany. The workshop will be held in English. Detailed information about the workshop and its location are available on the website <http://www.spi.uni-hannover.de>. The committee is looking forward to your participation.

As already in the last years, the Committee intends to publish a CPMT special issue comprising selected papers from the SPI 2005 edition.

### Main topics of the workshop will include, but are not limited to:

- Frequency Domain Measurement Techniques
- Time Domain Measurement Techniques
- Modeling of Package & On-Chip Interconnects
- Macro-Modeling
- Simulation of Interconnect Structures
- Electromagnetic Field Theory
- Analysis and Modeling of Power Distribution Networks
- Propagation Characteristics on Transmission Lines
- Coupling Effects on Interconnects
- Substrate Effects
- Guided Waves on Interconnects
- Radiation & Interference
- Electromagnetic Compatibility
- Power/Ground-Noise
- Testing & Interconnects
- Optical Interconnects

### Submission of abstracts:

Those who wish to contribute to the workshop should send (by e-mail only) a formatted paper of up to four pages to the Program Chair by **January 31, 2005** (please see the submission instructions on our website <http://www.spi.uni-hannover.de> and use the author's kit provided there to ensure a consistent layout). If the paper is accepted, it will be reproduced, as is, in the workshop proceedings. Notification about acceptance will be given by March 14, 2005.

### Workshop Standing Committee:

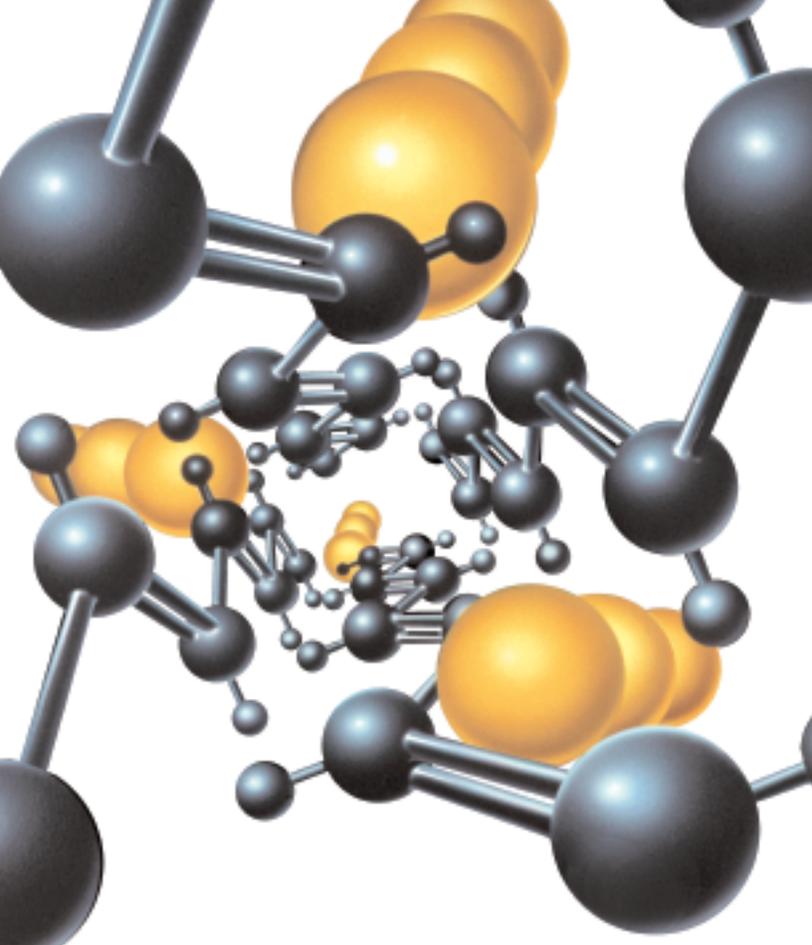
Flavio G. Canavero, Politecnico di Torino, Dipartimento di Elettronica, Torino (I); [canavero@polito.it](mailto:canavero@polito.it)  
Hartmut Grabinski, Univ. Hannover, Laboratorium für Informationstechnologie, Hannover (D); [grabinski@lfi.uni-hannover.de](mailto:grabinski@lfi.uni-hannover.de)  
Michel S. Nakhla, Carleton University, Department of Electronics, Ottawa (CAN); [msn@doe.carleton.ca](mailto:msn@doe.carleton.ca)  
Jose E. Schutt-Ainé, Univ. of Illinois at Urbana-Champaign, Electromagnetics Lab., Urbana, IL (USA); [jose@emlab.uiuc.edu](mailto:jose@emlab.uiuc.edu)  
Madhavan Swaminathan, Georgia Institute of Technology, Atlanta, GA (USA); [madhavan.swaminathan@ece.gatech.edu](mailto:madhavan.swaminathan@ece.gatech.edu)

**Chair:** Hartmut Grabinski, Laboratorium für Informationstechnologie, Schneiderberg 32, 30167 Hannover (Germany) - Phone +49-511-762-5030; Fax +49-511-762-5051; [grabinski@lfi.uni-hannover.de](mailto:grabinski@lfi.uni-hannover.de)

**Program Chair:** Uwe Arz, Physikalisch-Technische Bundesanstalt, On-Wafer Microwave Measurements (2.23), Bundesallee 100, 38116 Braunschweig (Germany) - Phone +49-531-592-2297; Fax +49-531-592-2228; [uwe.arz@ptb.de](mailto:uwe.arz@ptb.de)

### Technical Program Committee:

T.R. Arabi, Intel (USA)	E. Griese, Univ. Siegen (D)	J.L. Prince, Univ. of Arizona, Tucson (USA)
W. Bandurski, Univ. Poznan (PL)	H.-J. John, Siemens AG, Paderborn (D)	B. Ross, Teraspeed Consulting Group, (USA)
A. Cangellaris, Univ. Illinois (USA)	W. John, Fraunhofer IZM, Paderborn (D)	A. Rubio, Univ. UPC Barcelona (E)
J.L. Carbonero, ST (F)	G. Katopis, IBM, Poughkeepsie (USA)	A.E. Ruehli, IBM, Yorktown Heights (USA)
E. Chiprout, Intel (USA)	E. Kuh, Univ. of Calif., Berkeley (USA)	E. Sicard, INSA, Toulouse (F)
D. Deschacht, Univ. Montpellier II (F)	I. Maio, Politecnico di Torino, Torino (I)	G. Sommer, Fraunhofer IZM, Berlin (D)
T. Dhaene, Univ. of Antwerp (B)	N. van der Meijs, Univ. Delft (NL)	A. Weisshaar, Oregon State Univ. (USA)
H. Dirks, Univ. Kiel (D)	H.J. Pfeleiderer, Univ. Ulm (D)	T.M. Winkel, IBM, Böblingen (D)



# ACS/MRS/IEEE CPMT Organic Microelectronics Workshop

July 10 - 13, 2005  
Newport, Rhode Island, USA

The Workshop will bring together a broad spectrum of chemists, materials scientists, physicists, and engineers from both industry and academia in a stimulating forum to share information and ideas in the emerging field of Organic Microelectronics. The goal is to build an interdisciplinary community working on applications such as RFIDs, displays, sensors and photovoltaics while addressing some of the common scientific and manufacturing challenges to help these technologies advance in a more rapid, effective, and economical manner.

The technical program will focus on the areas of synthesis, theory, novel processing/ patterning/fabrication and device physics through a series of presentations by renowned invited speakers and poster sessions.

## Conference Chairs

Tobin J. Marks, Northwestern University  
Henning Sirringhaus, Cambridge University  
George G. Malliaras, Cornell University

## Location

Hotel Viking Newport  
One Bellevue Avenue  
Newport, Rhode Island 02840 USA  
Phone: 401-847-3300

Online reservations available at [www.hotelviking.com](http://www.hotelviking.com)  
(Group Code: #000015241)

Reservation Line: 1-800-557-7126

(Reference the Organic Microelectronics Workshop.)

The deadline to receive the group rate is June 13, 2005.

## Schedule Overview

July 10 - 6:00 pm - 8:00 pm

Welcome Reception  
Registration Opens

July 11 - 7:30 am - 8:30 am

8:30 am - 12 noon  
12 noon - 1:00 pm  
1:00 pm - 4:30 pm  
5:00 pm - 6:30 pm  
6:30 pm - 7:30 pm

Continental Breakfast/  
Registration Open  
Technical Program  
Lunch  
Technical Program  
Poster Session  
Dinner

July 12 - 7:30 am - 8:30 am

8:30 am - 1:00 pm  
1:00 pm - 6:00 pm  
6:00 pm - 7:00 pm  
7:00 pm - 9:30 pm

Continental Breakfast  
Technical Program  
"Free time" (Lunch on own)  
Dinner  
Technical Program

July 13 - 7:30 am - 8:30 am

8:30 am - 1:00 pm  
1:00 pm

Continental Breakfast  
Technical Program  
Adjourn

## For Additional Information

[www.organicmicroelectronics.org](http://www.organicmicroelectronics.org), online registration available  
Phone: 202-872-4600, Toll free: 1-800-227-5558  
E-mail: [acsprospectives@acs.org](mailto:acsprospectives@acs.org)



## **CALL FOR ABSTRACTS**

# **Second International Workshop on Nano & Bio-Electronic Packaging**

**March 22-23, 2005, Atlanta, Georgia**

Program Agenda and Further Information: [www.prc.gatech.edu/nanobiopack](http://www.prc.gatech.edu/nanobiopack)

The "Second International Workshop on Nano and Bio-electronics Packaging" is a two-day event offering informative keynote presentations and technical sessions on Nano technology. The currently scheduled technical sessions and their chairs are as follows:

### ***Nano Package Design***

James Libous - IBM & Madhavan Swaminathan - Georgia Tech

### ***Nano Biomedical Packaging***

Jorma Kivilathi - Helsinki University of Technology and Terry Dishongh - Intel

### ***Nano Photonics***

Avi Bar-Cohen - University of Maryland and Ephraim Suhir - Designed Nano-Materials

### ***Nano Packaging Materials***

Goran Matijasevic - University of California

### ***Nano Manufacturing***

Srinivas Rao - Solectron and Randy Rannow - Hewlett-Packard

### ***Industry Perspective***

Charles Lee - Infineon, Singapore

### ***NEMS & Fluidics***

Michael Wahl - University of Siegen

### ***Nano Interconnections***

Andrew Tay, National University of Singapore

### ***Nano Lithography***

Ajay Malshe, University of Arkansas

### ***Nano Testing, Modeling and Imaging***

Sheng Liu, Wayne State University

**Conference Coordinator:** Dr. Swapan Bhattacharya ([swapan@ee.gatech.edu](mailto:swapan@ee.gatech.edu))

An IEEE-CPMT Society workshop, sponsored in cooperation with NEMI and the Georgia Tech Packaging Research Center

---

---

**First**

# International Workshop

**on 3S** (SOP, SIP, SOC)

# Electronic Technologies

---

**September 22 & 23, 2005**

**Global Learning & Conference Center at Technology Square --84 Fifth Street, Atlanta, GA, 30308 USA**

**Sponsored by Georgia Tech's Packaging Research Center and the IEEE-CPMT Society**

**General Chair:** Rao R. Tummala, Director, Packaging Research Center, Georgia Institute of Technology

**for more information on web : [www.prc.gatech.edu/3s](http://www.prc.gatech.edu/3s)**

The SOP paradigm changes the current chip-centric SOC methodology to a cheaper, faster-to-market IC-package-system co-design flow. The advantages of the SOP paradigm over SOC appear overwhelming due to SOP's design simplicity, lower cost and higher system function integration, electrical performance, without the intellectual property issues that dominate SOC. The SOP is also different from and offers advantages over 3D packaging and SIP. The 3D packaging is typically stacking of similar, or dissimilar, chips such as DRAMS. The SIP goes beyond to embed both actives and passives but the passives are discrete, thick and bulky components. The SOP goes one step further in the ultimate 3D integration of components in thin film form at microscale, in the short term, and nanoscale in the long term. The SOP focuses on integrating both single function as well as heterogeneous system functions, optimizing ICs for transistors and package for integration of digital, RF, optical, sensor and others. It accomplishes this by both build-up SOP, similar to ICs and stacked SOP, similar to parallel board fabrication.

This workshop reviews the latest R & D and manufacturing status of each of the 3 electronic technologies around the world. It will also attempt to compare and contrast SOC, 3D stacking, SIP, SOP and MCM.

## SOP, SIP, SOC and 3D Technologies

- Mixed Signal Design
- Embedded Digital integration and modules
- Embedded RF integration and modules
- Fabrication and Assembly
- Mixed Signal Reliability
- Stacked Packages
- Applications & Products
- Mixed Signal Tools
- Embedded Optical integration and modules
- Multifunction integration and modules
- Mixed Signal Test
- Stacked ICs
- Manufacturing