

First International Workshop on 3S Electronic Technologies

September 22 & 23, 2005

Global Learning & Conference Center
at Technology Square
84 Fifth Street, Atlanta, GA, 30308 USA

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The SOP paradigm changes the current chip-centric SOC methodology to a cheaper, faster-to-market system-driven IC-package-system co-design flow. The advantages of the SOP paradigm over SOC appear overwhelming due to SOP's design simplicity, lower cost, higher system function integration and electrical performance, without the intellectual property issues that dominate SOC. The SOP is also different from, and offers advantages over, 3D and SIP. The 3D packaging is typically stacking of similar, or dissimilar, chips such as DRAMS. The SIP goes beyond to embed both actives and passives with different functions but the passives are discrete, thick and bulky components leading to sub-system modules. The SOP goes one step further in the ultimate 3D integration of components in thin film form at microscale, in the short term, and nanoscale in the long term leading to system boards.. The SOP focuses on integrating of both single function as well as heterogeneous system functions, optimizing ICs for transistors and package for integration of digital, RF, optical, sensor and others. It accomplishes this by both build-up SOP, similar to ICs and stacked SOP, similar to parallel board fabrication.

This workshop reviews the latest R & D and manufacturing status of each of these 3 "hottest" electronic technologies around the world. It will also attempt to compare and contrast SOC, 3D stacking, SIP, SOP and MCM.



Online registration & program updates:

<http://www.prc.gatech.edu/3s>

CALL FOR ABSTRACTS

Due June 15, 2005

Send abstracts (300 words or less) to Program Coordinator Boyd Wiedenman at boyd.wiedenman@ece.gatech.edu

Keynote Speakers

SOC - TBD

SOP - TBD

SIP - TBD

Sessions

Mixed Signal Design & Tools

Embedded Passives & Capacitor

Embedded Optical Integration & Modules

Embedded RF Integration & Modules

Multifunction Integration & Modules

Wafer Level Nano Interconnects & Assembly

Mixed Signal Test

Mixed Signal Reliability

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