



ISEPT - China

CALL FOR PAPERS

Sixth International Symposium on

Aug. 30 - Sept. 2, 2005

Electronics Packaging Technology

Shenzhen, China

Who Should Attend: Attendees of this conference in the past have been researchers, developers, producers and users of packaging technology for IC, MEMS, optoelectronics, LEDs, LCDs, magnetic heads, sensors and PC Boards and assembly. There were over 400 attendees at the past five ISEPT conferences in China.

Conference Chair: Keyun Bi, China Electronic Technology Corporation, China

Co-Chair: Rao R. Tummala, Georgia Institute of Technology, U.S.A.

General Secretary: Xiang Wu, China Electronic Technology Corporation, China

Organizing Committee

Chunqing Wang, Harbin Institute of Technology -
wangcq@hit.edu.cn

Fuhan Liu, U.S.A. - fliu@ece.gatech.edu

Y. C. Chan, Hong Kong

K. N. Chiang, National Tsing Hua Univ., Taiwan

Sei Ichi Denda, JIEP, Japan

William T. Chen, ASE, U.S.A.

Shenli Fu, I-SHOU Univ., Taiwan

S. T. Gao, Heibei Inst. Semiconductor

Ken Gilleo, Cookson, U.S.A.

Yifan Guo, Conexant Systems, U.S.A.

Peter Ku, Chipmos, Taiwan

John H. Lau, Agilent, U.S.A.

Dale Lee, Valor, U.S.A.

Ning-Cheng.Lee, Indium, U.S.A.

Ricky Lee, H.K.S & T Univ., Hong Kong

M. Y. Li, China

T. B. Lim, IME, Singapore

Charles Lin, Bridge Semiconductor, Taiwan

C. Y. Lu, Ardentec, Taiwan

James E. Morris, PSU, U.S.A.

Michael O'Donoghue, IMAPS, U.S.A.

Kyung W. Paik, KAIST, Korea

Bruce Romenesko, JH Univ., U.S.A.

Sarah Shen, Kingston, U.S.A.

Tadatomo Suga, Tokyo Univ., Japan

K. Suganuma, JIEP, Japan

S. Wakabayashi, Shinko, Japan

C. Q. Wang, China

Richard Wang, Amertron, U.S.A.

C. P. Wong, U.S.A.

Feijian Wu, Chipbond, Taiwan

Jianhua Wu, Anadigics, U.S.A.

Y. P. Wu, China

C. P. Yeh, Innosis, Taiwan

Phil Zarrow, ITM, U.S.A.

Abstracts due May 25, 2005: If you are interested in presenting a paper at this conference, please send an abstract (500-1000 words) via email to wangcq@hit.edu.cn. Please include your affiliation, email address, postal code, mailing address, and phone number in your submission.

System Packaging

SIP, SOP, 3D

Electrical & Mechanical Design

BGA, CSP, MCM, flip chip, 3D package, WLP, SIP

Materials & Processes

Underfill, thin films, coatings, substrates

Reliability

Modeling and testing analysis

MEMS, LED & Optoelectronics Packaging

Materials, processes, applications

High Density Substrates & Dielectrics

Advanced technologies & materials, processing

Surface Mount Technology

Screen print, picking up, reflow, AOI, equipment

Manufacturing

Modeling, yield and cost

Flip Chip & Wafer Level Packaging

Lead-free materials, bumping, soldering, assembly processes

Posters

CIE



EPTS

Sponsored by Electronics Packaging Technology Society (EPTS, CIE) and the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society