

First International Workshop on 3S Electronic Technologies

September 22 & 23, 2005

Global Learning & Conference Center at
Technology Square

84 Fifth Street, Atlanta, GA, 30308 USA

General Chair: Prof. Rao R Tummala, Director GT-PRC
Technical Chairs: Erich Klink (IBM) & Evan Davidson (IBM-ret)

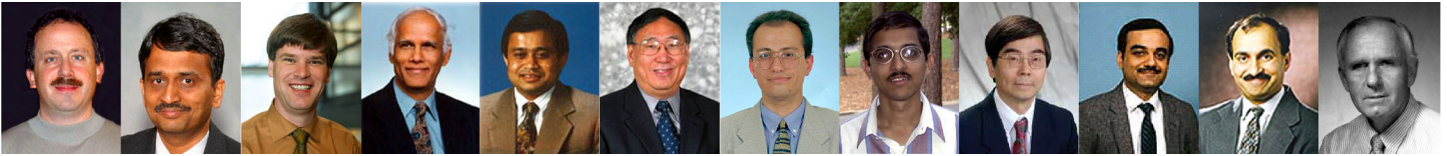
Program Coordinator: Boyd Wiedenman
boyd.wiedenman@ece.gatech.edu



CALL FOR ABSTRACTS

Due June 15, 2005

Send abstracts (300 words or less) to Boyd Wiedenman:
boyd.wiedenman@ece.gatech.edu



Packaging of electronics is no longer making discrete components and interconnecting them, since it leads to bulky, costly and low-performance and low-reliability systems. The new and emerging paradigm is about package and systems integration enabled by thin film component integration leading to ultra miniaturized, lower cost, higher performance and higher reliability systems. This Package integration is taking place every where—at IC level, package or module level and at system level. At IC level, it is by means of a package overlay on CMOS; at module level, it is by means of SIP; and at system level, it is by means of SOP. The SOP paradigm changes the current chip-centric SOC methodology to a cheaper, faster-to-market, system-driven, IC-package-system co-design flow. The advantages of the SOP and SIP paradigms that are based on package integration appear overwhelming due to their design simplicity, lower cost, higher system integration and electrical performance, without the intellectual property issues that dominate SOC. While package integration is common, SOP and SIP are different. The 3D packaging is typically the stacking of similar or dissimilar chips. The SIP goes one step beyond by stacking packaged components leading to sub-system modules. The SOP is the ultimate 3D integration of thin film components at IC, package and system levels leading to heterogeneous digital functions.

This workshop reviews the latest R & D and manufacturing status of each of these 3 “hottest” electronic technologies around the world. It will also attempt to compare and contrast SOC, 3D stacking, SIP, SOP and MCM.

Keynote Speakers

System-In-Package (SIP) - Ken Brown, Mgr. Non-CPU Packaging (Intel)

System-In-Package Roadmap – Joe Adams (Sky Works)

System-On-Chip (SOC) - Mahesh Mehendale, TI Fellow (TI)

Wafer Level SIP - Pieter Hooijmans, V.P. & RF Program Mgr. (Philips)

SOCs with 3D Interconnects – Bernie Pogge, IBM Fellow (IBM)

System-On-Package (SOP) - Rao Tummala, Director (GT PRC)

Sessions/ Chairs

Mixed Signal Design & Tools - Madhavan Swaminathan (GT PRC)

Embedded Optical Integration & Modules - Gee-Kung Chang (GT PRC) & Ray Chen (University of Texas)

Embedded RF Integration & Modules - Manos Tentzeris (Georgia Tech PRC)

SOP Fabrication in Ceramics vs. Organics - Venkatesh Sundaram (Georgia Tech PRC)

Wafer Level Assembly - C. P. Wong (GT PRC) & Dr. Luu Nguyen (National Semiconductor)

Mixed Signal Electrical Test - Abhijit Chatterjee (GT PRC)

Mixed Signal Package Reliability - Suresh Sitaraman (GT PRC)

SIP – Joe Adams (Sky Works) & George Conner (Philips)

Embedded Actives & Passives – Dr. Mahadeva Iyer (IME, Singapore)

Panel Discussion

SOP vs. SIP vs. SOC – Rao Tummala

Online registration & program updates:

www.prc.gatech.edu/3s

