Components, Packaging, and Manufacturing Technology Society Newsletter

IEEE

CPMT

The Global Society for Microelectronics Systems Packaging

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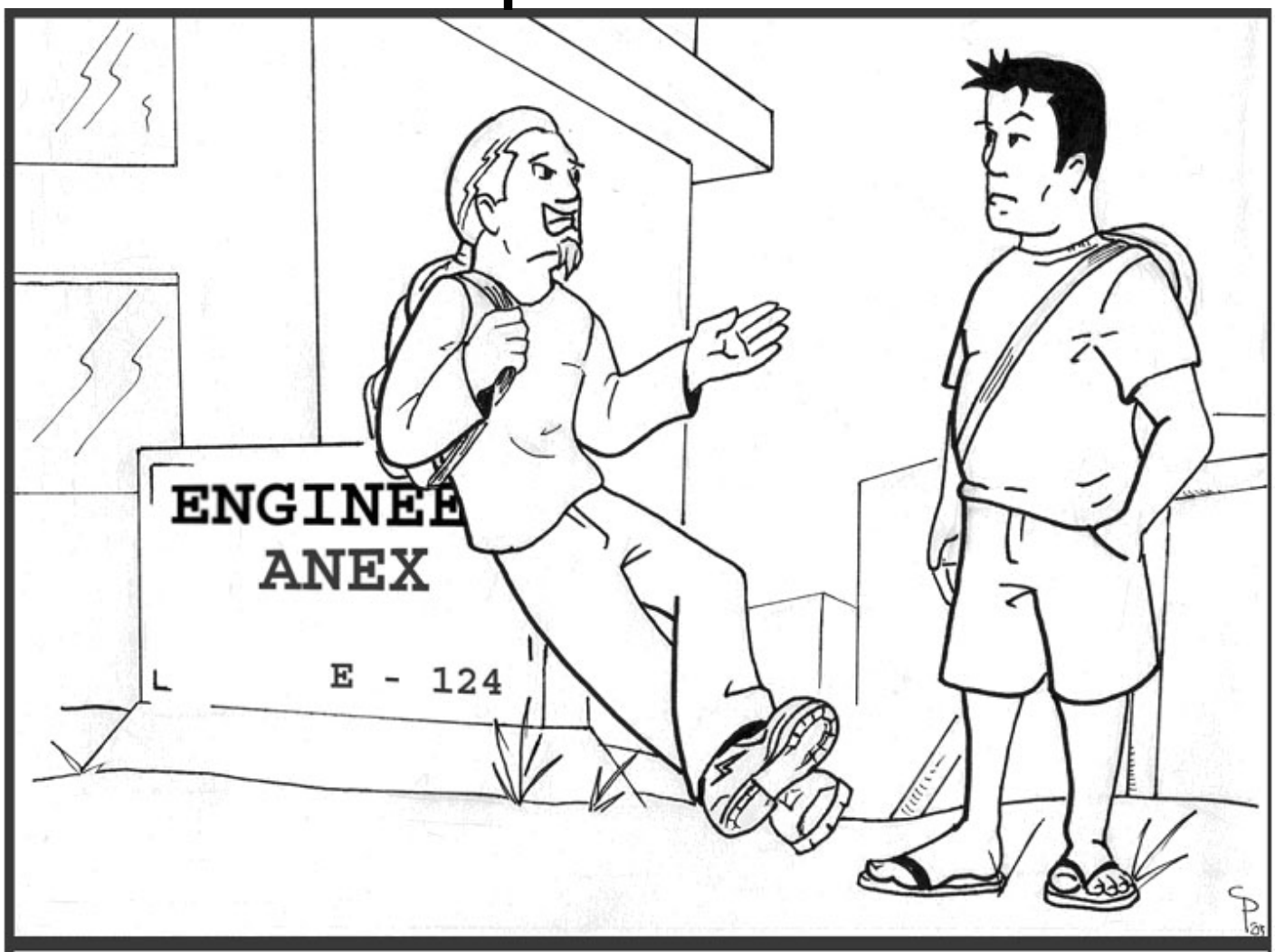
www.cpmt.org
www.ewh.ieee.org/soc/cpmt/newsletter

Student's Perspective of Globalization



MY ADVISOR SAYS INDIA, CHINA, AND JAPAN HAVE TAKEN OVER THE DESIGN, DEVELOPMENT, AND MANUFACTURE OF SOFTWARE AND ELECTRONICS. BUT DON'T WORRY! WHEN PEOPLE NEED GOOD FRIES, OR OBNOXIOUS LAWYERS, THEY WILL HAVE TO COME TO US.

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Next News Deadline: December 5, 2005

Members-only Web:
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Beginning a New Era

With this issue, we bid farewell to our gallant NEWSLETTER editor for about the last 20 years - Dr. David Palmer of Sandia National Laboratories. We've become so accustomed to emailing him our news, conference information, and committee updates that it's going to be hard to make the adjustment. Yes, Dave will still be around, but he has found other hobbies to occupy his spare time. We'll miss you, Dave!

Beginning with the December issue, we introduce Dr. Vasudeva Atluri of Intel Corp in Chandler, AZ USA as the editor of the CPMT Society's NEWSLETTER. Vasu has been very active in the Phoenix Chapter over the past 15 years, serving as Chapter Chair and as Workshops Chair. He even served a term as Chair of the Phoenix Section. Besides organizing events and bringing in funds for the Section and Chapter, he also founded the Section's Student Scholarship Endowment.

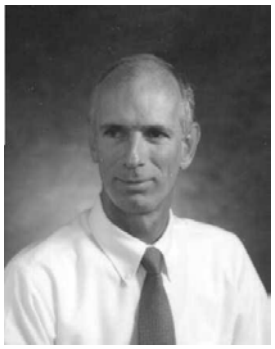
He is Silicon Integration Manager in Assembly Technology Development at Intel, with interests in electronic packaging. His group is responsible for ensuring that all technical issues are properly managed to enable successful interface between silicon and assembly technology development groups, with a major focus on first-level interconnects. He is also responsible for the design of test chips that help validate performance and reliability of silicon after it has been packaged and helps in defining design rules for product designs.

His BS degree is in Chemical Engineering, and he went on to get three advanced degrees from University of Arizona (Tucson, Arizona) including M.S. in Materials Science and Engineering, M.S. in Metallurgical Engineering, and a Ph.D. in Materials Science and Engineering with a minor in Electrical Engineering and specialization in Silicon fabrication. He is an inquisitive individual, with good editing skills developed on in-house Intel publications, and I'm sure you will all enjoy working with him and reading the CPMT news in future issues.

As a final paragraph, I want all CPMT Members to know about the spiffy new interface to IEEE's XPLORE on-line research site (ieeexplore.ieee.org). You no longer need to be an IEEE Member to scan journal tables of contents, retrieve abstracts, and run full-text or keyword searches (even "saved searches" that email you when a new paper gets posted that meets your criteria!) Any researcher is encouraged to set up his/her own "MyXPLORE" account, at no cost. Of course, only Members/subscribers can download the actual papers - but these days, many of you have IEL/XPLORE subscriptions to the full IEEE collection (1.2 million papers, and all of CPMT's papers back to 1954), so you are welcome to retrieve as many as you like. We encourage you to use this prior art in solving your current problems and guiding your next efforts.

And I forgot to tell you - you can use Google to search the full IEEE collection, including full-text search; IEEE has released all the metadata and text of the papers for the Google engine to catalog. How cool is that!? So, the next time you wonder what has been done already in your areas of interest, do a quick XPLORE or Google search and see what your fellow professionals have been publishing on the subject.

--Paul Wesling, Vice President Publications



Paul Wesling, VP Publications

Rao Bonda, CPMT Awards

CPMT Board to Meet in Dallas

The first week in November is traditionally when the many committees of the ECTC meet near the Dallas Airport for selection from the submitted abstracts for the June meeting to be held in San Diego. In conjunction with this gathering, all day Saturday November 5, your Board of Governors will be meeting under the leadership of President Phil Garrou. The Board encourages any ECTC volunteers that want to do more for the CPMT Society to stay for part of this meeting. In addition, CPMT members in the Dallas area who would benefit from more networking and volunteer work with their colleagues from across the world are invited to attend. Please contact Executive Director, Marsha Tickman, at telephone 1 732 562 5529 to reserve a chair and nourishment. For example, this Newsletter would benefit from a new volunteer showing up with a camera and a zest to summarize the meeting in a catchy way now that the old editor has run out of steam. -- submitted by Dave Palmer

Editor's Turn

I am just an acting editor for this issue, giving our new editor, Vasu Atluri, a chance to enjoy his hard earned Intel Sabbatical before picking up the yoke of this Newsletter. My thanks again for those that sent in material for this issue, particularly Yan Zhang for the great coverage of the Shanghai HDP05 meeting, Jan Vardaman and Luu Nguyen for IEMT coverage, and Paul Wesling for picking up the slack. In addition, many of our members on conference program committees have submitted calls to give opportunities to all members.

What can you do as a member to keep your Society helping your colleagues and yourself?

Support those long term outputs by CPMT:

Transactions: submit articles and try to scan each issue for at least one article that can help your interests. Electronically scan all past issues when you are starting work in a new technology area.

Meetings: Go to one CPMT meeting a year. Submit a paper if you have only been an attendee to date. Become a session co-chair if you want to start networking with engineers that think your projects are interesting.

Newsletter: read it quickly and pass it on to one of the many engineers in your workplace that never quite get around to joining the Society that helps all of us.

Lastly, when it is time to stop being a volunteer, Stop. Don't let anyone convince you to do "one more newsletter". Even a boring person, like an editor, has many rewarding ways to invest their time.

CPMT Shanghai HDP'05 Success

With the support and help of the Science and Technology Commission of the Shanghai Government, the 7th IEEE CPMT International Conference on High Density Microsystem Design, Packaging and Component Failure Analysis (HDP´05) has been successfully held in Shanghai University.
This conference is sponsored by the IEEE CPMT and undertaken by SMIT Center, Shanghai University. We were honored to have Baiyu Guan, Deputy Director of the Department for Major Projects for Component and Devices, Ministry of Electronics Industry, P. R. China, Jianping Wang, Deputy chief-engineer of Science and Technology Commission of Shanghai Municipality, Ricky Lee, vice president of IEEE CPMT, Min Wang, vice-president of Shanghai University, and Lars Andreasson, general consul of Sweden in Shanhgai to give opening speeches for the conference.

There were more that 120 participants coming from more than 20 countries and regions, including the USA, UK, France, Sweden, Japan, Malaysia, Singapore, Finland, Hong Kong and Taiwan, and there were about 85 papers published. And we were much honored to have famous electronics package experts such as Prof. C. P. Wang, Prof. Ricky Lee, Prof. James E. Morris, Dr. Shangguan Dongkai, Mr.Wong Ee Hua, and Multi National Companies (MNCs) such as Intel, Kingston, Huawei and large universities such as Shanghai University, Fudan University, Central South University, Hua Zhong Central University of Science and Technology, Dalian University of Science and Technology, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Science and other famous universities and institutes to participate in the conference.

--Submitted by Yan (Emilia) Zhang

Dr. Dongkai Shangguan

Mr. Wong Ea Hua

Professor Thorvald Andersson, Chalmers Univrsity of Technology, Sweden at poster session

Visit to Flextronics, Shanghai

Ricky Lee, vice president of IEEE CPMT

Visit by the Consulate General of Sweden, Shanghai

IEMT Success in Bay Area

The 30th International Electronics Manufacturing Technology Symposium (IEMT'05) was held in San Francisco on July 11-12, just before the Semicon West show. The IEMT, an international forum on electronics components and systems manufacturing, was a joint effort between SEMI and the IEEE CPMT society. The theme addressed this year involved "Manufacturing at the Wafer Level".

About 70 people attended the conference featuring invited talks on wafer level packaging, packaging for Cu low-k, system-in-packages (SiP), and testing of memory devices.

IEMT is offered as a technical formal symposium held at the large trade show in San Francisco sponsored by SEMI

E. Jan Vardaman congratulates Bob Pfanl for his Electronics Manufacturing Technology Award while Bill Chen hosts occasion.

Four professional development courses were offered on July 11, but due a technicality, only three were actually held. Attendance was as follows:

Introduction to Flip Chip Technology - A user's guide by Dev Gupta: 31;

Advanced packaging to today's solutions by Ray Fillion: 54;

Introduction to nanotechnology by Florin Ciontu and Bernard Courtois: 46.

Sanjeev Sathe of ASE started the conference with an overview of the "Evolution of wafer level CSP in high volume implementation". Extension of wafer level CSP to higher functionality applications and the challenges involved was covered by Luu Nguyen of National Semiconductor in "Beyond low pin count WLP". Challenges in memory testing with a potential for WLP applications were covered by Beth Skidmore of Micron Technology in "Bare die testing - DRAM/PSRAM". Issues in packaging Cu/low k devices were outlined by Kishor Desai of LSI Logic in "Packaging challenges for Cu low-k silicon technologies."

Before the luncheon talk, the 2005 IEEE Electronics Manufacturing Technology Award was given to Bob Pfahl of iNEMI for "his prominent role in reducing environmental impact from electronic manufacturing processes and fostering collaboration within the manufacturing technology community." Afterwards, the luncheon speaker, Tom Gregorich of Qualcomm, covered SiP and RF integration challenges in "SiP solutions."

Deborah Keller of Intel highlighted the value propositions of SiP in "Rebirth of SiP." "Implementation of chip scale modules in wireless mobile devices", and especially strategies for lowering module costs, was addressed by Yinon Degani of Sychip. Closing out the afternoon focus on SiP, Mike Buckley of Henkel Technologies outlined issues involved with "Development of a SiP test package, and the evaluation of a SiP material set".

Co-located with a number of other events organized by SEMI, conference attendees were also able to benefit from the Semicon West Keynote Speaker, Dr. Tien Wu, President of ASE Americas and VP of Strategic Marketing and Sales, Europe, talking about the state of the semiconductor industry in "SEMI Play or SEMI Syndrome?"

The next IEMT is planned to be in San Jose, CA USA with a Call For Papers to be issued shortly. The Professional Development Courses were held in the Moscone Convention Center and Marriott Hotel. For the last few years the Packaging part of SEMICON West was held in San Jose but in the much larger Moscone Center both wafer and packaging were located together to give more interaction.

The presentations from IEMT'05 are being placed on the CPMT Members-Only website, for download – get them now at **www.cpmt.org/mem**/.

-- submitted by Luu Nguyen, National Semiconductor

New Senior Members

Shuhe Li -- Los Angeles, California
Rod I Martens -- Oakland-East Bay, California
Kimberly E. Newman -- Denver, Colorado
Sante Saracino -- Central & South Italy
P. R. Suresh -- Bangalore
Robert J. Wenzel -- Central Texas
Tao Zhang -- Shanghai Subsection

Congratulations to the new Senior Members in CPMT. For those not yet senior members, please look up "Senior Member" at "www.ieee.org". If you have been a college student and engineer for a total of ten years you probably qualify. If you have been active in local or global IEEE activities you probably know a few senior members that will be glad to write a few words of recommendation. If you don't know who could help your nomination, write to the CPMT Executive Director, Marsha Tickman (m.tickman@ieee.org) to get a list of possible supporters.

CALL FOR NOMINATIONS

2006 IEEE COMPONENTS, PACKAGING & MANUFACTURING TECHNOLOGY

IEEE's Components, Packaging & Manufacturing Technology Award is presented for meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies.

The Award is sponsored by the CPMT Society. The recipient of the award receives a bronze medal, certificate, and cash honorarium.

This IEEE CPMT Award was established in 2002. The technical field for this award includes all aspects of device and systems packaging including packaging of microelectronics, optoelectronics, RF and wireless and micro-electro-mechanical systems (MEMS).

This award may be presented to an individual or a team of not more than three.

The award is administered by the Technical Field Awards Council of the IEEE Awards Board.

The nomination deadline is 31 January 2006. For nomination forms, visit the IEEE Awards Web Site, www.ieee.org/awards, or contact:

IEEE Awards Activities
445 Hoes Lane,
Piscataway, NJ, USA
08855-1331

tel: +1 732 562 3844; email: awards@ieee.org.

--submitted by Dennis Olsen

ECTC Now Looking for Organic Device Packaging

You might be interested in a new development for ECTC next year. The Emerging Technologies program committee has added "Organic Device Packaging" to the two topics which ran in 2005, ("Nano-scale Packaging" and "Biomedical Packaging.") The title should be interpreted liberally, since papers in all aspects of organic device development will be considered, not just those on packaging. (Of course, other areas of polytronics will continue to be included in the regular program.) Full details can be found at www.ectc.net The abstract deadline is October 15th

--submitted by Jim Morris

Upcoming Conferences - Calls for Papers and Announcements

**11th International Workshop on Thermal investigations of ICs (THERMINIC'05) -- Lake Maggiore, Italy -- 27-30 September 2005
**IEEE/CPMT Workshop on 3S Electronic Technologies: SOP, SiP, SOC -- Atlanta, GA USA -- 22-23 September 2005
**POLYTRONIC'05: IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics -- October 23-26, 2005 -- Wroclaw, Poland
**Future Directions in IC and Package Design Workshop (FDIP'05) -- October 23, 2005 -- Austin, TX USA (see EPEP, below)
**14th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP 2005) -- October 24-26, 2005 -- Austin, Texas
**Phoenix Section Workshop: Devices, Interconnects, and Packaging for Next Generation computing and Communication Applications -- November 10, 2005 -- Arizona State University, Tempe, Arizona.
**7th Electronics Packaging Technology Conference (EPTC 2005) -- 7-9 December 2005 -- Singapore
**Printed Electronics USA2005 -- December 6 - 9, 2005 -- Naples, Florida USA -- www.printelec.com
**International Conference on Electronics Materials and Packaging (EMAP 2005)-- 11-14 December, 2005, tokyo Institute of Technology.
**Electrical Design of Advanced Packaging and Systems (EDAPS) -- 12-13 December, 2005 -- Bangalore, India
**International Symposium and Exhibition on Advanced Packaging Materials -- March 15-17, 2006 -- Georgia Tech, Atlanta Georgia. Info at e-mail: jianmin.qu@me.gatech.edu
**Third International Workshop on Nano & Bio-Electronic Packaging -- Call for Papers -- March 20-22, 2006 -- Atlanta, GA USA
**ISQED 206, International Symposium on quality Electronic Design -- March 27-27, 2006 -- San Jose, California.
**ITERM -- May 30 thru June 2, 2006 -- San Diego, CA USA Electronic Components and Technology Conference, ECTC -- May 30 to June 2 -- San Diego, CA USA
**International Conference on High Density Microsystem Design, Packaging and component Failure Analysis (HDP'06) -- June 27-30, 2006 -- Shanghai University, China

IEEE Election is Afoot

This is the time of year to choose whom you would like to see in leadership positions at the IEEE. We hope that you will take the time to complete and submit your ballot.

Election ballots have been mailed to all IEEE members who are eligible to vote. If you have not already received yours, it should be arriving soon. Contact the IEEE at corp-election@ieee.org if you do not have your ballot. To help you make an informed decision this voting season, please visit the election Web site at:

http://www.ieee.org/elections

There, you can link to the candidates' statements and their background information.

In 2005, members may choose from one of several ways to cast their ballots.

-- submitted by Lyle M. Smith

CPMT Volunteers in Action

Luu Nguyen, USA West Coast Industry tech leader

Connie Swager, USA East coast wonder

Andrew Tay, Southeast Asia Packaging

Build a career firmly on a foundation of 1mil wire: George Harman and Rolf Aschenbrenner

CPMT Award Nominations Requested

IEEE-CPMT Society Awards for Year 2006
(Nomination Due Date: January 31, 2006)

CPMT Society offers the following awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and CPMT Society.

David Feldman Outstanding Contribution Award: To recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.
Prize: $2,500 and Certificate
Basis for Judging: Contributions to the organization or enterprises connected with the field, to CPMT Chapter, Section or Board of Governors activities, and to the fields encompassed by the CPMT Society.
Eligibility: Recipient must have been a member of IEEE and CPMT for the past five (5) years, including 2005.

Outstanding Sustained Technical Contributions Award: To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society.
Prize: $2,500 and Certificate
Basis for Judging: Technical contributions must be sustained and continuing over a period of at least five (5) and preferably 10 years. One major contribution will not qualify. Contributions must be documented by open literature publications such as papers, patents, books and reports (available to the public).
Eligibility: Must have been a member of the IEEE and CPMT Society for the past three (3) years, including 2005.

Electronics Manufacturing Technology Award: To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society.
Prize: $2,500 and Certificate
Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Work in the management of CPMT conferences or its BoG may be contributory but not sufficient to receive the award.
Eligibility: No need to be a member of IEEE and CPMT Society.

Exceptional Technical Achievement Award: To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the CPMT Society.
Prize: $2,500 and a Certificate.
Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in CPMT's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.
Eligibility: Recipient(s) must have been a member of IEEE and CPMT for the past three (3) years, including 2005. There are no requirements for service to the IEEE or CPMT Society.

Outstanding Young Engineer Award: To recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.
Prize: $1,500 and Certificate plus one year free membership in CPMT with all CPMT Transactions.
Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the CPMT Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.
Eligibility: Must have been a member of the IEEE and CPMT (member grade or above) for the past three (3) years, including 2005, and must be 35 years of age, or younger, on December 31st, 2005. Please provide Date of Birth (Month/Year) to ensure eligibility.

Guidelines for Nominators:

Ø Minimum three reference letters must be submitted in support of all nominations. Reference letters can be provided by IEEE/CPMT members and non-members.
-- Past recipients of an award are not eligible to receive that same award. For the list of past awardees, see the CPMT Society Home page (**www.cpmt.org/awards**).
-- An individual may submit only one nomination per award but may submit nominations for more than one award.
-- It is the responsibility of the nominator to provide quality documentation to assist the Awards Committee in evaluating the candidate.
-- Please send nominations to CPMT Society Awards Committee Chair by e-mail, fax or mail:

Rao Bonda, Ph.D.
Freescale Semiconductor, Inc.
2100 East Elliot Road,
Mail Drop: EL725
Tempe, AZ 85284, USA
Phone: +1-480-413-6121
Fax: +1-480-413-4511

Email address: r.bonda@ieee.org or rao.bonda@freescale.com
Winners will be notified by 28 February 2006, and the awards will be presented at the 56th Electronic Components and Technology Conference, May 30- June 2, 2006, in San Diego, California, USA.

Sample Award form is on the follow pages

CPMT Society Awards for Year 2006 Nomination Form

(Due date: January 31, 2006)

AWARD SUGGESTED: *(See description at the end*) Check only one box.

[ ] David Feldman Outstanding Contribution Award
[ ] Electronics Manufacturing Technology Award
[ ] Outstanding Young Engineer Award*
(*Please provide Date of Birth: Month/Year to ensure eligibility)

[ ] Outstanding Sustained Technical Contribution Award
[ ] Exceptional Technical Achievement Award

PROPOSED CANDIDATE: (PLEASE TYPE OR PRINT)

Name:

Position:

Work Address:

Work Telephone: ( )

Email:

IEEE/CPMT Membership Years/Status:

The CPMT Society Awards Recognition Committee reserves the right to consider any nomination for awards other than the award suggested when, in its opinion, the support and justification may more appropriately apply to other CPMT Society awards.

1. Please state briefly why the nominee deserves of recognition, keeping in mind the purpose of the award and the individual's accomplishments. Please feel free to mail supporting documents to strengthen your nomination. Endorsement letters may be submitted separately. Self-nominations **will not** be considered. **(PLEASE TYPE OR PRINT)**

Date received by the CPMT Society Awards Committee:

Please provide the following information. Please note that the information you provide serves as the basis for the evaluations. The Committee will endeavor to confirm the validity of the information it receives, but it cannot supply or elaborate on statements.

2. What IEEE, CPMT Society (or other professional societies) responsibilities has the nominee had in the last five years that have been related to professional activities? (Please provide approximate dates.)

3. What specific significant or distinguished contributions or achievements made you decide to submit this nomination?

4. What factors suggest to you that these contributions or achievements are substantially above and beyond those reflecting the good job expected of any occupant of this position(s).

5. Please use this space to provide details concerning the nominee and his or her professional activities, contributions or achievements. Your comments should amplify your brief responses to items 1, 3, & 4. Exhibits may be sent separately. Please note that the evaluations are based upon accomplished and identifiable activities.

NOMINATOR:

Name: IEEE Member Grade:
Position: E-mail Address:
Work Address: Home Address:

Work Telephone: ( ) Home Telephone: ( )

If others are submitting endorsements to support this nomination, please provide their names and addresses.

Name	Address
Name	Address
Name	Address
Name	Address

- **Minimum <u>three</u> reference letters must be submitted in support of all nominations. Reference letters can be provided by IEEE/CPMT members and non-members.**

ESTC 2006

1st Electronics Systemintegration Technology Conference

September 5 - 7, 2006
Conference Center
Dresden, Germany

1st CALL FOR PAPERS Abstracts due February 1, 2006

Introduction

It's our pleasure to invite you to submit an abstract for the 1st Electronics Systemintegration Technology Conference (ESTC), to be held September 5 - 7, 2006 in Dresden. Germany.
This international conference is organized by the Electronics Packaging Laboratory (German abbrev.: IAVT) of Dresden University of Technology and the Association of Knowledge and Technology Transfer of TU Dresden Ltd. (German abbrev.: GWT). It is sponsored by the IEEE Components, Packaging and Manufacturing Technology Society (CPMT).
The ESTC comprises papers and topics covering a wide spectrum of the latest developments in all areas of micro- and nanosystems technology - e.g. assembly, packaging, system on package, quality and reliability, materials, optoelectronics, nano and bio packaging, and simulation.
We encourage you to submit an abstract on your recent unpublished work to the 1st ESTC. We hope to see you in Dresden.

Paper Submission

You are invited to submit a 500 word abstract that describes the scope, content and key points of your proposed paper. Please send the abstract to abstract@estc-conference.net.

The **abstract** must be received by **February 1, 2006**. Your submission must include the mailing address, business telephone number and facsimile number and email address of the presenting author and affiliations of all authors. Please indicate up to two major topics as listed in this announcement your paper should be assigned to.

Authors will be notified of paper acceptance with instructions for publication by April 1, 2006. At the discretion of the program committee, abstracts submitted may be considered for poster presentation.

Manuscripts are due in final form for publication in the Conference Proceedings by June 1, 2006.

Executive General Chair:
Klaus-Jürgen Wolter
Dresden University of Technology, Germany

Executive Program Chair:
Chris Bailey
University of Greenwich, UK

Executive Chair:
Thomas Zerna
Dresden University of Technology, Germany

Please visit the ESTC website
www.estc-conference.net
for additional conference information.

Major Topics

Papers presenting new developments and knowledge in the following areas are invited. The work submitted should be original and avoid the inclusion of commercial content.

⇒**Advanced Packaging:** New packaging technologies, systems packaging, designs, materials, and configurations addressing performance, density and thermal management for single chip, multichip, wafer-level, MEMS and power packages. Special emphasis on flip-chip, fine pitch and high lead count packaging in CSP, BGA, CGA, LGA and SMT packages, SiP and SoP solutions.

⇒**Materials & Processing:** Processes for IC Packaging that enhance performance (mechanical and electrical) and cost effectiveness. Technology, development and application of adhesives, encapsulants, chip underfills, solders and lead free alloys, magnetic and optical materials, ceramics, composites, dielectrics, thin films, nanomaterials, thermal materials, bonding and plating processes.

⇒**Optoelectronics:** Packaging for fiber-optic modules, infra-red wireless, consumer optoelectronics, flat-panel, projection and microdisplays, solid state lighting, optital amplifiers, lasers, detectors, OEICs, optical data interconnect, optical backplanes, passive components, and WDMs.

⇒**Manufacturing Technology:** Advanced process development and equipment improvement for wafer thinning, bumping, stacking, and low-k chip packaging, high-density interconnect and embedded component substrates, testing and burn-in. Emphasis on product level integration and optimization for different product applications, cost, yield, performance and environmental improvements, process characterization, new product introduction and ramp-up, design for flexible manufacturing and testing.

⇒**Microsystems Technology:** First-level electronic interconnection technologies, including flip-chip, 3D interconnect, lead-free interconnects, wire-bonding, TAB, and conductive polymers; under bump metallurgy, substrate metallurgy and interconnect, wafer and device level interconnection, electrical issues of advanced interconnect structures, novel interconnects, and electromigration of bumped interconnects.

⇒**Electrical Modelling:** Electrical modelling, simulation and characterization of packaging solutions including system-level applications. Prediction of electrical behaviour, signal integrity and functionality.

⇒**Thermal-Mechanical Modelling:** Multiphysics modelling and optimization, simulation and characterization of packaging solutions including system-level applications. Prediction of thermal and mechanical performance of packages and modules. Thermal design.

⇒**Emerging Technologies:** Nano-Scale Packaging, micro-to-nano transition and interfaces. Packaging of nano-scale electronic and sensing devices. Nano-materials, nano-patterning, nano-interconnections, and characterization. Nano-electro-mechanical systems (NEMS). Packaging of biomedical devices. Microfluidic devices. Biocompatible materials. Integrated biotech devices using sample preparation, processing and data communication, test procedures and results.

⇒**Quality & Reliability:** Assessment, failure analysis, reliability testing and data analysis, failure and acceleration models, qualification of components and systems, KGD, incremental quality improvement, and TQM.

⇒**Passive Components:** New passive or active component technologies, integrated embedded components, RF and wireless component applications, component performance, systems, and reliability.

⇒**Posters:** Papers may be submitted on any of the listed major topics; presentation of papers in a poster format is highly encouraged at ESTC.

⇒**Short Courses:** Proposals are also solicited from individuals interested in teaching educational short courses (4 hours) on topics described in the Call for Papers. Proposals including course descriptions must be submitted by February 1, 2006 to courses@estc-conference.net

IAVT GWT forschung+innovation IEEE CPMT IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Updated as of 12 September 2005

ADVANCE PROGRAMME

7TH ELECTRONICS PACKAGING TECHNOLOGY CONFERENCE (EPTC 2005)

7 – 9 DECEMBER 2005
GRAND COPTHORNE WATERFRONT, SINGAPORE

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International Microelectronics and Packaging Society

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For regular updates about the conference and registration, please visit

www.eptc-ieee.net

CALL FOR PAPERS

Abstract Submission: Please send your title and 300-word abstract, electronically, to nbep@ece.gatech.edu by **October 14, 2005**. For further info, please visit www.prc.gatech.edu/nanobiopack

Third International Workshop on — March 20-22, 2006

Nano & Bio-Electronic Packaging

Georgia Institute of Technology
Technology Square Research Building
www.gatech.edu/technology-square

General Chairs

Prof. Rao Tummala (rao.tummala@ee.gatech.edu), Director, Packaging Research Center - *Georgia Institute of Technology*
Prof. Z. L. Wang (zhong.wang@mse.gatech.edu), *Director, Center for Nanoscience & Nanotechnology - Georgia Institute of Technology*

Technical Chair

Prof. C.P. Wong (c.p.wong@mse.gatech.edu) - *Georgia Tech PRC (Others to be determined.)*

Conference Coordinator: Dr. Swapan Bhattacharya (swapan@ee.gatech.edu) - *Georgia Tech PRC*

International Planning Committee

Avi Bar-Cohen (abc@eng.umd.edu), *University of Maryland*
Karl Becker (becker@izm.fhg.de), *Fraunhofer Institute of Technology*
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Goran Matijasevic (goran@uci.edu), *University of California, Irvine*
Jim Morris (j.e.morris@ieee.org), *Portland State University*
Randy Rannow (randy.rannow@hp.com), *Hewlett-Packard*
Srinivas Rao (srinivasrao@ca.slr.com), *Solectron*
Andrew Tay (mpetayao@nus.edu.sg), *National University of Singapore*
Michael Wahl (michael@rs.uni-siegen.de), *Universitat Siegen*

SHORT COURSES — March 20

Half day course on Nano Packaging

Profs. C. P. Wong & Rao Tummala

PLENARY SESSION — March 21

Half day of keynote addresses from renown guests

TECHNICAL SESSIONS — March 21-22

Nano Biomedical Packaging

Jorma Kivilathi - *Helsinki University of Technology*
Roger Narayan - *Georgia Institute of Technology*

Nano Photonics

Avi Bar-Cohen - *University of Maryland*
Ali Adibi - *Georgia Institute of Technology*

Nano Packaging Materials

Goran Matijasevic – *University of California*
C. P. Wong - *Georgia Institute of Technology*

MEMS, NEMS & Sensors

Farrokh Ayazi - *Georgia Institute of Technology*
Ajay Malshe - *University of Arkansas*

Nano Interconnections

Andrew Tay - *National University of Singapore*

Nano Thermal Interfacing Materials

William Chen – *ASE Inc.*
Srinivas Rao – *Solectron*

Packaging of Nano Cu-Low K

G.Q. (Kouchi) Zhang – *Philips Semiconductors*

INFORMATION UPDATES

www.prc.gatech.edu/nanobiopack

IEEE

An IEEE workshop sponsored in cooperation with the IEEE-CPMT Society, iNEMI and the Georgia Tech Packaging Research Center

CPMT

iNEMI

Georgia Tech
ALTERNATIVE TO SYSTEM-ON-CHIP
SYSTEM-ON-PACKAGE
PACKAGING RESEARCH CENTER

ELECTRICAL DESIGN OF ADVANCED PACKAGING AND SYSTEMS (EDAPS)

4th Asian Workshop

12 and 13 December (Monday and Tuesday) 2005, Bangalore, India

Windsor Manor Sheraton & Towers, 25 Sankey Road, Bangalore 560052

Objective

The EDAPS Workshop is to enhance the technical awareness in the Asia region specifically in area of package and system electrical design concepts, issues and challenges ahead for next generation electronic products.

International Advisory Committee

Alina Deutsch : IBM Corp., USA
Andreas Cangellaris : Univ. of Illinois, USA
Andreas Weisshaar : Oregon State Univ., USA
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Rajkumar : Texas Instruments, India
Anil Kumar M : SLN Tech. Pvt. Ltd.
MK Gunasekaran: Indian Inst. Of Science, India

Joint Organisers

Technically sponsored by:
IEEE CPMT TC-12 Subcommittee on Electrical Design, Modelling and Simulation

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e-mail: ieee.cpmt.blr@gmail.com
URL: http://ewh.ieee.org/r10/bangalore/cpmt/events.html

14th Topical Meeting on
Electrical Performance of Electronic Packaging

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

EPEP 2005

October 24-26, 2005
Austin, Texas

Sponsors

The IEEE Components, Packaging and Manufacturing Technology Society

IEEE Microwave Theory and Techniques Society

Call for Papers

The **general subject of the meeting** is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. Authors are invited to submit papers describing new technical contributions in the areas broadly covered below:

- Current and future issues related to on-chip interconnections
- Router friendly models and modeling tools: accuracy & efficiency
- Modeling and design of high speed digital IO circuits: signal propagation and reception
- On-chip power delivery and regulation
- Advances in modeling core switching noise, and design of novel solutions
- On-chip measurement techniques
- Package analysis, including numerical methods
- Electromagnetic analysis tools
- Advances in transmission-line techniques
- Power distribution and package resonance
- Long distance propagation in large switching complexes
- Switching noise in multi-layered systems
- Macromodeling techniques
- Signal integrity in mixed signal integrated circuits
- Electrical issues in MEMS packaging
- New and innovative interconnect packaging structures and their electrical performance
- RF/microwave packaging structures and their electrical performance
- MMIC modules and high density packaging
- Experimental characterization techniques
- EMC/EMI sources & effects
- Prediction/measurement of radiation from on-chip sources, interconnect structures and packages
- Electrical design implications for low cost, high volume packaging
- Packaging concerns for wireless communication: design and modeling
- Packaging solutions for one chip radios: design and modeling
- Performance of packaging for automotive radar systems

Conference Co-chairs: Robert W. Jackson, University of Massachusetts; Moises Cases, IBM

Conference Web Page: Detailed information can be found at **www.epep.org**

Paper Submission: Information for authors can be found on the conference web page. Electronic submissions of no more than four pages must be received no later than **July 9, 2005.**

Student Paper Award: Two awards will be presented to the best two papers submitted by students

Short Courses/Workshops: On Sunday, October 23, 2005, a workshop entitled "**Future Directions in Packaging**" will be presented and short courses/tutorials will be offered.

Announcement

Future Directions in IC and Package Design Workshop, FDIP'05

sponsored by:

IEEE Components, Packaging, and Manufacturing Technology Society

organized by:

CPMT Technical Committee on Electrical Design, Modeling, and Simulation (TC-EDMS)

October 23, 2005
Austin, Texas

The goal of this workshop is to provide a forum to address the future needs associated with the design of next generation ICs and packages. The Technical Program Committee will solicit invited presentations from experts in the university and industrial communities. The workshop will be held in conjunction with the **IEEE Topical Meeting on Electrical Performance of Electronic Packaging** in order to enhance this conference with presentations that give directions for future requirements and developments in the area of electrical analysis and design. The workshop will foster active participation and discussions from all the speakers and attendees during the meeting.

The following talks are planned:

- ***Designing Servers In a Commodity World – Carl Anderson, IBM Corporation***
- ***Signal Interconnect Trends and Challenges Inside the CEC – George Katopis, IBM Corporation***
- ***High Volume Signal and Power Integrity Design for ASICs – Brian Young, Texas Instruments***
- ***Electromagnetic Field Visualization System for IC/Package Design Based on Optical Techniques – Mizuki Iwanami, NEC Corporation***
- ***Harnessing the Power of Parallel Computation on the IBM BlueGene/L to Analyze Complex Digital and RF Systems – Raj Mittra, Pennsylvania State University***
- ***Computational Electromagnetics for Circuits Simulations – the Challenges – Weng Cho Chew, University of Illinois, Urbana-Champaign***

Workshop will be held at the Radisson Hotel & Suites Town Lake, 111 E. Cesar Chavez, Austin, Texas 78701 (512) 478-9611. They are holding a block of rooms at $109.00 plus tax. Reservations must be made by September 30, 2005 in order to guarantee this rate. Be sure to mention that you are attending the EPEP conference in order to secure this rate. For more information on the hotel go to http://www.radisson.com/austintx. Additional information can be obtained at www.epep.org. Workshop chairs are Alina Deutsch (deutsch@us.ibm.com) and Madhavan Swaminathan (madhavan.swaminathan@ece.gatech.edu)

7th International Conference on Electronics Materials and Packaging (EMAP 2005)

December 11-14, 2005, Tokyo Institute of Technology, Japan

Announcement and

CALL FOR PAPERS

The 7th International Conference on Electronics Materials and Packaging will be held at Tokyo Institute of Technology, Japan. The former six conferences were held in Singapore (1999), Hong Kong (2000), Korea (2001), Taiwan (2002), Singapore (2003) and Malaysia (2004) all of which were successful and have gained a reputation as a premier electronics materials and packaging conference in Asia Pacific where the bulk of the packaging activities are taking place.

The purpose of the conference is to promote awareness of new advances in materials, design and simulations, fabrication, reliability, and thermal management of microsystem/MEMS packages. This will also provide an excellent opportunity for researchers and engineers to gather to discuss generic and practical applications and new directions.

The organizing committee seeks original papers that demonstrate how new technologies and applications are expanding and redefining the international role of microelectronics. Contributions are very welcome from industry participants and researchers from academic institutions. The topics of interests are specific to micro systems/MEMS, their packaging, electronics materials and reliability issues. Papers are being sought from, but not limited to, the following subjects:

- Automotive Electronics
- Chip-Scale Packaging/Flip Chip
- Electrical Modeling & Signal Integrity
- Electronic Inspection
- Green Materials
- High Density Displays
- High Density Packaging
- Interconnection Technologies
- Low Cost Packaging Methods
- Manufacturing Technologies
- Mechanical Modeling and Structural Integrity
- MEMS Packaging and Applications
- Microelectronic Materials & Processes
- No Flow Underfilling Process
- Optoelectronics/Photonics
- Polymer Materials & Microelectronic Applications
- Printed Wiring and Flex Boards
- Quality & Reliability
- Thermal Design, Analysis, and Characterization
- Thick & Thin Film Materials
- Wafer Scale Packaging
- Wireless Sensor Packaging & Applications
- Vibration on Electronic Devices

SECRETARIAT

All inquires concerning the conference should be addressed to:

Prof. Satoru AIHARA, Secretary General of EMAP2005
EMAP2005 Secretariat (I1-36)
Tokyo Institute of Technology
2-12-1 Ookayama, Meguro-ku, Tokyo 152-8552, JAPAN
Phone & Fax: +81-3-5734-2532
E-mail: info@emap2005.sms.titech.ac.jp

Conference Information & Contacts

Website: http://www.sms.titech.ac.jp/emap2005

IMPORTANT DATES

Submission of Abstract: June 30, 2005
Notification of Acceptance: July 31, 2005
Submission of Manuscript: September 30, 2005

EXTENDED ABSTRACT AND PAPER SUBMISSION

Extended abstracts are invited to describe original and unpublished work. The extended abstract should be about 500 words starting clearly the purpose, methodology, results and conclusions of the work. Key references to prior publications and how the work enhances the existing knowledge should be included in the extended abstract. Authors are requested to designate appropriate areas for the purpose of abstract review. All submissions must be in English and should be made via the conference web site. The required file format is either MS Word or Adobe Acrobat PDF with only one single file for each submission.

SELECTION OF PAPERS

The Technical Committee of the 7th EMAP will select papers with quality and originality for presentation at the Conference and for publication in the Conference Proceedings. Only papers of those authors who have paid the registration fee and intend to attend the Conference will be published in the Conference Proceedings (Author Registration).

CONFERENCE SCHEDULE

Sunday, December 11 (evening)	Registration and welcome drink
Monday, December 12	Keynote Lectures
Tuesday, December 13	Keynote Lectures Technical Sessions Banquet/Student Reception
Wednesday, December 14	Technical Visit (full day)

COMMITTEE

General Chair: Prof. Kikuo KISHIMOTO
Tokyo Institute of Technology, Japan

Co-Chairs

Prof. Mikio HORIE	Tokyo Institute of Technology, Japan
Dr. Takashi KAWAKAMI	Toshiba Corporation, Japan
Prof. Noriyuki MIYAZAKI	Kyoto University, Japan

Visit **www.sms.titech.ac.jp/emap2005/**

for the Advance Program and registration information

CALL FOR PAPERS

IEEE CPMT

International Symposium and Exhibition on

Advanced Packaging Materials

Processes, Properties and Interfaces

March 15-17, 2006
Georgia Tech Hotel and Conference Center
800 Spring Street NW
Atlanta, GA 30308

Abstract Deadline: January 31, 2006

The 2006 International Symposium and Exhibition on Advanced Packaging Materials will be held at the Georgia Tech Hotel and Conference Center, Atlanta, GA, March 15–17, 2006. The symposium is sponsored by the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society.

The symposium is devoted to the advances made in electronic packaging materials. Topics of presentations will include, but are not limited to, lead-free, Cu low-k, 3D packaging, adhesion, underfills, encapsulants and coatings, bumping and solders, substrates including HDI, high thermal and dielectrics, reliability, nano-functional and passive materials.

Attendees at this symposium in the past have been comprised of researchers, developers, producers and users of materials for single and multichip packages, interconnections, substrates, microwave applications, optoelectronic packages and display panels.

To submit an abstract, please logon to:

http://www.me.gatech.edu/APM06-IEEE/

For more information, please contact:

Professor Jianmin Qu, School of Mechanical Engineering, Georgia Tech, Atlanta, GA 30332-0405, Phone: 404-894-5687, E-Mail: jianmin.qu@me.gatech.edu.	Professor C.P. Wong, School of Materials Science and Engineering, Georgia Tech., Atlanta, GA 30332-0405, Phone: 404-894-8391, E-Mail: cp.wong@mse.gatech.edu.

ITHERM 2006

ITherm 2006 is an international conference for scientific and engineering exploration of thermal, thermomechanical and emerging technology issues associated with electronic devices, packages, and systems. ITherm 2006 will be held simultaneously with the 56th Electronic Components and Technology Conference (ECTC 2006 - http://www.ectc.net/), a premier electronic packaging conference. One unique feature for ITherm 2006 is that one entire afternoon session will be dedicated to the Poster Presentation along with the Vendor Exhibits. In addition to paper and poster presentations and vendor exhibits, ITherm 2006 will include panel discussions, keynote lectures by prominent speakers, and professional short courses.

To submit a paper for consideration, please enter a 250-word abstract in plain text providing succinct summary of the work including important conclusions by September 04, 2005. No figures and tables are allowed. The Abstracts will be considered for oral or poster presentations based on their originality, relevance, strength and archival value of the work.

**To submit a abstract for consideration, please use the on-line abstract submission form. All abstracts must be received by September 04, 2005.
**To submit your DRAFT PAPER, please use the on-line submission form. All draft papers must be received by November 18, 2005.
**To submit your FINAL PAPER, please use the on-line submission form. All final papers must be received by March 03, 2006.
**The full content of the Call For Papers is available in PDF version here. You need Adobe Acrobat from Adobe, Inc. to view the PDF file.

Original papers are solicited in the general areas of:

Thermal Management: Natural and forced Convection Air Cooling , Liquid Cooling
Novel Cooling Techniques: Phase Change, Heat Pipes, Thermosyphon, Liquid-Cooled Heat Sinks and Evaporation Microchannel, Micro- and Nano-Scale Heat Transfer and Fluidics
Thermal Management Issues in High Power Dissipation Packages and Systems including Novel Heat Sinks
Active: Thermo-Electric, Air Movers, Refrigeration, Thermo-acoustic refrigeration
Thermal Management in Military Electronics, RF Packages, Portable/Handheld, Automotive, Networking and Peripheral Hardware
Methods for Mitigating Effects of Extreme Thermal Environments
New Approaches to Microelectronics Thermal Management
Experimental Characterization: Methods and Measurement Techniques in Thermal Management, Thermal Contact Resistance, Flow and Temperature Visualization, Performance of Thermal interface Materials (Adhesives, Pastes, etc.)
Mechanics Mechanics of Materials , Pb-free Solder Materials and Reliability , Constitutive Modeling and Viscoplasticity
Failure Mechanics and Damage Modeling, Experimental Techniques and Characterization
Mechanics of Environmental-Friendly Materials In Electronics
Reliability
Package Level Reliability Investigation , Board and Product Level Reliability
Impact, Drop and Vibrational Analysis of Packages, Sub-Systems, and Systems
Modeling and Simulation
Coupled Analysis Physics/Thermal/Mechanics , Role of Fracture Mechanics in Electronic Packaging ,Solder Joint Reliability
Materials
Characterization of Micro- and Nano- Materials & Interfaces
Emerging Technologies: Thermal, Thermomechanical and/or related underlying multidisciplinary issues
Space Systems: Earth Orbiting and Deep-Space Missions
Sensors (Medical, Military, Consumer, Structures, Diagnostic, etc.)
Nanotechnology: Thermal, Mechanics, Material and Process Related Issues in Nanostructures, Nano/Molecular Electronics
Micro-Fluidics
Fiber-Optics Interconnect Systems & Free Space Optical Interconnects
MEMS: Device and Package Level Reliability Issues
Integrated Biochips and Bioelectronics
Medical, Telecommunication, and Automotive Systems
Software Tools & Techniques: Design, Analysis, Simulation, CAD, CFD, FEA, EDA software tools and trends

More information: **www.itherm.org/**

Polytronic 2005

5th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics

http://www.polytronic2005.org

Polytronic 2005, the 5th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics, will be held on **October 23-26, 2005** in Wroclaw, Poland.

The conference provides a unique opportunity for the meeting of polymer developers with polymer users from the electronics industries. Research paper presentations will cover all aspects of adhesives and polymers in microelectronics and photonics, including new polymers, organic devices, polymers in packaging, and adhesive applications.

Polytronic 2005 will be the fifth in the Conference series, begun in 2001 as an amalgamation of the previously successful series of IEEE Conferences on adhesives and polymers: Polymeric Materials for Microelectronic & Photonic Applications (POLY), Adhesives in Electronics, and Polymeric Electronics Packaging (PEP).

The topics that will be covered include:

Materials: Thermosetting/thermoplastic systems; inorganic adhesives; composites; filler materials; isotropic conductive adhesives; anisotropic conductive adhesives; underfill compounds; pastes and films; heat seal connectors; thermally conductive adhesives; polymers with adapted refractive index; photosensitive polymers; high temperature materials; PCB materials, polymer thick and thin films, low and high dielectric materials.
Processing and Manufacturing: Advanced packaging; lamination; printing; dispensing; spraying; transfer techniques; underfilling; potting; adhesion improvement; curing; equipment; statistical process control; economic analyses.
Design and CAD: Design, modeling, simulation, CAD of compounds and processes; thermo-mechanical behavior.
Reliability and Testing: Degradation mechanisms; adhesion; hermeticity; accelerated testing; humidity and environmental sensitivities; non-destructive testing methods; stress behavior.
Functional Polymers for Microelectronics: Conductivity of polymers; electronic transport; self-assembly; photoactivity; polymeric materials for molecular electronics.
Applications: Polymer electronic devices; polymer optical fibers; polymer wave guides; organic displays; polymer batteries; e-paper; flexible electronics.
Environmental Issues: Ecology and toxicology; life cycle analyses.

Submission of abstracts (31 May 2005)

Abstract should include the following:

- **ABSTRACT TITLE**
- **AUTHOR LISTING** (principal author first): First (given) name, Last (family) name, and affiliations, mailing address, telephone, fax and e-mail address.
- **PRESENTATION:** Indicate which Session Topic your paper matches and whether you prefer to do an Oral Presentation or a Poster Presentation. Placement is at the Chair's discretion.
- **ABSTRACT TEXT:** Not less than 250 words; preferably 1500 words.
- **KEY WORDS** List a maximum of five key words.
- **BRIEF BIOGRAPHY** (of principal author) Approximately 50 words.

Note: Electronic submission only. Submit abstracts to: papers@polytronic2005.org. Detailed information about the submission process for final papers will be posted later on the official conference web site (http://www.polytronic2005.org).

- **Notification of acceptance: 15 June 2005**
- **Final papers due: 05 September 2005**

Download the Advance Program today:

www.polytronic2005.org

Institute of Electrical and Electronics Engineers, Inc.

Phoenix Section

Components, Packaging and Manufacturing Technology Society Chapter

&

Waves and Devices Chapter

PRESENT AN ALL-DAY WORKSHOP ON

Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications

Date: Thursday, November 10th, 2005 **Time:** 7:00 A.M. – 5:00 P.M.
Location: Arizona State University, Tempe, Arizona – ASU Memorial Union (Arizona Room)

Abstract

The one-day workshop will focus on device, interconnect and packaging challenges for next generation computing and communication applications. Participants will hear from leading contributors from industry, academia and the national labs. Long-range technology roadmaps will be reviewed and state-of-the-art processor, memory, and mixed-signal technologies will be addressed. Chip, package, and board-level interconnect issues will be discussed. Key materials, process, and performance challenges for physically realizing the required devices, interconnects and packaging will be presented. Market trends in computing and communications are within the scope of the workshop as well. A panel discussion on the future of computing and communications will bring closure to the day's workshop. Vendors representing the entire supply chain of chip, package, and board will display their products and services.

Topics

- **System & Architecture: Future computing approaches (local vs. net-centric, personal & server computer); convergence of computing and communication; advances in processor technology such as multi-core, high-bandwidth buses and advanced drivers/receivers; memory/processor integration; SoC partitioning, modeling, and testing challenges/issues.**
- **Materials & Processing: ITRS roadmap for CMOS technology; Moore's law/prognosis in the context of the next few technology nodes; BEOL processing (low-k/Cu, ultra low-k/Cu); advances in memory technologies.**
- **Simulation & Modeling: Simulation for advanced devices; EM simulation in RF circuit/module/package design; signal noise analysis for SoC.**
- **Advanced Packaging: New packaging technologies, especially flip-chip, lead-free, 3D interconnect, multi-chip, and RF modules.**
- **Special Topics: Signal integrity; power delivery and distribution; cooling/thermal management.**
- **Panel discussion on the future of computing and communications.**

Vasu Atluri	(480) 554-0360	Bishnu Gogoi	(480) 413-8836	Mali Mahalingam	(480) 413-5368	Ravi Sharma	(480) 792-7920
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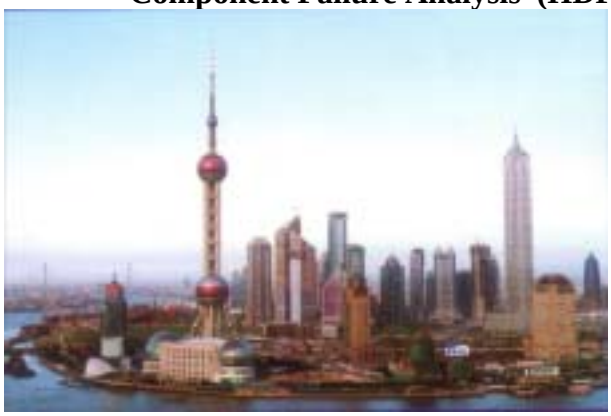
Announcement and Call for Papers
The 8th IEEE CPMT International Conference on High Density Microsystem Design, Packaging and Component Failure Analysis (HDP´06)



Date: June 27 – 30, 2006
Venue: Yan Chang Campus, Shanghai University, China
Co-sponsored by
IEEE CPMT Society, IEEE CPMT Scandinavian Chapter, IEEE CPMT China Chapter
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Microsystem design, manufacturing, assembly and packaging technology is playing a key technology for the progress of the microsystems and microelectronics industry in the world. China is not an exception. Therefore, many multi-national companies are establishing new facilities in China for expanding their global business and interest. Following the successful previous conferences, we are proud to announce the 8th International IEEE CPMT Symposium on High Density Microsystem Design and Packaging and Component Failure Analysis in Electronics Manufacturing (HDP´06).

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For further information please contact Jane Lu at **smit@department.shu.edu.cn** or **johan.liu@mc2.chalmers.se** at SMIT Centre, Shanghai, China and Sweden. Further information will be posted at the website at **www.smit-shu.com**

CALL FOR PAPERS

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