Components, Packaging, and Manufacturing Technology Society Newsletter

IEEE CPMT

The Global Society for Microelectronics Systems Packaging

Vol. 28 No. 4, December 2005 (ISSN 1077-2999)

www.cpmt.org
www.ewh.ieee.org/soc/cpmt/newsletter

President's Column

Dr. Phil Garrou
IEEE Fellow and President IEEE CPMT Society
Research Triangle Park, NC USA
pgarrou@RTI.org

As my two year term as CPMT President comes to a close, there are a few thoughts I'd like to leave you with.

The Society is in good hands

I will be turning over the reigns of President to Dr. Bill Chen, a veteran in our industry who worked for IBM and is now with ASE. Bill most recently served on our Board of Governors (BOG) as Strategic Director for Asia and is well attuned to the operation of our organization and the plans we have in place. Please congratulate Bill on his new role and offer him the same strong support you all offered me.

It has been my pleasure to work with the Board members you have elected. They have been a hard-working group of individuals from around the globe who have our Society's and our industry's best interests at heart.

We are THE #1 Source of Information

The quality of our information continues to be CPMT's most important contribution to the industry. Through our professional meetings, journals and professional courses we are the #1 source in the world when it comes to information about device materials, packaging and manufacturing.

Our technical anchor, the yearly ECTC program, continues to draw the best presentations from around the world. We have also seen market acceptance of our CPMT-sponsored major Asian meeting EPTC (Electronic Packaging Technology Conference) which is held each fall in Singapore, and we have started what we hope will be a European equivalent in the "Electronic SystemIntegration Technology Conference" which will be held in Dresden in the Fall of 2006.

Please visit our newly reorganized web site – **www.cpmt.org** – to examine all our offerings.

A Truly International Organization

As most of you know, continuing our globalization process has been one of my goals for my term in office. I think we have accomplished this by revising the bylaws so that each region votes to elect its own board members based on its percentage of the overall membership. We are sure that this will allow CPMT management to better reflect the desires of our broad global membership.

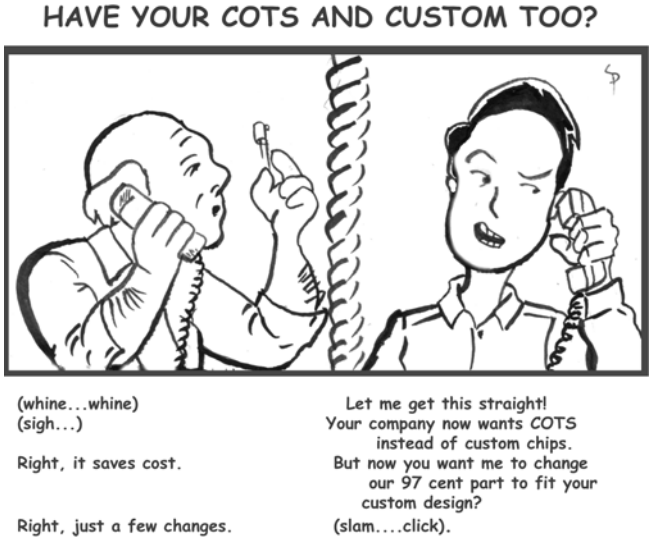
In summary

These have been a fun two years for me and I hope a productive two years for the Society. I wish you all a healthy and happy 2006!

IEEE CPMT Society Newsletter

Index

	Click
• **Presidents Message:**	1
• **Society News:**	2
• **John L. Prince Memorial:**	9
• **Member Recognitions:**	10
• **Workshop / Conference Reports:**	10
• **Chapter Reports:**	15
• **New "Contacts" book**	19
• **Announcements:**	20



CPMT Officers

President:	Phil Garrou	+1-919-248-9261
Technical VP:	Rolf Aschenbrenner	+49-30-46403164
VP (Admn.):	H. Anthony Chan	+021-6502788
Treasurer:	John Segelken	+1-732-920-3023
VP (Publ.):	Paul B. Wesling	+1-408-331-0114
VP (Conf.):	Ricky Lee	+852-2358-7203
VP (Educ.):	Albert Puttlitz	+1-802-879-0466 (Fax)
Sr. Past Pres.:	John Stafford	+1-602-413-5509
Jr. Past Pres.:	Rao Tummala	+1-404-894-9097
Secretary:	Ron Gedney	+1-703-834-2084
Ex. Director:	Marsha Tickman	+1-732-562-5529
IEEE VP TAB:	Ralph Wyndrum	+1-732-219-0005

Elected Board Members

2008:
Vasudeva P. Atluri, Li Li, Dongkai Shangguan, Patrick Thompson, Klaus-Jürgen Wolter, and Kishio Yokouchi

2007:
Eric O. Beyne, Steve J. Bezuk, N. Rao Bonda, Rajen Chanchani, Kitty Pearsall, and C.P. Wong

2006:
William D. Brown, Philip C. H. Chan, Charles Lee, Johan Liu, Thomas G. Reynolds III, Ephraim Suhir

CPMT Society Newsletter

Editor:	Vasudeva P. Atluri, email: vpatluri@ieee.org Tel: +1-480-554-0360, FAX: +1-480-563-0049
Associate Editor:	Li Li, li.li@ieee.org, +1-480-413-6653
Associate Editor:	Debendra Mallik, dmallik@ieee.org +1-480-554-5328

CPMT Archival Publications

Publications VP:
Paul Wesling, email: p.wesling@ieee.org, Tel: +1 408 331 0114.
Transactions-CPT Editor:
Avram Bar-Cohen, Univ. of Maryland, 2181B Martin Hall, College Park, MD - 20742 USA, Tel: +1-301-405-3173;
Email: barcohen@eng.umd.edu
Transactions AdvP editor:
G. Subbarayan, Purdue University, Mechanical Engineering Dept., Tel: +1-765-494-9770; email : ganeshs@ecn.purdue.edu
Transactions EPM Editor:
R. Wayne Johnson, Tel : +1-334-844-1880, johnson@eng.auburn.edu

Technical Committee Chairs

TC-ECCC (1) Electrical Contacts, Connectors and Cables:
Gerald Witter, Chugai, +1-708-244-6025
TC-Assy (3) IC and Package Assembly:
Martin Goetz, IBM, mgoetz@us.ibm.com
TC-EM (4) Manufacturing Design & Process:
Walt Trybula, TTF, +1-512-695-4026, w.trybula@ieee.org
TC-M (5) Materials:
Rajen Chanchani, Sandia Labs, +1-505-844-3482, r.chanchani@ieee.org
TC-HDSB (6) High Density PWB packaging:
Yoshitaka Fukuoka, weisti.fukuoka@rose.zero.ad.jp
TC-ASTR (7) Environmental Stress & Reliability Test:
Kirk Gray, k.a.gray@ieee.org
TC-Therm (9) Thermal Management & Thermomech. Design:
Tony Mak, Dallas Semi, +1-972-371-4364
TC-Opto (10) Fiber Optics & Photonics:
Susan Law, Fax: +612-9351-1911, Email: s.law@oftc.usyd.edu.au
TC-Test (11) Electrical Test:
Bruce Kim, Bruce.Kim@asu.edu, Tel: +1 480 965 3749
TC-EDMS (12) Electrical Design, Modeling and Simulation:
Madhavan Swaminathan, GIT, +1-404-894-3340
TC-PEP (13) Power Electronics Packaging:
Doug Hopkins, SUNY Buffalo, +1-607-729-9949, d.hopkins@ieee.org
TC-SP (14) Systems Packaging:
Erich Klink, eklink@de.ibm.com
TC-RF+W (16) RF and Wireless:
Craig Gaw, Freescale, +1-480-413-5920, c.a.gaw@ieee.org
TC-MEMS (17) MEMS and Sensor Packaging:
Eric Jung, IZM, Berlin, email: erju@izm.fhg.de
TC-WLP (18) Wafer Level Packaging:
Michael Toepper, IZM, Berlin, toepper@izm.fhg.de
TC-Ed (19) Education:
Paul Wesling, p.wesling@ieee.org
TC-GEMP (21) Green Electronics Manufacturing and Packaging:
Hansjoerg Griese, griese@izm.fhg.de
TC-NANO Nano Packaging:
Rao Tummala, GaTech, rao.tummala@ee.gatech.edu

Standing Committee Chairs

Student Chap. Dev.:	William D. Brown, wdb@engr.uark.edu
Disting. Speakers:	A.F. Puttlitz, +1-802-879-0466 (Fax)
Fellows Search:	Rao Tummala, rao.tummala@ee.gatech.edu David Palmer, d.palmer@ieee.org
Fellows:	C. P. Wong, cp.wong@ieee.org
Const. & Bylaws:	Tony Mak, +1-972-371-4364,
Finance:	Ralph Wyndrum, Jr, r.wyndrum@ieee.org
IEEE Books & C and D Magazine Editor:	Joe Brewer, j.brewer@ieee.org, +1-352-475-1480
Membership and Chap. Development:	Ralph Russell, II, cpmt-membership@ieee.org
Nominations:	John Segelken, +1-732-920-3023
International Rel.:	Europe - Ephraim Suhir, +1-908-582-5301 Asia - W. T. Chen, +65-874-8110
Jt. Comm. on Sem. Manufacturing:	G.C. Cheek
iNEMI Roadmap Coord. Comm.:	www.ectc.org/nemi Rolf Aschenbrenner, aschenbr@izm.fraunhofer.de Phil Garrou, philgarrou@worldnet.att.net

IEEE Components, Packaging, and Manufacturing Technology Society Newsletter is published quarterly by the Components, Packaging, and Manufacturing Technology Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. 41.00 per member per year (included in Society fee) for each member of the Components, Packaging, and Manufacturing Technology Society. Printed in U.S.A. periodicals postage paid at New Your, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE CPMT Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854.

2006 Deadlines for Submitting Articles:
March 5th, 2006
June 5th, 2006
September 5th, 2006
December 5th, 2006
Members-only Web:
UserName: **(join CPMT, for access)**
Password:

CPMT Society Officers
Results of Election

Marsha S. Tickman, Executive Director – CPMT Society

Every two years, Voting Members of the CPMT Society Board of Governors elect a President and five Vice Presidents to serve for a two-year term. A President may serve a maximum of two consecutive two-year terms. There is no limit on consecutive terms for Vice Presidents. The following individuals have been elected to serve for a two-year term as Officers of the CPMT Society starting January 1st, 2006 thru December 31st, 2007:

President:	William T. Chen
Vice President Technical:	N. Rao Bonda
Vice President Publications:	Paul Wesling
Vice President Conferences:	Rolf Aschenbrenner
Vice President Education:	Albert F. Puttlitz
Vice President Finance:	Thomas G. Reynolds III

We congratulate all officers on their election to serve CPMT Society for two years and thank them for their interest and willingness to serve. Please review the new Officers' accomplishments, contributions, and interests in the biographical sketches below, and contact them individually regarding issues and directions you'd like to help us pursue in the CPMT Society.

WILLIAM T. CHEN (M '92, SM '03) received his engineering education at University of London (B.Sc), Brown University (M.Sc) and Cornell University (PhD). He joined IBM Development Laboratory at Endicott New York in 1963. His early assignments were in physical modeling and reliability simulation of electronic components in IBM systems and led the implementation of finite element modeling for microelectronic packaging components in IBM. From the late 70's he worked in a broad range of IBM microelectronic packaging products development ranging from design, materials, manufacturing processes and reliability. In IBM he was a strong proponent in developing university education and research in microelectronic packaging related disciplines. He was elected to the IBM Academy of Technology for his contributions. He retired from IBM in 1997 and joined the Institute of Materials Research and Engineering (IMRE) in Singapore, where he became Principal Research Fellow, and Director of the Institute, contributing to the growth in facilities, resources and facilities of IMRE as a full fledged materials research center for the region. He joined ASE in 2001 where he has the position of Senior Technical Advisor.

He has been a Member-at-Large of the CPMT BoG, and is an active member of the CPMT Santa Clara Valley Chapter. He has served as CPMT Strategic Director for Region 10, supporting the CPMT activities in the Asia Pacific region. He is the Co-Chair of the ITRS Assembly and Packaging Roadmap International Technical Working Group. He had been active in the Electronics Packaging Division of ASME. He is a Fellow of ASME. He has published extensively in the fields of microelectronics packaging and solid mechanics. He has served as an Associate Editor of *ASME Journal of Electronic Packaging*, and IEEE/CPMT Transactions.

In the past years the Society has made giant strides towards achieving the goal of a global professional society. We have CPMT chapters and individual memberships situated in far flung cities and regions around the world. An important step in our globalization focus would be to increase the communication channels between BoG and chapters, and between chapters and chapters. In this way new ideas and new ways to serve the memberships will bubble up. Opportunities for professional programs, and networking between individual professionals in different regions and among diverse disciplines will expand and multiply. The global CPMT Society will continue to grow as the professionals in our industry, wherever they may be, see and appreciate the value proposition in belonging to CPMT.

N. RAO BONDA (M'97, SM'02) is currently a member of research and development staff in Freescale Semiconductor, Inc. (formerly known as Motorola's Semiconductor Products Sector) in Tempe, AZ. He received a Ph.D. in Materials Science and Engineering from the University of Pennsylvania, Philadelphia, PA, in 1985. He has been serving the IEEE CPMT Society since 1997 as the Chair of the Awards Committee.

After receiving Ph.D., Rao continued research in materials science at the Ohio State University, Columbus, OH and the University of Wisconsin, Madison, WI until 1989. From 1989 to 1994, he was a research member at IBM T.J. Watson Research Center, Yorktown Heights, NY, and IBM Microelectronics Division, Endicott, NY. In IBM, he developed electronic packages and processes involving C4 and wire bond chip joining methods, and worked on qualification of several ceramic and plastic packages. His other research work in IBM included failure mechanism studies of Pb/Sn solder alloys to improve the thermal fatigue and reliability of solder joints in electronic packages.

In 1994, Rao joined Motorola's Semiconductor Products Sector in Tempe, AZ, as a team leader for packaging of an optical display module. He developed a fine pitch flip chip bonding process for this display module and improved its yield and reliability through innovative designs. After completion of the display module project, he led new package introductions from design to manufacture implementation and qualified plastic packages for wireless communication and networking systems applications. He currently provides packaging development and technical support for a major wireless communications customer and works with package assembly subcontractors to fulfill the customer's product requirements and packaging roadmaps. He has over 20 technical publications and a US patent.

Rao has been the Chair of the CPMT Awards Committee for the last nine years, and has coordinated the selection process for the awards. Working with the Awards Committee and the Board of Governors, he has facilitated several strategic decisions to align the awards process with the CPMT Society goals. He is the CPMT Chair for the Motorola Graduate Fellowship for Research on Electronic Packaging and is a member of the TC16 committee on RF and Wireless. He has also served on the selection committee for the CPMT Chapter of the Year

award. He is very active in CPMT Phoenix Chapter and IEEE Phoenix Section. He has served as the chair and program chair for the Chapter and as the treasurer for the IEEE Phoenix Section. He is currently the secretary for the Phoenix Section.

Rao has been actively participating in the Electronic Components and Technology Conference (ECTC) for several years. He has served as the chairman of the Components and RF subcommittee and has chaired the sessions at the ECTC. He has chaired the ECTC's Professional Development Courses committee and served on the committee for three years. He was the Web Administrator for the ECTC last year and is currently the assistant program chair.

Rao is a member of the IEEE and the American Society for Materials International (ASM). In addition to a Ph.D., he holds an MS and a BS in Metallurgical Engineering from Indian Institute of Technology, Kanpur, and Regional Engineering College, Warangal (India), respectively. He also received an MBA from the Arizona State University, Tempe, AZ, in 1998.

Action plans as the Technical VP of CPMT Society: Promote the technical interests of our members through Technical Committees (TCs) and policy enhancements in the BoG. Increase the participation and collaboration of TCs in conferences, both in US and abroad. Look for new and emerging technologies and form TCs in those areas. Enhance communication among the TCs to share their activities and opportunities for growth.

PAUL WESLING (M '70, SM '84, F '04) received his BS in

electrical engineering and his MS in materials science from Stanford University. Following assignments at GTE/Lenkurt Electric (component engineering), ISS/Sperry Univac (bubble memory development, reliability, manufacturing engineering), Datapoint Peripheral Products (VP - Product Integrity), and Amdahl (design analysis, mainframe testing, console peripherals), he joined Hewlett Packard (Tandem NonStop Division) in 1985. As a member of the development team for advanced IC packaging, he designed several multi-chip module prototypes, supervised their fabrication, and tested them. In the Education Group he developed courses on reliability, managed the Distinguished Lectures series, and was on the Technology Initiative team. Retired in 2002, he now serves as editor and webmaster for the IEEE S.F. Bay Area Council. He organizes a number of advanced technology and professional skills development courses for engineers and developers in the Santa Clara Valley.

Mr. Wesling has published a number of technical papers and authored a book chapter. As CPMT's current Vice President-Publications, he supervises four archival journals, a newsletter, and the website, oversees authors for IEEE Press books, manages the Special Sections for the Society Transactions, and organizes the electronic publishing initiatives for the Society.

He is a Fellow of IEEE, and received the IEEE Centennial Medal, the CPMT Board's Distinguished Service Award, the Society Contribution Award, and is a CPMT Distinguished Lecturer. He has organized over 240 short courses for the Santa Clara Valley CPMT Chapter, many of them held at Stanford University. As part of his interests in education, he serves as Vice-Chair of TC-Education, is on the ECTC's Packaging Education program committee, administered the joint CPMT/NSF grant program for packaging education, and is on the SCV Section K-12 Education Committee.

He also served 15 years as scoutmaster of a local Boy Scout Troop and is now advisor for a Venturing Crew, webmaster for CPMT and for the Pacific Division of the ARRL, and enjoys backpacking, fly fishing, and amateur radio.

ROLF ASCHENBRENNER (M'97, SM '04) was born in

Buchen, Germany, in 1961. He received the M.S. degree in mechanical engineering from the University for Applied Science, Gießen, Germany, in 1986 and the B.S. degree in physics from the University of Gießen, Germany, in 1991.

From 1991 to 1992 he worked at the University of Gießen in the area of new materials and was engaged in a project for the German Space Lab Mission D2. In 1993 he joined the research center Technologien der Mikroperipherik at the Technical University of Berlin, working in the area of electroless metal deposition. Since March 1994 he has been employed at the Fraunhofer Institute Reliability and Microintegration Berlin (IZM) where he is presently head of the department of Chip Interconnection Technologies. In 2000, he became the Deputy Director of the Fraunhofer Institute IZM.

Rolf Aschenbrenner's research work has spanned from manufacturing process fundamentals in adhesive joining to applied manufacturing problems. Broadening his research contributions beyond those are made in thin and flexible electronic assemblies and development and analysis of innovative process technologies for all aspects of system level packaging.

He has authored and co-authored more than 80 articles in journals or proceedings in the area of electronic packaging and he holds five patents and has eight pending patents in the field of microelectronic packaging. In 1995 he obtained the best paper award from the Surface Mount International Conference (SMI) in San Jose.

In terms of professional services, Rolf Aschenbrenner has taken roles as a member of the Board of Governors for the IEEE CPMT Society. He was General Chair of the first International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics. He was a Program Chair of the IEEE System Packaging Workshop in 2001 and of the European VLSI Packaging Workshop in 2000. He also serves as a member on several technical committees including ISEPT 98, Materials 99, 00 and 01, Adhesives in Electronics 98 and 00, EMAP 2000, EPTC 2000, Interpack 2001 and Electronic Goes Green 2000.

As a member of the IEEE CPMT Society Board of Governors, Rolf has worked as a European representative on the Conference Advisory Committee, and has played an active role in the globalization of IEEE CPMT in terms of Membership and Chapter development. He previously served as Strategic Pro-

gram Director, European Activities, and currently serves as Vice President, Technical.

ALBERT F. PUTTLITZ (M '88, SM '92) received his Ph.D. degree in Engineering Mechanics from Michigan Technological University in 1968. During 36 years with IBMCorp., he has held group leader/engineering assignments in semiconductor process development, reliability, testing, contamination analysis, manufacturing engineering, failure analysis, tooling, mechanical analysis/design and education. He is the recipient of IBM's first level Invention Achievement Award and has been an Invention-Disclosure-Review Board member. He has taught college-level engineering courses at Michigan Tech. and IBM. Dr. Puttlitz retired from IBM in 1992 and now consults. He is also active as a licensed Realtor in the State of Vermont.

Albert has numerous external and internal IBM publications. He is the presenter and/or co-author of papers at four ECTC Components sessions (1985, '86, '89, '92). He received the best CPMT Transactions Paper Award in 1985 (with Sang Kim). He is a 18-year member of the IEEE CPMT Society, served on the ECTC Components and RF Paper Review Committee for the past fifteen years, was the ECTC Components and RF Subcommittee Program Chairman during 1991-1993, and has served as the ECTC Components and RF session Chairman or Co-chairman for nine years. He was the ECTC Professional Development (Short) Course Chairman for eight years, rotates as its chair every three years with other members of the Professional Development Course committee and is a member of the ECTC Professional Development Course Committee for the Y2006 ECTC. Albert introduced "Continuing Education Units" credits for Professional Development Courses (sponsored by the IEEE Education Department) and responsible for the institution of the CPMT "Professional Development Certificate of Achievement".

Dr. Puttlitz was elected to four terms as a Member-at-Large on the CPMT Board of Governors. He has been the CPMT Vice President of Education for the past eight years and currently holds that position.

His accomplishments as CPMT VP of Education for the past five years include:

- As an initiative to promote the CPMT Society worldwide, he lead a delegation to Hong Kong in Y2000 and was a member of the Y2000 Singapore delegation.
- He was a member of the ECTC Electronic Packaging Paper Review Committee and was Chairman of several of the ECTC Electronic Packaging Sessions for 4 years.
- He was a member of the Electronic-Packaging-Education-Faculty Grant-Committee (with Leyla Conrad, Paul Wesling, and Andrew Tay). Over 12 Grants, sponsored by CPMT and PRC of Georgia Tech., have been awarded for developing multimedia/web-based Electronic Packaging Courses for the 21st Century. The last grants were awarded at the Y2003 ECTC.
- He obtained CPMT approval (and money) and arranged for the production of CPMT sponsored CD-ROM Courses by the IEEE Education Department for Y2000 and Y2001. Due to the high IEEE financial debt load, these productions are now on hold and may be done in a less costly manner.
- He is the Chairman of the CPMT Distinguished Lecturer program. To date, the program has 20 Distinguished Lecturers. The program is in wide use with new members being added yearly.
- He is a member of the CPMT-Motorola Fellowship Committee responsible for awarding a yearly fellowship in Electronic Packaging to a Ph.D student at ECTCs. This fellowship is chaired by Dr. Andrew Skipor of Motorola.

My goal for the next two years as VP of Education is to continue to promote CPMT worldwide as the premier packaging society by continuing to offer educational courses, programs and opportunities for its members. I'm ready to lead a delegation to promote CPMT to almost any part of the world. I will continue to be active in all of my current activities which includes attempting to introduce Engineering education at the high school level. Additionally, I will seek to find a less expensive way to produce and market CPMT sponsored courses via CD-ROMs and multi-media/web. And lastly, I will attempt to get at least one more industrial sponsor for an educational program.

Albert holds the IEEE membership grade of Senior Member, is a member of ASME, is a member of the US Power Squadron, and is active in community and church activities.

THOMAS G. REYNOLDS III (M'92, SM '04) Dr. Reynolds received his PHD from Brown University in 1972 where he worked on synthetic inorganic chemistry of electronic materials. His MS (1966) and BS (1964) were from the University of Virginia in Materials Science and Mechanical Engineering respectively. Tom has worked in the field of electronic ceramic materials and other advanced technologies for more than 35 years.

From 1992 to present, Tom has been the Director of Technology at Murata Electronics N.A., Inc. He has worked in the areas of leading edge designs in decoupling capacitors, hard disk drive activation, LTCC modules, and integrated passive components. He has acted as liaison between American designs and Asian development activities, as well as in merger and acquisition analysis. Prior to joining Murata, Dr. Reynolds worked for Philips Electronics for 18 years in both the US and Europe, developing processes and methods for electronic (dielectric) ceramics, and from 1968 to 1973 he was staff scientist at Texas Instruments.

Tom has been involved with CPMT and ECTC (Electronic Components Technology Conference) for more than 13 years. He was General Chair for ECTC in 2000 and continues to be active as Finance Chairman. He is also a Senior Member of IEEE.

Additional activities and responsibilities include Treasurer of the Ft Walton Sail & Power Squadron of the United States

Power Squadron and he is currently the Vice Commodore of the Ft Walton Yacht Club. Tom is also a member of the Institute for Senior Professionals, an association of business, professional, medical and military professionals to advise and serve the local community based on their experience and expertise.

Dr. Reynolds will bring a breadth of experience, both local and international, to the Board. He will enthusiastically offer his efforts to the CPMT vision of continuing globalization and service to the profession.

****

CPMT Society Board of Governors
Results of Election

John Segelken, Nominating Committee Chair

The following individuals (in alphabetical order) have been elected to serve for a three-year term as Members-at-Large to the CPMT Society Board of Governors starting January 1st, 2006 thru December, 31st 2008:

Vasudeva P. Atluri, Li Li, Dongkai Shangguan, Patrick Thompson, Klaus-Jürgen Wolter, Kishio Yokouchi

We thank all candidates for their interest and willingness to serve. Please review the new Board members' interests in the biographical sketches below, and contact them individually regarding issues and directions you'd like to help us pursue in the CPMT Society.

VASUDEVA P. ATLURI (M'91, SM'00) is currently a Silicon Integration Manager in Assembly Technology Development, Intel Corporation, Chandler, AZ. He received a Ph.D. in Materials Science and Engineering from University of Arizona in 1998 with a minor in Electrical Engineering and specialization in silicon fabrication.

Vasudeva joined Intel Corporation in 1995, managing a group responsible for ensuring successful interface between silicon and assembly technology development. Earlier he was employed at Motorola and worked on reliability aspects of plastic packages. He has more than thirty technical publications and has filed for six patents.

He has served as CPMT Phoenix Chapter Chair and IEEE Phoenix Section Chair and currently chairs the Awards Committee for IEEE Phoenix Section and the Workshop Committee for the IEEE CPMT Phoenix Chapter. He is also serving as Student Activities Coordinator for IEEE Region 6 Southwest Area. He is a nomination committee member for selecting candidates for IEEE Region 6 Director-Elect. He is on the ECTC program committee, and is the new Newsletter editor. He would like to take already useful and informative newsletter to a higher level. He is serving as editor for Intel Assembly and Test Technology Journal for last eight years of which last four years as chief editor.

Dr. Atluri was presented multiple awards over last seven years by IEEE CPMT Phoenix Chapter and IEEE Phoenix Section for his multiple outstanding contributions to Electronic Packaging and IEEE including organizational and technical leadership. He received Individual Achievement awards from Southwest Area part of IEEE Region 6 during 2004 and from IEEE Region 6 during 2005.

LI LI (S'93, M'95, SM'03) is currently a Distinguished Member of Technical Staff at Freescale Semiconductor (formerly Motorola Semiconductor Products Sector) in Tempe, Arizona, USA. She has received B.S. and M.S. in Material Science and Engineering and a Ph.D. in Electrical Engineering at SUNY-Binghamton. She has done extensive research and development in the field of electronic packaging and has been supporting the IEEE CPMT Society in various roles.

She has worked in various areas of packaging materials and process development, including flip chip interconnect and chip scale package development, underfill materials, Sn-Pb and Pb-free solder wafer bumping, and adhesive interconnects. She is currently working on RF module development, component design libraries for effective RF module design flows, integrated passives design and simulation on ICs and organic substrate, and flip chip in RF modules.

Li Li has published more than 40 technical papers, co-authored a book chapter in Conductive Adhesives in Electronics Packaging, and received four issued patents with one pending. She is the chair of the Components and RF sub-committee of ECTC and has served as a session chair. She also contributes to CPMT Newsletters. In recognition of her significant contributions to both materials and electrical aspects of electronic packaging and for her service to the CPMT Society, Li Li was awarded the CPMT Society "Outstanding Young Engineer Award" for the year 2002. Li Li would like to work on programs to attract and encourage young engineers to pursue this challenging and multi-disciplinary career in electronic packaging.

DONGKAI SHANGGUAN (M'01, SM'02) received his BS degree in Mechanical Engineering from Tsinghua University, China, Ph.D. degree in Materials from the University of Oxford, U.K., and MBA degree from the San Jose State University. He conducted post-doc teaching and research at the University of Cambridge and then at The University of Alabama. He lectured at Wayne State University as Adjunct Faculty, and is currently a guest professor at Shanghai University.

Dongkai worked for 10 years at Ford/Visteon as Senior Technical Specialist and Supervisor of Advanced Electronics Manufacturing, before he joined Flextronics in 2001 where he is currently Senior Director for Advanced Assembly and Environmental Technologies.

He has published 1 book and over 160 papers, and his latest book "Lead-Free Solder Interconnect Reliability" will be published soon. He has 20 U.S. and international patents issued and a number pending.

Dongkai has received a number of recognitions for his contributions to the industry, including the "Total Excellence in Electronics Manufacturing Award" from SME and the "Soldertec Lead-Free Soldering Award". He has given numerous techni-

cal presentations and keynotes at various conferences, and chaired technical sessions and panels including the Advanced Packaging Materials Symposium, ECTC, and HDP. He has also given several seminars at IEEE CPMT chapter meetings.

Dongkai wants to focus on the area of assembly technology to enhance the cross-integration of the assembly technology roadmaps among several professional organizations, including CPMT, SMTA, iNEMI, IPC, etc, as he believes that the global scope of the CPMT membership will add significant value to the roadmapping process, the Roadmap itself, and the global utilization of the Roadmap.

PATRICK THOMPSON (M'87, SM'92) received his BS, MS and Ph. D. degrees in Chemical Engineering from the University of Missouri-Rolla in 1979, 1981 and 1983, respectively.

Pat has spent more than 20 years in the area of advanced packaging research, development and transfer to manufacturing. He has led development teams at Bell Labs, AMI Semiconductors and Motorola (now Freescale), working on technologies ranging from flip chip fabrication and packaging, flip chip on board to chip scale packages, multi-chip packaging, MEMS and opto-electronic packaging. Since 2001, he has been a Senior Member of the Technical Staff at Texas Instruments, where he leads the development of packaging solutions for high performance microprocessors and the conversion to Pb-free bumps for Texas Instrument's flip chip package portfolio.

Pat is active in industry-consortia and industry-university partnerships. He is currently the chair of the Georgia Institute of Technology Packaging Research Center Industrial Advisory Board and a member of the PRC Executive Advisory Board. He is TI's primary representative to the Sematech 3D IC working group, and is also active in TI's 3D IC program with IMEC. Pat is a TI member of the SRC Packaging/Interconnect TAB, and currently mentors two custom packaging research projects.

Pat has five patents and over two dozen publications. He has presented packaging tutorials and given invited talks at leading packaging conferences. He has been a member of the Electronic Components and Technology Conference (ECTC) technical program committee since 1983, where he has held multiple positions. He is currently the General Chair of the 2006 ECTC. He has served at both the local and Society level of the CPMT holding positions including Member at Large, Administrative Vice President, and Technical Vice President of the CPMT. He served as a member of the *IEEE Spectrum* Editorial Advisory board from 1998-2000. In addition to IEEE, Pat is a member of the American Society for Quality.

KLAUS-JÜRGEN WOLTER (A'05) Prof. Dr.-Ing. habil. Wolter's professional experience includes: 2003 Director of the Electronic Packaging Lab at Dresden University of Technology; 2002 Director of the Centre of Microtechnical Manufacturing; 1989 Assistant professor at the Institute of Electronic Technology; 1989-1973 Research and development in the microelectronic industry.

Klaus-Jürgen Wolter's fields of research include substrate technologies; assembly technologies of devices, components, MEMS; joining technologies; reliability of electronic packages; and nondestructive test methods. He is a member of: IEEE CPMT, IMAPS, SMTA, and VDE. He was Chair of the "International Spring Seminar on Electronic Technology", Chair of the 5th and 8th International Academic Conference on Electronic Packaging Education and Training, and Vice Dean of Education for the Department of EE.

His publications include: co-author of the monograph, Scheel: Electronic Assembly Technology Electrochemical Publications LTD, 2004; Wolter, K.-J.; Wiese, St.: Interdisziplinäre Methoden der Aufbau- und Verbindungstechnik der Elektronik, Gdb goldenbogen, Dresden 2003; co-author of the monograph, Sauer: Prozesstechnologie der Elektronik, Carl Hanser Verlag München Wien 2003, and Wolter, K.-J.; Sauer, W. (Editor): Elektronik-Technologie in Forschung und PraxisVerlag Dr. Markus Detert, Templin, Band 1 – 9.

The research activities result in more than 80 conference presentations/proceedings and in 3 patents. He has been an IEEE CPMT member since 2005. He served as a member of Program Committee on Education of the 53rd, 54th and 55th ECTC.

KISHIO YOKOUCHI (M'02) received his bachelor's and master's degrees in applied chemistry from the Yokohama National University in 1977 and 1979, respectively. In 1979, he joined Fujitsu Laboratories Ltd., where he has been mainly engaged in R&D work on microelectronics materials. During this period, he developed the world's first copper conductor co-fired 60-layer 8 inch ceramic circuit board, Low-k polymer thin film circuit boards for MCMs of mainframe computers, and high-density buildup circuit boards. Also, he has been involved with development of direct immersion cooling technologies for high-speed servers, including liquid helium cooling for Josephson devices and liquid nitrogen cooling for HEMT devices.

From 2000 to 2004, he was the director of the Advanced Optoelectronics Technology Dept. of Fujitsu Laboratories of America Inc., where he directed R&D work on optical integrated devices and optical interconnection technologies. He is currently a senior vice president of the Device & Materials Laboratories of Fujitsu Laboratories in Japan.

Mr. Yokouchi is a member of several scientific societies which include IEEE, IMAPS, OSA, and JIEP. He presently serves as a TC-6 committee member of the CPMT Society. Also, he co-chaired the Plenary Seminar of the 54th ETCT and CPMT Seminar at 55th ECTC. He also contributed as a technical committee member of IEMT/IMC in Japan.

He is the author or co-author of 55 technical presentations and publications, and invented or co-invented 29 U.S. and Japanese patents. He co-authored three technical books entitled "Thin Film Metallization for Aluminum Nitride" published by Trans Tech Publications Inc, "CSP/BGA Technologies" and "CSP Packaging Technologies" published by the Nikkan Kogyo Shimbun.

****

Save these pages of "profiles"; introduce yourself at the next conference or workshop!

CPMT Society Board of Governors Meeting

November 5th, 2005 - Dallas, Texas USA

The fall CPMT Society Board of Governors meeting was held on Saturday, November 5th, 2005, in Dallas, Texas, USA from 8:30 AM to 4:30 PM. The agenda was as follows:

8:30 Call to Order: Rolf Aschenbrenner
8:35 Review and Approval of Agenda: Rolf Aschenbrenner
8:40 Approval of Minutes of June 2006 BoG Meeting: Rolf Aschenbrenner
8:45 Report of Incoming President: Bill Chen
9:15 Finances: John Segelken
9:35 ECTC Integration - Report of Strategic Program Director: C.P. Wong
9.55 Publications - Report of Vice President / Strategic Program Director: Paul Wesling
- *Motion: Approval of IEEE Transactions on Components and Packaging Technologies Editors-in-Chief*

10:25 Education - Report of Vice President / Strategic Program Director: Albert Puttlitz
- *Motion: Approval of new Distinguished Lecturer*

10:55 Administration
- Report of Vice President: H. Anthony Chan
- Standing Committee Reports
- Nominations: John Segelken
- Fellows Evaluation: C.P. Wong
- Fellows Search: Dave Palmer and Rao Tummala
- Constitution and Bylaws: Tony Mak

11:15 Region 8 Programs - Report of Strategic Program Director: Johan Liu
11:45 Presentation
12:00 Lunch
1:00 Region 10 Programs - Report of Strategic Program Director: William Chen
1:30 Student Programs - Report of Strategic Program Director: William Brown
2:00 Conferences - Report of Vice President / Strategic Program Director: Ricky Lee
2:30 Technical - Report of Vice President / Strategic Program Director: Rolf Aschenbrenner
3:00 Awards and Recognition
- Report of Strategic Program Director Rao Bonda
- CPMT Technical Field Award

3:30 Global Membership and Chapters - Report of Strategic Program Director: Ralph Russell
4:00 Marketing - Report of Strategic Program Director: Connie Swager
4:20 New Business
4:30 Next Meetings Confirmation
- BoG Meeting – 2-3 June 2006 following 56th ECTC, San Diego, CA, USA
- BoG Meeting – November 2006 following ECTC Paper Selection Meeting, Dallas, TX, USA

4:35 Adjournment

Class of 2005 CPMT Fellows

Our congratulations to the following CPMT members of the IEEE Fellows Class of 2005! These leaders in our field were evaluated by the CPMT society (the first seven) and by other Societies (the final four).

Dr. William Chen, ASE Group
Santa Clara, CA USA

For contributions to packaging and assembly technology

Dr. Michael Lebby
Apache Junction, AZ USA

For contributions to optoelectronics technology

Prof. Johan Liu, Chalmers University of Technology
Department of Microtechnology & Nanoscience
Gothenburg, Sweden

For contributions to environmentally compatible electronic materials and processes

Prof. Madhavan Swaminathan
Georgia Institute of Technology
School of Electrical and Computer Engineering
Atlanta, GA USA

For contributions in design tools, design methodologies and electromagnetic interference (EMI) control for power delivery in digital and mixed signal systems

Dr. Michael McShane, Freescale Semiconductor, Inc.
Austin, TX USA

For contributions to the advancement of semiconductor packaging technologies

Prof. Paul Franzon, North Carolina State University
Raleigh, NC USA

For contributions to chip-package codesign

Dr. Gary May, Georgia Institute of Technology
Atlanta, GA USA

For contributions to semiconductor manufacturing and engineering education

Dr. Nikolaos Uzunoglu, National Technical Univ of Athens
Athens Greece

For contributions to electromagnetic theory with applications to scattering and guided wave propagation

Dr. Todd Hubing, University of Missouri-Rolla
Rolla, MO USA

For contributions to numerical electromagnetic modeling of complex printed circuit boards as applied to electromagnetic compatibility (EMC)

Dr. Qi-jun Zhang, Carleton University
Department of Electronics
Ottawa, Ontario Canada

For contributions to linear and nonlinear microwave modeling and circuit optimization

Prof. Gary Bernstein, University of Notre Dame
Department of Electrical Engineering
Notre Dame, IN USA

For contributions to techniques for fabricating nanoscale devices and circuits

****

CPMT's New Senior Members

Submitted by Marsha S. Tickman, Executive Director

Congratulations to the following CPMT Society members for achieving Senior Member status after August, 2005:

Albuquerque Section:	Alton D. Romig
Bangalore Section:	Kuppuswamy Raghunathan
Boise Section:	Chin Aik Le
	Wlliam Marsh, P.E.
Buenaventura Section:	Michael Diamond
Central Texas Section:	Leo Higgins
France Section:	Tarik Bourouina
Hong Kong Section:	Edmund Y. Lam
Orlando Section:	Scott Clary
Seoul Section:	Sung-Hoon Choa
Taipei Section:	Kuo-Ning Chiang
U.K. & Ireland Section:	Christopher Bailey
	John Goward

****

Membership & Chapters Update

Ralph W. Russell, II
CPMT Society – Strategic Director for Membership & Chapter Development
r.w.russell@ieee.org

Thank you for your support of the CPMT Society.
Thanks for renewing your membership each year.
Thanks for serving on the various committees.
Thanks for subscribing to CPMT publications.
Thanks for attending CPMT conferences.
Thanks for being a CPMT Chapter leader.
Thanks! Thanks! Thanks!

Each year the CPMT Society recognizes an outstanding Chapter. If you are a Chapter leader, please let us know about the great work your Chapter has done during 2005 and nominate your group for the Chapter of the Year Award.

****

In Memory of John Luther Prince III

Published by Tucson.com on 12/19/2005

John Luther Prince, III was born November 13, 1941 in Austin, Texas, to Glynda and J.L. Prince, Jr. He died December 16, 2005 in Tucson, AZ. He was a man full of faith. His family and friends were very important to him. He is survived by his high school sweetheart and wife of 45 years, Martha; children: Cindi (Dan) Cooke, John Prince IV, Alan (Cindy) Prince, and David Prince. While his children were young, John served as a coach in various baseball leagues and Y.M.C.A. baseball programs. He was a director of a youth football program as well. John was a member of Community of Hope Lutheran Church in Tucson, and considered it a privilege to serve as adult education teacher, council member, Stephen Minister, and in several other ministries there. He was a member of Alcoholics Anonymous for over 20 years, and served in several volunteer capacities through that organization. He enjoyed riding motorcycles, traveling, and collecting stamps and slide rules. His love of music ranged from Bob Dylan to medieval, to classical, shape-note singing and contemporary Christian.

John graduated from Southern Methodist University Magna Cum Laude with a B.S.E.E., and he earned an M.S.E.E. and Ph.D. from North Carolina State University. He was a member of the Technical Staff at Texas Instruments in Dallas, Texas, from 1969-1975. In 1975 he had the opportunity to apply his experience in industry at Clemson University in South Carolina. By the time he left there in 1980 he was a tenured professor in Electrical Engineering. From 1980-1983 he was Director of Reliability Assurance for Intermedics, Inc. In 1983 John and his family moved to Tucson where he returned to his true calling as a Professor of Electrical & Computer Engineering at University of Arizona. He served in numerous capacities including Director of the Center for Electronic Packaging Research. He founded the packaging program at the university and brought significant funding to the research program. He truly enjoyed advising his graduate students, some of whom became good friends and colleagues. He also published many technical journal articles and books. John served as a Distinguished Visiting Scientist and Director (Acting) of Packaging Sciences for Semiconductor Research Corp. in 1991-1992. John was a Fellow of IEEE, and a member of the Electron Devices, Microwave Theory and Techniques, Reliability, Solid-State Circuits, Components, Packaging & Manufacturing Technology groups of IEEE. He was a member of Sigma Xi, Phi Kappa Phi, Eta Kappa Nu, and Phi Eta Sigma honorary societies. Among his awards were the Inventor Award from SRC in 1988, and the 1988 Semiconductor International Technology Achievement Award. In 1991 he received an award as Arizona Innovator of the Year. John Prince will be missed by many - family, friends, and colleagues. The family suggests that in lieu of flowers, memorials be given to the Salvation Army, in John's name.

Additional Notes:

Ravi Kaw, Agilent Technologies – "My best friend John decided to say a final goodbye. I feel sad but calm as well, since he was a deeply spiritual person at heart. We talked often about what to do during retirement, and his wish was to help people, which he did all his life, and also to spend time in solitude in a seminary. That is what drove him to help the poor and with the mentoring etc that he used to do. He helped develop people professionally as well. He was a great organizer, motivator, teacher, and a devil's advocate to get his point across. I shall certainly miss him - especially that ever-present smile. I know he is in a better place."

Alina Deutsch, IBM Corp. – "There have been a handful of people in my life who influenced me significantly, and John was one of those. His memory shall be very dear to me always.

This is a great shock to us all. John had some health problems but he recovered very well and seemed quite energetic. I do not think he missed more than two EPEP meetings in fourteen years. He had a tremendous dedication to the conference and made great contributions to its success. He always brought up some issues to argue about but he was very wise and insightful. He brought Paul Baltes, Kelly Sutton and Pam Dwyer on board and that was the most significant step for the organization of the EPEP conference. The team has made the smooth running

of fourteen successful years for the conference possible. John is probably one of the most well recognized and respected person in the CPMT society and he was the founder of the packaging center at University of Arizona. He mentored many good students that were hired at Intel, IBM and other companies and he always supported their work and was there for them in spite of his many travels. He has visited every possible packaging research center in the world and everybody knew him and respected his work. He had a broad vision for packaging that he embodied in all the activities that he touched.

We will all miss him."

****

C.P. Wong to Assume Smithgall Institute Chair

Dr. C.P. Wong, a Regents' professor in the School of Materials Science and Engineering, has been named the Charles Smithgall Chair, one of two Institute chairs at Georgia Tech.

"I'm pleased that Professor Wong has accepted this chair," Provost Jean-Lou Chameau said. "His reputation and distinction on our campus and in the field of materials embodies the spirit of the role for a senior leader at Georgia Tech." A member of the National Academy of Engineering, Wong joined the faculty in 1996 as a professor and as a research director of the Packaging Research Center (PRC). In 2004 he received Tech's Distinguished Professor Award, the most prestigious award bestowed upon Tech faculty members.

He leads a team in the PRC's Assembly, Reliability, Thermal Management and Electrical Testing Thrust areas. He has recruited 15 new member companies and has also become the PRC's director of Tech Transfer and Industrial Collaboration.

"I thank the Smithgall family for their generosity and commitment to research and education," he said. "As one of two Institute endowed chairs, I'm very pleased to assume this title and honored to represent Georgia Tech in this way."

Wong holds a bachelor's degree in chemistry from Purdue University and a doctoral degree from Pennsylvania State University.

****

Conference and Workshop Reports

Future Directions in IC and Package Design Workshop

FDIP' 05, Austin, TX

Workshop co-chairs: Alina Deutsch, IBM and
Madhavan Swaminathan, GIT

This year's workshop was held once again on the Sunday afternoon before the start of the EPEP'05 conference, on October 23, 2005. Attendance was very good again with 70 participants. The workshop was sponsored by the TC-EDMS technical committee on electrical design, modeling, and simulation and co-chaired by Prof. Madhavan Swaminathan from Georgia Institute of Technology and Alina Deutsch from IBM Corporation. Prof. Swaminathan is also the chair of the TE-EDMS that sponsors five workshops across the world.

FDIP'05 was divided into three sessions namely, System Design, Modeling and Measurement Methods for Signal Integrity, and Computational Electromagnetics. The three session chairs were Tawfik Arabi from Intel, Anand Haridass from IBM, and Ramesh Abhari from McGill University. The first session started with the presentation made by Carl Anderson from IBM Austin. The title of his talk was Designing Servers in a Commodity World. The key message he tried to convey was the fact that the high-end servers need to provide the high performance using only commodity technologies due to cost measures. The high-volume market of personal computers that are selling for $1,000 is the fastest growing and driving the introduction of low cost technologies. The only solution then for high-end systems is to use multi-core chips (Carl sees 8+ cores on chip by 2010) with on chip switch, use of multi-threading, standard I/O's such as PCI Express, power efficient designs, systems that scale out into blades, with system level reliability delivery, and software that can take advantage of GRID computing for cost competitive solutions.

The second talk entitled Signal Interconnect and Challenges Inside the CEC was delivered by George Katopis from IBM Poughkeepsie The main message he tried to convey was the need to change the industry's focus from chip design to interconnects as the key system performance detractor. He reported on a very detailed analysis of single- versus differential-ended transmission. The study considered power, data bandwidth, bit data rate, and chip area per bit. George predicted that by 2010, interconnect bandwidth requirement will reach 5-10 GHz with a required spectrum of interest up to 25-50 GHz. At a 95 mm node, the single-ended lines can achieve 0.012 mm^2/line, 1.25-2.5 Gbps/line and 104-208 Gbps/mm^2 for 30 inch lengts. The equivalent differential links, for 6 inch lengths, have 0.25 mm^2/line, 5.4 Gbps/line and 22 Gbps/mm^2. Clearly the differential solution is much more extendable. It has 60-70% bandwidth advantage. This advantage comes at a significant cost in power and chip area. The performance advantage is also degraded by packages with large discontinuities such as long via stubs. DE solution is equivalent to SE where loses are dominant but where noise induced jitter is the main concern, DE is preferred. Another important message to the academia was that for 25-50 GHz spectrum, there is a very strong need for better measurement techniques and modeling tools. Both the tools and the characterization need to address the full complexities of product like structures.

Brian Young from Texas Instruments brought forth a new design methodology in his talk entitled High Volume Signal and Power Integrity Design for ASICs. Brian indicated that the ASIC chips of today have clock frequencies of over 500 MHz, power levels as high as 10W, integrated links up to 6 Gbps. In order to design the packages needed for such high-end chips in very short time (around one month), a pre-characterization procedure was developed with separate signal and power integrity analyses. A large data base is created with >18K results that can be looked-up when the selection needs to be made. Superposition is used to sum worst-case conditions of noise for the power supply and interconnects and multiple evaluations are made to explore the design space for number of layers, I/O's, placement, bypass capacitors, interconnect length, etc.

The fourth presentation made by Mizuki Iwanami from NEC, entitled Electro-magnetic Field Visualization System for IC/Package Design Based on Optical Techniques, showed a very novel probing technique. A magneto-optic/electro-optic (MO/EO) crystal glued at a fiber edge was used for very small LSI circuit probing. An incident light in the MO/EO crystal is reflected by a dielectric mirror on the bottom surface and re-enters the fiber. During one round trip, the light responds to the magnetic/electric field surrounding the DUT and thus near-field distribution can be scanned over the DUT. Examples were shown for the field distribution scanning of 20 μm meander micro-strip lines over the frequency range 10 MHz to 2.46 GHz. Magnetic field was also scanned in LSI package and EMI around the decoupling capacitors was detected. The probe is considered very useful for both signal and power integrity analysis. The probe position height could vary in the range of 3-15 μm above the DUT.

The last two talks covered two approaches in computational electromagnetics. Prof. Raj Mittra from Pennsylvania State University talked about harnessing the power of Parallel Computation on the IBM Blue Gene/L to analyze complex digital and RF systems. Due to the increasing complexity and problem size requirements for electrical modeling, the development of techniques that allow the use of parallel platforms has been gaining momentum. Raj introduced the Parallel Finite Difference Time Domain full-wave solver that takes full advantage of the very efficient processor-to-processor communication of the Blue Gene supercomputer. Efficiency close to 90% was shown on up to 256 processors due to the only near-neighbor interactions needed by PFDTD. Both the CBMOM and PFDTD solvers were used on very large problems with close to 10B unknowns and simulation examples were shown.

The last talk in the workshop was given by Prof. Weng Cho Chew from University of Illinois. Prof. Chew showed examples of 20 million unknowns using integral equation solutions on SP type clusters . The equivalence principal algorithm, EPAL, developed at UIUC allows the mixing of circuits and wave physics as needed by practical packaging structures. While quasi-static solvers can handle billion unknowns, full-wave problems can only reach millions due to the need for far-neighbor interaction capturing. He talked about the recently developed mixed-form fast multi-pole algorithm that can work seamlessly from static to the microwave regime. It is both accurate and error controllable, as well as being memory efficient.

In the case where both wave physics and circuit physics are important, such as a large structure with many small details as found in a computer system, it is more expedient to put Huygens' equivalence boxes around each region with fine details, and decouple the exterior problem from the interior problem. This can be regarded as having replaced a region with fine details with an N-port representation. Inside the Huygens' boxes, low-frequency techniques can be used to solve the problem so that low-frequency physics is correctly captured, with the ensuing geometry details. Outside the Huygens' boxes, when wave-like interactions are computed, less number of unknowns are needed to capture the wave physics, but meanwhile, the ability to model fine details is not foregone.

Low-frequency breakdown is encountered for numerical solvers when structures are smaller < λ. For integral equation solvers, low-frequency breakdown is prevented by using quasi-Helmholtz decomposition, while for fast algorithm, low-frequency multi-level fast multi-pole algorithm LF-MLFMA and low-frequency multi-level inhomogeneous plane wave LF-FIPWA have been developed to overcome this problem. Furthermore, a mixed form fast multi-pole algorithm MF-FMA has been developed to realize the broad frequency range modeling. Solution speed is accelerated and workload and memory requirements are decreased from $O(N^2)$ to O(N). Very large problem sites with < 1 GB memory needed were shown to run on typical personal computer platform with the use of such advanced numerical techniques.

****

Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications

Submitted by Vasudeva P. Atluri, Ph.D., Workshop Chair and Charles E. Weitzel, Ph.D., Workshop Co-Chair

The IEEE Phoenix Section's CPMT Chapter with the Waves and Devices Chapter jointly held an all-day Workshop on Thursday, November 10th, 2005, at Arizona State University, Tempe, Arizona. The workshop was very well attended with about 196 registrants. The breakdown of registrants included 27 organizing committee members, 12 speakers, 22 vendor representatives, 72 IEEE members (included 5 student members), and 63 non-members (including 1 student). The workshop agenda included these talks: (PDFs of the slides will soon be available in the CPMT Members-Only web area: www.cpmt.org/mem).

1. "*Keynote Presentation: Moore's Law Redux: Research in the Age of On-Chip, Converged Communication and Computing*", Dr. Krishnamurthy Soumyanath, Intel Corp.
2. "*A 2005 Perspective on MOSFET Scaling Challenges and Technology Innovations Through the End of the Roadmap*",. Peter Zeitzoff, SEMATECH International
3. "*Advanced Devices for Future CMOS Nodes*", Dr. Suresh Venkatesan, Freescale Semiconductor, Inc.
4. "*Challenges for TCAD for Advanced Devices*", Dr. Mark Law, Univ of Florida.
5. "*Opportunities and Challenges of III-Nitride Semiconductors*", Dr. Zlatko Sitar, North Carolina State Univ.
6. "*Wireless Integrated MicroSystems (WIMS): Coming Revolution in the Gathering of Information*", Dr. Kensall Wise, Univ of Michigan
7. "*Flip Chip Packaging Technology for Next Generation Computing Applications*", Raj Master, AMD
8. "*Future Decoupling Technology for High-Speed Integrated Circuits*", Richard Ulrich, Univ of Arkansas
9. "*Electromagnetic and Circuit Co-Simulation – The Key to Next Generation Interconnect Design*", Dr. Zoltan Cendes, Ansoft Corp.
10. "*Hot-Spot Driven Thermal Management for Next Generation Computing and Communication Technology*", Dr. Avram Bar-Cohen, Univ of Maryland
11. "*Pb Free Interconnect: Industry Status & Trends*", Tim Olson, Ahmer Syed, and Jeff Cannis, Amkor Technology

12. "*3D Integration Technologies – Motivation and Status*", Dr. Rajen Chanchani,
13. Panel Discussion "*Future of Computing and Communications.*"

The morning session with a focus on Moore's Law Redux, A 2005 Perspective, Advanced Devices, Challenges, Opportunities and Future was very received by the workshop audience. Dr. Krishnamurthy Soumyanath suggested that the availability of low cost and power efficient MIPS (a direct consequence of Moore's law) makes ubiquitous mobile communications possible. The talk described a "digitally assisted analog" chip design methodology for on-chip, converged, communications and computations. Dr. Peter Zeitzoff summarized the overall scaling trends and issues for logic MOSFETs from the perspective of the 2005 International Technology Roadmap for Semiconductors (ITRS). Critical challenges with scaling include unacceptable increases in gate leakage current, increasing impact of polysilicon gate depletion, difficulty in obtaining adequate control of short channel effects, as well as others. Key technological innovations (referred to as "potential solutions" in the ITRS) to address these challenges include high-k gate dielectric, metal gate electrode, strained silicon channel to enhance the carrier mobility, and eventually, non-classical CMOS devices such as fully depleted, ultra-thin body, multiple-gate MOSFETs (e.g., FinFETs). Dr. Suresh Venkatesan covered the advanced device requirements and challenges for future CMOS nodes. With the non-scaling of gate oxides over the past few technology nodes, innovations in mobility scaling have been paramount to maintain performance requirements (different market segments having different power/performance operating points). Dr. Mark Law asserted that as Moore's Law drives device scaling, TCAD becomes both important and difficult. TCAD often becomes the only way to debug a problem or investigate an issue. His talk discussed modeling frameworks for making progress and covered recent experimental work that sheds light on the directions that need to be pursued for model development for future technologies. Dr. Zlatko Sitar indicated that unique properties of III-Nitrides (AlN, GaN, InN) make them superior for high power and high frequency applications. High current values in III-Nitride FETs can be combined with very high breakdown voltages, resulting in high power outputs. These devices have potential to replace traditional GaAs based microwave power FETs used in wireless communications. In his talk, a completely new approach was offered by the ability to grow controllably polar domains of different orientations side-by-side. These structures make use of the crystal polarity as a new degree of freedom for novel device structures that will be insensitive to surface charge. Dr. Ken Wise suggested that wireless integrated microsystems promise to become pervasive during the coming decade in applications ranging from health care and environmental monitoring to homeland security. Merging low-power embedded computing, wireless interfaces, and wafer-level packaging with microelectromechanical systems (MEMS), the resulting button-sized modules will serve as smart information-gathering nodes that will effectively wire the planet, extending communication networks to a wide range of new information-gathering applications. This talk highlighted two emerging microsystems – an implantable neural microsystem and a wristwatch-size environmental monitor.

The afternoon session focused on packaging technology, decoupling technology, electromagnetics and circuit simulations, thermal management, lead free, 3D integration, and panel discussion. Mr. Raj Master's talk included an overview of flip chip technology and challenges, package technology and manufacturability / design challenges, assembly technology and challenges, thermal issues and solutions, and overview / challenges of low K. Dr. Richard Ulrich explained that decoupling is the practice of bridging the power and ground planes of interconnect substrates with capacitors, which are distributed in location and value between the power supply and the IC. These caps provide the power to run the chip; the power supply just recharges the caps between clock cycles. The presentation reviewed the decoupling problem in general, the limits of using discrete capacitors, and the family of proposed future approaches that utilize embedded capacitance, including ferroelectric and paraelectric dielectrics, their possible inclusion into PWB's, their electrical performance and manufacturing issues. Dr. Zolton Cendes stated that engineers designing servers, storage devices, multimedia PCs, entertainment systems, and telecom systems that have driven an industry trend to replace legacy shared parallel buses with high-speed point-to-point serial buses. His talk presented a new reference design flow for high-speed serial interconnect simulation. The new flow included electromagnetic models for interconnects combined with advanced circuit simulation technology to model modern multi-gigabit transmission. Recent work on PCI Express backplane design, the Xilinx 10 Gb/s Backplane Design Kit, ultra-wideband radio design, and RFIC full chip extraction with on-chip spiral inductors was presented as application examples. Dr. Avram Bar-Cohen suggested that as Moore's Law progresses into the domain of nano-scale electronic, RF, and photonic features, steep increases in die heat flux and power dissipation results with the emergence of on-chip hot spots as the primary driver for advanced thermal packaging techniques. Following a brief review of the iNEMI thermal management roadmap for IC technology and the primary thermally-driven failure mechanisms, he talked about the thermal packaging "frontier" and the research required to address these emerging challenges. Mr. Tim Olson mentioned that with the July 1, 2006 European RoHS (Reduction of Hazardous Substances) directive deadline approaching, the electronic production supply chain is facing an unprecedented challenge in conversion to Pb free interconnect materials. His talk addressed the technical merits and existing concerns with respect to the implementation of the various RoHS compliant solutions. Dr. Rajen Chanchani provided an overview of 3D integration technologies including the motivation, description of the key technologies, and status of the technologies. The main motivating factors are 3D integration that enables miniaturization of Microsystems, a wider variety of technologies can be integrated with 3D integration, and electrical performance of 3D technology will be better. Various 3D technologies were described including issues associated with each category of technologies.

The day ended with an hour long panel discussion consisting of nine speakers and moderated by Dr. Stephen M. Goodnick. The topic was "Future of Computing and Communications". About 40 people were in audience for the panel discussion.

The Premier Sponsors included Freescale Semiconductor, IEEE Phoenix Section, and Intel Corporation. The Standard

Sponsors included Arizona State University Department of Electrical Engineering and Connection One Center, the local chapters of APS, CPMT, MTT, Motorola, and RF Micro Devices. Many workshop attendees, including both IEEE and non-IEEE members, stopped by the IEEE display and were impressed by the information about local chapters, literature, and membership forms. This sparked quite a bit interest among non IEEE members for joining IEEE. Total of 18 vendors displayed at the workshop. Vendors included 3M Electronics, Advanced Packaging & Systems Technology Laboratories, Ameriprise Financial Services, Ansoft Corporation, Cadence Design Systems, CMC Interconnect Technologies, Fluent, GE Silicones, Jacket Micro Devices, Namics Technologies, Optimal Corporation, Phoenix Analysis & Design Technologies, Rogers Corporation, SONNET Software, Tango Systems, Techsearch International, Tektronix, and Zeland Software.

By bringing renowned speakers to address the most relevant topics, the workshop once again provided an excellent learning opportunity for professionals in valley. In addition to raising funds for IEEE's Phoenix Section, CPMT chapter and WAD chapter, one of the goals of the workshop is to help increase the IEEE Phoenix Section Scholarship Endowment at the Arizona State University Foundation. Continuing with the tradition from the previous three years, 50% of the surplus was donated to the Endowment. This year US$11,000 was donated, bringing the total contributions from the last four workshops to about $28,000. This endowment is helping IEEE Phoenix Section give awards to undergraduate IEEE student members. The students from Arizona State University, Devry Institute, Embry-Riddle Aeronautical University, and Northern Arizona State University are eligible to apply for these scholarships. Additional information about the workshop including organizing committee and logistics can be obtained at www.ieee.org/phoenix.

Picture of organizing committee members and volunteers in front of IEEE Phoenix Section display at the workshop

****

EDAPS 2005: A workshop on Electrical Design of Advanced Packaging and Systems

Submitted by K. Raghunathan, Chair, IEEE CPMT Bangalore Chapter

The EDAPS 2005 conference was held at Bangalore India on Dec 12th & 13th coinciding with the first anniversary of the launching of the local CPMT chapter. The conference sponsored by CPMT technical committee and mentored by Prof. Madhavan Swaminathan of PRC, Georgia Tech. The response to the conference was very positive with nearly 100 attendees and 14 invited speakers from Japan, Korea, China, India, Canada and USA. The participants were from 3 diverse groups: Practicing engineers from semiconductor industry, government/ public sector companies and academia. The feedback has been very positive with request for more in-depth presentations and also addressing practical issues encountered. The previous chairs from EDAPS (2002 - 2004: Dr. Mahadevan Iyer, Singapore; Prof. Joungho Kim, Korea; Dr. Toshio Sudo, Japan) graced the occasion to make it successful through their presentations and participation.

Day 1 tutorials covered issues in Power Delivery and Signal Integrity for high speed Design; it was followed by RF and microwave packaging. Earlier in the key note Bill McCaffrey of Cadence highlighted the acceptance of SiP as a solution; he went on to elaborate and indicated uniform extraction capability for accurate modeling and mixed technology simulation are being addressed at the tool level.

Day 2 started with a keynote from Rao Tummala from Georgia Tech PRC; he outlined in his talk that embedding extra elements in substrate (especially lossless) could lead to minimizing the size; the future holds promise for bio and nano devices; the Mantra is SoP. P. R. Patel of Intel eloquently explained the multi-disciplinary nature and the intrigues of the interdependencies. Limitations in packaging performance due to thermal, reliability and material issues compared to electrical issues was highlighted. The invited papers were grouped into Power Delivery, High speed signal integrity, RF & Microwave packaging and System design challenges. The topics varied from small form factor for DDR2 interface to tuning the impedance for ultra high speed designs with high power dissipation.

A glimpse of the audience at the workshop

The next EDAPS 2006 is planned to be held at Shanghai, China under the chairman ship of Wen-Yan Yin. EDAPS 2005 Program committee chairman Suresh Subramanyam (Intel) with the volunteers has done an outstanding job of hosting the conference in Bangalore. The Chief Guest at the inauguration of the conference K. Ramachandra Kini, Director, SAMEER (Society for Applied Microwave Electronic Engineering & Research) emphasized the need for developing indigenous packaging capability soon. IEEE Fellow and IEEE Bangalore section President Surendra Pal highlighted the benefit of microminiaturization in the launch of satellites especially the pico satellites. Overall this has been a very useful workshop to the participants and appreciates the support from all over the globe.

A photograph of speakers who presented at the workshop

****

14th Topical Meeting on the Electrical Performance of Electronic Packaging

Robert W. Jackson,
Professor, Dept of Electrical and Computer Engineering
University of Massachusetts, Amherst, MA, USA

The 14th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP) was held October 24-26, 2005 at the Radisson Hotel, in Austin Texas. EPEP provides a forum for the presentation and discussion of the latest advances in the electrical design, analysis and characterization of on chip and off chip package interconnections and structures. One of the key objectives of this meeting is to bring together researchers and practicing engineers from industry, universities, and government laboratories from around the world to address all current and future issues affecting the electrical performance of high speed electronic systems. The meeting is jointly sponsored by the IEEE Microwave Theory and Techniques Society, and the IEEE Components, Packaging and Manufacturing Society.

The conference was organized into eleven sessions of oral presentations and one open forum (poster) session spread over the three days. The meeting began with a keynote speech entitled "The Role of System Integration and Packaging in Future Computing Systems," by Mark Papermaster, VP, Microprocessor Technology Development, IBM Corporation. This was followed by sessions dedicated to System Design and Technology, Power Distribution and Noise, Electromagnetic Issues, Transmission Lines, Measurements, On-Chip Issues and Interconnection Macro-modeling. The open forum was held in the afternoon of the second day (Tuesday) and the open bar with hor d'oeurvres encouraged relaxed technical discussions. A technical highlight of the conference was a special session entitled, "Accurate Full Wave Interconnect EM Modeling from DC to 100 GHz" organized by Professors A. Cangellaris and W. C. Chew of University of Illinois. Three short courses were offered on the Sunday prior to the start of the meeting. These tutorials were given by well-known experts in their fields and covered important topics in the design of high-speed interconnect, power distribution networks and I/O circuits.

A total of 20 student authors competed in the prestigious Best Student Paper contest. The two award winners were announced on the last day of the meeting. The best student paper award sponsored by IBM Corporation was presented to Satoshi Aoyama, Shizuoka University for her paper entitled, "A High-sensitivity Active Magnetic Probe Using CMOS Integrated Circuit Technology". The best student paper award sponsored by Intel Corporation was given to Lei Luo, North Carolina State University for his paper entitled "Signal Integrity Robustness of ACCI Packaged Systems." On behalf of the entire Technical Program Committee, the chairs of the 14th EPEP want to extend their thanks to Intel Corporation and IBM Corporation for sponsoring these awards. They really add a lot to the conference.

Keynote speaker Mark Papermaster, Vice President, Microprocessor Technology Development, IBM Corporation

The 15th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP) will be held at the Radisson Fort McDowell Resort in beautiful Scottsdale, Arizona on October 23 – 25, 2006. Moises Cases of IBM and Paul Franzon of North Carolina State University will be co-chairs. Mark your calendars and keep an eye on **www.epep.org** for the latest developments.

****

7th Electronics Packaging Technology Conference (EPTC 2005)

7th – 9th December 2005

Grand Copthorne Waterfront, Singapore

Report by Singapore REL/CPMT/ED Chapter

The 7th Electronics Packaging Technology Conference (EPTC 2005) was successfully organized on 7th -9th December at the Grand Copthorne Waterfront Singapore. The conference was well attended over the 3 days. A total of 87 delegates participated in the short courses on 7th December 2005. This is by far the best turn-out for any EPTC-organized short course.
The conference on 8th-9th December was attended by a total of 265 delegates from over some 19 countries. EPTC 2005 was organized by IEEE Reliability/CPMT/ED Singapore Chapter, sponsored by IEEE CPMT Society with technical sponsorship from IMAPS. EPTC 2005 also enjoyed corporate conference sponsorship from Advanced Micro Devices Singapore, Agency for Science, Technology and Research Singapore (A-Star), Micron Semiconductor Asia and United Test & Assembly Center (UTAC).

The conference was inaugurated by Dr William Chen, IEEE CPMT Region 10 Strategic Director and CPMT President Elect, who endorsed EPTC as "a premier Asian Conference with global participation" and encouraged delegates to maximize their time at the conference through interaction, learning and sharing. He also sealed the commitment from CPMT to the EPTC series for many years to come.

In the plenary session, Dr Robert Darveaux from Amkor Technology discussed the "Current Trends and Critical Issues in Flip Chip Packaging" and Dr Chiang Shiuh-Kao from Prismark, to gave an insight on "The Global Packaging Business and Technology". An invited talk "CPMT and EPTC: A study in Symbiosis" was delivered by the CPMT representatives Dr William Chen, Prof Klaus-Jürgen Wolter and Dr Ricky Lee during the conference day 1 luncheon.

The EPTC series ran into its seventh year and has enjoyed a steady growth in terms of attendance and technical paper submissions. It has also attracted all aspects associated with the packaging of high performance electronics. EPTC 2005 featured 159 presentations in 34 sessions from experts coming from some 21 countries and dealt with advancements in core technologies such as interconnect technologies, electrical and thermal design, materials and processes, mechanical modeling and characterization, assembly and reliability assessment methodologies; as well as state-of-the-art packaging platforms in System-in-Package & MEMs packaging.

Three pre-conference short courses were offered to provide learning avenues from leading experts in specific technical fields. Dr George Harman conducted a wire bond interconnection course covering all aspects of wire bond technology as well as its application for copper low-k. The second course was a comprehensive lead-free reliability class that dealt with material, reliability & modeling aspects to lead-free implementation and development. Its course instructors included, Dr John HL Pang, Dr Rainer Dudek, Dr Tee Tong Yan, Dr Lim Chwee Teck and Dr Jason Wu. Lastly, the wafer level packaging course instructed by Dr V. Kripesh and Dr Luu T. Nguyen, dealt with process, technology, materials and applications for WL-CSPs. In conjunction, the conference also featured a table-top exhibition where about 12 exhibitors showcased their technical products and services.

The EPTC conference banquet had become a trademark of EPTC and so in continuing this tradition, a river taxi cruise from the hotel to the Marina Bay area was organized. Delegates traveled along the Singapore River in bumboats and were treated to the sights and sounds of the Singapore's financial and entertainment district. They also caught a close-up of the Merlion statue and the grandeur of the Esplanade by the Bay. The banquet dinner held at the Colors-by-the-Bay treated the delegates to local delicacies such as chilli crabs, satay, kueh tutu, etc.

Contribute an abstract for EPTC'06; visit our website:
www.eptc-ieee.net

CHAPTER NEWS

BOSTON CHAPTER:

IEEE/CPMT News and Pictures by Dan Bauks Boston Chair

The Boston CPMT chapter (www.ieeeboston.org) continues to have a busy local chapter season with all meetings held at Sun Computer in Burlington, MA. (pic #1) This May (2006) we celebrate our 3rd ELECTRO Technical Conference with the Nepcon-East Symposium and our 1st Medical Electronics Conference with IMAPSNE.

Meetings:

11/30/04 Ion Beam Milling Inc., Robert Quagan – President (pic #2) "Laser Diode Heat Spreaders for Photonics and Electronic Packaging"

12/21/04 Konarka Inc., Dan McGahn – Ex VP & Chief Mkt Officer, "Building photo voltaic cells on low cost flexible light weight plastics"

2/15/05 SI2 Technologies , Erik Handy Ph.D, « Direct write technology using laser transfer placement for drone military aircraft antennas"

3/29/05 V.J. Electronix , Don Naugler – GM, "Advanced imaging techniques for lead free & other x-ray inspection challenges"

4/26/05 CST of America, Roy Arsenault –Tech Sales Mgr, "Broadband signal integrity optimization with CST microwave studio" (pic #3)

5/4/05 IEEE Electro Technical Conference (pic #4), MRSI/Newport Corp, Peter Cronin – Product Specialist, "Die placement equipment in the micro electronic industry" – V.J. Electronics Inc., Don Naugler – GM "Advanced x-ray imaging inspection challenges with multi-laser assemblies"" – Photomachining Inc., Ron Schaeffer, Ph.D – CEO, "Laser micromaching applications in the microelectronics industry"" – Polymer Assembly Technology, Jim Clayton – President " Flip chip assembly using conductive polymer adhesives" – CST of America, Roy Arsenault Tech Sales Mgr, "Simulation software for high frequency problems for electronic components" – Quantum Leap Packaging, Mike Zimmerman –Founder, "Next Generation high power RF & microwave packaging based on liquid crystal polymer technology" (pic #5) " – Sky Works, Joe Adams, - VP Strategic Mktg, "The ITRS and NEMI packaging roadmap overview"

10/29/05 Bleck Design Group, Inc., Jim Bleck – President, "Industrial Design in Electrical Engineering"

2/24/06 CheapTubes, Inc. Mike Foley, "Nanotubes 101: what are they, how are they made, what are the properties?"

3/21/06 Polymer Assembly Technology, Jim Clayton – Founder, "Conductive polymer adhesive assembly applications in space & on the earth"

4/18/06 DS&A, Dave Saums – Principal, "Thermal testing of interface materials"

5/10/06 IEEE Electro Technical Conference, Dan Bauks– ElectroChair, Six to eight sessions planned this year

5/16/06 IMAPSNE Tech Symposium, Dan Bauks – Session Chair, Medical electronics session - three to four speakers planned

(1) Boston IEEE/CPMT meetings at Sun (2) Dan Bauks & Bob Quagan (3) Dan Bauks & Roy Arsenault (4) IEEE "Electro" CPMT Conference (Jim Clayton & Ron Schaeffer) (5) Mike Zimmerman and Dan Bauks

SANTA CLARA VALLEY Chapter:

News from Paul Wesling, Chapter Advisor

Our Chapter has so many good speaker candidates now that we have expanded our program to feature one dinner meeting plus one lunch meeting in most months. For the final months of 2005, we had the following speakers:

"Kirkendall Voids in Lead-Free Solder Joints: A Reliability Issue" Zequn Mei, Cisco -- September Dinner.

"Robert Noyce: The Man Behind the Microchip" Dr. Leslie Berlin, Stanford Univ -- September Lunch.

"Imprint Patterning: An Alternative Circuit Fabrication Process" Craig Davidson, Dimensional Imprint Technology, Inc. -- October Dinner.

"Drop-Testing of Components in Portable Applications" Dr. Luu Nguyen, National Semiconductor -- October Lunch.

"Carbon Nanotubes: Enhancing Conductivity of Conductive Plastics" Dana Hammer-Fritzinger, NanoDynamics -- November Dinner.

"The Future of Printed Circuit Boards" Robert Tarzwell, Director of Technology, Sierra Proto Express -- December Dinner.

In most cases, the slides from these talks (in PDF format) are available on the meeting web page. See

www.cpmt.org/scv/past.html

or the CPMT Members-Only website.

The Santa Clara Valley Chapter's AdCom planning meeting in December. **Upper photo:** Ed Aoki (Agilent), Paul Wesling (IEEE), Bill Chen (ASE), Dan Donahoe (Exponent), John Jackson (Analog Devices). **Lower photo**: Allen Earman (Finisar – with chop sticks), Bernie Siegal (TEA), Liz Logan (LV Sensors), John Jackson (Analog Devices), Annette Cheung (Corwil), Tom Tarter (Neophotonics). The photographer (not shown) was Janis Karklins, our Membership Development chair.

REGION 10 CHAPTER ACTIVITY ROUND-UP:

Dr. P.B. Parikh, Region 10, Mumbai, India

Hong Kong Chapter:

Dr. Ming Li – Chairman - Hong Kong Chapter has arranged three one-day workshops as follows:-

(a) "Impacts of EU RoHS and China RoHS on Design, Materials, Process, Manufacturing, and Reliability of Electronics Products" by Dr. John Lau on 6th May, 05.

(b) "Polymers for Electronic and Photonic Packaging:- Materials, Process and Reliability" by Prof. C. P. Wong on 21st June, 05.

(c) "Packaging and Board Assembly: Technology Trend Materials, Processes and reliability" by Dr. Dongkai Shangguan being scheduled on 15th December, 2005.

The Chapter also organised a half day workshop on 25th August, 2005 on "Virtual Thermo-Mechanical Prototyping and Qualification of Microelectronics and Microsystems" by Dr. C. Q. Zhang. The Chapter has nominated Five IEEE members to be upgraded to senior membership this year.

Dr. Ming Li has informed all that Dr. Derek Or will be their new Vice-chair and Chair-elect and that there will be no election for Chapter Vice-chair and Chair-elect this year.

Singapore Chapter:

Dr. K. L. Pey has reported that the Singapore Chapter has successfully arranged four Technical talks, one Workshop, one Short Course and two major events during the second half of 2005 (June-Dec. 2005).

The Technical talks are as follows:

a. "From TDDB Reliability to Circuit Reliability" on 21st July, 2005 by Dr. Ernest Y. Wu, IBM System and Technology Group.
b. "Nanotube and Nanowire Transistors" on 5th September 2005 by Prof. Gehan Amaratunga, Engineering Department, Cambridge University, UK.
c. "Reliability of RoHS (e.g. Pb-Free) product with Emphasis on Solder Joints" on 12th October, 2005 by Dr. John Lau, Agilent Technologies, USA.
d. "Compact Modeling of Thermal Noise in the MOS Transistor Using the EKV Model" on 30th November, 2005 by Prof. Christian Enz, Swiss Center for Electronics and Microtechnology.

The Chapter also organised a one-day Workshop on Nanometer CMOS Technology (WIMNACT-Singapore) on 2nd July, 2005. A one-day Short Course on "Negative Bias Temperature Instability in p-MOSFET Devices" by Prof. Souvik Mahapatra, IIT Bombay was arranged on 7th November, 2005. Dr. K. L. Pey has also reported to have arranged two major events as follows:-

a. 12th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2005), 27th June to 1st July, 2005.
b. 6th Electronics Packaging Technology Conference (EPTC 2005), 7th to 9th December, 2005. Since this is a major international event related to IEEE CPMT, a detailed Report on this conference has also been given elsewhere in this Newsletter.

Dr. Alastair Trigg represented the IPFA Board to attend the ESREF' 05 plans, in October, 2005 and Dr. Radhakrishanan represented the IPFA Board to attend the ISTFA'05 meeting in November, 2005 USA.

The Chapter has also planned 13th IPFA meeting to be held next year from 3rd to 7th July, 2006 in Singapore.

Bombay Chapter:

India Council Chapter with **SMTA** India Chapter jointly organised a national level one day seminar on "Issues related to implementing LEADFREE Technology in electronic production" on 8th September, 2005 in New Delhi. The Seminar was well attended by about 45 delegates from all over India including eight IEEE CPMT members. State of the art technology papers were presented by Dr. Dieter Friedrich – Germany, Mr. Peter Lensch – ERSA, Dr. Krishan Kumar, Dr. R. Sengupta and others. This was followed by a dinner hosted by ELCINA – India.

The Chapter has also actively Co-sponsored IMAPS India two days conference on "Microelectronics and VLSI" at IIT Bombay on 20th and 21st December, 2005. The conference would be preceded by four parallel sessions of tutorials on 19th December, 2005. Eight Technical Sessions including three Poster Presentation Sessions have been planned. More than 200 delegates have already registered for the conference. A full report of the conference will be presented at the next issue of the CPMT Quarterly Newsletter.

****

CALL FOR NOMINATIONS

2006 IEEE Components, Packaging & Manufacturing Technology Award

Submitted by Dennis Olsen, Ph.D.

IEEE's Components, Packaging & Manufacturing Technology Award is presented for meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies.

The Award is sponsored by the CPMT Society. The recipient of the award receives a bronze medal, certificate, and cash honorarium.

This IEEE CPMT Award was established in 2002. The technical field for this award includes all aspects of device and systems packaging including packaging of microelectronics, optoelectronics, RF and wireless and micro-electro-mechanical systems (MEMS).

This award may be presented to an individual or a team of not more than three. It is administered by the Technical Field Awards Council of the IEEE Awards Board.

The nomination deadline is **31 January 2006**. For nomination forms, visit the IEEE Awards Web Site:

www.ieee.org/awards

or please contact:

IEEE Awards Activities
445 Hoes Lane,
Piscataway, NJ, USA
08855-1331
Tel: +1-732-562-3844
Email: awards@ieee.org

****

CPMT Society Awards for Year 2005

Nomination Form

(Due date: January 31, 2006)

We invite your nomination of fellow practitioners for the many CPMT Society awards to be presented this year. For nomination forms and descriptions of all the available awards, please see the September CPMT NEWSLETTER, or download the nomination forms from the Awards website:

www.cpmt.org/awards

Nominations are due by **January 31, 2005**. For more information, please contact Awards Chair Rao Bonda, Freescale Semiconductor, at **r.bonda@ieee.org.**

Jobs With CPMT Society – Now Available

You've noted that some new volunteers have been elected to the CPMT Society Board of Governors. A new CPMT NEWSLETTER editor starts service with this issue, and several new Editors-in-Chief have been selected this year for our Transactions. So, how do these fortunate people manage to find such great positions as key members of our management and implementation team?

The answer is: they volunteer!

Now the secret is revealed: all you need to do is KNOW about an assignment (or invent your own) and then talk to the right person. You, too, can help our profession by investing a few hours every month. Who knows – perhaps you'll be one of the next chairs of a Technical Committee, or take a key position supporting our web and communications services, or coordinating our conferences. In this "business," the sky is the limit!

Of course, the salary is minimal (in fact, it's zero). But the satisfaction is high, and you'll be working with the "best of the best" in our field.

Here are some current opportunities, and who to contact. Watch this space in future NEWSLETTERS for additional openings. Or, specify the type of assignment that appeals to you in an email or attachment – then send it to our new Society President, Dr. William (Bill) Chen (**wt-chen@ieee.org**).

Visit the CPMT Society website:
www.cpmt.org

In this issue we'll cover certain volunteer positions within communications and publications. For additional details, and to volunteer, contact Paul Wesling, **p.wesling@ieee.org**

- **Assistant Webmaster – Expanded Services**: cover a portion of the website work, such as taking responsibility for the TC/Chapter sites, or the educational modules. Requires HTML, FTP, Server knowledge; has a budget of several thousand dollars, plus access to our web resources.
- **Assistant Webmaster – Streaming Modules**: streaming technology, server mirroring, on-line meetings software -- select potential software or services; interview target CPMT groups and understand their desired usage, install on our systems or select ISPs; prepare instructions for use, guide new users. Access to dedicated space on the EWH server in New Jersey; will work with Powerpoint, Sync-O-Matic, Real Producer and other authoring environments.
- **Assistant Webmaster – Collaboration**: bring collaboration, blogging, and on-line meetings software into use by CPMT TCs, committees, working groups – interview potential users, select software or services; install on our systems or select ISPs; prepare instructions for use, guide new users.
- **Assistant Webmaster – ListServ**: Work with TC and Chapter chairs to set up IEEE ListServ directed-email aliases for their units; train TC/Chapter webmasters and guide them in usage; expand current tutorials as needed.
- **Web Strategy/Interface Advisor**: Develop strategies for no-cost/low-cost changes to our website or interface that can be implemented by others; understand our HTML editing, look-and-feel, etc. Work directly for the VP of Publications.
- **IEEE Press Liaison**: Develop the structure for soliciting authors for manuscripts suitable for IEEE to publish or co-publish, on CPMT's behalf; work with Joe Brewer, our IEEE Press Liaison.

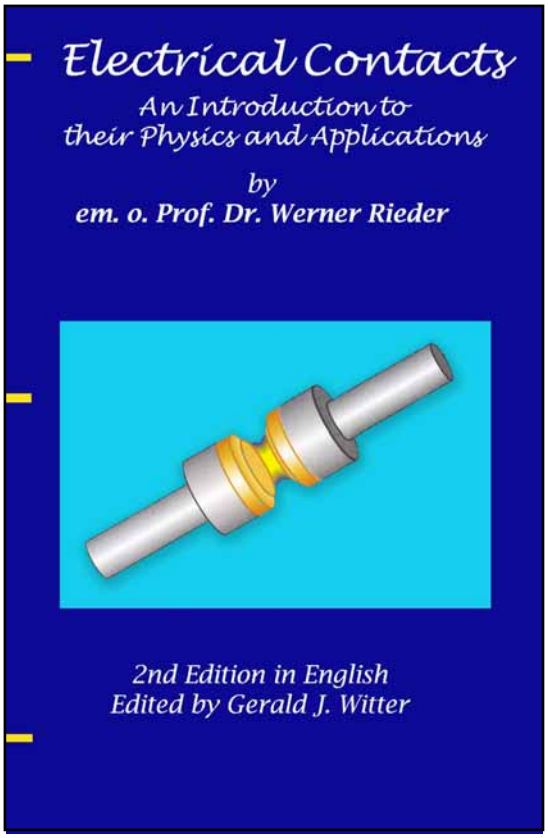
•Other assignments: I can offer all or part of any of the jobs outlined above, or we can custom-fit one to your interests and skills. Many of our members see our publications and web/email communications as being the primary reasons for belonging; we want to enhance our publications offerings and visibility, for a stronger Society.

I'll look forward to hearing from you!
Paul Wesling
p.wesling@ieee.org

A new book from the CPMT Society Press

Electrical Contacts

An Introduction to their Physics and Applications



Previously only available in German, this instructive book now has been printed in this Second Edition in English. The project was undertaken by the CPMT Society's Technical Committee on Electrical Contacts, Connectors, and Cable (TC-ECCC), with the direct involvement of Gerald Witter, TC Chair.

SUMMARY: An introduction to the physics and application of both static and switching contacts, including: mechanisms of arcing and ways to control the switching arc; reasons for contact resistance, contact welding and contact erosion and methods for minimizing these effects; contact material selection; switching in vacuum; and characteristics of electronic and electromechanical switching.

INTENDED AUDIENCE: Written for technicians and engineers involved with designing, fabrication and/or applying switching devices for their numerous applications.

Softbound, 90 pages
IEEE Product No.: BP2005
List Price: US$35.00
IEEE Member Price: US$25.00
Product Size: 14cm x 22cm (**5.5" x 8.5")**
ISBN: 0-7803-9639-1

To purchase your own copy, please visit the IEEE's online store:

shop.ieee.org

For selection criterion, use the IEEE Product Number (**BP2005**) or the ISBN (**0-7803-9639-1**).

Direct link:
shop.ieee.org/ieeestore/Product.aspx?product_no=BP2005

This book is suitable for teaching electrical contacts in university and corporate settings. Quantity discounts are available for instructors or departments:

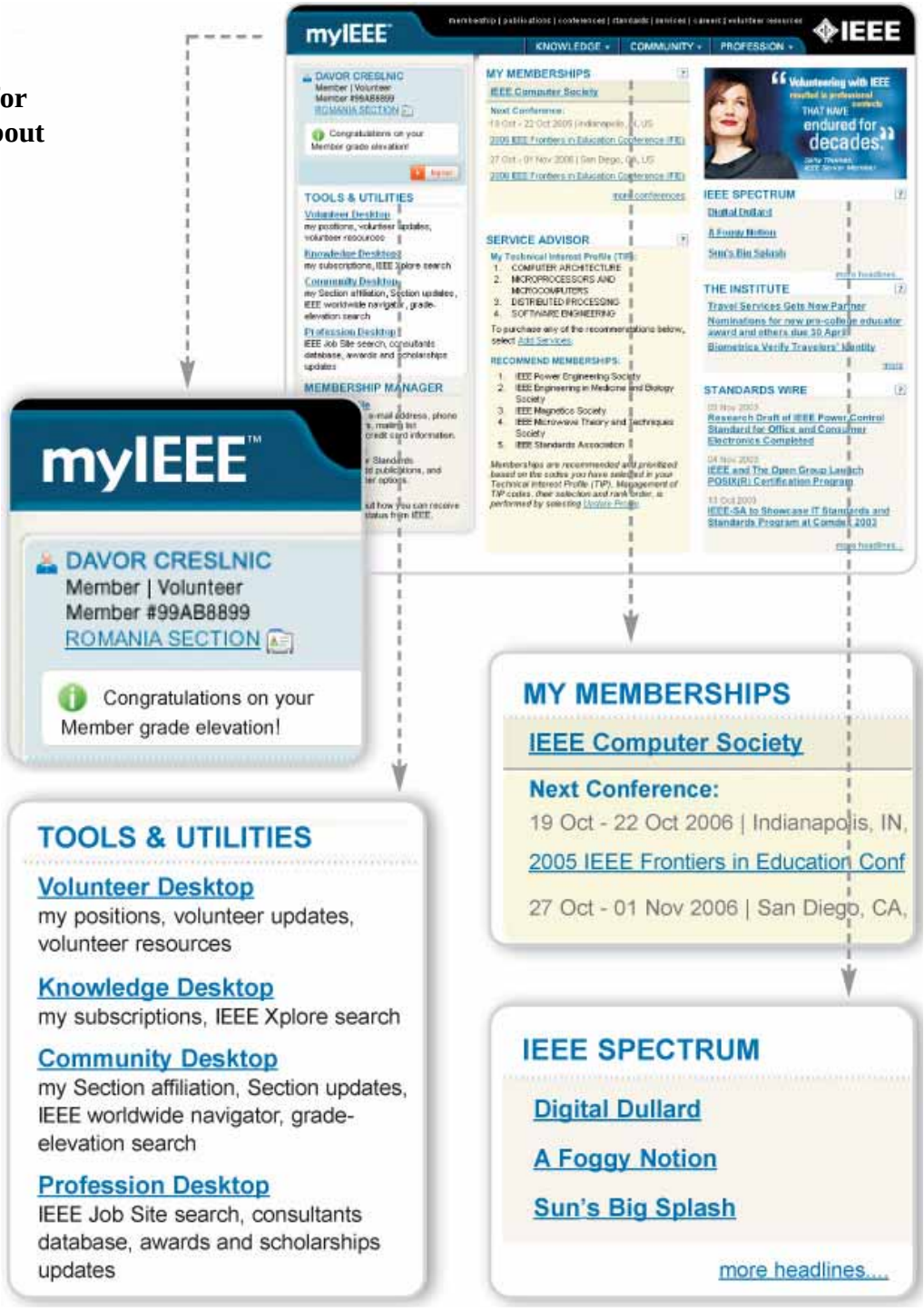
Quantity	Discount from List Price
10 or more	20%
50 or more	25%
100 or more	30%

Discount is automatically computed at the IEEE Online Store. Shipping/handling charges are extra.

myIEEE
Your Exclusive Gateway to IEEE Membership

Log into myIEEE today for personalized information about your IEEE membership:

- **Connect** with your local Section
- **Engage** your member benefits
- **Manage** your personal information and subscriptions
- **Link** directly to IEEE Societies
- **Learn** about upcoming conferences in your field
- **Search** the IEEE Job Site and Consultants Database
- **Research** the latest technology publications through the IEEE *Xplore*® digital library
- **Get the latest news** from *IEEE Spectrum*, Standards Wire, *The Institute* and your local IEEE Section



Discover the Benefits of your IEEE Membership!
Visit www.ieee.org/myieee

IEEE CPMT

International Symposium and Exhibition on

Advanced Packaging Materials

Processes, Properties and Interfaces

March 15-17, 2006
Georgia Tech Hotel and Conference Center
800 Spring Street NW
Atlanta, GA 30308
www.me.gatech.edu/APM06-IEEE/

Abstract Deadline: January 31, 2006

The symposium is devoted to advances made in electronic packaging materials. Topics of presentations will include, but are not limited to, lead-free, Cu low-k, thermal interface materials, 3D packaging, adhesion, underfills, encapsulants and coatings, bumping and solders, substrates including HDI, high thermal and dielectrics, reliability, nano-functional and passive materials.

To register, please go to: **www.me.gatech.edu/APM06-IEEE/**

Featuring Keynote Speakers

Dr. Masuo Mizuno
Cheif R&D Officer
Sumitomo Bakelite Co., LTD., Japan.

Professor Herb Reichl
Director of Fraunhofer IZM and Head of the Research Center for Microperipheric Technologies-System Integration, Technical University of Berlin, Germany.

Dr. Ho-Ming Tong
Corporate Vice President and General Manager of Corporate R&D, ASE Group, Taiwan.

Professor Rao Tummala
Pettit Chair Professor in Microsystems Packaging and Director NSF-ERC in SOP Technology, Georgia Institute of Technology, USA.

Professional Development Workshop

A half-day workshop on Packaging Materials and Reliability will be given by Professors C.P. Wong and Jianmin Qu. The workshop is free to registered attendees.

Conference Proceedings

A Conference Proceedings will be published. To be included in the proceedings, a full paper (4 pages) must be received by Jan. 31, 2006.

Local Attractions

World of Coca-Cola at Atlanta: http://www.woccatlanta.com/
CNN Studio Tour: http://www.cnn.com/StudioTour/
The Largest Aquarium in the World: http://www.georgiaaquarium.org/

May 30 – June 2, 2006
San Diego, CA USA

The **56th Electronic Components & Technology Conference** will be held at Sheraton San Diego Hotel & Marina, San Diego, California, USA on May 30 – June 2, 2006. This premier international conference is sponsored jointly by the IEEE Components, Packaging and Manufacturing Technology Society (CPMT) and the Electronic Components, Assemblies, and Materials Association (ECA), the electronic components sector of the Electronic Industries Alliance (EIA).

The audience includes representatives from leading universities and companies eager to stay abreast of rapidly changing and emerging technologies in the electronics field. This is the big annual CPMT Society all-technology meeting. The primary goal of the conference is to offer quality coverage of technological innovations in the areas of packaging design, materials, processes, quality and manufacturing of devices, components and systems. The Program Committee represents a wide variety of disciplines and expertise from the electronics industry. We are committed to assembling the highest quality program for the 56th ECTC, and we have many excellent papers to meet this commitment.

The ECTC Program Committee met on November 3-4, 2005 in Dallas, Texas, USA and reviewed about 550 abstracts submitted for the conference from 21 countries. At the 56th ECTC, over 300 papers will be presented by companies, universities and research institutions from around the world in 36 oral sessions and two poster sessions. These papers will cover a wide spectrum of topics, including electronic components, materials, assembly, packaging, system packaging, optoelectronics, quality & reliability, modeling & simulation, and emerging topics such as nanotechnology and biotechnology.

The ECTC also comprises of professional development courses covering 16 different topics offered by world-class experts in their fields. Participants can catch up with new technology developments and broaden their technical knowledge base. In addition, workshops on Tin-Whiskers and Education, a panel discussion on “3D Packaging and Novel Interconnects”, a plenary session entitled, “Look into the Crystal Ball: Arising New Applications, Technologies and Challenges”, and a seminar on “Advanced Substrate Technologies for SiP/SoP” will be held at the ECTC.

The technical program and professional development courses are supplemented by the technical exhibition corner. Leading companies in the electronic components, materials, and packaging field exhibit their latest technologies and products.

The day before the ECTC sessions begin, the CPMT Society is holding its 9th annual International Workshop on Microsystems Packaging Education, better known as the **Academic Conference**. Organized this year by Paul Wesling and Rao Tummala, it provides a venue for professors and instructors from around the world to gather a day early to review new initiatives in teaching undergraduate and grad courses in electronics packaging and manufacturing sciences. Also covered are innovative ways to bring technology to industry practitioners. We invite all university people to arrive “a day early” at ECTC to participate in this no-cost event.

Please visit www.ectc.net for additional conference information. Registration for the conference starts in January 2006. Early registration discount applies until May 12, 2006.

2006 IEEE Systems Packaging Japan Workshop

Hotel de YAMA, Hakone, Japan
January 30th through February 1st, 2006

General Chair: Fumiyuki Kobayashi
Vice Chair: Haruhiko Yamamoto
Treasurer: Masakazu Yamamoto
Technical Committee Chair: Erich Klink

Dear Colleagues,

The Systems Packaging Japan Committee would like to invite you to participate in the 2006 IEEE Systems Packaging Japan Workshop to be held at the Hotel de YAMA, in Hakone town, Japan on January 30th through February 1st, 2006. The location of Hotel de YAMA can be reached in about 2 hours from Tokyo by train and bus.

This workshop will be the eleventh one since the beginning in 1986, which covers the systems packaging technology from personal systems to high performance systems. Also the committee is planning to set up a technical tour on Wednesday.

The workshop will be held in English. All attendees are expected to be specialists in the field and to participate in discussion. For the further information about the workshop, please have a look at: **www.ewh.ieee.org/soc/cpmt/tc14/JWS8/papercall.html**.

We are confident that the technical meeting will be rewarding and useful. We are looking forward to your participation.

Guidelines:

- ✓ No proceedings will be published.
- ✓ Papers present new development or critical overviews.
- ✓ All attendees are expected to participate in discussions during the workshop.

Registration:

Attendees are requested to complete 'Registration Form' and forward it to **hiroshi.go.wt@hitachi.com**, or facsimile it to +81 463 87 7183, Hiroshi Go of Hardware Technology Development Dep. Hitachi Ltd., Enterprise Server Division.
Registration Fee
Pre-Registration fee until January 13th, 2006:42,000 Yen by card: Visa and MasterCard are acceptable.
After January 14th, 2006 or on-site registration:45,000 Yen in cash at the on-site desk.
Registration fee includes two lunches, two dinners, and a technical tour.
Registration fee does not include payment for the short sight seeing around Moto-Hakone that is planed as an optional tour on of January31st, 2nd day of the workshop. Registration fee does not include payment for hotel accommodations.
After arrival of your Registration Form, an invoice will be sent to you with follow.

Hotel Accommodations:

Attendees are requested to fill out 'Accommodation Form' and facsimile it to 81-42-767-1012, Kazuhiro Otka, Chief of the Reservation Center of Hotel de YAMA, Hakone. Hotel de YAMA provides special SPJW rates for all participants:

12,000 Yen for a single with breakfast
10,000 Yen each for a twin with breakfast

Room rates do not include a 5% tax and a 150 Yen fee for hot spring baths. Capacity of the Hotel de YAMA is around 80 to 90 persons for single use. After the Hotel de YAMA is fully occupied, the Hotel will refer attendees to nearby hotels at their normal rates.

For further information about the hotel, please visit to:
www.odakyu-hotel.co.jp/yama-hotel/english/

Recommendation for Hotel Reservation after the Workshop:

The workshop will be finished with a technical tour in the evening on February 1st. You will be brought with your entire luggage in buses during the technical tour. After stopping at Kokubunji station of JR Chuo line briefly, the buses will arrive at the final destination, Shinjuku station of JR Chuo line. You will be able to find a lot of convenient hotels in Tokyo area, especially around Shinjuku station, for the night on February 1st.

If you need further information and/or assistance, please feel free to contact Hiroshi Go of Program Chair, 2006 IEEE SPJW Committee.

2006 IEEE Systems Packaging Japan Workshop
Program Chair: Hiroshi Go
Hardware Technology Development Dep. Hitachi Ltd., Enterprise Server Division.
Phone: +81 463 88 1747 / Facsimile: +81 463 87 7183
E-mail: **hiroshi.go.wt@hitachi.com**

7th International Symposium on

QUALITY ELECTRONIC DESIGN

March 27-29, 2006
DoubleTree Hotel, San Jose, CA, USA

www.isqed.org

The International Symposium on Quality Electronic Design (ISQED) is a premier Manufacturing, Design & Design Automation conference, aimed at bridging the gap among electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. ISQED is the pioneer and leading conference dealing with design for manufacturability and quality issues front-to-back. The conference attendees are primarily designers of the VLSI circuits & systems (IP & SoC), process/device technologists, semiconductor manufacturing specialists including equipment vendors, and those involved in the R&D and application of EDA Tools & design flows. ISQED emphasizes a holistic approach toward design quality and intends to highlight and accelerate cooperation among the IC Design, EDA, Semiconductor Process Technology and Manufacturing communities. The conference spans three days, Monday through Wednesday, in three parallel tracks, hosting over 100 technical papers, six keynote speakers, two panel discussions, workshops /tutorials and other informal meetings. ISQED proceedings are published by IEEE Computer Society and hosted in the digital library. Proceedings CD ROMs are published by ACM.

CONFERENCE HIGHLIGHTS

TUTORIALS/WORKSHOPS

ISQED 2006 is pleased to offer a single full-day tutorial track, presented by six experts in their respective fields. This tutorial track consists of two (2) major topics shown below. The first topic examines the critical and timely issues of "variability" and its impact in design with 65nm and finer CMOS technologies. The second topic explores the exciting field of emerging Nanoelectronic technologies and their application toward future ULSI designs.

Variability and its Impact on Design	Emerging Technologies for VLSI Design
Dr. Keith Bowman, *Intel Corporation*	***Dr. Rajiv Joshi,*** *IBM T J Watson Research Center, NY*
Dr. Michael Orshansky, *University of Texas-Austin*	***Dr. Kaustav Banerjee,*** *University of California, Santa Barbara, CA*
Dr. Sachin S. Sapatnekar, *University of Minnesota*	***Dr. Andre DeHon,*** *California Institute of Technology, Pasadena, CA*

PLENARY SESSIONS

Two plenary sessions will be held on Tuesday and Wednesday mornings. Six industry & academia leaders will discuss the issues surrounding electronic design, design for yield and manufacturability and other critical topics from various points of view. Plenary keynote speakers are:

Dr. Risto Suoranta, Principal scientist & Research Fellow, Nokia
Dr. Tohru Furuyama, GM, Toshiba SoC Research and Development Center
Dr. Di Ma, Vice President of Field Technical Support, TSMC
Dr. Raul Camposano, Sr. Vice President, CTO, and GM, Synopsys
Dr. Changhyun Kim, Vice President and Fellow, Samsung Electronics
Dr. Philip Wong , Professor, Stanford University

PANEL DISCUSSIONS

ISQED is pleased to offer two high-power evening panel discussion sessions, where many leading experts, address the important issue of quality design. These panels would focus on the following topics:

1 Power management and optimization challenges for sub 90nm CMOS designs - What is the real cost of long battery life?

2 Soft IP Quality: Who is responsible to ensure quality throughout the design process?

LUNCHEON SPEECH

Simplicity and Executability: Cornerstones of Quality
Michael Keating, Synopsys

VENDOR EXHIBITION

The exhibition is being held for the 1st time in conjunction with ISQED, features vendors offering design tools and methodologies in the area of design for manufacturing and quality. Exhibit floor will be open on Tuesday March 28, in parallel with technical sessions.

TECHNICAL SESSIONS

ISQED Technical sessions start on Tuesday March 27, and continue until the afternoon of Wednesday, March 29. Beside the above plenary sessions, panel discussions, and workshops, the program consists of nineteen technical sessions featuring over 100 papers on various challenging topics related to design for manufacturability and quality. Detail program would be available on the web at **www.isqed.org**.

- **EDA Tools, Flows & IP Blocks; Interoperability (EDA)**
- **Design for Manufacturability & Quality (DFMQ)**
- **Design Verification and Design for Testability (DVFT)**
- **Package - IC Design Interactions & Co-Design (PDI)**
- **Robust Device, Interconnect, and Circuits (RDIC)**
- **Physical Design, Methodologies & Tools (PDM)**
- **Effects of Technology on IC Design, Performance, Reliability, and Yield (TRD)**
- **System Level Design, Methodologies and Tools (SDM)**

Please refer to ISQED web site at **www.isqed.org** for information regarding the tutorials, conference, and hotel registration. Direct all conference inquiries to **isqed@isqed.org**. Early registration is recommended to take advantage of the discounted registration fee.

ESTC 2006 - The European One

1st Electronics Systemintegration Technology Conference

The 1st **Electronics Systemintegration Technology Conference** will take place in only 9 months in Dresden (Germany). As a result of the ESTC program chairs meeting in October we present you the complete Executive and Program Committee List on our website: **141.30.122.65**. Excellent engineers and scientists from all over the world are ready to review your abstracts.

Please be aware the abstracts deadline is **February 15th, 2006**!

The 2nd Call for Papers is available now: **141.30.122.65/DOCS/Second-Call-Web.pdf**

KEYNOTE SPEAKERS: (preliminary list)

Systemintegration: **Herbert Reichl**, Director of the Fraunhofer Institute for Reliability and Microintegration, Fraunhofer IZM Berlin, Germany

Reliability: **Katsuaki Suganuma**, Head of the Department of Nanomaterials and Enviromentally Conscious Technology, The Institute of Scientific and Industrial Research, Osaka University, Japan

Automotive: **Steve Prosser**, Chief Engineer – Technology, Electronic Control Systems, TRW Automotive, Solihull, UK

Semiconductor: **Ralf Plieninger**, Senior Director Technology, Assembly and Test, Communications Group, Infineon Technologies AG, Regensburg, Germany

Avionics: **Robert M. Newman**, Technology Consultant Electronic Packaging, Goodrich Engine Control systems, Birmingham, UK

Special Paper Recognition

Best Paper Award: ESTC will select the best paper whose author(s) will receive an award and share a check for EUR 1.000,-.
Best Poster Award: ESTC will select the best poster whose author(s) will receive an award and share a check for EUR 1.000,-.
High quality level papers will be published after the conference based on a peer review process in different IEEE Transactions.

ICT-2006

The 25th International Conference on Thermoelectrics

University of Vienna
Vienna, Austria, Europe
August 6-10, 2006

First Announcement

This 25th International Conference on Thermoelectrics (ICT 2006) will examine a spectrum of plenary, invited and contributed presentations to provide an overview of the status of research and development in thermoelectric materials, devices and applications. Recent activity in this field will highlight a combination of new ideas, materials and device concepts in Europe, the USA and Asia. Recent energy issues will make this a timely conference and should be an excellent forum to assess the current status and future of the field of thermoelectrics.

Organization of ICT'06

Conference Chairman
Univ. Prof. Peter Rogl
University of Vienna
peter.franz.rogl@univie.ac.at

Secretariat of ICT-2006
Dr. Andrij Grytsiv
Habil Dr. techn. Martin Rotter Institute of Physical Chemistry
Faculty of Chemistry, University of Vienna
Tel. +43 1 4277 524 56 (57 or 69) Fax: +43 1 4277 9524

For more information or to submit an abstract:

www.univie.ac.at/ICT06

Conference e-mail address:
am.physchemie@univie.ac.at

Past Proceedings from ICT:
www.cpmt.org/proceedings/order.html

Papers also available online: ieeexplore.ieee.org
Search for "thermoelectric"

Abstract Due Date: June 1, 2006

PORTABLE-2007

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

CALL FOR PARTICIPATION

IEEE International Workshop on **Portable Information Devices** (PIDs)

Joint IEEE @ CTIA Wireless 2007 Interdisciplinary Intersociety Event

Orange County Convention Center, Orlando, Florida, USA

March 25-29, 2007

PORTABLE 2007 will bring together electrical, materials, mechanical, optical, reliability, industrial and manufacturing engineers, as well as business leaders involved or interested in various types of Portable Information Devices (PIDs), to address and discuss the state-of-the-art, challenges, attributes and pitfalls in PIDs and related areas. The expected attendance is 120-150 people. We are looking for technical paper contributions (initially, in the form of extended abstracts, and then in the form of full-length papers), coupled with tutorial, panel discussions, and demonstration (trade show type) proposals on various aspects of the PID engineering, including, but not limited to:

- Functional (electrical, optical) and Physical Design; Packaging, Physics, Mechanics, Materials, Manufacturing and Reliability of PIDs, Cellular Phones and other Mobil/Wearable Devices,
- Hardware/Software Interaction; and Power Generation, Supply and Conversion;
- Special Areas of Applications (e.g., Bio-Medical) and Use of Nano-technologies,
- Multi-Modal Man-Machine Communication; Anywhere/Anytime Access to Information; and Audio and Video Recognition and Processing;
- Predictive Modeling and Experimental Evaluations and Testing;
- Economics, Business, Government/Regulatory and Homeland Security Related Issues;
- Home Entertainment Systems and Networks, and other Social Areas, and Impact on society.

Eight half-day tutorials (short courses) will be held on Sunday, March 25. Keynote presentations, invited talks, technical sessions and business-related panel discussions will be held on Monday through Wednesday, March 26-28. An IEEE Pavilion featuring technology exhibits will be open on Tuesday, Wednesday and Thursday, March 27-29.
General Co-Chairs of the Workshop are: Ephraim Suhir (University of California, USA), Curtis Siller (IEEE ComSoc President, USA), and Tom Gurley (IEEE BTS President, USA)

EXTENDED ABSTRACT and/or a **TUTORIAL PROPOSAL** and/or a **PROPOSAL FOR A TECHNOLOGY OR BUSINESS APPLICATION PANEL DISCUSSION** should be submitted to Mrs. Nicole Tom, UCSC, at **nicole@soe.ucsc.edu**, with a copy to **suhire@aol.com** by **June 1, 2006**. The abstract should contain about 1500 words, and relevant figures and tables, and should include the following sections: background/incentive/motivation; objective(s); approach; major results; conclusions and recommendations; future work; references. The author(s)/instructors/panel-organizers will be notified on the paper/tutorial/panel-discussion acceptance by **July 1, 2006.** The final decision will be made based on the **FULL-LENGTH PAPER** (typically eight-pages long) and/or **TUTORIAL HANDOUTS** and/or **PANEL MATERIALS** that should be submitted by December 1, 2006 to Mrs. Nicole Tom, UCSC, at **nicole@soe.ucsc.edu**, with a copy to **suhire@aol.com**. The registration deadline for tutorials is February 1, 2007.

PROPOSALS FOR DEMONSTRATIONS (EXHIBITS) should be submitted by **June 1, 2006** to Mr. Brian Bigalke at **b.bigalke@ieee.org**, and should describe the main contributions of the demonstration and the merits of the proposed ideas. Authors should indicate if their demonstration presentation is a prototype or a poster. Proposals that demonstrate actual prototypes should include space, power and networking requirements. Submission details, including proposal templates, can be found on the conference web site at: **www.ieee-ccnc.org/author_info.** The potential exhibitors will be notified of the demonstration acceptance by July 1, 2006. Final camera-ready two-page exhibit/poster paper submission deadline is December 1, 2006, and registration deadline is January 1, 2007.

16th Biennial University Government Industry Microelectronics Symposium

UGIM

San Jose State University
San Jose, CA
June 25 – June 28, 2006

CALL FOR PAPERS

The purpose of this symposium is to bring together leading engineering educators and researchers from university, government, and industry around the world to promote microelectronics and other forms of micro/nano-fabrication. Representatives of university fabrication labs, ranging from new start-up labs to nationally recognized facilities, have found this symposium an excellent forum for exchanging information. Government agencies such as NSF, NIH, NIST, SEMATECH, SRC, DARPA and ONR regularly participate with papers and updates on funding opportunities. Industry interactions with universities, including technology transfer, collaborative research, and training efforts are frequently presented.

The scope of the symposium is:

- New Initiatives in University microelectronics programs, courses, laboratories, technology transfer, industry interaction
- Government-University microelectronics research programs
- Microelectronic research projects in the areas of materials, simulation, design, processes, testing, and reliability
- Process equipment development, manufacturing, statistical process control and design of experiments
- MEMS programs, courses, applications, processing, interactions, and research
- Standard silicon and compound semiconductors
- Bioengineering and Biotechnology
- Nanotechnology and nanofabrication
- Metrology and sensors
- University microelectronics research facilities

SUBMISSION INFORMATION

Abstracts (one text page + one figure page) must be submitted electronically on the symposium web site by 5:00pm (MST) February 17, 2006. Authors should indicate preference for oral or poster presentation, as well as their institution and contact information. Final manuscripts (4-6 pages maximum) must then be submitted electronically by April 3, 2006. These manuscripts, both papers (20 minute presentation) and posters, will be published in the symposium proceedings.

For more information, visit the 2006 UGIM Symposium web site at:

www.engr.sjsu.edu/ugim2006

General Chair

David W. Parent
San Jose State University
One Washington Square Hall
San Jose, CA 95192-0084
(408) 924-3963
dparent@email.sjsu.edu

Event Logistics Chair
John Lee

Treasurer
Gregory Young

Technical Program Chair
Koorosh Aflatooni, Foveon/SJSU

Technical Committee
Emily Allen, San Jose State
Greg Cibuzar, U. Minnesota
Karl Hirschman, RIT
Robert Pearson, RIT
Mary Tang, Stanford
John Shott, Stanford
Joel Kubby, UCSC
Jack Judy, UCLA
Stephen Parke, Boise State
Ali Shakouri, UCSC
Kevin Walsh, U. Louisville
Mark Crain, U. Louisville
James Zhou, WNLO-China
Paul Rissman, Stanford
Dipu Pramanik, Synopsys
Boris Polsky, Synopsys
Russel Martin, Foveon
Farnaz Parhami, Cypress S.
Bin Yu, NASA

New Year's Party

New Year's Party

Wishing You a Happy, Prosperous, and Healthy New Year 2006

Visit the CPMT Society website:
www.cpmt.org