

Components, Packaging, and Manufacturing Technology Society



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Newsletter



The Global Society for Microelectronics Systems Packaging



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President's Column.....



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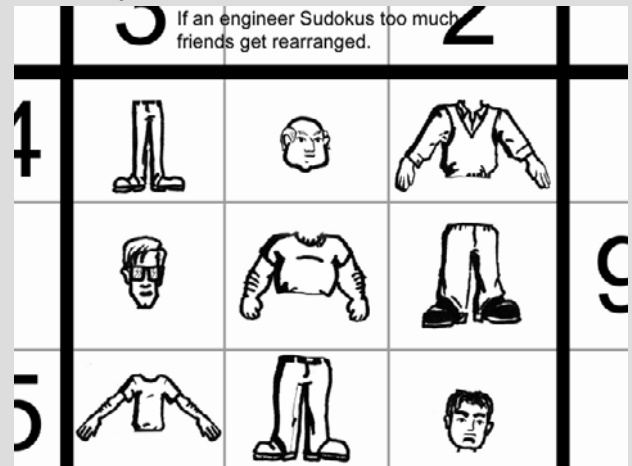
Greetings!!!

Membership in the IEEE and the CPMT Society

A little over a month ago I was approached by a firm commissioned by the IEEE Technical Activities Board (TAB) for an interview. There is a TAB project to understand the Society President's view on the benefits that the societies offer to their members and the role that societies play in their members' professional careers. The interviewer told me that the objective is to interview all society presidents for this purpose. Actually this very topic was addressed in depth at the TAB review of the CPMT Society February 14th this year. In this column I have frequently written about the CPMT value propositions and their contribution to the profession. I would speculate that this project would also give a different perspective in understanding the reasons behind the declining membership trend in IEEE and in the societies. During the IEEE TAB meetings we regularly discussed the IEEE membership fee cost, membership benefits and whether the level of the fees charged had become a barrier to joining IEEE.

The interview started with me describing what the acronym CPMT stands for: the Components Packaging and Manufacturing Society. I explained to her that our Society hosts the profession commonly known as Electronics Packaging, Assembly and Manufacturing. Our ranks are filled with engineers and scientists from different disciplines in engineering and science ranging from electrical engineering, mechanical engineering, chemical engineering, manufacturing engineering, materials science and engineering, chemistry, physics, metallurgy, ceramics, mathematics, and so on. We are an integral part of the technology chain associated with electronics product design and manufacturing. Situated in-between semiconductor devices and electronic products, we are far less known, but no less important, in the US 1.3 trillion dollars electronics technology industry supply chain. While the industry had its roots in North America, Europe and Japan, it is now widely distributed around the globe with a significant proportion of electronic manufacturing located in Asia. Electronic Packaging Technology is experiencing a period *(continued, page 3)*

Cartoon of the Month:



... By Dave Palmer

ECTC 2009 Conference

The 59th Electronic Components and
Technology Conference

May 26th – May 29th, 2009

Sheraton San Diego Hotel & Marina
San Diego, California, USA

IEEE CPMT Society Newsletter

September, 2008

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Refer to www.cpmt.org for CPMT Society Chapters and Student Branches list

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2008/09 Deadlines for Submitting Articles:

February 25th, 2009

May 25th, 2009

August 25th, 2009

November 25th, 2008

Only Articles sent to nsltr-input@cpmt.org
will be included in the newsletter

Members-only Web (www.cpmt.org/mem/)

UserName: [available to Members --

Password: join CPMT!]

President's Column (Continued from Page 1)

of great innovation and invention driven as much by the market as by the technology. At the same time the industry continues to be under pressure to produce more for less.

I explained to the interviewer our CPMT Society's globalization initiative to bring greater global participation in CPMT activities in conferences, publications, technical committees, recognition, education, chapters and membership. Virtually all of the CPMT activities come from volunteer efforts from engineers and scientists from around the world, many of whom are CPMT members. They form the core of CPMT constituency.

I told her that an important element in our strategy to reach out to our constituents worldwide is through technical conferences and workshops. Since conferences are the places where fellow professionals meet and talk face to face, they are where we feature and promote CPMT society value propositions. Our goals at each conference are to hold publication workshops and technical committee meetings, set up recognition events, professional development courses, chapter chair meetings and membership recruitment drives. In short, we pack full the conference agenda. At the ECTC conference this year and last year we have had some committee meetings and a publication workshop starting at 7:00 am. While ECTC is an international conference with half of its papers and participants from outside North America, it is important to have high-quality flagship conferences in other parts of the world. In Europe the CPMT UK and RI chapters sponsored the 2nd ESTC conference in Greenwich UK in September. The conference adopted the basic ideas described previously for ECTC and applied them in their own way. We will replicate similar initiatives at EPTC in Singapore, another major conference being held in Asia. CPMT organizes and sponsors many technical conferences around the world. The crucial point is that for each of the technical conferences, there is a group of committed volunteers – the regional CPMT chapter members -- passionate and committed to make their events successful. In addition to conferences there are CPMT workshops and seminars around the world. At all of these events one would find authors, reviewers and readers for our technical journals, and lecturers and students for educational programs. They are the stakeholders of the CPMT society value propositions. It is their passion, enthusiasm and dedication that we want to nurture, support and recognize. I told the interviewer that while I have spoken with much enthusiasm about technical conferences and workshops, I would be just as enthusiastic on the topics on CPMT publications, educational programs, recognitions, membership and chapters. While I think we are making headway in building the base for CPMT constituents, we are still behind in recruitment into IEEE membership.

The interviewer asked me for my thoughts, moving forward, on how to reverse the trend in declining membership in IEEE and CPMT. My response is that the reasons for many people to join and participate in the CPMT Society and IEEE are networking with the leaders in their specific fields, keeping up with advancing technology, and access to the broad knowledge base of packaging technology and science.

Equally important is the belief in CPMT as the trusted forum and source of knowledge for our dynamic profession. While I cannot quantify the importance of the IEEE fee structures and benefits in membership decisions in IEEE and the CPMT society, it is important for IEEE and for CPMT to address this issue in a positive way. The interview lasted about an hour and I expressed my good interest to read her study report.

What are your thoughts on this topic? I would very much welcome your thoughts and comments. Write to me at:

wt-chen@ieee.org

CPMT Society News:

Republishing Conference Papers

R. Wayne Johnson
Vice President of Publications

The republishing of selected and peer reviewed conference papers in our Transactions was an issue raised by the IEEE Technical Activities Board review of CPMT publications this past year. Under the heading "RESPONSIBILITIES OF MANUSCRIPT AUTHORS" the IEEE Publication Services and Products Board Operations Manual states:

"Except as indicated in IEEE Policy 6.4 (Multiple Publication of Original Technical Material in IEEE Periodicals), authors should only submit original work that has neither appeared elsewhere for publication, nor which is under review for another publication. If authors have used their own previously published work(s) as a basis for a new submission, they are required to cite the previous work(s) and very briefly indicate how the new submission offers substantive novel contributions beyond those of the previously published work(s)."

The referenced IEEE Policy 6.4 states:

"IEEE's technical publications shall include original material which appears only once in the archival literature. Unusual circumstances may allow for exceptions to this policy. The appropriate procedures to be followed shall be specified in the PSPB Operations Manual."

The publication of a conference paper or papers in an IEEE periodical is permitted at the discretion of the Editor provided that all the papers have undergone the standard peer review for the specific periodical in question."

In the past, we have republished selected conference papers in Special Sections of our Transactions. We have also published conference papers independently submitted by the author. These previously published manuscripts have gone through the standard peer review process all manuscripts submitted to CPMT Transactions go through. The level of revision required has ranged from 'Publish as Written' to "Major Revisions Required" and occasionally a selected/submitted conference manuscript has been ultimately rejected. The value in republishing conference papers was collecting related papers into a single Transactions volume and the peer review process.

While we can debate with IEEE over our interpretation of the IEEE Policies, we need to look at the bigger question: is there still value in republishing? IEEE Explorer and web access have changed the value of republishing manuscripts in transactions

Call for Nominations for the 2009 CPMT Society Awards
(Nominations Due by January 31, 2009 – Download form at www.cpmt.org/awards)

Kitty Pearsall

CPMT Strategic Director for Awards

after peer review. Using a key word search, all IEEE conference and transactions papers related to that key word are listed. It no longer matters if the papers are in a single transaction or published in multiple transactions and conference proceedings. There is still the value of peer review. If an Explorer search finds a paper with the same title and authors listed both in a conference proceedings and a transactions, the searcher knows the transactions manuscript was peer reviewed. However, they would have to examine both versions of the paper to determine the extent of the revisions required in the peer review process.

The CPMT Publications Committee has been debating how to address republishing conference papers going forward. The ideas have run the spectrum from continue the current practice to completely stop republishing manuscripts. After much discussion a policy has been developed. It states:

1. A manuscript that has been previously published must be substantially modified before submission to a CPMT Transactions.
2. The modifications should be substantial enough to result in a title change for the manuscript.
3. The original publication must be cited in the modified manuscript's list of references.
4. The author must indicate the manuscript is a modified version of a previously published manuscript when submitting the manuscript to a CPMT Transactions.
5. The author must detail the modifications made to the manuscript and why he/she believes the changes are significant.
6. The Associate Editors and Reviewers will consider the modifications discussed by the author as part of the peer review process.

One challenge noted by the Committee with this policy is to define 'substantial'. I agree and we will have to work through this with the assistance of the authors, the editors and the reviewers. Examples of modifications that could be considered include:

1. New data is included in the modified manuscript. We **do not** want to encourage people to hold back data from the conference paper, but quite often additional data is taken and presented that is not included in the original paper because of the deadline.
2. The authors may provide a more detailed discussion of the relevant literature and how their models/experiments will differ or add to the previous work. This would be in the Introduction. In the Discussion section, the authors would then compare and contrast their results with the literature. This type of in-depth analysis is not common for a conference paper, but is important for an archival Transactions paper.
3. A re-write of sections based on questions and comments received during the presentation.

As a Society, we must operate within the rules of IEEE. It is my belief that the policy adopted above will keep us within the rules and is a practical realization that IEEE Explorer and web based searches has fundamentally changed the value of republishing conference papers. I welcome any feedback or suggestions from the CPMT membership. Thank you for your support of OUR publications.

This is a Call for Action!!!! Once again it is that time of the year for you to put your thinking caps on and consider those individuals that should be recognized for their contribution to our society. I am sure that you know those individuals that have gone above and beyond in their contribution to their technical community and to the CPMT Society. Don't hesitate to put their names forth. The Awards committee is currently accepting nominations for the 2009 CPMT Awards. All nomination packages are **due by January 31, 2009**. Winners will be notified by 28 March 2008 and the awards will be presented at the 59th Electronic Components and Technology Conference, May 26th - May 29th, 2009, in San Diego, California, USA. I look forward to receiving many nominations in all the categories listed below:

CPMT Society offers the following 5 awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of the CPMT Society.

1) David Feldman Outstanding Contribution Award: This award recognizes outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.

Prize: \$2,500 and Certificate

Basis for Judging: Contributions to the organization or enterprises connected with the field, to CPMT Chapter, Section or Board of Governors activities, and to the fields encompassed by the CPMT Society.

Eligibility: Recipient must have been a member of IEEE and CPMT for the past five (5) years, including 2008.

2) Outstanding Sustained Technical Contributions Award: To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society.

Prize: \$2,500 and Certificate

Basis for Judging: Technical contributions must be sustained and continuing over a period of at least five (5) and preferably 10 years. One major contribution will not qualify. Contributions must be documented by open literature publications such as papers, patents, books and reports (available to the public).

Eligibility: Must have been a member of the IEEE and CPMT Society for the past three (3) years, including 2008.

3) Electronics Manufacturing Technology Award: To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society.

Prize: \$2,500 and Certificate

Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Work in the management of CPMT conferences or its BoG may be contributory but not sufficient to receive the award.

Eligibility: No need to be a member of IEEE and CPMT Society.

4) Exceptional Technical Achievement Award: To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the CPMT Society.

Prize: \$2,500 and a Certificate.

Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in CPMT's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.

Eligibility: Recipient(s) must have been a member of IEEE and CPMT for the past three (3) years, including 2008. There are no requirements for service to the IEEE or CPMT Society.

5) Outstanding Young Engineer Award: To recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.

Prize: \$1,500 and Certificate plus one year free membership in CPMT with all CPMT Transactions.

Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the CPMT Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.

Eligibility: Must have been a member of the IEEE and CPMT (member grade or above) for the past three (3) years, including 2008, and must be 35 years of age, or younger, on December 31st, 2008. Please provide Date of Birth (Month/Year) to ensure eligibility.

Guidelines for Nominators:

- Minimum **three** reference letters must be submitted in support of all nominations. Reference letters can be provided by IEEE/CPMT members and non-members.

- Past recipients of an award are not eligible to receive that same award. For list of past awardees, see the CPMT Society Home page (<http://www.cpmt.org/awards>).
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- It is the responsibility of the nominator to provide quality documentation to assist the Awards Committee in evaluating the candidate.
- Please send nominations to CPMT Society Awards Committee Chair by e-mail, fax or mail:

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IEEE Components, Packaging and Manufacturing Technology Award – 2009

Leonard Schaper, IEEE CPMT Awards Chair

The CPMT Award committee is changing as current committee members Rajendra Singh, Patrick Thompson, and Dennis R. Olsen retire and new members join. Many thanks to these gentlemen for their service. New members include Bob Pfahl (NEMI), Kanji Otsuka (Meisei University), and Luu Nguyen (National Semiconductor). Continuing members include Chair - Leonard Schaper, John Stafford, Yutaka Tsukada, and Erich Klink. The committee encourages new nominations for the CPMT Award each year. Information for potential nominators can be found on the IEEE website. The deadline for nominations is January 31, 2009.

With that said, I am delighted to report that the recipient of the 2009 IEEE CPMT Award has been approved by the IEEE Board of Directors. He is: **GEORGE G. HARMAN (LF'IEEE) - NIST Scientist Emeritus (Retired NIST Fellow), Consultant, Gaithersburg, MD, USA, "for achievements in wire bonding technologies."**

George Harman was hired at NBS/NIST in 1950 as an Electronic Scientist. In 1955, he filed for a patent on an electroluminescent microwave detector (# 2,928,937). He then studied the high frequency properties of various electroluminescent materials and discovered a new class of ferroelectric electroluminescent materials. His first 15 papers were generally in the area of applied physics and were published in the J. Appl. Physics, and similar journals. He studied contacts and surface states of several new unstudied (at that time) semiconductors (SiC, BC, etc.) and in the process obtained several US semiconductor device patents.

In 1968, a Navy strategic missile under development (Poseidon) had major reliability problems in its wire bonded interconnections. The urgency resulted in Harman being assigned to help solve that problem. This led to an extensive laboratory investigation designed to understand ultrasonic bonding and its evaluation. He developed a 25 μm diameter constricted, floating-cone capacitor microphone to plot the ultrasonic vibration modes of tools at

60 kHz, and applied those measurement methods to understanding and solving other problems in ultrasonic bonding machines and processes. Later, he used a laser interferometer to refine those earlier measurements. In 1971 he started the ASTM F-01.07 committee to standardize wire bond testing methods, which included pull test, nondestructive test, and ball bond shear test. Also, standards for bonding wire inspection methods, etc., were developed during that period. Harman, who currently chairs ASTM Committee F-01.07 (Wire Bonding, Flip Chip, and Tape Automated Bonding), updated and re-balloted the original wire bonding standards in 2005-06. Note that Harman's IEEE fellow citation (in 1982) was "for development of process control and screening procedures for microelectronic welding and bonding". He continues to contribute to the wire bonding area. Recently, an extension of his laboratory work and publications on wire bonding to soft substrates led to applying those principles to wire bonding on Cu-LoK chips. Other recent publications discussed projected metallurgical wire bond problems in NASA extreme temperature planetary exploration probes.

During the 1970's, Harman contributed to the military standards for testing wire bonds (at that time these were the only semiconductor/package standards publicly available and in general use), attended JEDEC meetings, and contributed data to be incorporated in their standards. He wrote the bond pull test method for MIL-S-19500 which was subsequently added to MIL-STD-750C, and supplied data and curves for the most used wire bond pull test in MIL-STD-883. He wrote the first version of the nondestructive bond pull test in MIL-STD-883 and has defended its use numerous times, and his paper on that subject in the IEEE IRPS stands alone for the statistical and metallurgical understanding of that test method. Currently, that test is required for most critical parts flown by NASA.

In his NIST Fellow position, George Harman has served as a national and international consultant in the field of wire bonding, advising and solving problems in chip-package interconnections for numerous organizations each year. He has taught most US and many foreign engineers both metallurgical and practical aspects of wire bonding in the 8-hour short-courses sponsored by UAZ, IMAPS, HKUST, and many others organizations for 20 years. He used the well developed and organized content of such lectures, in 1989, and published the first edition, and in 1997 the second edition of the only book(s) on that subject. It is frequently referred to as "the wire bond bible" and has been used by thousands of engineers (over 5000 copies of second edition have been sold by McGraw Hill). Two wire bond manufacturers have given a copy with each major machine purchased ("to educate and save us time and service calls to our customers"). These books have been a major world-wide contribution to the field by Harman.

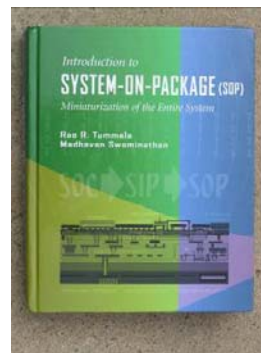
Most of George Harman's career has been engaged in understanding, standardizing, implementing improvements into the industry's tooling, and disseminating wire-bond technology. He is the individual most responsible for transforming a labor-intensive manual bonding technology whose results depended upon an operator's skill, with attendant poor reliability, to a well-understood, highly automated (>8 bonds

per second) method with an outstanding reliability record. As a result of Mr. Harman's work, wire bonding has become the industry standard. It accounts for more than 95 percent of the interconnections made between chips and the next level of assembly in electronic products manufactured worldwide. Approximately 7×10^{12} wire bonds are created each year. George Harman's work has had a profound impact on the industry, and likely benefited anyone utilizing an electronic product. George's award will be presented at the 2009 ECTC.

Book Reviews:

Introduction to System-On-Packaging (SOP), Miniaturization of the Entire System

By Rao R. Tummala and Madhavan Swaminathan
MacGraw-Hill, 2008, pp. 785



This is a complete introduction to the on-going research and development of SOP. The authors have co-authored several chapters and edited the rest written by leaders in the field. The basic theme is that there is plenty of room for further miniaturization even after the IC digital evolution call Moore's Law. There is no question that the many components and boards of a system are undergoing continual miniaturization using techniques other than

those from the CMOS juggernaut. However, the transistor count has gone up 9 orders of magnitude and the transistor miniaturization improved by 6 orders, whereas the SOP miniaturization appears limited to 2 orders (may just be the reviewers conservative view). None the less, all this technology will be needed to win in the marketplace over the next decade.

This book describes where SOP technology is being expanded and directions technology may take, but does not really address any economic destiny. Remember CMOS is slowing for economic not technical reasons. The SOP is not an irresistible BORG spaceship assimilating all technology in its integration effort, but one future direction proved plausible by the many great developments discussed in this book. Many university and industrial advances are presented in detail within this book.

Before discussing the details, it is important to note that each section of this book presented new exciting facts and new technology interconnections to any reader except those with many years developing integrated packaging. The large number of "AHAs" is a mark of a great tech book.

The integration of unusual single MEMs or photonic element into a highly integrated system is quite a challenge. The MEMs and Optoelectronics chapters in this book give several options to accomplishing this level of integration in addition to discussing economic packaging of single MEMs and photonic devices. Other chapters address many integration aspects of Biosensor, electrical module testing, thermal management, wiring, RF, mixed signal, and stacked ICs.

The RF chapter uses LTCC and LCP integrated packaging as the basis for SOP creation. Particularly informative discussions occur on how to miniaturize and add gain to module antennas. Discus-

sion of RF MEMs switches and their pros and cons as well as popular RFIDs are also well covered.

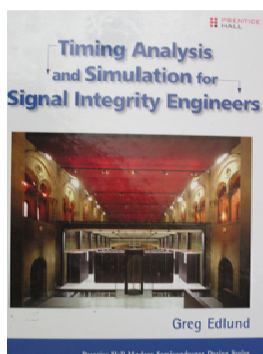
One practical aspect of system realization is not discussed in the book (it may be too soon). With the existing system of miniaturizing / integrating the digital and small signal analog signals in integrated circuits and interconnecting them with other components on boards there are well established methods to modify (tweak) the design on the board level when the simulations missed a little in timing or noise levels. The higher level of miniaturization of SOP does not appear to have these options so may require higher fidelity simulations.

In addition to clear descriptions and explanations, each chapter has extensive references so that the working developing engineer can quickly study the foundation of any aspect of this field before they invest in further efforts. This book is a pleasant necessity for any engineer or manager involved in miniaturization of systems and modules.

Timing Analysis and Simulation for Signal Integrity Engineers

By Greg Edlund

Prentice Hall Modern Semiconductor Design Series
2008, 250 pages



This book would make a fine supplementary text to a prototype design course, however more use will be made of this book by a working engineer associated with a design that has small design margins and needs a mid project re-design. The author makes many humorous comparisons between what the company needs right now versus the time good design methods require. This tone

revives the beaten down engineer into returning to the good path. He understands the pressures but guides the reader to know “when the design is ready to build.” The book is more like a mentor and less prescriptive.

The book stresses in detail the I/O circuits which are pivotal to the signal integrity issue as well as the need to do 3D EM simulation of the package, components, and interconnections. “In the years ahead, the most successful signal integrity engineer will be those who are able to expand their vision beyond voltage and currents and into the realm of electromagnetic fields.” For example, he details the study of a Land Grid Array interface and a SMA connector. The 3D modeling approach described is intended also for multichip modules, printed wiring board, sockets, connector cables, flex circuits, terminators, filers, and passive components. Most of the book is written as if the circuit designer does not have substantial input to the chosen packaging and interconnect technology so that one must compensate for the worst choices of others. However, after a designer masters this book it is hard to believe they will not be listened to by the packaging members of the design team.

Although the text examples allow the reader to perform similar methods to their specific module, you are reminded regularly that one must establish their own “bag of tricks” based on their particular business. In addition, knowing when each trick is best called upon is the wisdom between the lines of this book. For example, admitting that one can not model every net in the circuit in great detail, he presents a list of measures by which you can pick the nets most critical to your circuit. In another example, he differentiates when you can assign model making to the supplying vendor and when you had better do it yourself.

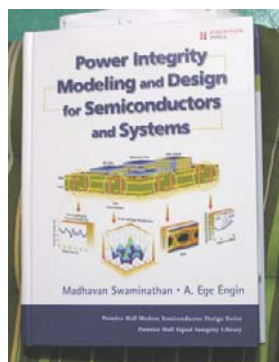
One exceptional feature of this book for those no longer used to final exams is the review appendices where one can quickly get up to speed on CMOS, SPICE, and Maxwell’s equations. He also bases this book on software tools that most universities and companies have available: High frequency SPICE, Agilent’s ADS, and CST Microwave Studio.

One favorite quote from the book ... “job of engineer is to play role of seer...without becoming a whiner”. In summary, if this is your business than this is your book.

Power Integrity Modeling and Design for Semiconductors and Systems

By Madhavan Swaminathan and A. Ege Engin

Prentice Hall Modern Semiconductor Design Series
2007



Most Electrical Engineering departments center their curriculum around circuit design. This CPMT Newsletter reviews design textbooks from the perspective of how the component, packaging, and manufacturing issues are integrated into the text design discussion. Based on our metric this textbook by Swaminathan and Engin receives good grades. The package design is completely integrated into the circuit design for the Power

delivery network (PDN). The integration of package design with system design has been a strength of the Georgia Institute of Technology, home of the authors.

The student should feel confident in modeling a complex IC system and performing design trade-offs with explicit packaging design options upon completion of a course centered on this book. However, the professor centering a course around this book will have to provide the practical specifics of components and materials in any class projects since the book does not go down to this level of detail. For example, the planes in the power distribution network are described mathematically but are not made specific by customizing to LTCC, or LCP, or BCB-Cu.

Strong points of this book include frequent pertinent examples/problems within the chapters; listing of many different power and ground strategies to maintain integrity while CMOS logic is switching on a massive scale; and detailed examples from Sun Microsystems, IBM, National Semiconductor, Cisco, DuPont, Panasonic, and Rambus. It may be useful to review one of these commercial examples in the last chapter every time an important modeling skill is mastered in the earlier chapters so the student recognizes the power gained by each method.

While scanning the book, questions came up regularly but each time the answer was found only a few pages away demonstrating the tight organization of the material. One slight detraction was the constant use of 3-letter abbreviations with seldom a repetition of the originating phrase. Fortunately their excellent index serves well as a glossary.

This book will function well as a structured textbook for a course on modeling digital board level systems as well as a reference for a practicing engineer asked to design and model something a bit beyond normal expertise. The extensive references at the end of each chapter allow further digging into any topic needing further understanding for a particular application.

Conference Reviews:

Conference Report from ESTC 2008

Submitted by Nihal Sinnadurai & Chris Bailey

Report & photos: www.cpmt.org/docs/0809estc.pdf

The 2nd Electronics System-Integration Technology Conference (ESTC-2008) was held at the magnificent buildings of the historic Old Royal Naval College on the banks of the River Thames in Greenwich, London from September 1-4, 2008. This premier international conference is held every two years in Europe and brings together scientists, engineers and managers in the field of micro and nano electronics, photonics, MEMS, and bio components, their integration and packaging.

ESTC-2008 was organised jointly by the University of Greenwich and the UK&RI Chapter of IEEE-CPMT and sponsored by CPMT-IEEE, the University of Greenwich, and supported by IMAPS-Europe. The conference compliments the corresponding CPMT global conferences ECTC and EPTC held in the USA and Singapore respectively and the European EMPC organised by IMAPS-Europe. The collaboration agreement in Europe results in us sharing alternate years for ESTC organised by IEEE-CPMT in Europe and EMPC organised by IMAPS-Europe. In this way we serve the interests of the delegates to provide ongoing major conferences without diluting the resource to deliver them.

The Executive and Technical Programme committees of the 2nd ESTC extend their sincere thanks to all the authors, presenters, short course instructors, session chairs, exhibitors, sponsors and delegates, who helped make ESTC-2008 a resounding success.



A Truly International Event

Contributions from 32 countries made ESTC-2008 a truly global conference. Authors from academia, industry and research institutes presented 252 papers at forty oral sessions and eight poster sessions to 384 delegates. Nine professional development courses attended by 67 participants on the preliminary day of the Conference added to the technical excellence of the event.

The strong technical range of the conference papers and courses covered the technical themes of Advanced Packaging, Emerging Technologies, Healthcare, Manufacturing & Test, New Materials and Processes, Modelling and Simulation, Optoelectronics, Reliability and special request topics such as Power Electronics and Assembly of Alternative Energy Sources. A themed technical exhibition with exhibits from 15 organisations, complimented the event and provided delegates with the opportunity to discuss commercial needs.

Special invited themes led and by international experts provided leading-edge insight in three technical themes on Prognostics and Health Management, Asia-Pacific Photo-Voltaics, and Standards, and a very special session on Greening the Blue Planet looked deeply into the impact and solutions that man and his technology has on the planet. 'When 'Technology Meets Market' provided constructive business decision insights from special panellists and knowledgeable delegates.

Greening the Blue Planet



Keynote lectures by Dr Nakita Vodjdani on the European Programme for Ambient Assisted Living, Dr Jean-Marc Yannou on SiP technologies and Dr Stuart Strickland who described Building Mobile Connectivity gave a great start to each conference day. The anchor Closing Session was chaired by Nihal Sinnadurai, the Executive Chair of ESTC-2008 and Chair of IEEE-CPMT-UK&RI. The session was kicked off with the Challenging Keynote by Professor Peter Cochrane on 'The Challenge of the Non-Linear' during which he asserted that systematic, i.e. linear, approaches were inadequate for the complex technology challenges of the future.

The Challenge of the Non-Linear

Prof. Peter Cochrane



Chris and Rolf



Nihal and Chris



Of course, this conference would not be complete without the awards of certificates and cheques from CPMT for the best papers and posters of the conference, and certificates to the organisers.

A Great Social Ambience

We aimed to establish a strong social ambience for ESTC and left a memorable impact, not least built on the wonderful World Heritage site. The Gala Dinner was in the fantastic historic Painted Hall with great atmosphere, great food and great entertainment – singers amongst the diners. Even the Exhibitors’ reception kept the delegates’ in the Exhibition Hall until the security guards had to encourage them to depart. The finale was the ‘River Cruise’ with the centrepiece the memorable journey on the panoramic ‘London Eye’.

The Gala Dinner



Conference Report ICEPT-HDP2008

Submitted by Prof. Keyun BI, President of China Electronic Packaging Society, Mr. Ronnie LI, Executive Director of China Electronic Packaging Society, China, and Dr. William Chen, CPMT Society President.

The Joint International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP2008) was successfully held from the 28th to 31st of July in Shanghai, China. This conference attracted 280 abstracts and col-

lected 250 papers. Almost 400 people from 13 countries or regions attended this conference. The Program included: opening speech by Prof Bi, CEPS, 10 keynotes, 150 oral presentations and 100 papers in poster session. Additionally, 3 workshops, including an ITRS Workshop and 4 training courses were held successfully.



The Leading People

The ICEPT-HDP2008 is organized / sponsored by China Electronic Packaging Society of China Institute of Electronics (CIE-CEPS), the Components, Packaging and Manufacturing Technology Society of the Institute of Electrical and Electronics Engineers (IEEE-CPMT), the International Microelectronics and Packaging Society (IMAPS), and Fudan University of China, with support from the Ministry of Industry and Information Technology, China, China Institute of Electronics, Shanghai Science and Technology Association, China, Shanghai Foreign Affairs Office, China, Shanghai Science Academy, China, Shanghai Integrated Circuit Industrial Association, China. Thanks to ASE Group, CPMT, ASTRI from Hong Kong, Shanghai Zhangjiang Group, Shanghai Xinyang Company, iNEMI, etc, who greatly helped to cover the conference expenses. Thanks to NXP who supported the Outstanding Paper Award and to CPMT and ASE who supported the Best Student Paper Award with Bonus. CPMT gave additional support to the Conference through it’s Distinguished Lecturer Program, which provided travel funding for several of the Keynote and Short Course Speakers.



The Chairman

Invited speakers included many of the leading people in the electronics packaging field for plenary keynotes, technical keynotes, or training courses, including Prof. Rao Tummala and Prof. C.P.Wong from Georgia Institute of Technology, USA; Prof. Michael Pecht from University of Maryland, USA; Prof. James Morris from Portland State University, USA; Dr. Cor Claeys from IMEC, Belgium; Prof. Tadatomo Suga from University of Tokyo, Japan; Mr. Steven Adamson from IMAPS, USA, Dr. Enboa Wu from ASTRI, Hong Kong, China, Prof. Ricky Lee from HUST, Hong Kong, China; Dr. Roy Yu from IBM, USA; Dr. Jim Huneke from Henkel, USA; Dr. Rainer Dudek and Dr. Rolf Aschenbrenner from Fraunhofer IZM, Germany; Prof. Xuejun Fan from Lamar University, USA; Prof. Johan Liu from Shanghai University, China; Dr. Lei Shan from IBM, USA; Dr. Daniel Lu from Henkel, China; Dr. N.C. Lee from Indium, USA; Dr. Ken Cheung from ASM, Hong Kong, China. Dr. William Chen, President of IEEE-CPMT; Mr. Steven Adamson, President of IMAPS and Dr. Jim McElroy, President from iMEMI came to congratulate the conference. Prof. Shichang Zhou, the academican from CAS and president of SICIA, came to congratulate and delivered a keynote speech.

The electronics packaging industry in China occupies over 50% of the output in the semiconductor industrial chain. Although at present, market demand in China focuses on middle or low-end packaging, more and more IC products from advanced packaging are needed day by day on a large scale. ICEPT-HDP provides a communicating platform for domestic and overseas experts, researchers, engineers on electronic packaging technology development and new ideas. This conference attracted people from well-known organizations, such as ASE, Intel, Henkel, Huawei, Freescale, Sumsung, Asymtek, JCET, ASTRI, and universities from China, such as Tsinghua University, Beijing University, Fudan University, Shanghai Jiaotong University, Huazhong University of Science and Technology, Hong Kong University of Science and Technology, Harbin Institute of Technology, South China University of Technology, Shanghai University, Nantong University, and research institutes such as Shanghai Institute of Microsystem and Information Technology of CAS, Hebei Semiconductor Research Institute, etc.



CPMT Student Paper Award

This successful conference represents a joining of the International Conference on Electronic Packaging Technology (ICEPT), previously organized by China Electronic Packaging Society, Chinese Institute of Electronics (CIE-CEPS), and the International Symposium on High Density Packaging (HDP), previously organized by Shanghai University. The strong, high-quality technical program, good organization and facilities put the Conference on the path to becoming one of the international brand conferences in the electronic packaging field, together with ECTC, ESTC and EPTC.



Opening Session



IEEE SW Test Workshop Semiconductor Wafer Test Workshop

**18th Annual IEEE Semiconductor
Wafer Test Workshop
(SW Test Workshop)
June 8 to 11, 2008
San Diego, CA**

The 18th Annual IEEE Semiconductor Wafer Test Workshop (SW Test) was held at the Paradise Point Resort in San Diego, CA, from June 8 to 11, 2008. The conference consisted of a technical program, supplier exhibits (which ARE NOT open during the technical sessions), and plenty of time for informal interaction, social events, and great networking with colleagues. Within the broad technical program there were many in-depth presentations and a few embedded tutorials that provided background information for the advanced presentations and for those new to the wafer probe business. The total number of conference attendance was just under 500 with over 30% international attendees representing over 20 countries.

On Sunday afternoon, workshop started with an excellent survey presentation on I/O Pad and Bump Damage by Ken Karklin of Touchdown Technologies that was co-authored by several other probe technologists from the SW Test Program Committee. Ken gave an excellent overview of the causes, effects, metrology/characterization methods and the potential impact on assembly of uncontrolled I/O pad damage.

After dinner, Jerry Broz, Ph.D., SW Test General Chair, gave a fast-paced "Probe Year In Review" presentation after which the

Keynote Presentation, entitled "Wafer Test Industries Impact on ATE", was made by Debbora Ahlgren, Vice President and Chief Marketing Officer of Verigy, Inc. She outlined how demanding consumers are clearly in the driver's seat when defining the requirements for global electronics growth. She said, "The prevailing technology laws pushing the semiconductor industry forward are defined by the well-known Moore's Law (semiconductor capacity doubles every 18-months), lesser known Amdahl's Law (increasing throughput through parallelism) and Hwang's Law (Samsung has doubled semiconductor capacity every 12-months) were considered as the end-products have an ever-growing dependence on semiconductors. To keep up, relatively cost-effective approaches to testers, test strategies, and parallel-based wafer sort methods are needed and must keep evolving. Ahlgren noted that optimizing DRAM test cost versus parallelism is crucial when considering the dramatically increasing advanced probe card costs. To emphasize this point, Deb outlined the DRAM test cell cost breakdown shift from 1997 (~32 die per touchdown) when the probe card was 27%, tester was 63%, and prober was 6% to 2010 (~512 die per touchdown) where the probe card is 52%, tester is 42%, and prober is 4%. She also noted that our future has a critical need for innovation and collaboration – across the boundaries of design, test and fabrication – to support the "faster", "more" and "cheaper" that are the requisites of the consumer economy.

The 2008 technical program began on Monday morning with the Welcome and Lifetime Achievement Award session by Dr. Broz. The 2007 SW Test Lifetime Achievement Award was presented to Don Snow, who is now retired from Applied Precision, Inc. Don's career spans across almost 50-years in the semiconductor industry. Starting at Fairchild Semiconductor in 1959, Don made key contributions to the wafer sort industry through overseas business development, tester innovations, linear axis wafer prober development, and probe card metrology.



Pictures from Technology EXPO

Pictures from Technical Program

The next two days were filled with technical presentations covering every facet of the wafer test process from *MEMs for Production Probing* to *Improving Test Cell Performance*. Overall, this year's workshop had 35 podium technical presentations with 60% from suppliers, 18% from semiconductor manufacturers, and 22% joint presentations from manufacturer collaborating with suppliers. The **Best Presentation** was awarded to the team of Jan Martens (NXP Semiconductors - Hamburg), Simon Allgaier (FeinMetall, GmbH), and Jerry Broz, Ph.D. (International Test Solutions); **Best Data Presented** went to the technical team of John D. Wolfe, James Tong, and Norman Armendariz, Ph.D. (Texas Instruments); **Best Presentation, Tutorial in Nature**, went to the collaborative work by Steven T. Clauter (Integrated Technology Corporation) and Taichi Ukai (Taitech); the **Most Inspira-**

tional Presentation was awarded to the technical team of Jung Pyo, Dave Oh, and Kyung-hwan Kim (TSE, Ltd); the *Best Poster* went to Terence Q. Collier (CVInc) and David B. Rennie & Chuck Lhota (Air Products & Chemicals); and the infamous "*Golden Wheelbarrow Full of Crap for the Poorest Disguised Sales Pitch*" ... Well, let's just say, "what happens at SW Test stays at SW Test".

The Technology EXPO was expanded for 2008 and the number of exhibitors grew from 40 to 52 and the number of Corporate Supporters expanded to ten companies. During the EXPO, all aspects of the wafer sort industry and associated infrastructure suppliers were represented with over fifteen probe card vendors, two of the major prober manufacturers, probe card analyzer and probe process metrology companies (one company introduced a new on-line probe mark volume metrology approach), companies specializing in probe card cleaning, micro-pogo pin suppliers, and a variety of other probe related service providers. Many of advanced probe card manufacturers showed their new one-touch 300 mm probe cards. There were also 10 poster board presentations with the authors present to describe their activities and answer questions during specified times when the exhibits were open.

All the presentations (including the tutorials, keynote, technical program, and posters) from 2008 as well as previous workshops (1993 to 2007), are available on the SW Test website, <http://www.swtest.org>. Next year, the 19th Annual SW Test Workshop and EXPO will be held June 7 to June 10, at the Paradise Point Resort in San Diego. Abstract submission for podium and poster presentations will be open starting January 1, 2009.

MAKE PLANS NOW!

Attend the 59th **Electronic Components and Technology Conference (ECTC 2009)**, being held May 25-29, 2009 in San Diego, CA USA. For more information, visit:

www.ectc.net

Watch for more information in the December CPMT Society Newsletter.

IEEE CPMT Society Newsletter

**Send inputs, suggestions, and
articles by email to
nsltr-input@cpmt.org**

..... Editor

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Table of Contents Alert

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The website link is:

ieeexplore.ieee.org/xpl/tocalerts_signup.jsp

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Here are the journals we suggest you select for monitoring:

- Advanced Packaging, IEEE Trans on
- Components and Packaging Technologies, IEEE Trans on
- Electronics Packaging Manufacturing, IEEE Trans on

Japan Institute of Electronics Packaging

A meeting was held at ECTC in Orlando, FL USA between members of the CPMT Board of Governors (including Bill Chen, Rao Bonda, Rolf Aschenbrenner and Charles Lee) and Dr. Yutaka Tsukada, President of JIEP. The objective is to develop further cooperation between the Society and JIEP, following CPMT's technical co-sponsorship of ICEP in Tokyo last summer.

JIEP was formed from former electronics packaging organizations and events, including ISHM/IMAPS-Japan, JIPC, the International Microelectronics Conference (IMC), and the CPMT Society's IEMT Symposium in Japan.

An article in the December issue of this Newsletter will give further details about JIEP and its activities, and some of the joint efforts that may be undertaken. Dr. Tsukada has been elected as a CPMT Society Distinguished Lecturer, so we may be hearing about some of his research in the coming years during talks at our Chapter meetings and conferences.



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CONFERENCES IN 2008:

NOVEMBER:

2nd Int'l **Symposium on Photonic Packaging**
November 13, 2008; Munich, Germany
www.mcc-pr.de/photonics/site
Contact: photonics@mcc-pr.de

DECEMBER:

9th **VLSI Packaging Workshop in Japan**
December 1 - 2, 2008; Kyoto, Japan
vlsi-pkg-ws.org
Contact: Michitaka Kimura, Renesas Technology Corp,
kimura.michitaka@renesas.com

10th **Electronics Packaging Technology Conference** (EPTC 2008) www.eptc-ieee.net
December 9-12, 2008; Singapore
Contact: Dr. Tong Yan Tee, tytee@amkor.com

Electrical Design of Advanced Packaging and Systems (EDAPS 2008) www.edaps2008.org
December 10-12, 2008 COEX Conference Center
Seoul, Korea
Contact: S.M Yang, yangsm@ee.kaist.ac.kr (Office:
+82-42-869-5458)

2nd Int'l Conference on **Thermal issues in Emerging Technologies, Theory and Applications** (ThETA2)
December 17-20, 2008 Cairo, Egypt
www.thetaconf.org
Contact: thetaconf@gmail.com

CONFERENCES IN 2009:

JANUARY:

2009 **European Systems Packaging Workshop** (ESPW) www.semi-therm.org
February 2-4, 2009 Kinsale, Ireland
Contact: Alan Mathewson, alan.mathewson@tyndall.ie

FEBRUARY:

8th Annual **FLEXIBLE Electronics & Displays Conference & Exhibition** www.flextech.org
February 2-5, 2009 Phoenix, AZ, USA
Contact: Alan Mathewson, events@usdc.org

MARCH:

2009 **Semiconductor Thermal Measurement and Management Symposium** (SEMI-THERM 25)
www.semi-therm.org
March 15-19, 2009 San Jose, CA USA
Contact: Tom Tarter, ttarter@ieee.org

APRIL:

Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP)
cmp.imag.fr/conferences/dtip/dtip2009
April 1-3, 2009 Rome, Italy
Contact: Chantal Benis-Morel, chantal.benis@imag.fr

International Conference on Electronics Packaging (ICEP) www.jiep.or.jp/icep
April 14-16 Kyoto, Japan

10th Int'l **Conference on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems** (EuroSimE 2009)
www.eurosime.org
April 26-29 2009 Technical University of Delft, The Netherlands
Contact: eurosime@astefo.com

MAY:

Workshop on Signal Propagation on Interconnects (SPI'09) spi.univ-brest.fr
May 12-15, 2009 Hotel Sofitel, Strasbourg, France
Abstracts due: February 7, 2009
Contact: Denis Deschacht, denis.deschacht@lirmm.fr

59th **Electronic Components and Technology Conference** (ECTC 2009) www.ectc.net
May 25-29, 2009 San Diego, CA USA
Contact: Jean Trehwella, jeanmh@us.ibm.com

JUNE:

European Microelectronics and Packaging Conference & Exhibition (EMPC 2009)
www.empc2009.org
June 14-17, 2009 Rimini, Italy
Abstracts due: December 31, 2008
Contact: Pragma Congressi, segreteria@empc2009.org

IEEE International Workshop on **Advances in Sensors and Interfaces** (IWASI'09) iwasi.poliba.it
June 25-26, 2009 Trani, Italy
Papers due: February 28, 2009
Contact: Prof. Daniela De Venuto, d.devenuto@poliba.it

SEPTEMBER:

2009 **IEEE Holm Conference on Electrical Contacts (Holm 2009)**
www.ewh.ieee.org/soc/cpmt/tc1/h2009/h2009top.html
Sept. 14-16, 2009 Vancouver, BC, Canada
Papers due: January 9, 2009
Contact: April Coles, a.coles@ieee.org

See the CPMT Society website for updates:

www.cpmt.org/conf

EPTC 2008

10th Electronics Packaging Technology Conference
9th - 12th December 2008 @ Grand Copthorne Waterfront Hotel, Singapore

EPTC 2008 is a 4-day event in conjunction with our 10th-year anniversary celebration. The EPTC Technical Committee with over 100 technical experts has reviewed a total of 351 abstracts from 30 countries submitted for the conference. 260 quality papers from engineers and researchers have been selected for presentation in 48 technical sessions. These papers cover a wide spectrum of topics, including electronic components, materials, assembly, packaging, system packaging, optoelectronics, quality & reliability, modeling & simulation, and emerging technology topics.

We are privileged to have 3 distinguished **keynote speakers**, Dr. GQ Zhang of NXP Semiconductor, Prof. Michael Pecht of the University of Maryland, and Prof. CP Wong of Georgia Tech, to deliver keynote talks. We are also glad to invite 6 pioneers from 6 regions to share their reviews in the plenary session: "**3D System Integration - Where Is It Heading? US, Europe or Asia?**". This year, 18 invited paper talks will be given during the technical sessions by experts from various fields of packaging technologies, so that attendees will have much deeper insight into the latest research challenges in packaging.

The EPTC also features **professional short courses** and forums, covering 8 different topics offered by world-class experts in their fields. A tabletop **exhibition** featuring suppliers of materials, equipment, components, software and service providers for the microelectronics and electronic assembly industries will be held during EPTC. Last but not least, we have specially arranged a memorable **10th anniversary EPTC banquet** at the Singapore Turf Club, an excellent social event for professional networking.

Register online at www.eptc-ieee.net

You may download the **Advance Program**:

eptc.elite.sg/2008/download/EPTC%202008%20Advance%20Program.pdf

We are looking forward to seeing you at EPTC in Singapore!

Best regards

Dr. Tong Yan TEE

General Chair, EPTC 2008

tytee@amkor.com



Dr. Teck Kheng LEE

Technical Chair, EPTC 2008

techchair@eptc-ieee.net



IEEE COMPONENTS, PACKAGING AND
MANUFACTURING TECHNOLOGY SOCIETY

SYMPOSIUM on

Design, Test, Integration & Packaging of MEMS/MOEMS

This series of Symposia is a unique single-meeting event expressly planned to bring together participants interested in manufacturing microstructures and participants interested in design tools to facilitate the conception of these microstructures. Again, a special emphasis will be put on the very crucial needs of MEMS/MOEMS in terms of packaging solutions. The goal of the Symposium is to provide a forum for in-depth investigations and interdisciplinary discussions involving design, modeling, testing, micromachining, microfabrication, integration and packaging of structures, devices and systems.

DTIP

of MEMS & MOEMS

Abstracts are requested, by **November 10, 2008**

For further information, visit our website:

cmp.imag.fr/conferences/dtip/dtip2009



Alternating with the IEEE ESTC, EMPC is a Europe's premier conference planned every two years in a different European country, bringing together specialists from industry and academia. EMPC addresses "everything in electronics between the chip and the system".

The Technical Program Committee of EMPC 2009 **invites you to send abstracts** of original work describing recent developments in microelectronics technologies:

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- Embedded Passives on Wafers and Substrates
- High Frequency and High Power Packaging;
- LTCC Ceramics Technologies
- PCB and BGA Substrates Design and Technologies, Laminates, Micro-Vias and Build-Up Technologies, Flex

INTERCONNECTION TECHNOLOGIES:

- Thick and Thin Film Technologies
- Wire Bonding, Bumping, Flip Chip Bonding
- Cu/Low-k Wafers, Through Silicon Vias
- Lead-Free Soldering and Adhesive Joining

POWER ELECTRONICS:

- Application in Consumer, Telecom, Automotive, Wearable, Space and Defense

MORE THAN MOORE:

- MEMS Packaging: MEMS Based Sensors and Actuators Packaging, RF-MEMS, Optical MEMS, Bio-MEMS
- Optoelectronics: Power LED Packaging and Light Guiding, Packaging of Optoelectronic Modules suitable for Gb/s Fiber Optic Communication
- Solar Energy (Photovoltaics): Packaging Design to improve Efficiency of Photovoltaic modules Reliability and Qualification Approaches
- Nano Technologies: Smart Materials, Interconnections, Nano-Scale Packaging
- Medical Electronics: Applications, Design, Development, Manufacturing that comply with complex and demanding regulations and market requirements.

MANUFACTURING TECHNOLOGIES AND MATERIALS:

- Process Development, New Equipment, Yield Improvement, Cost and Cycle Time Reduction, Green Mfgng
- Adhesives, Encapsulants, Underfills, Moulding Compounds, Lead-Free Solder Alloys, Halogen Free Materials, Dielectrics and Ceramics.

Abstracts due: **December 31, 2008**

More information:

www.empc2009.org

2009 European Systems Packaging Workshop

February 2-4, 2009 Kinsale, Ireland

Systems Packaging deals with optimizing all aspects of technology at the product level. It encompasses architecture, electrical design, thermal management, all levels of packaging and cost from a holistic perspective. As a result, Workshop attendees will get an overview and insight into all aspects of the electronics industry. The CPMT Society's **TC on Systems Packaging** began in 1968 and its members possess a great amount of industry experience that newcomers can tap into. Workshops are informal, with many opportunities to network with and learn from your peers. The 2009 workshop topics are:

Smart Systems
Communications Systems
High Performance Computing

Biomedical Systems
Photonics

If you want to see leading edge work in electronics, this is the meeting to attend. More information can be found at the following website:

www.ewh.ieee.org/soc/cpmt/tc14/

*This workshop will be the 11th one held in Europe by the TC on Systems Packaging.
We hope to see you in Kinsale (County Cork), Ireland next February.*

The 2009 IEEE International Workshop on Portable Information Devices

September 20 – 22, 2009, Anchorage, Alaska, USA



CALL FOR ABSTRACTS/PARTICIPATION

The **Portable 2009 Conference** will be co-located with the 70th IEEE Vehicular Technology Conference at the Anchorage Hilton, AK, USA, from September 20 – 22, 2009. Portable 2009 will bring together electrical, materials, mechanical, optical, reliability, industrial and manufacturing engineers, as well as business leaders involved or interested in various types of Portable Information Devices (PIDs), to address and discuss the state-of-the-art, challenges, attributes and pitfalls in PIDs and related areas.

We are looking for **technical paper contributions** (initially, in the form of **extended abstracts**, and then in the form of full-length papers), coupled with **tutorial, panel discussions, and demonstration** (trade show type) proposals on various aspects of PID engineering, including, but not limited to:

- Functional (electrical, optical) and Physical Design, Packaging, Physics, Mechanics, Materials, Manufacturing and Reliability of PIDs, Cellular Phones and other Mobil/Wearable Devices;
- Hardware/Software Interaction and Power Generation, Supply and Conversion;
- Special Areas of Applications (e.g., Bio-Medical) and Use of Nano-technologies;
- Multi-Modal Man-Machine Communication; Anywhere/Anytime Access to Information and Audio and Video Recognition and Processing;
- Predictive Modeling and Experimental Evaluations and Testing;
- Economics, Business, Government/Regulatory and Homeland Security Related Issues;
- Home Entertainment Systems and Networks, and other Social Areas, and Impact on society.

Submit abstracts to William Yeager, Sun Microsystems: yeager_william@earthlink.net

PORTABLE 2009 Website: www.ieeevtc.org/portable2009

FIRST CALL FOR PAPERS: SPI'09

The 13th IEEE Workshop on

SIGNAL PROPAGATION ON INTERCONNECTS

Hotel Sofitel, Strasbourg, France

May 12-15, 2009

During the last twelve years, the **IEEE Workshop on Signal Propagation on Interconnects** has developed into a forum of exchange on the latest research and developments in the field of interconnect modeling, simulation and measurement at the chip, board, and package level. The event is also meant to bring together developers and researchers from industry and academia in order to encourage cooperation. In view of the last years' successes, the committee is looking forward to the 13th SPI where world class developers and researchers will share and discuss leading-edge results. The workshop will be held in English.

Submission of abstracts:

Those who wish to contribute to the workshop should send (by e-mail only) a formatted two-page to four-page paper to the Program Chair by **February 7, 2009** (please see the submission instructions on our website).

If the paper is accepted, it will be reproduced, as is, in the workshop proceedings.

Notification about acceptance will be given by March 16, 2009.

Detailed information about the workshop and its location are available on the website:

spi.univ-brest.fr

The committee is looking forward to your participation.

Call for Papers:

**Thermal, Mechanical and Multiphysics
Simulation and Experiments
in Micro-Electronics and Micro-Systems**

EuroSimE

Delft, The Netherlands April 26-29, 2009

The conference addresses the results of both fundamental research and industrial application for thermal, mechanical and multiphysics solutions of (micro)-electronics and microsystems, focusing on advanced simulation and experiments. You are invited to submit an abstract in any of the following areas:

- Mechanical simulation (static & dynamic)
- Thermal simulation (steady state & transient)
- Failure analysis and failure mode extraction
- Material characterisation, experiments and modelling
- Validation of simulations by experiments
- Failure criteria and damage-modelling
- Behavioural modelling
- Compact modeling and model order reduction

Back to its roots! EuroSimE 2009 will be celebrating its tenth anniversary, as it was born in March 2000 in the Netherlands. Join us for this great and unforgettable event!

- Short courses for professional training.
- Three days of technical sessions for oral and poster presentation.
- A parallel exhibition from hardware, simulation and optimization software companies.

Applications:

- Components and packaging
- Opto-electronic packages
- High temperature packaging
- Piezoelectric components
- Packaging for harsh environments
- Wafer processing, chip design and reliability
- Nanoelectronics
- PWB design and application
- Electronics system assembly
- Photovoltaics

Upload your abstract on our website:

www.eurosime.org

Abstracts must be received by **November 15, 2008**

2009 European Systems Packaging Workshop

February 2 – 4, 2009

Kinsale (County Cork), Ireland

The IEEE Technical Committee on Systems Packaging (TC-SP) wishes to invite you to its 11th European Workshop. Our goal is to view all types of packaged electronics from the macro perspective with emphasis on the overall technical system attributes, choices and challenges. This includes the product specifications, system architecture, technologies, electrical performance, power design and thermal management. We approach the product characteristics by focusing on all levels of packaging as the "glue" that holds the entire hardware system together. Consequently, designing the total package requires an intimate knowledge of all the technologies that go into the final product. This perspective leads to a broad knowledge of what's going on in all aspects of the worldwide electronics industry. So if you can't go to all the sub-specialty conferences and you want an in-depth big picture view of the latest developments in the field of electronics, you should seriously consider attending this workshop.

The workshop will be conducted in English. It will be held at the Trident Hotel. Program, hotel and registration information can be found at this website as it becomes available. The committee is looking forward to your participation.

Session Topics are:

- + Smart Systems
- + Biomedical Systems
- + Communications Systems
- + Photonics
- + High Performance Computing

For more information, visit the website:

www.ewh.ieee.org/soc/cpmt/tc14/Cork09/ESPW09.html



December 10-12, 2008 Seoul, Korea

The EDAPS Symposium is to enhance the technical awareness and depth in the Asia region specifically in area of package and system electrical design concepts, issues, and challenges ahead for next generation electronic products.

- * Specially selected technical papers
- * Single session in a single room.
- * Oral presentation (about 30 papers)
- ... * poster session (about 30 papers)
- * Plenary talks from leading industry and academia
- * Tutorials
- * Exhibition
- * Student Paper Award

Topics

- * High-speed Digital Signal Integrity Modeling, Design
- * Power Distribution Network Modeling, Measurement
- * SiP/SoP Design
- * High-performance Packaging for SoC
- * RF/Microwave Packaging for Wireless Communication
- * Interconnect Modeling, Simulation, and Measurement
- * Embedded Passives Modeling and Measurement
- * High-speed Channels Modeling and Measurement
- * EMI/EMC Modeling and Measurement
- * EDA tools for chip, package, and board co-design

Download the Advance Program:

www.edaps2008.org

Contact: S.M Yang, yangsm@ee.kaist.ac.kr
(Office: 82-42-869-5458)



Printed Electronics USA08

December 2-5, 2008
San Jose Convention Center
San Jose, CA USA

**The world's largest and
most comprehensive event
on the new electronics**

The **fifth annual Printed Electronics USA** conference and exhibition covers all the applications, technologies and opportunities. Anticipating over 800 delegates and 80 exhibitors, this is the World's largest event on the topic.

Printed Electronics USA gives the big picture, not least by inviting leading speakers from across the world. Commercialization and the full range of technologies are the emphasis, with inorganic solutions receiving equal emphasis with organic and hybrid solutions – thus reflecting the situation in the real world.

A full range of devices, materials and production technologies will be explained by best-in-class speakers, with many first announcements. Samples and demonstrations will be available and many subjects will be aired for the first time.

There will be sessions on the latest breakthroughs in electronics on paper and on many new types beyond silicon, such as smart skin patches and photovoltaics.

Over 100 world class speakers - some presenting exclusively for the first time here - cover components, materials and applications in the following sessions:

- Analyst forecasts and trends
- Healthcare and bionic man
- Radical new printed electronic products
- Improving traditional electronics
- New possibilities with printed electronics
- Flexible lighting and its applications
- Thin film photovoltaics and batteries
- Sensors
- Smart substrates/stretchable electronics
- Materials
- Manufacture

The Exhibition (Dec 3-4)

Covering the world of organic and printed inorganic solutions: Companies exhibiting cover materials, manufacture, device production, consulting, academic research and more. 80 anticipated exhibitors will make this the largest exhibition on Printed Electronics in the world.

Save through November 14th. For more information, visit

www.IDTechEx.com/peUSA

IEEE Components, Packaging and Manufacturing Technology Society

Marsha Tickman, Executive Director
PO Box 1331 / 445 Hoes Lane
Piscataway, NJ 08855 USA

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