Components, Packaging, and Manufacturing Technology Society Newsletter

IEEE

CPMT

The Global Society for Microelectronics Systems Packaging

Vol. 32 No. 2, June 2009 (ISSN 1077-2999)

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www.ewh.ieee.org/soc/cpmt/newsletter

President's Column…..

Dr. William T. Chen
IEEE Fellow
President, IEEE CPMT Society
Santa Clara, CA, USA
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The summer President's message usually is about ECTC, and this year is not an exception. Many of you have received the email "2009 ECTC Highlights" from Rao Bonda. It brought back vividly memories of the exciting 59th ECTC conference at San Diego. Prior to the conference we had concerns with the conference programs and participation. The worldwide recession had reduced the travel budget in many companies. For participants from Asia there were travel restrictions due to concern with H1N1 influenza. In Rao Bonda's ECTC highlight message he clearly showed that despite these impacts, the 59th ECTC was outstandingly successful. We missed seeing many of you, but we are happy to meet the many who managed to come against all odds.

CPMT technical conferences, such as ECTC, are the Town Hall and Main Street of our profession. We come from around the globe, as a community of professionals, to present our technical findings and to learn the latest in our technologies. Along the hallways, between sessions, during breakfasts and coffee breaks, we meet old friends and make new ones, touching base on the happenings in industry, research facilities, and universities. The conferences are global network centrals for our profession. In these trying times keeping up with the network is of crucial importance for all of us.

With a good balance between contributions from industry, research institutions, and academia, ECTC technical programs provided excellent insight on what would soon become high volume production in the market place as well as to what might be happening three to five years out. From 3D Packaging - TSV, nano materials, optoelectronics, flip chip and wirebond, reliability, materials processing and materials science and emerging technologies, there was a surfeit of interesting and important work to listen and learn. It took some good study of the technical program not to miss what I wanted to attend. Usually the day started with technical committee meetings at 7:00 am and ended with Panel sessions that finished at 9:00 pm.

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….. Editor

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Refer to www.cpmt.org for CPMT Society Chapters and Student Branches list

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Circulate your printed or PDF copy of this NEWSLETTER to co-workers. All may subscribe to the e-Nsltr; visit www.cpmt.org/subscribe

President's Column (cont.):

Traditionally the CPMT Luncheon recognizes of achievements of many of our peers in the profession. We presented IEEE and CPMT Society awards recognized important and significant achievements and great contributions within our own community. We recognized best papers from CPMT transactions. This year, the Society created a new award, the CPMT Student Travel Award, which enabled sixteen students to participate in the ECTC Conference. It is an important message to the younger generation in our midst: the CPMT Society is their society and the ECTC conference is their conference.

This year we have started a tradition to honor and recognize the many dedicated volunteers in the ECTC program committees. Volunteers are the backbone of the ECTC, our Society and our profession. In this very difficult year, with the economy in trouble and the success of the ECTC in jeopardy, each and every one of the teams have worked long and hard to make this 59th conference the best ever.

Besides the professional development courses, panel sessions and technical programs, what does one do during ECTC? One of my favorite activities was the Best Practices Publication Workshop. It was held two times during the ECTC week. The workshop was led by Wayne Johnson, CPMT VP for Publications. The workshop is designed for those in our midst who do great research, make great presentations, and now want to write great technical papers and get them published in CPMT Transactions. In the workshop Wayne described the key attributes in a great journal paper and the best practices to achieve them. Developments in the electronic packaging industry are moving at a rapid and accelerating pace. It is crucially important to put one's significant research contribution into the best technical publications in our profession. Wayne will be holding the workshop at other CPMT Technical Conferences. Please be on the lookout for it.

ECTC is one of the many technical conferences in our global CPMT community. In my list of things to do is to complete the paper review assignment for EPTC conference in Singapore in December. In my own calendar for the month of August , there will be the ICEPT – HDP conference in Beijing, China, and the flexible electronics workshop in Binghamton NY. Please review the newsletter and the CPMT website for the complete listing.

The employment picture continues to be severe and daunting. In the spring message I mentioned that I expected deep downward trends for membership renewal and for new membership. Please pass the word out that for those of our members who have become unemployed they are eligible for 50% off IEEE and CPMT dues and subscriptions. They will be able to exercise this discount when it comes time to renew for 2010. This discount also applies to new membership as well. Additionally, IEEE has a number of career resources, including a job site listing to connect those who have jobs and who need jobs.
http://www.ieee.org/web/careers/home/index.html.

CPMT Society News:

Congratulations to IEEE CPMT Society Award Winners Presented at 59th ECTC in San Diego, CA

Submitted by Leonard W. Schaper, Kitty Pearsall, and Wayne Johnson

CPMT Field Award:

The 2009 IEEE CPMT Award, the most prestigious award in the CPMT fields of study, was presented to GEORGE G. HARMAN (LF'IEEE) - NIST Scientist Emeritus (Retired NIST Fellow), Consultant, Gaithersburg, MD, USA, at the 2009 ECTC Conference.

The citation reads: "For pioneering achievements in wire bonding technology."

George Harman was hired at NBS/NIST in 1950 as an Electronic Scientist. In 1955, he filed for a patent on an electroluminescent microwave detector (# 2,928,937). He then studied the high frequency properties of various electroluminescent materials and discovered a new class of ferroelectric electroluminescent materials. His first 15 papers were generally in the area of applied physics and were published in the J. Appl. Physics, and similar journals. He studied contacts and surface states of several new unstudied (at that time) semiconductors (SiC, BC, etc.) and in the process obtained several US semiconductor device patents.

In 1968, a Navy strategic missile under development (Poseidon) had major reliability problems in its wire bonded interconnections. The urgency resulted in Harman being assigned to help solve that problem. This led to an extensive laboratory investigation designed to understand ultrasonic bonding and its evaluation. He developed a 25 µm diameter constricted, floating-cone capacitor microphone to plot the ultrasonic vibration modes of tools at 60 kHz, and applied those measurement methods to understanding and solving other problems in ultrasonic bonding machines and processes. Later, he used a laser interferometer to refine those earlier measurements. In 1971 he started the ASTM F-01.07 committee to standardize wire bond testing methods, which included pull test, nondestructive test, and ball bond shear test. Also, standards for bonding wire inspection methods, etc., were developed during that period. Harman, who currently chairs ASTM Committee F-01.07 (Wire Bonding, Flip Chip, and Tape Automated Bonding), updated and re-balloted the original wire bonding standards in 2005-06. Note that Harman's IEEE fellow citation (in 1982) was "for development of process control and screening procedures for microelectronic welding and bonding". He continues to contribute to the wire bonding area. Recently, an extension of his laboratory work and publications on wire bonding to soft substrates led to applying those principles to wire bonding on Cu-LoK chips. Other recent publications discussed projected metallurgical wire bond problems in NASA extreme temperature planetary exploration probes.

During the 1970's, Harman contributed to the military standards for testing wire bonds (at that time these were the only semiconductor/packaging standards publicly available and in general use), attended JEDEC meetings, and contributed data to be incorporated in their standards. He wrote the bond pull test method for MIL-S-19500 which was subsequently added to MIL-STD-750C, and supplied data and curves for the most used wire bond pull test in MIL-STD-883. He wrote the first version of the nondestructive bond pull test in MIL-STD-883 and has defended its use numerous times, and his paper on that subject in the IEEE IRPS stands alone for the statistical and metallurgical understanding of that test method. Currently, that test is required for most critical parts flown by NASA.

In his NIST Fellow position, George Harman has served as a national and international consultant in the field of wire bonding, advising and solving problems in chip-package interconnections for numerous organizations each year. He has taught most US and many foreign engineers both metallurgical and practical aspects of wire bonding in the 8-hour short-courses sponsored by UAZ, IMAPS, HKUST, and many others organizations for 20 years. He used the well developed and organized content of such lectures, in 1989, and published the first edition, and in 1997 the second edition of the only book(s) on that subject. It is frequently referred to as "the wire bond bible" and has been used by thousands of engineers (over 5000 copies of second edition have been sold by McGraw Hill). Two wire bond manufacturers have given a copy with each major machine purchased ("to educate and save us time and service calls to our customers"). These books have been a major world-wide contribution to the field by Harman.

Most of George Harman's career has been engaged in understanding, standardizing, implementing improvements into the industry's tooling, and disseminating wire-bond technology. He is the individual most responsible for transforming a labor-intensive manual bonding technology whose results depended upon an operator's skill, with attendant poor reliability, to a well-understood, highly automated (>8 bonds per second) method with an outstanding reliability record. As a result of Mr. Harman's work, wire bonding has become the industry standard. It accounts for more than 95 percent of the interconnections made between chips and the next level of assembly in electronic products manufactured worldwide. Approximately 7x10(+12) wire bonds are created each year. George Harman's work has had a profound impact on the industry, and likely benefited anyone utilizing an electronic product.

CPMT Society Awards:

The CPMT Award Committee is made up of a 7 cross-geographic members chaired by Kitty Pearsall. Team members are Charles Lee, Ning-Cheng Lee, Ralph Russell, Kwang-Lung Lin, Klaus-Jürgen Wolter, Petri Savolainen and Ephraim Suhir. As you can imagine there are many challenges in selecting the single, "BEST" candidate for each of the 5 CPMT Categories: Outstanding Young Engineer, Electronics Manufacturing Technology, Exceptional Technical Achievement, Outstanding Sustained Technical Contribution and the David Feldman Awards. This year awards were once again presented at the CPMT Luncheon at the 59th ECTC Conference held in San Diego. We were fortunate to have his son and daughter receive his award in his absence. Congratulations to all the winners!!! Job well done!

Outstanding Young Engineer Award:

The Outstanding Young Engineer Award is given to recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation. This year's award is being presented to **Dr. Madhusadan K. Iyenger** for his exceptional and sustained technical innovation over the last 5 years that has resulted in cutting edge cooling technology and products with realizable benefits to the IT industry and its' customers which has resulted in several patents and refereed publications. Dr Avi Bar-Cohen presented Madhusadan's award personally since he was his Graduate Studies Professor.

IEEE Mission

IEEE's core purpose is to foster technological innovation and excellence for the benefit of humanity

Electronics Manufacturing Technology Award:

The Electronics Manufacturing Technology Award is given to recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society. This year's award is being presented to **Ho-Ming Tong**. Dr Ho-Ming is known world wide for his pioneering development, manufacturing and implementation work in flip chip packaging in applications that spanned from high-end computing at IBM to cost sensitive applications covering computing, communications, consumer and car electronics at ASE, the world's largest IC assembly and test service provider. The award was accepted on behalf of Ho-Ming Tong by his son Carl Tong and daughter Irene Tong.

Exceptional Technical Achievement Award:

The Exceptional Technical Achievement Award is given to recognize an individual, or group of individuals for exceptional technical achievement in the fields encompassed by the CPMT Society. This year's award is being presented to **Dr. Sheng Liu** for his pioneering work on multi-physics and multi-scale modeling for manufacturing process modeling and reliability qualification coupled with the development of various validation tools. His work has resulted in many papers and publications in conference proceedings, 3 book chapters, 2 books (in preparation), over 300 technical papers, more than 70 patents filed or granted, and many keynote and invited talks. The award was accepted on behalf of Dr. Sheng Liu by his colleague.

Outstanding Sustained Technical Contribution Award:

The Outstanding Sustained Technical Contribution Award is given to recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society. This year's award goes to **Moises Cases**. He is a renowned expert in system level electrical packaging design and integration including system level timing for high performance digital systems encompassing multiple boards and cable subsystems which is noted by his numerous IBM and Professional awards, 50 issued patents as well as more than 92 publications in refereed journals.

David Feldman Award:

The David Feldman Award is given to recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions. This year's award is being presented to **CP Wong**. Dr Wong has been untiring in his passion and dedication to the IEEE and CPMT Society by serving in various CPMT leadership roles for the last 22 years that include serving as President, CPMT BoG (numerous terms), Chair/Member of the CPMT Fellow Committee and several Executive ECTC roles, such as General Chair of ECTC, Materials and Process Technical Sub Committee, CPMT ECTC Rep for 16 continuous years, as well as numerous IEEE roles. All of this in addition to having been recognized in 2002 as the first recipient of the CPMT Exceptional Technical Award highlight CP as an excellent David Feldman recipient.

CPMT Transactions – Best Paper Awards:

At the ECTC CPMT Award luncheon, awards were presented for the best 2008 papers published in the Transactions on Advanced Packaging and in the Transaction on Components and Packaging Technologies. The top papers were selected based on reviewer

comments during the peer review process and then the Associate Editors voted to select the winners. The objective of these awards is to recognize excellence and foster continuous improvement in our Transaction.

The winners were:

Transaction on Components and Packaging Technologies (TCPT):

Xuejun Fan, G. Q. Zhang, Willem D. van Driel, and Leo J. Ernst
"Interfacial Delamination Mechanisms during Reflow with Moisture Preconditioning"
T-CPT, Volume 31, Issue 2, June 2008

TCPT presentation: left to right: Wayne Johnson, Coauthors Leo Ernst and Xuejun Fan, William Chen

Abstract
This paper first examines the commonly-used thermal-moisture analogy approach in thermal-moisture analogy approach. We conclude that such an analogy using a normalized concentration approach does not exist in the case of soldering reflow, when the solubility of each diffusing material varies with temperature or the saturated moisture concentration is not a constant over an entire range of reflow temperatures. The whole field vapor pressure distribution of a flip chip BGA package at reflow is obtained based on a multiscale vapor pressure model. Results reveal that moisture diffusion and vapor pressure have different distributions and are not proportional. The vapor pressure in the package saturates much faster than the moisture diffusion during reflow. This implies that the vapor pressure reaches the saturated pressure level in an early stage of moisture absorption, even the package is far from moisture saturated. However, the interfacial adhesion degrades continuously with moisture absorption. Therefore, the package moisture sensitivity performance will largely reply on the adhesion strength at elevated temperature with moisture. A specially designed experiment with a selection of six different underfills for flip chip packages was conducted. Results confirm that there is no correlation between moisture absorption and the subsequent interface delamination at reflow. The adhesion at high temperature with moisture is the only key modulator that correlates well with test data. Such a parameter is a comprehensive indicator, which includes the effects of thermal mismatch, vapor pressure, temperature and moisture. In this paper, a micromechanics based mechanism analysis on interfacial delamination is also presented. With the implementation of interface properties into the model study, it shows that the critical stress, which results in the unstable void growth and delamination at interface, is significantly reduced when the effect of moisture on debonding is considered.

Transactions on Advanced Packaging (TADVP):

Kyung Suk (Dan) Oh, Frank Lambrecht, Sam Chang, Qi Lin, Jihong Ren, Chuck Yuan, Jared Zerbe, and Vladimir Stojanovic
"Accurate System Voltage and Timing Margin Simulation in High-Speed I/O System Designs"
T-AdvP, Volume 31, Issue 4, November 2008

TADVP presentation: left to right: Wayne Johnson, Coauthor Dan Oh, William Chen

Abstract
Accurate analysis of system timing and voltage margin including deterministic and random jitter is crucial in high-speed I/O system designs. Traditional SPICE-based simulation techniques can precisely simulate various deterministic jitter sources, such as intersymbol interference (ISI) and crosstalk from passive channels. The inclusion of random jitter in SPICE simulations, however, results in long simulation time. Innovative simulation techniques based on a statistical simulation framework have been recently introduced to cosimulate deterministic and random jitter effects efficiently. This paper presents new improvements on this statistical simulation framework. In particular, we introduce an accurate jitter modeling technique which accounts for bounded jitter with arbitrary spectrum in addition to Gaussian jitter. We also present a rigorous approach to model duty cycle distortion (DCD). A number of I/O systems are considered as examples to validate the proposed modeling methodology.

E-MAIL ALIAS AND IEEE WEB ACCOUNT NEEDED

2009 CPMT Society Board of Governors Election Goes Web-Based

Submitted by Marsha Tickman, Executive Director, IEEE CPMT Society

This year marks the implementation of a web-based balloting process for the CPMT Board of Governors election.

Eligible voting members will receive notification by e-mail in the Fall of this year with instructions for voting on-line. You will need an IEEE Web Account to access the ballot and cast your vote. This Web Account is the same one you may use for IEEE services such as renewing membership and accessing IEEE Xplore.

If you do not recall your Web Account username and password, or aren't sure whether you have established an account, please go to http://www.ieee.org/web/accounts to recover your password or establish a new account.

Please be sure to update your IEEE membership record with you current e-mail alias. If you DO NOT HAVE AN E-MAIL address or would prefer to receive a paper ballot by mail, please send your name, mailing address and IEEE Member Number by Tuesday 1 September to:

Marsha Tickman
IEEE CPMT Executive Office
445 Hoes Lane
Piscataway, NJ 08854 USA

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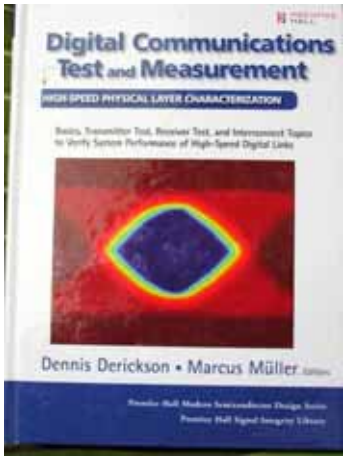
Book Reviews:

Submitted by Dr. David Palmer, IEEE Fellow

Digital Communications Test and Measurement High-Speed Physical Layer Characterization

Edited by Dennis Derickson and Marcus Muller

Price: $83.20 (Amazon)



This book is an excellent tutorial and guide for making high-speed measurements on communication hardware. The measurement set-ups are described in detail including cautions against common errors. Motivation for each measurement is given. This book is almost 1000 pages and could be used in a university laboratory class for in depth understanding if specific communication systems are provided to measure.

The first chapter reviews the digital communication system on a functional block level and Chapter three presents specific communication links so all measurements in the book have a focus.

For CPMT society members chapter 13 on physical interconnection measurements and modeling and appendix C detailing coaxial cables and connectors will be the most useful, but all the rest will be needed to allow efficient trade-offs on the system level. The book has five areas of concentration: bit error ratio measurements, high-speed digital waveform analysis, jitter in digital data stream, receiver testing, and characterization of the physical interconnection structures.

I was particularly impressed with the Time domain reflectometry discussion as applied to interconnections. Many issues confusing to the occasional lab user were clearly presented and made simple in execution.

The editors integrated the many author contributions in an efficient way so that each chapter can be used in isolation yet the user feels there is little duplication within the book.

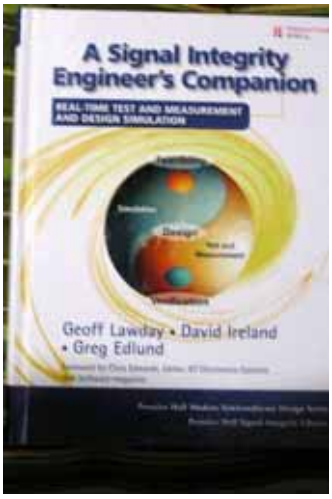
This book will find use in any cross-discipline design team. In particular, it will allow the package integration expert to understand the jargon and the trade-off pressures felt by others on the team.

A Signal Integrity Engineer's Companion Real-Time Test and Measurement and Design Simulation

By Geoff Lawday, David Ireland, and Greg Edlund

Prentice Hall Modern Semiconductor Design Series

Price: $80.00 (Amazon)



This book does a great job of teaching an approach to going from concept to product for high-speed digital systems. New design methods depending on complex signal integrity tests and measurements are presented. The presentation assumes a team is working on a complex design. However, considerable course or hardware experience is needed to gain the maximum from this text. This reader would have been helped by a glossary of all the initials used (apparently with the assumption that the reader already used them daily).

The writing is first class with catchy phrases like "probing has been the Cinderella of instrumentation" and "adequate instruments are only half the (troubleshooting) story, the partner in their work is the stimulation instrument – the signal source." Humor is used to keep the reader engaged while grappling with difficult concepts. The major concerns of reflections, attenuation, crosstalk, poor grounding, timing errors, and EM radiation are addressed from specifications to hardware testing.

Chapter five on the need, fundamentals, and subtleties of probes proved very important and is not included in many similar topic books. Each chapter has a motivational introduction and often a wise conclusion that underlines important lessons. The complete book integrates the analog perspective needed with the digital design process so robust at low frequencies. The book treats the importance of fixtures lightly despite a history of precision fixtures being used to test blocks/modules of the system when they are independently finished.

The last chapter brings in the perspective and tools (SPICE & ADS) needed for the many systems that now have wireless features in addition to the high-speed digital complexity. This chapter sets the

stage so the engineer knows what help they may need in this area should it require more depth.

This book will be of great value to many engineers but they will have to self-identify based on their experience and current projects.

Introduction to System-On-Packaging (SOP), Miniaturization of the Entire System,

By Rao R. Tummala and Madhavan Swaminathan

MacGraw-Hill, 2008, pp. 785

This is a complete introduction to the on-going research and development of SOP. The authors have co-authored several chapters and edited the rest written by leaders in the field. The basic theme is that there is plenty of room for further miniaturization even after the IC digital evolution call Moore's Law. There is no question that the many components and boards of a system are undergoing continual miniaturization using techniques other than those from the CMOS juggernaut. However, the transistor count has gone up 9 orders of magnitude and the transistor miniaturization improved by 6 orders, whereas the SOP miniaturization appears limited to 2 orders (may just be the reviewers conservative view). None the less, all this technology will be needed to win in the marketplace over the next decade.

This book describes where SOP technology is being expanded and directions technology may take, but does not really address any economic destiny. Remember CMOS is slowing for economic not technical reasons. The SOP is not an irresistible BORG spaceship assimilating all technology in its integration effort, but one future direction proved plausible by the many great developments discussed in this book. Many university and industrial advances are presented in detail within this book.

Before discussing the details, it is important to note that each section of this book presented new exciting facts and new technology interconnections to any reader except those with many years developing integrated packaging. The large number of "AHAs" is a mark of a great tech book.

The integration of unusual single MEMs or photonic element into a highly integrated system is quite a challenge. The MEMs and Optoelectonics chapters in this book give several options to accomplishing this level of integration in addition to discussing economic packaging of single MEMS and photonic devices. Other chapters address many integration aspects of Biosensor, electrical module testing, thermal management, wirering, RF, mixed signal, and stacked ICs.

The RF chapter uses LTCC and LCP integrated packaging as the basis for SOP creation. Particularly informative discussions occur on how to miniaturize and add gain to module antennas. Discussion of RF MEMs switches and their pros and cons as well as popular RFIDs are also well covered.

One practical aspect of system realization is not discussed in the book (it may be too soon). With the existing system of miniaturizing / integrating the digital and small signal analog signals in integrated circuits and interconnecting them with other components on boards there are well established methods to modify (tweak) the design on the board level when the simulations missed a little in timing or noise levels. The higher level of miniaturization of SOP does not appear to have these options so may require higher fidelity simulations.

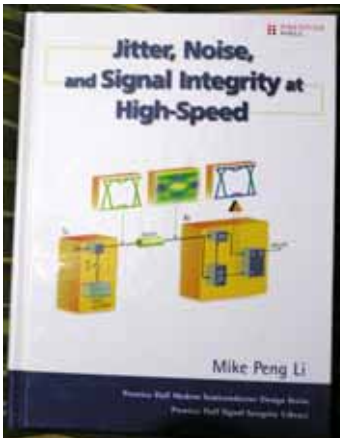
In addition to clear descriptions and explanations, each chapter has extensive references so that the working developing engineer can quickly study the foundation of any aspect of this field before they invest in further efforts. This book is a pleasant necessity for any engineer or manager involved in miniaturization of systems and modules.

Jitter, Noise, and Signal Integrity at High Speed

By Mike Peng Li

Prentice Hall Modern Semiconductor Design Series

Price: $80 (Amazon)



As clock speeds and analog signals frequencies are increasing, the system packaging design becomes the important component to maintaining Signal Integrity. The best system architectures can be sabotaged by not including package design from the very beginning. The author has clearly been involved in many difficult system designs that had noise challenges, some of which were unanticipated at the start.

This book fulfills the need in describing the fundamentals of Noise and Jitter so design tradeoffs can be made with reasonable certainty of eventual performance. Although not directly addressing modern micropackaging, the sources of noise are detailed so the experienced packaging engineer can quantify the contribution of each design choice.

Although this is the best book around for a university course on this material, I suspect that this subject matter can not really be learned

until one is well within a complex industrial design and the slow realization that the margin of signal integrity is shrinking dawns on the team. By analogy, this subject is like a thermodynamics course for an undergraduate; the students will survive and maybe get a good grade but they will never understand until they have faced a few real life designs that depend on true understanding.

Thus I recommend that every design team (including package experts) have this book in their meeting room where they can take turns studying it and trying to tutor each other as the inevitable need arises. For example, the only books on this topic my firm has today were written about 15 years ago when frequencies were gentle and packaging had more margin based just on rules of thumb. Since then I/O frequencies have increased from 1 to 40 Gbs, and at least one designer must really understand the features that increase noise / crosstalk and degrade the Bit Error Rate.

Do not feel neglected if you do not need this book; your designs are probably very challenging on some other basis such as cost or miniaturization. We can't all struggle up the frequency spectrum.

Conference News:

59th ECTC Overview:

Submitted by Eric Perfecto, Senol Pekin, Rao Bonda, Pat Thompson, and Bill Chen – ECTC 2009 Committee

The 59th Electronic Components and Technology Conference was Alive and Well in San Diego, CA

Sheraton San Diego Hotel & Marina was the venue for the 59th ECTC in May 26-29th, 2009.

Although the attendance was not the highest ever due to worldwide recession and the H1N1 flu worries, the 59th ECTC in San Diego was a great success. Thanks to the authors and the ECTC program committee, they presented 336 high quality papers in 38 oral sessions and three poster sessions. About 46% of the papers presented were from North America, 37% from Asia and 17% from Europe. With 551 conference attendees and 185 professional development course (PDC) attendees, the 59th ECTC pulled it through successfully in an industry that is working on rebounding from a worldwide recession. In addition to technical sessions, the conference was enhanced by 16 Professional Development Courses, 14 new exhibitors totaling to 52, luncheons, raffle drawings, evening receptions, best paper awards, ECTC Panel Discussion chaired by William Chain of ASE, and Plenary Session co-chaired by Jie Xue of Cisco and Senol Pekin of Intel. Technical sessions started on Tuesday and continued through Friday.

A Big Thanks to the Executive Committee of the 59th ECTC!

From left to right: David McCann, Rao Bonda, Steve Bezuk, C. P. Wong, Wolfgang Sauter, Lisa Renzi, Glyndwr Smith, Kitty Pearsall, Eric Perfecto, Patrick Thompson, Jean Trewhella, Rajen Dias, and Torsten Wipiejewski (not shown)

Tuesday:

185 attendees attended 16 professional development courses. Eight of these courses were new for this year. The courses were organized by the PDC Committee chaired by Kitty Pearsall of IBM.

ITRS Assemblies and Packaging Technology Committee held its meeting on Tuesday from 8:00 am until 5:00 pm. In parallel, and with increased focus in optical packaging, two special sessions were organized by the Optoelectronics committee.

In the evening, students attended the ECTC Student Reception where they had an opportunity to learn about how the technical subcommittees work to select the abstracts.

The ECTC Student Reception was hosted by Lei Shan of IBM TJ Watson Research Center.

Following the students reception, the 59th ECTC General Chair hosted a reception for the speakers and session chairs.

IEEE Vision

IEEE will be essential to the global technical community and to technical professionals everywhere, and be universally recognized for the contributions of technology and of technical professionals in improving global conditions.

Wednesday:
Technical sessions started on Wednesday at 8:00 AM and prior to that in the morning, the speakers and session chairs met at breakfast to prepare for the sessions. Three coffee breaks everyday created the opportunity for networking and exchanging information among the conference attendees.

The 2008 Best and Outstanding papers for the oral presentations and posters were also presented at the ECTC luncheon.

On Tuesday night, ECTC Panel Discussion on "Consumer Electronics and Packaging Technologies in Times of Recession and Recovery" chaired by William Chen of ASE attracted the attention. Conference attendees had an opportunity to listen to Jim Walker, VP of Research at Gartner-Dataquest; Ron Stager, Partner In-charge at KPMG; Mark Brillhart, VP of technology and Quality at Cisco Systems; Joyce Koo, Materials Lab Manager at Research in Motion; Raj Master, General Manager of IC Packaging, Quality and Reliability at Microsoft; and Michael Nealon, Director of Hardware and Design at IBM Server Group.

Jim Clifford, Senior Vice President and General Manager of Operations, Qualcomm CDMA Technologies gave a talk at the ECTC Luncheon. His presentation is posted at the ECTC web site due to popular demand.

Mr. Jim Clifford is the Senior Vice President and General Manager of Operations at QUALCOMM CDMA Technologies (QCT). In this role, Mr. Clifford is responsible for IC and Packaging Technologies, Procurement, Integrated Supply and Demand Planning, and Quality in addition to managing the overall operations functions for the QCT division.

Mr. Clifford has been at QUALCOMM since 1994, when he joined the company as a director of business development and oversaw product development in its OmniTRACS division. In 1996 he moved to QCT as director ASICs, and has focused on sourcing IC chips during the explosive growth for CDMA technology. He was promoted to vice president of operations in 1997, senior vice president in 2000, and GM of Operations in 2003. Prior to his career at QUALCOMM, Mr. Clifford had more than 20 years of experience at Unisys in positions ranging from IC design to vice president and general manager of mainframe computer manufacturing. Mr. Clifford holds a Bachelor's of Science in Physics from San Diego State University, and is a graduate of the Executive Program for Scientists and Engineers offered by the University of California, San Diego.

Mr. Clifford's luncheon presentation at ECTC on "Less and Moore: Wireless, Fabless, Factory-less" covered an overview of the expanding mobile applications that are driving the semiconductor landscape. He talked about the importance of the evolving collaborative models across the value chain to meet product requirements such as low cost, low power, small form factors and high performance. Innovative technology solutions and co-design of architecture, design, silicon and packaging are requirements to meet consumer demand for increased features and capabilities. Mr. Clifford's presentation is posted on the ECTC website www.ectc.net.

In the evening, exhibitor reception provided another opportunity for networking and exchanging information among the conference attendees.

General Chair Rao Bonda hosted the program subcommittee chairs and assistant chairs in his suit and thanked them for their leadership in selecting the 336 technical papers out of 564 abstracts which was the second highest number of abstracts received in the ECTC history.

On Wednesday night, Jie Xue of Cisco and Senol Pekin of Intel Corporation co-chaired the ECTC Plenary Session titled "Product Qualification Strategies in the Semiconductor Industry". Panelists Tin-Lup Wong, DE and Executive Director of Product Q&E at Lenovo; Bruce Euzent, VP of Q&R at Altera; Tom Gregorich, CP of IC Packaging at Qualcomm; Jean Trewhella, Director of packaging R&D at IBM Corporation; and Jim Walker, VP of Research at Gartner-Dataquest concentrated on time-to market, improving innovation, and enhancing customer satisfaction. This panel was held as a continuation in a series that concentrates on critical issues related to the semiconductor industry by bringing the experts and leaders together in the framework of text-book theory, and real life challenges and applications.

Thursday:
The 2009 CPMT Awards were presented at the Luncheon. Madhusudan Iyenger, Ho-Ming Tong, Sheng Liu, Moises Cases, C. P. Wong and George Harman were honored with various awards.

Industry veteran and wire bonding expert, George Harman, was among the ones that were honored due to their contributions. He received 2009 IEEE CPMT Field Award.

General Chair Rao Bonda of Freescale Semiconductor received an award from CPMT Representative C. P. Wong for contributions to the ECTC conference.

Fifty two exhibitors took part in the Technology Corner Exhibit which continued on Thursday.

On Thursday, ECTC Program Committee met in preparation for the ECTC 2010 in Las Vegas. CPMT Representative C. P. Wong announced that Wolfgang Sauter of IBM Corporation will serve as the Assistant Program Chair for 2010. Senol Pekin of Intel Corporation joined the Executive Committee as the new Web Administrator.

Thursday evening was always fun at the ECTC as the conference attendees and their spouses got plenty of time to talk at the well-catered ECTC Gala Reception.

In the far back of the photo above, Debb Kaller of Parallel Semiconductor and Lee Smith of Amkor can be seen exchanging information.

Shown in the picture above is the "A-Team" for 2010: (from left to right) Assistant General Chair Rajen Dias of Intel Corporation, Program Chair David McCann of Amkor, Assistant Program Chair Wolfgang Sauter of IBM, and 60th ECTC General Chair Jean Trewhella of IBM.

Friday:

Technical sessions continued till 5 PM. Conference attendees enjoyed the Program Chair luncheon at the last day of the conference, thanks to the raffle drawings announced by Thomas Reynolds.

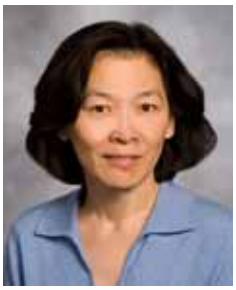
Tin-Lup Wong, DE and Executive Director of Product Q&E at Lenovo, who joined the conference for the first time this year to speak at the ECTC Plenary Session is likely to attend next year also, since he won a free registration for next year's conference.

The First Call for Papers for 60th ECTC is already out and can be found at www.ectc.net. You are invited to submit a 750-word abstract by October 15, 2009. In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses.

See you at the 60th ECTC in Las Vegas, Nevada next year!

59th ECTC 2009 Plenary Session:

Product Qualification Strategies in the Semiconductor Industry was under the Spotlight at the 59th ECTC in San Diego, CA



Jie Xue of Cisco and Senol Pekin of Intel Corporation moderated the discussion to highlight the strategies in integrating qualification into product development with emphasis on cost-cutting, time-to-market and improved innovation.

59th ECTC 2009 Plenary Session Participnats

Session Chairs are Jie Xue of Cisco and Senol Pekin of Intel Corporation. Panelists included Tin-Lup Wong, DE and Executive Director of Product Q&E at Lenovo; Bruce Euzent, VP of Q&R at Altera; Tom Gregorich, CP of IC Packaging at Qualcomm; Jean Trewhella, Director of packaging R&D at IBM Corporation; and Jim Walker, VP of Research at Gartner-Dataquest.

Reliability qualification is often the bottleneck in semiconductor product development and can significantly delay deployment. In an industry that is working on rebounding from a world wide recession, high level experts took the stage and discussed product qualification strategies towards enhancing customer satisfaction, at the Plenary Session organized and co-chaired by Jie Xue of Cisco and Senol Pekin of Intel Corporation. The session attracted hundreds of engineers and managers. This panel was held as a continuation in a series that concentrates on critical issues related to the semiconductor industry by bringing the experts and leaders together in the framework of text-book theory, and real life challenges and applications.

Jim Walker, VP of Research at Gartner-Dataquest took the stage first by predicting that Semiconductor Industry will rebound faster from recession than most other industries. The World financial crisis has resulted in chaos and continued downside momentum for most industries. In contrast, the recession of 2001 prepared the semiconductor industry to be more astute in managing capital, inventories and resources in this current economic downturn that began in 2008. As a result, second half of this year should be improved, as seasonal increases in cell phone, PC and even consumer electronic products orders for IC's begin to increase due to inventory replenishment. Mr. Walker further stated that semiconductor packaging will play an important role in this upturn, since increased demand for the next generation of electronic products will result in the adoption of new packaging technologies and qualification schemes. He emphasized the importance of time-to market in revenue generation and margin improvement.

Jean Trewhella, Director of IBM Packaging Research and Development Center, challenged the status-quo by explaining that technology focused development done early can reduce the technical risks and enable truly streamlined qualification testing. However this is becoming increasingly difficult as the demands on packaging to overcome the thermal, bandwidth and chip packaging interaction challenges of semiconductors grow. In order to drive reliable solutions with high value the silicon technology and the packaging technology must be co-developed with target application architecture space in mind. Ms. Trewhella emphasized that collaboration through an eco-system across the value chain can enable non-vertically integrated companies to reap the benefits of end-to-end development.

Tom Gregorich , VP of IC Package Engineering at Qualcomm, stated that new technologies introduce new failure mechanisms. Over the past 20 years the mobile telephone has grown-up from being a trunk-mounted voice-only device to a handheld data portal to the World Wide Web and beyond. During this same time period, the semiconductor technologies used in these devices have evolved at ever-increasing rates. Extrapolating J.M. Juran's definition of quality ("fitness for use") over time, Mr. Gregorich explained that the key to maintaining reliability is by understanding and management of component stresses. He then introduced the time-to-market product development constraint and the challenges of parallel and simultaneous technology deployment. Mr. Gregorich referred to a series of technology changes which have had significant impact on the semiconductor industry. These technology changes include the following transitions: from leaded to SMT components; from trunk to handheld; from SnPb to Pb-free and from wire bond to flip chip. Finally he presented a list of "10 Easy Steps" to better reliability qualification.

Bruce Euzent, VP of Quality and Reliability at Altera, reminded that "one size does not fit all" in reliability qualification. He explained that there are many strategies for qualification of new components other than the traditional 3 lots for 1000 hours qualification exercise. Different applications and market segments introduce time to market and specific failure mechanisms that must be dealt with. Knowledge based qualification and application specific qualification strategies are used to address these concerns. No one methodology is applicable for every product, market, and application. He concluded that a successful qualification methodology requires the intelligent melding of multiple concepts.

Tin-Lup Wong, Distinguished Engineer and Executive Director, Product Engineering & Quality at Lenovo said "what is enough is not enough!" As notebook computer design becomes thinner and lighter, the design consideration and robustness of the second level packaging on Ball Grid Arrays (BGA) become a significant part of the reliability equation. The problem is compounded by highly mobile users, wireless computing and challenging user environment. Dr. Wong explained how the general assumptions and practices in the packaging world were affecting the reliability of ThinkPad notebook design, and how the design team collaborated with industry leaders, drove design innovations and improved on end-to-end process control to deliver reliable products to the market.

59th ECTC 2009 Panel Discussion:

The theme of the Tuesday night ECTC Panel Session was "Consumer Electronics and Packaging Technologies in Times of Recession and Recovery". It was chaired by William Chen, CPMT Society President, and Senior Technical Advisor at ASE. There panel session scheduled from 7:30 pm to 9:00 pm had attendance of about 200 participants.

The eclectic panel was composed of industry leaders, technologists, business consultants, and analysts.Panelists presented different perspectives in the consumer electronics recovery landscape and new opportunities in the new economy.

The panel addressed a number of questions at the crossroads of consumer market, global business and technology innovation including 3D packaging with particular focus of the impact of the deep recession and eventual recovery. Some of the questions addressed by the panelists were: How will the consumer electronics product landscapes look, as the economic recession moves into recovery? What

are the dynamics between market imperatives and technology innovations? How do these trends drive the direction of packaging technologies?

Picture of 59th ECTC 2009 Panel Session Participants - Joyce Koo, Manager, Materials Lab, Research In Motion; Michael Nealon, Director, Hardware and Design, IBM Server Group; Raj Master, General Manager, IC Packaging, Quality & Reliability, Microsoft; Mark Brillhart, Vice President, Technology and Quality, Cisco; William Chen, Senior Technical Advisor (Panel Chair, standing); Ron Steger, Partner in Charge, KPMG; Jim Walker, V.P. of Research, Semiconductor Manufacturing, Gartner/Dataquest.

The following paragraphs provide brief biography of the 59th ECTC 2009 Panel Session participants:

Dr. Y.C. Joyce Koo is currently serving as Material Interconnect Lab Manager at Research in Motion Ltd. He has extensive experience in the field of Microelectronic and Photonics packaging, related to commercial, military and telecommunications. She has held many senior positions at various companies, including Specialty Engineer at Litton System and Staff Engineer position at IBM Canada. Joyce obtained her PhD degree in the field of microcrystalline (nano-crystalline) silicon fabrication and characterization from the University of Toronto, Canada in 1992. Joyce currently is a lab manager at Research In Motion, Material Interconnect Lab.

Mr. Mike Nealon is the Director of System Hardware Design for IBM's Enterprise Systems Development Organization. His present responsibilities include the system design and hardware development of IBM's Enterprise Systems, including the High End zClass Servers, POWER Servers and High End Storage. Mike has been with IBM for 26+ years with assignments in processor and system packaging technology development, microprocessor design and system development serving in a variety of managerial and technical leadership positions.

Mr. Raj Master is currently General Manager of Hardware IC Packaging,Quality and Reliability Engineering for Microsoft. He is responsible for Game console, Keyboard, mouse, webcam, Zune and Surface computing. Raj was at AMD from 1996 to October 2008. At AMD, Raj was a Corporate Fellow and Chief Technologist. Raj is responsible to develop AMD strategy for C4, packaging, assembly and Thermal solutions. He led the Organic packaging development and manufacturing which is now in high volume production. Raj joined AMD after spending 21 years at IBM. He was Senior Technical Staff member at IBM prior to joining AMD. He was responsible for packaging development and manufacturing as related to C4, Ball Grid Array, Column Grid Array, Board Level Reliability and Multi Layer Ceramic Substrate.

Mr. Mark Brillhart leads Cisco's Technology and Quality organization, a global team responsible for delivering customer-driven quality and reliability solutions and infrastructure for Cisco products. With 300+ employees in locations around the world, Brillhart oversees a team responsible for developing industry-leading testing tools and technologies for leading-edge ASICs, PCBs, optical devices, custom memory modules, and complex interconnect technologies. Brillhart joined Cisco in 1999, first as a technical lead and then as manager of the Interconnect Reliability and Electronic Packaging teams. He has also served as Director of Hardware Reliability, Sr. Director of Component Quality and Technology, and Vice President of Manufacturing Operations Engineering. Prior to Cisco, he held a variety of engineering and technical lead positions at HP, as well as research and development positions in the medical products industry.

Mr. Ron Steger began his career with KPMG in 1976, and was admitted into the partnership in 1986. Mr. Steger is one of a select number of partners who has been appointed both an IFRS and U.S. SEC Reviewing Partner, the firm's senior-most technical positions. Mr. Steger has extensive experience serving clients in the technology, food service and consumer products industries. He is the former National Industry Director for Electronics, and currently serves as the leader of KPMG's Global Semiconductor Practice.

Mr. Jim Walker is a vice president of research with the semiconductor manufacturing team at Gartner-Dataquest. His research covers semiconductor packaging and assembly, manufacturing outsourcing services, MEMS and nanotechnology. Before joining Gartner Dataquest, Mr. Walker was the co-founder and vice president of marketing for Hana-USA, a subcontract IC package assembly company. At Dexter Electronic Materials and E.I. DuPont, he performed research, development, quality assurance and technical service utilizing polymeric materials for adhesive, composite, aerospace, electronic and semiconductor applications. At National Semiconductor, Mr. Walker held various roles, including surface mount packaging marketing manager. He is a founding member of the Surface Mount Technology Association (SMTA) and served as the national president.

CPMT ECTC Volunteer Recognition:

More than 200 volunteers that contributed to each ECTC are the key for making the ECTC a premier packaging conference. Many of these volunteers have served ten, twenty or even more years, representing an impressive time and energy contribution. In 2008, the CPMT BOG decided to recognize long-term volunteers, and created the CPMT ECTC Volunteer Recognition Award. The award recognizes two service milestones, 10 and 25 years. The first presentation of awards was made at the 2009 ECTC by Bill Chen, President of the CPMT. Since 2009 was the inaugural year, plaques were presented to "catch up" with volunteers' service. The 10-year plaques were presented to volunteers with 10 to 24 years of service, and the 25-year plaques were presented to volunteers with 25 or more years of service. In all, 56 volunteers received 10-year plaques, and four volunteers received 25-year plaques. The accompanying list contains the names of all recipients. Bill Chen and the entire CPMT BOG thank all ECTC volunteers for their contribution to the ECTC.

10-year recipients were Amit Agrawal, Yasuhiro Ando, Rao Bonda, Jo Caers, Michael Caggiano, Andreas Cangellaris, Moises Cases, Rajen Chanchani, Harry K. Charles, Mario Dagenais, Rajen Dias, Craig Gaw, Lih Tyng Hwang, Masataka Ito, Christine Kallmayer, Sung K Kang, George Katopis, Harry Kellzi, Bruce Kim, Claude

Ladouceur, Pradeep Lall, Michael Lamson, John Lau, Michael Lebby, Chin C. Lee, Timothy Lenihan, Jong-Kai Lin, Johan Liu, Erdogan Madenci, Tony Mak, Raj Master, Goran Matijasevic, David McCann, James E. Morris, Luu Nguyen, Donna M. Noctor, Dennis Olsen, Kyung-Wook Paik, Kitty Pearsall, Raj Pendse, Eric Perfecto, Tom Poulin, Albert Puttlitz, Sudipta Ray, Thomas Reynolds, Bill Ring, Leonard Schaper, Suresh K Sitaraman, Joseph Soucy, Ephraim Suhir, Madhavan Swaminathan, Tom Swirbel, Andrew A.O. Tay, Jan Vardaman, Torsten Wipiejewski, and Ping Zhou.

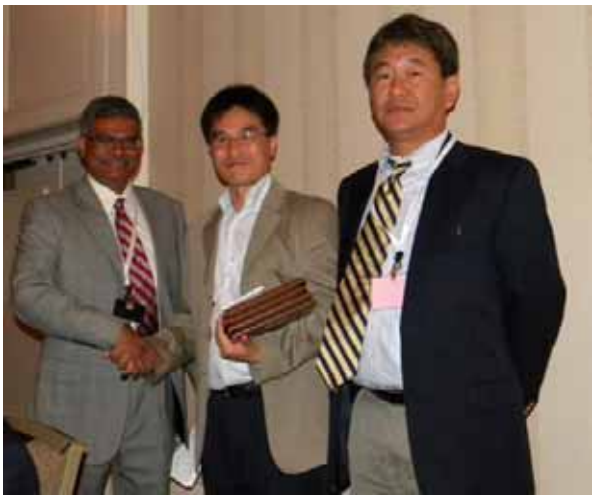
25-year recipients were DarvinEdwards, George G.Harman, PatrickThompson, and C. P.Wong.

Patrick Thompson receiving 25-year ECTC Volunteer Service award from Bill Chen

C.P. Wong receiving 25-year ECTC Volunteer Service award from Bill Chen

Best of ECTC 2008 Conference Papers:

The best paper awards for ECTC 2008 were presented at ECTC 2009 luncheon on May 27, 2009 in San Diego. Jean Trewhella, the Program Chair for ECTC 2008 coordinated the selection process and the awards were presented by Rao Bonda, the General Chair for the ECTC 2009.



Best Papers - 2008:
The authors of the Best Session Paper shared a check for US$2500 and the authors of the Best Poster Paper shared a check for US$1500.The winning authors also received a personalized plaque commemorating their achievement.

Best Session Paper
"Material Design and Package-Level Reliability of a Novel Low-Temperature Solder Based on Intermetallic-Compound Phases with Superior High-Homologous Temperature Properties" by Daewoong Suh and Chi-Won Hwang – Intel Corporation; Minoru Ueshima and Jun Sugimoto – Senju Metal Industry Company, Limited

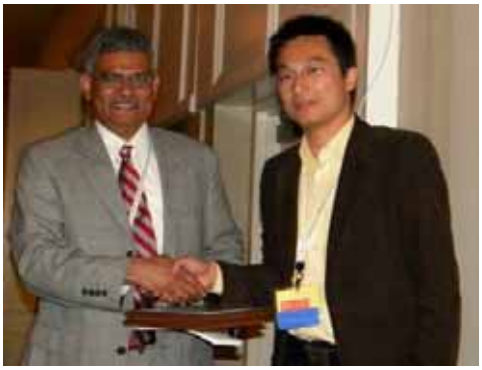
Best Poster Paper
"Development of a 50mm Dual Flip Chip Plastic Land Grid Array Package for Server Applications" by Sylvain Ouimet and Isabelle Dépatie – IBM Canada Limited; Jon Casey, Kenneth Marston, Jennifer Muncy,Virendra Jadhav, and Thomas Wassick – IBM Semiconductor Research and Development Center; John Corbin – IBM Systems and Technology Group

Outstanding Papers – 2008:
The winning authors for Conference Outstanding Session and Poster Papers received a personalized plaque commemorating their achievement and shared a check for US$1000.

Outstanding Session Paper
"Replacement of the Drop Test with The Vibration Test-The Effect of Test Temperature on Reliability" by T.T. Mattila, L. Suotula, and J.K. Kivilahti – Helsinki University of Technology

Outstanding Session Paper
"Replacement of the Drop Test with The Vibration Test-The Effect of Test Temperature on Reliability" by T.T. Mattila, L. Suotula, and J.K. Kivilahti – Helsinki University of Technology

Outstanding Poster Paper
"Interfacial Fracture Properties and Failure Modeling for Microelectronics" by A. Xiao, K.M.B. Jansen, J. de Vreugd, and L.J. Ernst – Delft University of Technology; H. Pape – Infineon Technologies AG; B.Wunderle – Fraunhofer IZM



Motorola Electronic Packaging Fellowship – 2008:
The winning student paper author received a three year fellowship grant of US$21,000 at his/her university. The following paper was selected based on the Motorola Electronic Packaging Fellowship paper competition conducted at 58th ECTC in Lake Buena Vista, Florida:

"3-D Stacking of Chips with Electrical and Microfluidic I/O Channels" by Calvin R. King Jr. (Student Author), Deepak Sekar, Muhannad S. Bakir, Joel Pikarsky, and James D. Meindl – Georgia Institute of Technology; Bing Dang – IBM T. J.Watson Research Center

CPMT Ph.D. Student Fellowship – 2008:
The winning student paper author received a one year Fellowship of $10,000 towards his/her Ph.D. studies in 2008 and 2009.The following paper was selected based on the CPMT Ph.D. student fellowship paper competition conducted at 58th ECTC in Lake Buena Vista, Florida:

"Microwave Design & Characterization of a Novel Nano-Cu based Ultra-fine Pitch Chip to Package Interconnect" by Tapobrata Bandyopadhyay (Student Author), Gaurav Mehrotra, P.M. Raj, Madhavan Swaminathan, and Rao Tummala – Georgia Institute of Technology; Mahadevan K. Iyer – Infineon Technologies

Intel Best Student Paper – 2008:
The winning student received a certificate and a check for $2500.The following paper was selected based on the Intel Best Student Paper competition conducted at 58th ECTC in Lake Buena Vista, Florida:

"Peridynamic Theory for Impact Damage Prediction and Propagation in Electronic Packages Due to Drop" by Abigail Agwai (Student Author), Ibrahim Guven, and Erdogan Madenci – University of Arizona

The awards for ECTC 2009 Best Papers will be presented at ECTC 2010 in Las Vegas, Nevada on June 2, 2010.

Kudos to 59th ECTC General Chair Dr. Rao Bonda:

Dr. Rao Bonda is currently a technology program manager in Freescale Semiconductor, Inc. (formerly known as Motorola's Semiconductor Products Sector) in Tempe, AZ. He received a Ph.D. in Materials Science and Engineering from the University of Pennsylvania, Philadelphia, PA, in 1985. After receiving Ph.D., Rao continued research in materials science at the Ohio State University, Columbus, OH and the University of Wisconsin, Madison, WI until 1989. Prior to joining Motorola in 1994, he was a research member at IBM T.J. Watson Research Center, Yorktown Heights, NY, and IBM Microelectronics Division, Endicott, NY.

Rao has been a member of the Board of Governors for the IEEE CPMT Society for over twelve years. He was the Chair of its Awards Committee from 1997-2005. At present, he is the Vice President-Technical for the Society. He is also an Associate Editor for IEEE Transactions on Advanced Packaging journal. He is very active in CPMT Phoenix Chapter and IEEE Phoenix Section. He has served as the chair and program chair for the Chapter and as the chair for the IEEE Phoenix Section.

Rao has been actively participating in the Electronic Components and Technology Conference (ECTC) for over twelve years. He has served as the chairman of the Components and RF sub-committee and has chaired the sessions at the ECTC. He has chaired the Professional Development Courses committee and served on the committee for three years. He was the Assistant Program Chair for the 2006 ECTC, the Program Chair for 2007 ECTC, Vice General Chair for 2008 and General Chair for 2009. He is currently the Jr. Past General Chair for 2010 ECTC.

Rao is a senior member of the IEEE. In addition to a Ph.D., he holds an MS and a BS in Metallurgical Engineering from Indian Institute of Technology, Kanpur, and Regional Engineering College, Warangal (India), respectively. He also received an MBA from the Arizona State University, Tempe, AZ, in 1998.

SWTW 2009 Update:

Submitted by Jerry Broz, Ph.D., General Chair of SW Test Workshop

The 19th Annual IEEE Semiconductor Wafer Test Workshop (SW Test) was successfully held at the Paradise Point Resort in San Diego, CA, from June 7 to 10, 2009. This yearly workshop brings together technologists, engineers, and managers as well as sales and marketing professionals involved with all aspects of probe technology and wafer level testing. The SW Test 2009 agenda consisted of a technical program, supplier exhibits (which ARE NOT open during the technical sessions), and a Casino Royale Social Event as well as plenty of time for informal interaction and networking with colleagues. The total conference and EXPO attendance was 175 with approximately 15% international attendees representing a total of 12 countries. Unfortunately, due to the H1N1 pandemic alert level, many of the usual international attendees were restricted from travelling to the United States.

The workshop began with a Sunday afternoon tutorial session organized by Technical Program Chair Brett Crump in conjunction with Darren James and Jeff Greenberg of Rudolph Technologies. This excellent three part tutorial provided new and experienced technologists key insights into many of the metrology problems facing the wafer test industry. Topics included an introduction into applied metrology concepts; a series of case studies focused on metrology tool capability assessments; and wrapped up with a practical discussion on the metrology approaches used to fix wafer sort floor problems.

After the welcome reception, Jerry Broz, Ph.D., SW Test General Chair, gave a short, "Probe Year In Review" presentation which set the stage for the Keynote Presentation, entitled, "Test Economics Driving Test Technology", made by Risto Puhakka, President of VLSI Research, Inc.

Mr. Puhakka discussed the key metrics tracked by VLSI which showed that the overall semiconductor industry was relatively healthy as the global recession began. Interestingly, these metrics demonstrated that half of the global chip recession was caused by overspending within the Taiwan memory sector. VLSI's global chip making climate trend index showed that the semiconductor industry has started slowly moving out of the "deep freeze". The data provided also showed that the general semiconductor business and capacity utilization rates are basically returning to normal but at an overall lower operating level.

The probe card market experienced a reduction in revenue of approximately 30% from 2008; with the most dramatic changes occurring in the advanced probe card technologies primarily used for memory test. FormFactor, Micronics Japan (MJC), and Japan Electronic Materials (JEM), respectively, remained as the top three probe card suppliers world-wide; however, the rest of the top ten saw a major reshuffle. Mr. Puhakka stated that VLSI has already seen that the back-end consumables and materials are bouncing back and expects the probe card and socket businesses to recover sooner than ATE. ATE is forecasted to remain less than half of total test hardware spending. Overall, VLSI's outlook for the semiconductor industry was very positive for the rest of 2009 and into 2010. Risto's keynote presentation will be available on the SW Test website (http://www.swtest.org) in July; in the meantime, it can be downloaded from the weSRCH.com website at http://electronics.wesrch.com/pdfEL1SE1ZTZAAXK.

The 2009 SW Test technical program began on Monday morning with the Welcome session by Dr. Jerry Broz. Dr. Broz gave a positive update on Bill Mann, Chair Emeritus, who is battling cancer and recognized the passing of long time SW Test contributor and Steering Committee member, Frank Pietzschmann (Qimonda-Dresden). Dr. Jerry Broz, Ph.D., was selected as a recipient for the IEEE Computer Society's Golden Core award, given for long-standing service to the society. Each year the IEEE Awards Committee selects up to a maximum of 50 recipients out of the more than 100,000 current IEEE Computer Society members and permanently includes the names in the Golden Core Member master list. The Golden Core is the highest level of membership designation in the IEEE Computer Society.

The next two and a half days were filled with a wide variety of technical presentations covering every facet of the wafer test process from *Large Area Array Probing Challenges* to *Damage Control and Low Force Probing*. Some individual highlights from the technical program included Michael Huebner, Ph.D., (FormFactor) and Scott Lindsey, Ph.D. (Aehr Test), discussing the future of increased pin counts and two different full wafer probing methods. The importance of consistent and accurate data tracking methods in the sort environment was detailed by Mark Winn (Intel) and Rob Marcelis (Salland Engineering). Jan Martens (NXP-Hamburg) discussed contact mechanisms behind copper metallurgy effects for sort process and cleaning performance. The technical hurdles experienced during an RF-probe card and ATE hardware qualification were discussed by Mike Slessor, Ph.D., (MicroProbe); Mark Roos (Roos Instruments) with Roger Hayward (Cascade Microtech); and Daniel Watson (Teradyne). Several other presentations, such as those by James Tong (Texas Instruments) and Gordon Vinther (Ardent Concepts) reviewed the use of standardized methodologies within the development environment and transitioning to a production test floor. Overall, the technical program had 29 podium presentations with 65% from suppliers, 15% from semiconductor manufacturers, and 20% collaborative presentations from both manufacturers and suppliers.

Best Presentation was awarded to the collaborative team of Yuan Huang, Gary Liu, Thompson Hsu (United Microelectronics Corp.) and Wensen Hung, Cahris Lin, Dean Yang (MPI–Taiwan) for their comprehensive work on vertical cobra probing on low-k wafers; *Best Data Presented* went to the technical team of Wolfgang Schaefer, Ph.D. and Gunther Boehm (Feinmetall GmbH) that discussed various aspects of high temperature probing; *Best Presentation, Tutorial in Nature*, went to Gert Hohenwarter (GateWave Northern) for his overview on key issues for power delivery verification; the *Most Inspirational Presentation* was awarded to Jason Mroczkowski and Ryan Satrom (Everett Charles Technologies) for their detailed work on wafer level test hardware using a signal integrity simulation; and although there were many eligible candidates for the infamous "*Golden Wheelbarrow Full of Crap for the Poorest Disguised Sales Pitch*" this award was not inflicted. All the presentations (including the tutorials, keynote, technical program, and posters) from 2009 as well as previous workshops (1993 to 2009), are available on the newly redesigned SW Test website (http://www.swtest.org).

Technology EXPO 2009 had a total of 31 industry exhibitors and five Corporate Supporters (Advanced Probing Systems, Buckling-

Beam Solutions, Electro-Scientific Instruments, International Test Solutions, and JEM). During the EXPO, all aspects of the wafer sort industry and associated infrastructure suppliers were represented with twelve probe card vendors, major prober equipment manufacturers, probe card analyzer and probe process metrology companies, companies specializing in probe card cleaning, micro-pogo pin suppliers, and a variety of other probe related service providers.

The 20th Annual SW Test Workshop and EXPO will be held June 6 to 9, 2010, at the Rancho Bernardo Inn, San Diego, CA (http://www.ranchobernardoinn.com). Abstract submission for podium and poster presentations will be open starting January 1, 2010.

Technical Program Pictures:

Technology Expo Pictures:

CONFERENCES IN 2009:

2009 International Conference on Electronics Packaging Technology/ High Density Design, Packaging and Microsystem Integration (ICEPT/HDP 2009)
August 10-13, 2009 Beijing, China
Contact: icept2009@tsinghua.edu.cn

2009 IEEE International Conference on Portable Information Devices (PORTABLE)
September 21-22, 2009 Anchorage, AK USA
http://www.ieeevtc.org/portable2009
Contact: Ephraim Suhir suhire@aol.com

2009 3rd International Conference on 3D System Integration (3DIC 2009)
September 28 – 30, 2009 San Fancisco, CA, USA
http://www.3dic-conf.org
Contact: P. Garrou pgarrou@rti.org

2009 31st Annual Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD 2009)
30 August – 4 September 2009 Anaheim, CA, USA
http://www.esda.org
Contact: Lisa Pimpinella lpimpinella@esda.org

2009 15th Int'l Workshop on Thermal Investigations of ICs and Systems (THERMINIC 2009)
October 7 – 9, 2009 Leuven, Belgium
http://cmp.imag.fr/conferences/therminic/therminic2009
Contact: Chantal Bénis-Morel, chantal.benis@imag.fr

2009 4th Int'l Microsystems, Packaging, Assembly and Circuits Technology (IMPACT 2009)
October 21-23, 2009 Taipei, Taiwan
http://www.impact.org.tw/2009/General/
Contact: Ms.Yaffy Liu service@impact.org.tw

2009 55th IEEE Holm Conference on Electrical Contacts (HOLM 2009)
Sept. 14-16, 2009 Vancouver, BC, Canada
http://www.ewh.ieee.org/soc/cpmt/tc1
Contact: Alicia Zupeck a.zupeck@ieee.org

2009 18th IEEE Electrical Performance of Electronic Packaging (EPEP 2009)
October 19-21, 2009 Portland, OR, USA http://www.epep.org
Contact: Kelly Sutton epd@engr.arizona.edu

2009 IEEE/CPMT Workshop on Accelerated Stress Test and Reliability (ASTR 2009)
October 7-9 2009 Jersey City, NJ USA;
http://www.ewh.ieee.org/soc/cpmt/tc7/ast2009/
Contact: Cheryl Tulkoff ctulkoff@austin.rr.com

2009 11th Electronics Packaging Technology Conference (EPTC 2009)
9-11 December 2009, Singapore
http://www.eptc-ieee.net/

2009 IEEE Electrical Design of Advanced Packaging & Systems Symposium (EDAPS 2009)
December 2-4, 2009 Hong Kong, China
http://www.edaps2009.org/
Contact: edaps2009@ee.cuhk.edu.hk

CONFERENCES IN 2010:

2010 60th Electronic Components and Technology Conference (ECTC 2010)
June 1 - 4, 2010 Las Vegas, NV, USA
http://www.ectc.net
Contact: Jean Trewhella, jeanmh@us.ibm.com

3nd Electronics Systemintegration Technology Conference (ESTC 2010)
September 13-16, 2010 Berlin, Germany
http://www.estc.biz/outlook_estc_2010/ Contact: Rolf Aschenbrenner, rolf.aschenbrenner@izm.fraunhofer.de

See the CPMT Society website for updates:

www.cpmt.org/conf

Student Chapter News:

Sumitted by Prof. Nihal Sinnadurai
Fellow IEEE, Fellow Institute of Physics, Fellow IMAPS, CEng, IEEE Distinguished Lecturer

An excellent CPMT Region 8 event (CPMT Hungary and Romania). TIE Galati, Romania.

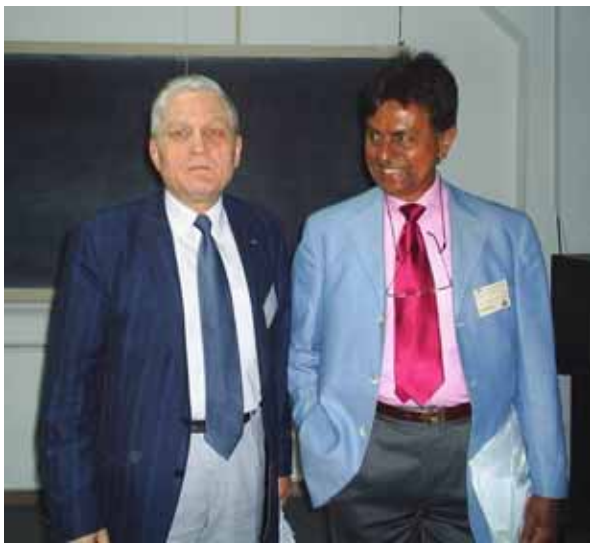
An innovative Electronics Interconnection Technology (TIE) Design competition was won by excellent students. Bogdan Raducanu was the top scoring student winner from the Polytechnic University of Bucharest. Others were not far behind

The TIE event on 9th and 10th April comprised two days of Workshops and a one day hands-on real-time competition for undergraduates in electronics.

The Workshops were discussion events with lectures by professionals intended to give students insight into the practicalities of the outside world. Two lectures from the Distinguished Lecturer Programme were given by Nihal Sinnadurai on the first day, one technical and the other on the benefits and opportunities from IEEE-CPMT membership. Some 70 people attended the workshops.

The excellent student competition followed the Workshop. Each undergraduate student competitor had to carry out a circuit design and layout project under time pressure. The design requirements were defined to the student competitors just before the competition began. Each student was provided with a computer with a suite of design software and a high definition colour screen. The students were required to develop a parts library, create component footprints, create a schematic and complete a layout. The adjudication was by small teams of experienced CAD designers plus anyone else who wishes to intervene, i.e. a fully transparent process. The event was very impressive and encouraged students in the electronics technologies relevant to CPMT.

Nihal Sinnadurai delivers the Distinguished Lecture



Paul Svasta, TIE Chair, and Nihal Sinnadurai

The competition under way

Some 39 students (both female and male) participated in the competition and I watched the impressive skills they displayed. The prizes to the top three were financial scholarships to support their ongoing education. All the funds received were from sponsors. Since then CPMT Society is also awarding a free one year CPMT Student membership to the winner.

The student winners: Third from left is Bogdan Raducanu who achieved the highest score. On the right is Prof. Paul Svasta who conceived the TIE competition and chairs the organizing team.

IEEE Fellow and Senior Member Grades:

Submitted by Dr. Vasudeva P. Atluri, IEEE CPMT Society Newsletter Editor

Fellow Grade:

An IEEE Fellow is a member of an elite group of global engineers with international recognition and known for their guidance and leadership in the world of electrical and electronic technology as it continues to evolve. The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

- Have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society.
- Hold Senior Member or Life Senior Member grade at the time the nomination is submitted.
- Have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.
- IEEE affiliate membership does not apply.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow. Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors. All those elevated will receive a congratulatory letter, a framed certificate, and a Fellow pin.

The IEEE Fellow Committee actively seeks newsworthy Fellows. Do you want members to learn more about you? Do you have something interesting that you want to share? If so, please forward your story to fellows@ieee.org. The IEEE Fellow Committee will contact you if your article will be featured in any IEEE publications.

Nominations for the IEEE Fellows class of 2011 are now open. While there are three methods of submission, IEEE highly recommend and urge your using the Electronic Fellow Nomination Process (EFNP). Thank you for participating in the nomination program.

Visit www.ieee.org fo additional information related to IEEE Fellow Program.

Senior Member Grade:

Senior Member is the highest grade for which IEEE members can apply. To be eligible for application, candidates must:

- Be engineers, scientists, educators, technical executives, or originators in IEEE-designated fields.
- Have experience reflecting professional maturity.
- Have been in professional practice for at least ten years.
- Show "significant performance" over a period of at least five of their years in professional practice.

Benefits of Senior Membership:

- Recognition: The professional recognition of your peers for technical and professional excellence.
- Senior Member Plaque: Since January 1999, all newly elevated Senior Members have received an engraved Senior Member plaque to be proudly displayed for colleagues, clients and employers to see. The plaque, an attractive fine wood with bronze engraving, is sent within six to eight weeks after elevation.
- US$25 Coupon: IEEE will recognize all newly elevated Senior Members with a coupon worth up to US$25. This coupon can be used to join one new IEEE Society. The coupon expires on 31 December of the year in which it is received.
- Letter of Commendation: A letter of commendation will be sent to your employer on the achievement of Senior member grade (upon the request of the newly elected Senior Member).
- Announcements: Announcement of elevation can be made in Section/Society and/or local newsletters, newspapers and notices.
- Leadership Eligibility: Senior Members are eligible to hold executive IEEE volunteer positions.
- Ability to Refer Other Candidates: Senior Members can serve as a reference for other applicants for Senior Membership.
- Review Panel: Senior Members are invited to be on the panel to review Senior Member applications.

Requirements for Senior Member Grade:

IEEE Bylaw I-104.3 sets forth the criteria for elevation to Senior Member grade as follows:

- A candidate shall be an engineer, scientist, educator, technical executive or originator inIEEE-designated fields.
- Candidates shall have been in professional practice for at least ten years.
- Candidates shall have shown significant performance over a period of at least five of those years.

In addition, candidates for Senior Member grade must supply three references from current IEEE members holding the grade of Fellow, Senior Member, or Honorary Member.

IEEE-designated Fields are Engineering, Computer sciences and information technology, Physical sciences, Biological and medical sciences, and Mathematics.

Ten years of professional experience:

The ad hoc Admission and Advancement (A&A) Review Panel that is evaluating your application will count the years you have been in professional practice. Your educational experience is credited toward that time as follows:

- 3 years for a baccalaureate degree in an IEEE-designated field.

- 4 years if you hold a baccalaureate and masters degree.
- 5 years if you hold a doctorate.

Five years of significant performance:
Many prospective applicants make the mistake of assuming that "significant performance" requires special awards, patents or other extremely sophisticated technical accomplishments; such is not the case. Substantial job responsibilities such as team leader, task supervisor, engineer in charge of a program or project, engineer or scientist performing research with some measure of success (papers), or faculty developing and teaching courses with research and publications, all are indications of significant performance well as the following:

- Substantial engineering, responsibility or achievement.
- Publication of engineering or scientific papers, books, or inventions.
- Technical direction or management of important scientific or engineering work with evidence of accomplishment.
- Recognized contributions to the welfare of the scientific or engineering profession.
- Development or furtherance of important scientific or engineering courses that fall within the IEEE designated fields of interest.
- Contributions equivalent to those of the above in such areas as technical editing, patent prosecution or patent law, provided these contributions serve to advance progress substantially in IEEE designated fields.

Significant performance that would serve to qualify an individual for elevation to Senior Member need not have occurred in the years immediately prior to the application. Thus, life and retired members are eligible for elevation.

References:
The applicant must also provide three references from current IEEE members holding Senior Member, Fellow or Honorary Member grade. Your professional colleagues are your best source of these references. If you have difficulty in locating Senior Members or Fellows to serve as references you have three options listed at www.ieee.org.

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Join the IEEE and the CPMT Society Today!!! Learn more at www.ieee.org and www.cpmt.org. IEEE and CPMT Society are offering a World of Opportunities and are making a World of Difference. The benefits include access to Peer-Reviewed Journals Dedicated to Members' Field of Interest; CPMT Society Quarterly Newsletter; Dynamic Worldwide Conferences, Workshops, and Symposiums; Educational Opportunities; Active Local Chapters; Technical Committees; IEEE Xplore® online journals; Prestigious Awards Program; IEEE Fellows Program; and Members-Only Web Page.

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CALL FOR PAPERS

Special Section on Solid-State Lighting Technologies

IEEE Transactions on Components and Packaging Technologies

In the 19th century, one of the most important inventions in terms of changing how people lived and worked was the incandescent light bulb. Starting in 1802 with Sir Humphry Davy's first demonstration of incandescent light, it took over 100 years of research before evolving into the incandescent light bulbs that we have today, and there are countless numbers of them in use in homes, cars, traffic lights, and commercial buildings all around the world and in outer space. As the world becomes more conscious of energy usage, with lighting accounting for approximately 20% of the electricity use in developed countries, the inefficiencies of incandescent bulbs have led to significant governmental support for energy-saving alternatives. The U.S. Department of Energy hopes to reduce electrical consumption for lighting across the country by 50 percent by the year 2025. Some of the most recent LED technologies are given below.

www.lumination.com

www.cree.com www

lumileds.com

The future seems bright for solid-state lighting technologies. With lifetimes of 50,000 to 60,000 hours and light outputs of over 100 lumens per watt, solid-state lighting offers better performance than many other lighting technologies. It is expected that it will replace all of the lighting technologies during next decade. Their lack of hazardous materials, such as mercury or halogen gases, makes them a more environmentally friendly alternative to fluorescent lamps. However, they are currently high cost and unable to match the light output of high-wattage light bulbs due to temperature limits on the materials. Global efforts to make SSL technology affordable are underway. This includes LED chips, packaging, thermal management, driver electronics, fixtures, and integration.

While the 19th century was the time for development of the incandescent light bulb, the 21st century is the time for development of solid-state lighting for residential, commercial, and industrial applications. We would like to draw attention to the recent efforts in this technology by publishing a special section in the *IEEE Transactions on Components and Packaging Technologies*, dedicated to solid-state lighting.

Topics of interest include, but not limited to:

- LED chip/substrate technology
- Semiconductor material development
- Packaging
- Thermal management
- Light quality (CRI, CCT) improvement techniques
- Efficiency improvements
- Fixture technologies
- System electrical efficiency and ROI (return on investment)
- Reliability

These developments can be in any solid-state lighting technology field. Both academic and industrial scientists are encouraged to submit their recent findings relevant to SSL technology. Papers will go through a rigorous review process based on IEEE guidelines and selected papers will be published in the CPT Transactions. Manuscripts are to conform to the standard IEEE transactions format, which can be found at http://www.cpmt.org/trans/transepm-auth.html.

Manuscripts must be submitted on line at ScholarOne Manuscripts: http://mc.manuscriptcentral.com/tcpt-ieee:

1. If you have not submitted a manuscript to the CPMT Transactions before -- create a user account for yourself.
2. Enter your Author Center and follow steps for submitting your manuscript.
3. *IMPORTANT:* In the Cover Letter window – note "Manuscript is submitted for Special Section on Solid-State Lighting Technologies.

To be considered for this Special Section, papers should be submitted by no later than **September 30, 2009.**

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EPTC 2009 Singapore

11th Electronics Packaging Technology Conference
9th – 11th December 2009
Shangri-La Hotel Singapore

Mark Your Calendar for EPTC 2009

CALL FOR PAPERS

Selected Publication in IEEE

ABOUT EPTC

The 11th Electronics Packaging Technology Conference (EPTC 2009) is an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter and sponsored by IEEE CPMT Society.

EPTC 2009 will feature technical sessions, short courses/forums, an exhibition, social and networking activities. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world.

CONFERENCE TOPICS

You are invited to submit an abstract, presenting new development in the following categories:

- Advanced Packaging: Wafer level packaging, 3D integration, TSV (through Silicon Via), embedded passives & actives on substrates, flip chip packaging, RF-ID, 3D SiP, Packaging solutions for MEMS, MOEMS, NEMS, Automotive electronics, optoelectronics
- Interconnection Technologies: wire bonding technology, flip chip technology, solder alternatives (ICP, ACP, ACF, NCP), under bump metallurgy, 3D and TSV connections, microbump, substrate technology,
- Materials & Processes: Materials and processes for traditional and advanced microelectronic systems, 3D packages, MEMS, solar, green and biomedical packaging that enhance mechanical, thermal, electrical and optical performance as well as cost effectiveness.
- Modeling & Simulations: Electrical Modeling & Signal Integrity, Thermal Characterization & Cooling Solutions: Mechanical Modeling & Structural Integrity
- Quality & Reliability: Component, board and system level reliability assessment, interfacial adhesion, accelerated testing and models, advances in reliability test methods and failure analysis.
- Emerging Technology: Packaging solutions for solar photovoltaic applications, systems and packaging in the areas of bioelectronics such as biomedical, bioengineering, biosensors and electronics for medical devices; wearable electronics, organic/printable electronics; portable power supplies such as fuel cells; and other novel packaging.

IMPORTANT DATES

Submission of abstract	15th June 2009
Notification of Acceptance	1st August 2009
Submission of manuscript	1st October 2009

ABSTRACT AND PAPER SUBMISSION

Abstracts are solicited to describe original and unpublished work. The abstract should be at least 500 words and it must clearly state the purpose, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications and how the work enhances existing knowledge should be included in the abstract as well.

Authors must designate two appropriate categories (found under CONFERENCE TOPICS) for abstract review. All submissions must be in English and should be made via the online submission system found at http://www.eptc-ieee.net. The required file format is Adobe Acrobat® PDF or MS Word in one single file for each submission.

The abstracts must be received by 15th June, 2009. Authors must include their affiliation, mailing address, telephone and fax numbers, and email address. Authors will be notified of paper acceptance and publication instruction by 1st August 2009. The final manuscript for publication in the conference proceedings is due by 1st October 2009. Selected papers will be published in IEEE/CPMT journals.

OUTSTANDING TECHNICAL PAPERS

The conference proceeding is an official IEEE publication. Author(s) of Best Technical Paper and Best Student Paper will receive an award at the next conference.

CALL FOR SHORT COURSES

The conference program includes short courses which will be conducted by leading experts in the field. Details will be updated in the conference website and available in subsequent mailings. Proposals for short courses can be submitted to seungwook.yoon@statschippac.com.

CALL FOR SPONSORSHIP / EXHIBITION PARTICIPATION

A tabletop exhibition featuring suppliers of materials, equipment, components, software and service providers of the microelectronics and electronic assembly industries will be held during the conference. Potential exhibitors and sponsors may email secretariat@eptc-ieee.net for details.

General Chairs: Mr. James HOW / Mr. Yew Cheong MUI
Technical Chair: Dr. Seung Wook YOON

Organized by IEEE Reliability/CPMT/ED Singapore Chapter

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IEEE COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY SOCIETY

IEEE

2009 IEEE Electrical Design of Advanced Packaging & Systems Symposium

December 2-4, 2009 Hong Kong / ShenZhen, China

http://www.edaps2009.org/ Email: edaps2009@ee.cuhk.edu.hk

Call for Papers

The 2009 IEEE EDAPS Symposium

The Electrical Design of Advanced Packaging & Systems (EDAPS) has been the premier international signal integrity symposium in Asia region since 2002. The symposium consists of paper presentations, industry exhibitions, workshops and tutorials. The 2009 EDAPS will be jointly sponsored by The Chinese University of Hong Kong, Applied Science and Technology Research Institute (ASTRI), Innovation and Technology Commission of Hong Kong SAR Government and the IEEE Components, Packaging and Manufacturing Technology Society (CPMT).

The purpose of EDPAS Symposium is to enhance the technical awareness and technology collaborations in the Asia region specifically in the electrical designs of chip, package and system levels from design concepts, technical challenges to the modeling and EDA tools. The papers of the symposium not only address the current technical issues but also bring out the challenges facing to IC design, SiP/SoP packaging, EMI/EMC, and EDA tools. The symposium is a major venue for creating the opportunity for the researchers and practitioners from the diverse fields to exchange information and build up the network.

Venue

The 2009 EDAPS will be held in the spectacular campus of The Chinese University of Hong Kong during December 3-4, 2009. In order to promote the state-of-the-art technologies to the electronics-related industries in China, a one-day session consisting of technical tutorials and workshops will be held in Shenzhen, China on December 2.

Important Deadlines and Dates:

Print-ready 4-page Full Paper Submission (up to 4 pages in PDF format only)	10 August 2009
Paper Acceptance Notification	14 September 2009
Advanced Program Available on Website	31 October 2009

Symposium Chair:

Prof. Ke-Li Wu,
klwu@ee.cuhk.edu.hk

Symposium Co-Chair:

Prof. Erping Li,
eleliep@nus.edu.sg

Technical Program Committee Chair:

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Local Arrangement Committee Chair:

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Call for Papers www.edaps2009.org

2009 IEEE Electrical Design of Advanced Packaging & Systems Symposium

December 2-4, 2009 Hong Kong / ShenZhen, China

Key Topics of the 2009 EDAPS:

- Signal integrity topics including High-speed Digital Signal Integrity Modeling, Design, and Measurement;
- Power Distribution Network;
- System in Package (SiP)/System on Package (SoP) Design;
- High-performance Packaging for System on Chip (SoC);
- RF/Microwave Packaging for Wireless Communication and Mobile Phone;
- Interconnect Modeling, Simulation, and Measurement;
- Embedded Passives Modeling and Measurement;
- High-speed Channels Modeling and Measurement;
- EMI/EMC and Electromagnetic Modeling and Measurement;
- EDA Tools for Chip, Package, and Board Co-design and Simulation.

Guidelines for Paper Submission:

Authors are requested to submit a preliminary paper up to 4 pages in length, including title, author's affiliation, abstract, figures and references.

All submissions must be made through EDAPS2009 website: www.edaps2009.org and must be in electronic format (PDF).

A MS-Word template is available on the symposium website. No hardcopy submission will be accepted.

Symposium Program:

Tutorials:	2 December 2009
Plenary Speeches:	3 December 2009
Oral Presentations:	3 – 4 December 2009
Poster Presentations:	3 – 4 December 2009
Exhibition:	3 – 4 December 2009
Banquette:	3 December 2009

Call for Papers www.edaps2009.org

11th International Conference on Electronic Materials and Packaging (EMAP 2009) Penang, Malaysia

Dec. 1-3, 2009

The 11th Electronic Material and Packaging Conference (EMAP 2009) is an international event organized by the School of Mechanical Engineering, Universiti Sains Malaysia (USM), with technical co-sponsorship from the CPMT Society of IEEE. EMAP 2009 will feature short courses, technical sessions, and an exhibition.

This conference is an international forum of experts and researchers for the exchange, dissemination and discussion of state-of-the-art technologies and recent developments in electronic materials, packaging, manufacturing and assembly. Since 1999, EMAP has gained a reputation as a premier electronic materials and packaging conference in the Asia-Pacific region where most of the electronic packaging activities are taking place.

Experts from reputed industries like Intel, Silterra etc. and academicians from major universities will deliver keynote lectures. A table-top exhibition from suppliers of materials, equipments, components and software, and from service providers of electronics industry will be held at the venue of the conference.

For more information, and the full Advance Program (when posted), visit:

mechanical.eng.usm.my/EMAP2009

Visit EMAP the week before EPTC, in Singapore!

15th International Workshop on Thermal investigations of ICs and Systems

Leuven, Belgium -- 7-9 October 2009

THERMINIC Workshops are a series of events to discuss the essential thermal questions of microelectronic microstructures and electronic parts in general. These questions are becoming more and more crucial with the increasing element density of circuits packaged together and with the move to nanotechnology. These trends are calling for thermal simulation, monitoring and cooling. Thermal management is expected to become an increasingly dominating factor of a system's cost. The growing power dissipated in a package, and the mobile parts of Microsystems, raise new thermal problems to be solved in the near future necessitating the regular discussion by the experts in these fields. Finally, there is an increasing need for accurate assessment of the boundary conditions used in the analysis of electronic parts, which requires a concurrent solution of the thermal behaviour of the whole system.

This year THERMINIC will address in addition to the "traditional" thermal management problems, also stress and thermal-stress-related-reliability issues, both in micro- and opto-electronics fields. These issues, including various nanotechnology applications, are of significant importance and of high interest to the engineering community engaged in the field of thermal phenomena in "high-tech" systems.

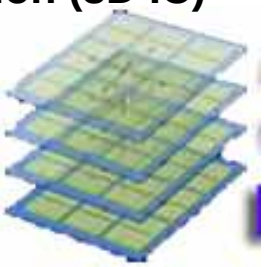
Leuven is a university town located 30km to the east of Brussels. The workshop is hosted at the Faculty Club, a unique conference and banqueting centre, welcoming guests to the calm and tranquility of the 13th century Infirmerie of the Grand Beguinage and the Convent of Chièvres, built in 1561.

For information, and to register:

cmp.imag.fr/conferences

IEEE International Conference on 3D System Integration (3D IC)

September 28-30, 2009 San Francisco



This conference combines the previous ASET and IEEE EDS Society sponsored **International 3D System Integration Conference**, held in Tokyo in 2007 & 2008, and the IEEE CPMT sponsored **3D System Integration Conference** held in 2005 & 2007 in Munich. The new, combined Conference will be held in San Francisco.

3D IC will cover all 3D IC topics, including 3D process technology, materials, equipment, circuits technology, design methodology and applications. The conference invites authors and attendees to submit and interact with 3D researchers from all around the world.

TOPICAL AREAS:

- 3D IC Technology
- 3D IC Circuits Technology
- 3D Applications
- 3D Design Methodology
- Test and Reliability of 3D Systems

To receive further information about 3D IC, or to register:

www.3dic-conf.org

ASTR 2009 Workshop on Accelerated Stress Testing & Reliability

October 7-9, 2009 Jersey City, NJ USA

The purpose of the ASTR Workshop is to share ideas on better ways of accelerating and detecting hidden defects, flaws, and weaknesses in electronic and electro-mechanical hardware that would result in failures during usage.

For more information:

www.ewh.ieee.org/soc/cpmt/tc7/ast2009

IEEE CPMT Symposium Japan

The VLSI Packaging Workshop in Japan (http://vlsi-pkg-ws.org/vlsi-pkg.html) has been held biannually since 1992 in Kyoto, and it has become a well-known international workshop for advanced packaging technologies. Due to ever increasing activities and changing demands, the committee has reviewed its mission, cooperated with the members of IEEE CPMT Japan Chapter, refurbished the workshop, and started the new symposium—IEEE CPMT Symposium Japan. It will provide component, packaging, and manufacturing researchers who are extending their activities beyond borders with opportunities to exchange technical knowledge and perspective. The committee strongly encourages you to attend this symposium and participate in the discussion, to understand the technology trends and find the best targets for your technology/business development. Bring your latest research results and share with the participants who are experts from the industry and the grove of Academe, and discuss with them. Anybody contributing to the achievement of a sustainable society through electronics is very welcome at this symposium.

Important information

- Submission of abstract: Feb. 15, 2010
- Notification of acceptance: Mar. 31, 2010
- Submission of manuscript: May 15, 2010
- Conference dates: Aug. 24, 25, and 26, 2010.
- Venue: The University of Tokyo, Japan

Technical area

+ System in a Package (SiP)
+ Advanced Fine Pitch Packaging
+ 3D Packaging & COC (Chip on Chip)
+ Wafer Level CSP
+ Packaging for Optoelectronics
+ Packaging for Automobile
+ RF Components & Modules / RF Tags
+ Integrated Passives / Embedded Components
+ Laminated Materials & Processing
+ Board level reliability
+ MEMS Packaging Technologies
+ Nano-Technology
+ Micro Bumping Technology
+ Electrical Performance & Thermal Management
+ Failure Mechanisms & Reliability Improvement
+ Materials for High Speed Application & Wafer Process
+ Green Material
+ Assembly and Packaging Challenges for Cu/Low-k Chips
+ Emerging Technologies

Contact person

General Chair: Hirofumi Nakajima, NEC Electronics Co. (hirofumi.nakajima@necel.com)
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Program Chair: Shigenori Aoki, Fujitsu Laboratories Ltd. (aoki.shigenori@jp.fujitsu.com)

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For more details:

www.cpmt.org/trans/

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Visit ieeexplore.ieee.org and download them

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Additional Information at www.cpmt.org/conf/

2009 IEEE Electrical Design of Advanced Packaging & Systems Symposium

December 2-4, 2009 Hong Kong / Shenzhen, China

The EDAPS has been the premier symposium on electrical designs at chip, module and system levels in Asia since 2002. The symposium consists of paper presentations, industry exhibitions, workshops and tutorials. The purpose of EDPAS is to enhance the technical awareness and technology collaborations in the Asia region specifically in the electrical designs of chip, package and system levels from design concepts, technical challenges to the modeling and EDA tools. The symposium provides a major venue for researchers and practitioners from the diverse fields to exchange information and for networking.

The EDAPS **online paper submission** is NOW on till 31 August 2009! We sincerely invite you and your colleagues or students to submit a paper and participate in this year's EDAPS. For details, please refer to the official website: **www.edaps2009.org**

In this year, EDAPS is to be held on December 2 in Shenzhen, China (for workshops and tutorials) and on December 3 and 4 in the spectacular campus of CUHK, Hong Kong, China.

The EDAPS has a wide technical coverage serving the communities of IC design, SiP/SoP packaging, EMI/EMC, and EDA tools, etc. All accepted papers will be included in IEEE Xplore and indexed by EI. Come to EDAPS 2009 to learn, to do business, to make new acquaintances and to network with old friends. See you in Shenzhen and Hong Kong in December 2009!

Important Dates:

Print-ready 4-page Full Paper Submission: 31 Aug. 09
Paper Acceptance Notification: 30 Sept. 09
Advanced Program Available on Website: 31 Oct. 09

The 2009 EDAPS is jointly sponsored by The Chinese University of Hong Kong, Hong Kong Applied Science and Technology Research Institute (ASTRI), Innovation and Technology Commission of Hong Kong SAR Government, and the IEEE Components, Packaging and Manufacturing Technology Society (CPMT).

SECOND FLEXIBLE ELECTRONICS SYMPOSIUM

DATE: Wednesday, August 19, 2009,
TIME: 7:30am - 4:45pm
LOCATION: Traditions at the Glen, Johnson City, NY

SPONSORS: BU Center for Advanced Microelectronics Manufacturing (CAMM); IEEE Components, Packaging and Manufacturing Technology Society (CPMT) -- Binghamton Chapter; Sandia National Laboratory; Cornell University

This symposium brings together leading researchers from academia, national labs, and industry in the fields of flexible electronics, functional printing, and emerging electronic materials to review and share new research findings in critical technology areas and identify issues for the rapidly growing flexible electronics field. It provides opportunities for discussion of key research and development areas and sharing of ideas and information. At the close of the technical agenda, attendees may tour the CAMM development facilities, a national research laboratory focusing on roll-to-roll electronics.

Symposium at a Glance

-- CAMM Research Program -- Industry-Academic Panel Discussion on Materials-Related Challenges in Flexible and Organic Electronics -- Industry Perspectives on Flexible Electronics Initiatives -- Pressure Sensors on Flex -- Stretchable Electronics -- CAMM Facility Tour (5:00-6:30 pm)

Technical events will be followed by an optional, no-host, Networking Dinner on the Binghamton University campus at 6:45pm ($30 fee). Registration is required for event attendence. No fee is required for attending technical events.

Information: **guest.cvent.com/EVENTS/Info/Agenda.aspx?e=60856a63-5f6b-44f0-addb-39e916f894d2**

COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

ECTC Electronic Components & RF Program Committee
CPMT RF & Wireless Technical Committee

60th ECTC June 1 – June 4, 2010

Paris Las Vegas Hotel

Las Vegas, Nevada USA

The ECTC Electronic Components & RF Program Committee and the CPMT RF & Wireless Technical Committee encourage you to submit an abstract to ECTC 2010 in the areas of passive components & networks, RF & Microwave components & modules, and subsystems. ECTC is the premier Electronic Components and Packaging conference held annually and attended by about 1000 delegates with equal participation from companies and academia. As in the past, Electronic Components, RF & Microwave, and MEMS related papers are solicited for focus sessions during this prestigious conference.

Discrete Passive Components

Design, materials, processes, and manufacturing considerations for discrete passive components: resistors, capacitors, inductors, and passive networks.

Integrated & Embedded Components

Design, materials, processing, modeling, manufacture, and characterization of integrated & embedded passive & active components on silicon, organic, ceramic, ultra-thin, and glass type substrates for digital, mixed signal, and RF applications; metamaterials, component integration for power converter modules.

RF & Microwave Components

Integrated antennas, filters, baluns, RFID/sensors, RF MEMS, MEMS, MEMS packaging, tunable devices and switches, high power and high efficiency RF/Microwave power amplifiers – design, technology and high frequency characterization

RF & Microwave Modules

Module Integration technologies in semiconductor, organic, and glass substrates – System in Package, System on Chip, Package on Package, and 3D integration; shielding and isolation

Materials, Processing, Reliability, & Manufacture of Electronic Components

Design, High permeability and high permittivity materials at high frequencies and their processing, yield and reliability aspects of electronic components, through silicon vias, wafer level RDL, and nanostructured materials and processes,

SUBMISSIONS:

Please submit abstracts using the ECTC web site: www.ectc.net by October 15, 2009. Abstracts must comply with the guidelines outlined at the website. To have your paper considered for inclusion in the "Electronic Components & RF" focused sessions

YOU MUST SELECT "Electronic Components & RF" *committee as your* ***PRIMARY*** *subcommittee preference* when you submit your abstract at the ECTC web site. Again, to have your paper considered for the electronic components & RF/microwave sessions, please do the following:

STEP #1: Submit abstract through the ECTC web site (www.ectc.net) and select **"Electronic Components & RF" as PRIMARY subcommittee** preference

STEP #2: Email abstract copy and author's email & contact information to: Craig Gaw at c.a.gaw@ieee.org & Amit Agrawal at amiagra2@cisco.com

Craig Gaw, Chair - CPMT RF & Wireless TC
Freescale Semiconductor Inc.
c.a.gaw@ieee.org

Amit P. Agrawal, Chair - ECTC Electronic Components & RF TC
Cisco Systems, Inc.
amiagra2@cisco.com

SEMI-THERM® 26

Semiconductor Thermal Measurement and Management Symposium
Hyatt Hotel, Techmart, Santa Clara, CA, USA
February 21-25, 2010

CALL FOR PAPERS

SEMI-THERM is the world's leading forum on the thermal management of electronics. For 25 years it has fostered the exchange of knowledge between practicing thermal engineers, professionals and industry experts, while showcasing the latest academic and industrial advances in electronics thermal management.

In its 26th year, SEMI-THERM will include Invited Speakers, Panel Sessions, Technical Sessions, Short Courses, an Evening Tutorial, Exhibits and dedicated Vendor Workshops. SEMI-THERM actively solicits student papers and awards travel stipends and reduced conference fees to student participants. Those papers deemed to be among the best in the conference will be invited to be published in the *IEEE Transactions on Components and Packaging Technologies.*

Subjects of Particular Interest

SEMI-THERM is soliciting papers on current thermal management technologies and practical application issues, modeling and measurement of electronic components and systems including, but not necessarily limited to, the following areas:

Component Level Thermal Management Die, Package	**Experimental Analysis** Liquid Cold Plates, Manifold Microchannels, DOE
System Level Thermal Management Boards, Enclosures	**Multidisciplinary Thermal Design** Acoustic interactions, Cost Trade-Off, Design for Reliability
Chip & System Packaging Materials TIMs, Heatspreaders, Nanomaterials, Material Characterization	**Datacenter Thermal Management** Metrics, Best Practices, Efficient Layout, Industry Trends
Modeling CFD, Compact Models, FEM/BEM, Novel Approaches	**Thermal-Aware Design** Energy Usage-optimized Designs, Leakage Power, CPU Power management, Airmover Control Technologies
Traditional & Enabling Technologies Conduction, Convection, Radiation, Air, Liquid, Two Phase, Vapor Compression/Refrigeration, Fans and Blowers, Solid State Airmovers,	**Application Environments** Consumer, High Volume, Portable, Harsh Environments, LED, Medical, Telecom, Automotive, Solar Photovoltaic, Military, Power and Storage Systems

The selection of papers for the Symposium is solely based on an extended abstract, which should provide a complete summary of the proposed paper comprised of work or results not previously presented or published. Submitted abstracts should be between 2 and 5 pages of single spaced text giving the key results, findings and conclusions, supported by additional pages of figures, tables and references as appropriate. **Abstracts are expected to demonstrate that the proposed papers are appropriate for SEMI-THERM and of high technical quality**. Abstracts must be submitted electronically in RTF, DOC or PDF formats via the SEMI-THERM web site.

The intent of technical papers is to communicate timely and relevant technical information to a technical audience. The paper should present an unbiased description of a certain method or product, discussing both pros and cons. Both subtle and blatant advertisement of any products or services is in direct conflict with the spirit of the Symposium. Examples of the former include repeated references to products or trade names and excessive use of corporate logos and trademarks in graphic illustrations. Photographs of commercial equipment are not permitted unless they add educational value. The SEMI-THERM Program Committee desires that all authors and presenters understand unambiguously that commercialism is inappropriate and will not be tolerated; authors are asked to abide by these constraints when preparing their abstracts, papers, and presentations.

Key Dates

Abstract Deadline	**Abstract Acceptance Notification**	**Photo-ready Full Manuscript Due**
August 17, 2009	October 10, 2009	December 17, 2009

For further information please contact the Program Chair via email:
Sai Ankireddi, Sun Microsystems Inc.
E-mail: sai.ankireddi@alumni.purdue.edu, Phone: 408-582-2231
Visit the SEMI-THERM web site at: http://www.semi-therm.org

IEEE Components, Packaging and Manufacturing Technology Society
Marsha Tickman, Executive Director
445 Hoes Lane
Piscataway, NJ 08854 USA

Future Directions in IC and Package Design Workshop (FDIP)

October 18, 2009, Portland, OR USA

Special Topic: What Research is Planned for EM Tools and How Are They Made Available to Computer Designers

FDIP includes 7 talks on key topics; see the Advance Program for the listing. FDIP is held immediately before EPEP – be sure to schedule this extra day into your travel plans! Register by September 20th, 2009

More information: **www.epeps.org**

CPMT and MTT Societies

18th Conference on Electrical Performance of Electronic Packaging (EPEP 2009)

October 19-21, 2009
Portland, Oregon USA

The general subject of EPEP is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. The goal is to be the leading conference dealing with advanced and emerging issues in electrical design of interconnect structures and assurance of Signal Integrity. Watch our website for this year's lineup of sessions and papers.

For full Conference details, please visit: **www.epep.org**

Visit our website
www.cpmt.org

Download the PDF version of this NEWSLETTER, to circulate to other professionals

www.cpmt.org/newsletter/

2009/2010 Deadlines for Submitting Articles:

August 25th, 2009 **November 25th, 2009**
February 25th, 2010 **May 25th, 2010**

Only Articles sent to nsltr-input@cpmt.org will be included in the newsletter

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