Components, Packaging, and Manufacturing Technology Society Newsletter

THE GLOBAL SOCIETY FOR MICROELECTRONICS SYSTEMS PACKAGING

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President's Column....

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I first began my career as packaging engineer with the Fraunhofer Gesellschaft in 1994 and joined the CPMT Society shortly thereafter. I believed then, as I do now, that professional associations such as ours are vital in the industry. The CPMT Society bridges the gap between theory and application, it encourages progress in the field by recognizing achievement and providing training, it advocates on behalf of its members, and provides ample opportunity for networking across geographic borders and cultural divides.

The crucial role played by our Society is never more necessary than in these difficult economic times. While in some sections of our industry, the tide has turned towards a "back-to-basics" approach, our work contributes to moving the industry forward, propelling it out of troubled waters by doing more, rather than less. As the premier international forum for scientists and engineers working in microelectronics, we provide a platform for developing and realizing innovative concepts and support the professional community by providing opportunities for information exchange, continuing education, and professional growth; we publish journals, sponsor conferences, and support local chapter and student activities. Not the least of our activities are our efforts to represent the microelectronic and microsystem packaging community as a whole and to serve as its advocate within the IEEE, the broader scientific and technical community, and society at large.

In fifteen years of membership in the CPMT Society, I have been involved at almost every level of the organization – briefly, I was a European representative on the Conference Advisory Committee,

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NEWSLETTER SUBMISSION DEADLINES:

15 August 2010
15 November 2010
15 February 2011
15 May 2011

Submit all material to nsltr-input@cpmt.org

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Refer to www.cpmt.org for CPMT Society Chapters and Student Branches list

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(www.cpmt.org/mem/)

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was committed to promoting membership and chapter development as part of globalizing the IEEE CPMT, and served as the Strategic Program Director of European Activities. From 2003 to 2005 I was Vice President (Technical) and from 2005 until my recent election to President I held the post of Vice President (Conferences).

The aims I have set for my term as President are by no means solely my own, but have synthesized over countless discussions with other CPMT Society members and board members. Over the remaining three and a half years, I hope to work together with you to create a new, broader vision for our Society's future. Crucially, we have to identify cutting-edge research opportunities and new application areas, and then further their progress with activities, workshops, conferences and publications. I am also pursuing four fundamental strategies to advance the Society's ability to provide high-quality products and services to our members: improving the effectiveness of the Society's organizational processes; reversing the negative membership trend by creating new value for our members; encouraging volunteer leadership; and continuing down the path of globalization in CPMT begun by past Presidents.

The first six months have already been very busy. Beyond preparing for the ECTC conference in Las Vegas in June, a lot of effort is going into the Electronics System Integration Technology Conference ESTC conference, to be held here in Berlin, Germany in September. Submissions have closed and the program committee is currently arranging 160 oral and 90 poster presentations into an exciting program. A total of 16 sessions in nine different system integration fields will be held, including some interesting tutorials. Keep an eye out for the advance program in mid-June, which will be posted on the conference website (http://www.estc-2010.de). Apart from the opportunity to participate in what we believe will be some truly inspiring research presentations, on a personal level I also hope the conference will be a chance for me to get to know more of our members. So please, join us for a perfect late summer conference at ESTC in Berlin and bring your ideas, comments and suggestions – anything at all that you feel will help us provide a better service to our members.

HERBERT REICHL RECEIVES 2010 IEEE COMPONENTS, PACKAGING & MANUFACTURING TECHNOLOGY AWARD

The IEEE Components, Packaging and Manufacturing Technology Award, sponsored by the IEEE Components, Packaging and Manufacturing Technology Society, recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies.

The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless and micro-electro-mechanical systems (MEMS), enhancement of technology, impact on the relevant technical community and the profession, benefit to society, and the quality of the nomination.

The 2010 Award was present to Dr. Herbert Reichl at the 60th Electronic Components and Technology Conference, 3 June 2010.

Herbert Reichl
Technical University of Berlin
"For contributions to the integration of reliability in electronics systems, and leadership in research and education in electronics packaging."

Herbert Reichl was one of the first researchers to foresee the importance of microelectronics packaging in bridging the gap between research and applications.

His pioneering work on heterogeneous integration, three-dimensional packaging, and embedded passive and active components set the path for future microelectronics, enabling applications ranging from mobile phones to wearable sensors.

As founding director of Germany's Fraunhofer Institute for Reliability and Microintegration (IZM), Dr. Reichl has led many integration strategies and shepherded their transfer to commercialization.

The exciting concept of electronic grains (or eGrains) is just one example. Functioning as tiny electronic sensors that can receive, process, and store information, eGrains are very small, autonomous modules that can communicate with each other wirelessly, enabling "smart" devices.

Dr. Reichl is currently a professor at the Technical University of Berlin, Germany, and continues to mentor generations of students and research staff in the area of R&D.

Dr. Reichl joins the following past recipients of this Award.

2009 – George G. Harman
"For achievements in wire bonding technologies."

2008 – Karl Puttlitz Sr. and Paul A. Totta
"For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages"

2007 – Dimitry Grabbe
"For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards."

2006 – C. P. Wong
"For contributions in advanced polymeric materials science and processes for highly reliable electronic packages."

2005 – Yutaka Tsukada
"For pioneering contributions in micro-via technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process."

2004 – John W. Balde
"For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing."

CONGRATULATIONS TO 2010 CPMT AWARD WINNERS

The CPMT Society annually recognizes individuals for contributions to the profession through technical achievements, service to the industry and to the Society. The following individuals received their awards at the 60th Electronic Components and Technology Conference, 3 June 2010.

David Feldman Outstanding Contribution Award is given to recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions. The 2010 recipient:

William Chen, ASE US
For leading the CPMT Society in defining its value propositions and executing strategic outreach to CPMT stakeholders in the major microelectronics development and manufacturing regions around the world.

Outstanding Sustained Technical Contribution Award is given to recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society. The 2010 recipient:

Frank Shi, University of California, Irvine
For his accomplishments in multiple fields including optoelectronic packaging technology development, device and packaging materials development, electronic packaging and manufacturing technology development; and his leadership in the technology transfer of these developments from a research environment to an industrial commercialization and production environment.

Exceptional Technical Achievement Award is given to recognize an individual, or group of individuals for exceptional technical achievement in the fields encompassed by the CPMT Society. The 2010 recipient:

Michael Pecht, University of Maryland
For his seminal contributions in the area of electronics reliability from which he developed the new and significant field of prognostics for electronics.

Electronics Manufacturing Technology Award is given to recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society. The 2010 recipient:

Ning-Cheng Lee, Indium Corporation of America
For being a driving force in removing the 'art' of SMT assembly and replacing it with science.

Outstanding Young Engineer Award is given to recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation. The 2010 recipient:

Shaw Fong Wong, ATD-Malaysia
For his contributions in the area of component level solder joint reliability for flip chip packaging, as well as his development of a reliability degradation model for thermal interface materials.

CPMT Society News....

E-MAIL ALIAS AND IEEE WEB ACCOUNT NEEDED 2010 CPMT SOCIETY BOARD OF GOVERNORS ELECTION ON-LINE

In order to vote in this year's CPMT Board of Governors election, members will need to have a valid e-mail alias on record with IEEE and also have an IEEE Web Account.

Eligible voting members will receive notification by e-mail in the Fall of this year with instructions for voting on-line. You will need an IEEE Web Account to access the ballot and cast your vote. This Web Account is the same one you may use for IEEE services such as renewing membership and accessing IEEE Xplore.

If you do not recall your Web Account username and password, or aren't sure whether you have established an account, please go to http://www.ieee.org/web/accounts to recover your password or establish a new account.

Please be sure to update your IEEE membership record with you current e-mail alias. If you DO NOT HAVE AN E-MAIL address or would prefer to receive a paper ballot by mail, please send your name, mailing address and IEEE Member Number by 20 August to:

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Publication News....

CPMT to Merge Transactions in 2011

At the November Board of Governors (BoG) meeting, VP of Publications, Wayne Johnson proposed merging CPMT's three transactions: *Transactions on Advanced Packaging, Transactions on Components and Packaging Technology and Transactions on Electronics Packaging Manufacturing* into a single transactions. The BoG approved the proposal. The new transaction will be titled: *Transactions on Components, Packaging and Manufacturing Technology*.

The proposal was motivated a recommendation from the IEEE Technical Activities Board (TAB) review of CPMT publications in November of 2007 to merge the CPMT Transactions. The primary observation made by the TAB review committee was the lack of clear and distinct identities for the three current Transactions. How did authors and readers know which Transactions covered which topical areas? The CPMT Publications Committee reviewed this recommendation. While each Transaction listed topical areas on the CPMT web site to aid authors, there was significant overlap between the lists for the three Transactions. A further review of published issues verified published papers in one Transaction that ideally would have been expected in one of the other Transactions. While the Editors-in-Chief did, on occasion, recommend to the author their manuscript be transferred to another Transactions, manuscripts are nearly always published in the Transactions the author initially selects.

The original idea to create three separate Transactions was to provide publications for communities of technical interest. Today, however, many readers access papers online. Using IEEE Xplore, a reader can search all three Transactions, as well as other IEEE publications for topics of interest. The benefit of three publications has decreased over time.

During 2010, we will continue publishing the three existing Transactions; no changes to the process will be made. Manuscripts in the review cycle that are not published in 2010, will be published in the new T-CPMT starting with the January 2011 issue.

Working with the CPMT Publications Committee, a plan for seamlessly implementing the *Transactions on Components, Packaging and Manufacturing Technology* in January of 2011 has been outlined. The new Transactions will have Sections that will segregate manuscripts into topical areas within each issue. The concept of having multiple Sections in one Transactions will give us the flexibility to add a Section if a new topic of interest emerges and to drop a Sections if interest (manuscripts) in the topic declines without having to change the name of the Transactions in the future. Each topical area will have a Co-Editor-in-Chief (Co-EiC) responsible for that Section. Authors will select the most appropriate Section when submitting their manuscript. This is the existing process for T-ADVP and T-CPT. The Co-EiC for that Section will review the manuscript for appropriateness to their Section before moving it to the Associate Editors who will manage the review process. Co-EiCs may recommend the manuscript be transferred to another Section if more appropriate. Currently, we have five EiC's (two for T-ADVP, two for T-CPT and one for T-EPM). While the number and name of the Sections have not been determined at this point, it is expected the current EiCs will transition to Co-EiCs responsible for a specific Section in the new T-CPMT. The current Associate Editors (AEs) will also transition with their current EiCs to the new Sections. AEs will have the opportunity to move to other Sections based on their technical interests if they chose. We will also be soliciting new AEs. We also plan to retain our current Reviewers and to increase their number.

We currently publish the three Transactions each on a quarterly basis, resulting in 12 total issues per year. For the merged Transactions, we will publish monthly online issues and combine two months of online content into the print edition for six print issues per year. Online publication of each manuscript occurs as soon as the manuscript is completed for the paper issue and does not wait for the entire issue to be completed and printed.

In the transition, we must address the important topic of Impact Factor. Impact factor is a measure of the average number of citations to the number of manuscripts published in a technical journal. The citations counted in the calculation are references to papers published in the last two years. With the creation of a new title, T-CPMT, we will not have a reported Impact Factor for two years. However, since T-CPMT is a consolidation of the T-ADVP, T-CPT and T-EPM, the effective Impact Factor of T-CPMT during its first year will be a composite of the Impact Factor for the three Transactions. During the second year of publication, T-CPMT will have an Immediacy Factor published by Thomson Reuter and T-ADVP, T-CPT and T-EPM will still have an Impact Factor published. Thomson Reuter will assist us in calculating an effective Impact Factor for T-CPMT based on a calculation of these numbers. Finally, in year three, T-CPMT will have its own Impact Factor based on two years of publication history. The CPMT Society will be pro-active during the first two years in providing an effective Impact Factor for T-CPMT and justification of its acceptance. While Impact Factor was a major concern and consideration in merging the Transactions, the consensus was the benefits outweighed the risk. By selecting T-CPMT as the new title and managing emerging technologies as new Sections without changing the publication title, we believe this will be the last title change needed unless the Society changes its name.

The CPMT Publications Committee will work to make the transition as smooth as possible and continue to increase the prestige and usefulness of the Society's publications. Your comments, suggestions and recommendations are always welcome. Please contact Wayne Johnson at rwjohnson@ieee.org.

2009 CPMT Best Transactions Paper Awards

Each year, the Editors of the three CPMT Society Transactions select the best papers published in the prior year. The papers are selected from among nearly 300 published papers and represent the best, based on criteria including originality, significance, completeness and organization.

2009 Transactions on Components and Packaging Technologies Best Paper

"Effect of Permittivity and Permeability of a Flexible Magnetic Composite Material on the Performance and Miniaturization Capability of Planar Antennas for RFID and Wearable Wireless Applications" by Lara J. Martin, Member, IEEE, Sooliam Ooi, Senior Member, IEEE, Daniela Staiculescu, Member, IEEE, Michael D. Hill, C. P. Wong, Fellow, IEEE, and Manos M. Tentzeris, Senior Member, IEEE, VOL. 32, NO. 4, December 2009.

This paper is an investigation of the feasibility of applying a mechanically flexible magnetic composite material to radio frequency identification (RFID) planar antennas operating in the lower ultrahigh-frequency (UHF) spectrum (~300500 MHz). A key challenge is that the magnetic loss introduced by the magnetic composite must be sufficiently low for successful application at the targeted operating frequency. A flexible magnetic composite comprised of particles of Z-phase Co hexaferrite, also known as Co_2Z, in a silicone matrix was developed. To the authors' knowledge, this is the first flexible magnetic composite demonstrated to work at these frequencies. The benchmarking structure was a quarter-wavelength microstrip patch antenna. Antennas on the developed magnetic composite and pure silicone substrates were electromagnetically modeled in Ansoft High-Frequency Sounder System full wave electromagnetic software. A prototype of the antenna on the magnetic composite was fabricated, and good agreement between the simulated and measured results was found. Comparison of the antennas on the magnetic composite versus the pure silicone substrate showed miniaturization capability of 2.4 times and performance differences of increased bandwidth and reduced gain, both of which were attributed in part to the increase in the dielectric and magnetic losses. A key finding of this paper is that a small amount of permeability (mu_r~2.5) can provide a substantial capability for miniaturization, while sufficiently low-magnetic loss can be introduced for successful application at the targeted operating frequency. This magnetic composite shows the capability to fulfill this balance and to be a feasible option for RFID, flexible wearable, and conformal applications in the lower UHF spectrum.

2009 Transactions on Advanced Packaging Best Papers (co-recipients)

"Fast Methodology for Determining Eye Diagram Characteristics of Lossy Transmission Lines" by Wei-Da Guo, Jeng-Hau Lin, Chien-Min Lin, *Member, IEEE,* Tian-Wei Huang, *Senior Member, IEEE*, and Ruey-Beei Wu, *Senior Member, IEEE*, VOL. 32, NO. 1, February 2009.

As the speed of signal through an interconnection increases toward the multigigabit ranges, the effects of lossy transmission lines on the signal quality of printed circuit boards becomes a critical issue. To evaluate the eye diagram and thus the signal integrity in the modern digital systems, this paper proposes a fast methodology that employs only two anti-polarity one-bit data patterns instead of the pseudo-random bit sequence as input sources to simulate the worst-case eye diagram. Analytic expressions are derived for the impulse response of the lossy transmission lines due to the skin-effect loss, while the Kramers-Kronig relations are employed to deal with the noncausal problem related to the dielectric loss. Two design graphs that can be used to rapidly predict the eye diagram characteristics versus the conductive and dielectric losses are then constructed and based on which, the maximally usable length of transmission lines under a certain signal specification can be easily acquired. At last, the time-domain simulations and experiments are implemented to verify the exactitude of proposed concept.

"Through-Silicon via Interconnection for 3D Integration Using Room-Temperature Bonding" by Naotaka Tanaka, Yasuhiro Yoshimura, Michihiro Kawashita, Toshihide Uematsu, Chuichi Miyazaki, Norihisa Toma, Kenji Hanada, Masaki Nakanishi, Takahiro Naito, Takafumi Kikuchi, and Takashi Akazawa, VOL. 32, NO. 4, November 2009.

One approach to 3D technology is chip stacking using through-silicon vias (TSVs). Interconnects in a 3D assembly are potentially much shorter than in a 2D configuration, allowing for faster system speed and lower power consumption. However, it is extremely important to use cost-effective process technologies in practical use. Therefore, in our study, we propose a basic concept for interconnecting stacked chips with TSVs using a cost-effective process technology. The principal feature is to use a ldquomechanical-caulkingrdquo technique, which has been used widely in the mechanical-engineering field, enabling 3D interconnections between stacked chips. This makes it possible to interconnect them by only applying compressive force at room temperature. This paper presents the results obtained by using mechanical-caulking connections at room temperature accomplished by manufacturing a prototype of a chip-stacked package with TSV interconnections. A 3D-SiP composed of an existing MCU, an interposer, and an SDRAM chip with TSV interconnections was also manufactured. However, a customized design, assuming TSV interconnections in the existing MCU, needs to be introduced for practical use to achieve SiO_2 etching with shorter turn around time (TATs) and high TSV yields of more than 99%.

2009 Transactions on Electronics Packaging Manufacturing Best Paper

"Fabrication of Molded Interconnection Devices by Ultrasonic Hot Embossing on Thin Polymer Films" by Puttachat Khuntontong, Thomas Blaser, and Werner Karl Schomburg, VOL. 32, NO. 3, July 2009.

Ultrasonic hot embossing allows fabrication of metal patterns onto a polymer film with a low cost and rapid process. A polymer layer with a thin metal film on top is welded onto the polymer

substrate where there are protruding micro structures on the tool. Edges around the protruding structures cut the metal layer and ensure electrical insulation. The entire process performs in a few seconds. The non-welded areas are mechanically removed after this process. An antenna of a radio frequency identification device (RFID) and a flexible membrane keyboard were fabricated by embossing 10-mum-thick conductive paths from an aluminum foil onto polypropylene films, 150 and 250 mum in thickness. Antenna circuits have been proven to show the expected resonance frequencies and the keyboard was successfully employed as an input device for a PC.

The awards were presented at the 60th Electronic Components and Technology Conference (ECTC), on 3 June 2010.

Subscribers to these publications can access the papers on-line in IEEE Xplore at: http://ieeexplore.ieee.org/xpl/browsePopular.jsp. Members can add the subscriptions to their membership at: https://sbwsweb.ieee.org/ecustomercme_enu/start.swe?SWECmd=Login&SWECM=S&SWEHo=sbwsweb.ieee.org

Chapter News....

TIE Event – Students' Contest

(submitted by Andreea Bonea, Press Officer of IEEE CPMT Student Branch Chapter of the Politehnica University of Bucharest, Romania andreea.bonea@cetti.ro)

The increasingly popular students' contest: Interconnection Techniques in Electronics (TIE-www.tie.ro) took place in April, between 14th and 17th. The beautiful town of Cluj-Napoca, Romania, was home of the 19th edition. The IEEE-CPMT Student Branch Chapter of the "Politehnica" University of Bucharest, Romania (Advisor Professor Paul Svasta) is involved together with the IEEE-CPMT Hu&Ro Joint Chapter in organizing this event and takes full credit for training the participants. In fact the Chapter promotes in our region many activities according with IEEE CPMT Society goal. Together with TIE event, another long tradition event is the SIITME Conference (www.siitme.ro), conference which will take place in fall's time.

The TIE Event is a major project our Chapter holds on annual basis and has become tradition for the technical academic environment in the area. For several years, it has promoted CAD design for Electronic Packaging with member universities of EPETRUN (Electronic Packaging Education Training University and Research Network).

The aim of this competition is to accustom students with the real requirements of the industrial and business environment. The selection of the participants takes place in stages, having both an initial local and a final stage. The best three participants from each university center are selected at the local stage and they will meet with other future engineers at the final stage.

The topics of the contest cover all fields of PCB CAD from parts and footprint creation, to designing schematic projects and developing optimal layouts according to various industrial restrictions (with special placement, routing and finishing issues), ending with post-processing output files. The Technical Committee (Director Dr. Norocel Codreanu) develops the up-to-date topics and assures also, with the help of Organizing Committee, that the contest takes place in a fair-play climate. Great care is given to creating a genuine climate of collegiality and respect between the competitors and also a transparent competition, which would leave no doubt regarding the correctness.

The contest in the final stage is a 4 hours challenge with requirements similar to the ones in industrial projects under time pressure. The Industrial Advisory Committee not only evaluates the correspondence of the requirements with the demands of the business environment, but also gives valuable feedback as it sets the line, at the end of the evaluation process, above which are located the people with real skills of professionals in the field of printed wiring design, who are recommended as PCB designer. This competition is recognized by employers as a certification of the participants' knowledge level.

(left to right) Prof. Zsolt Illyefalvi-Vitez, IEEE-CPMT Hu&Ro Joint Chapter, Vice-chair, Budapest University of Technology and Economics, Hungary, Prof. Dan Pitică, IEEE-CPMT Hu&Ro Joint Chapter Chair, Technical University of Cluj-Napoca, Romania and Prof Paul Svasta, "Politehnica" University of Bucharest, Romania.

Brainstorming session of the technical committee for creating the proposed subject for the 19th edition.

The results are evaluated by a team of professors following a clear grid of scores, which helps making the evaluation process as objective as possible. The design in Schematics and in Layout is highlighted: The proper separation of analog and digital ground layers are important issues, but attention is paid especially to the problems that could appear in the actual practical PCB design phase: the signals and high speed routes integrity for multiple layers in printed circuit boards.

Various types of CAD software can be used as long as the requirements are met. The students are not only provided with the specifications but also with datasheets for the parts that they have to create. Before the official start of the contest, the competitors have approx. 15 minutes to study carefully the design requirements and to understand the main ideas of the subjects, the inputs and the outputs. Then, during the contest time, they must take the optimal decisions in order develop and finish the electronic project (correct and functional), being finally ready for manufacturing.

TIE Awards Session. From left to right: Prof. Dan Pitică (Steering Committee Co-chair), Prof. Nihal Sinnadurai (IEEE Distinguished Lecturer), Tudor Dungă 1st Prize Winner - "Politehnica" University of Timişoara, Lect. Marius Rangu, Ph.D. - Representative of the "Politehnica" University of Timişoara, Zamfir Pică 2nd Prize Winner - Technical University of Cluj-Napoca, Péter Gross 3rd Prize Winner University of Technology and Economics, Budapest, Prof. Paul Svasta (Chair of the TIE Steering Committee).

The first three ranked students received a 10 months scholarship. Additionally, the winner of the TIE contest, Tudor Dungă, was awarded by CPMT Society with a full year IEEE CPMT Membership. CAD software providers also gave prizes for the students who had valuable results using the software they provide. Also two winners' cups were also awarded; the first was given to the winner to keep, while the second was given to the winner's university. The latter cup is transmissible from one year to another, now held by a previous winner of TIE, PhD Marius Rangu, who represents the "Politehnica" University of Timişoara.

The subjects and evaluation were done in English and an important role was held by the consultants in Europe, prominent personalities in promoting education and training activities in electronic packaging, whose presence is highly motivational for the students as well as for the organizers.

During the workshop taking place before the contest Professor Nihal Sinnadurai, IEEE Fellow, IEEE Distinguished Lecturer has presented to the participants the place of IEEE in the professional world and how important it is for the young students to join the community.

The aim of the TIE event is to help in the process of training young professionals, enable them to acquire skills and competences and become familiar with the requirements of the industry during their academic training. The fact that the contest has an international prestige means that all students who reach the final stage are, in a sense, winners as they had the opportunity to become familiar with a challenging project which surely represents a good starting point for their future professional life.

Through the TIE event we aim to train well-prepared professionals who will be competitive and proficient at the standards of the international market with valuable skills and knowledge.

We wish the participants all the best until the next year edition in Bucharest, Romania 13th–16th of April!

Participants to the TIE event.

SANTA CLARA VALLEY CHAPTER SUPPORTS MICROMOUSE

Your IEEE-SCV-CPMT Chapter contributed the $500 Region 6 Central MicroMouse Best Packaging award for 2010, as we have in the last several years. The 2010 MicroMouse competition was held at Stanford University. The judges were Oscar MahinFallah and Ed Aoki, with experience and support and equipment provided by Allen Earman. All 6 packaging entries were from the University of Hawaii, Manoa. The winning entry was White Mouse by Mitchell LaPuente. The 2nd place winner was Bosavi with team leader, Shane Sunada and team members, Malcolm S Menor, Joshua Miyamoto and Joseph Longhi. The 3rd place winner was "7-Year-Plan" with team leader, Louis Ridley and team member, Christopher Yoshizaki.

The MicroMouse Maze Time contest 1st place $500 winner was C2JRat from UC-Davis with team leader, Bob Miller and team member Kevin Stumpfa. No photo available. The 2nd and 3rd place prizes awarded by Region 6 were $300 and $200.

1st Place – White Mouse.

White Mouse - Mitchell LaPuente.

2nd Place – Bosavi.

Bosavi Team leader, Shane Sunada (Right) and team member Malcolm S Menor (Left).

3rd Place – 7-Year-Plan.

7-Year-Plan Team leader, Louis Ridley (Left) and team member, Christopher Yoshizaki.

Conference News....

The 60th Electronic Components and Technology Conference (ECTC) was the Display of the Industry Bounce-back in Las Vegas, NV, USA

A Big Thanks to the Executive Committee of the 60th ECTC! (from left to right; front row: Senol Pekin Jean Trewhella, David McCann, Rao Bonda, back row: Eric Perfecto, Rajen Dias, Steve Bezuk, Wolfgang Sauter, Patrick Thompson C. P. Wong, not shown: Lisa Renzi, Kitty Pearsall, and Torsten Wipiejewski).

At the 60th ECTC in Las Vegas, NV, USA, the electronic components industry showed a spectacular bounce-back from last year's worldwide recession and the swine flu worries. With more than 600 abstracts received and an acceptance rate of ~50%, ECTC continued to be the prime technical conference in the industry.

Percentage of papers submitted from Asia kept increasing to 39% in 2010 from 37% in 2009. Share of US papers increased to 47% from 46%, and share of European papers decreased to 14% from 17%. Percentage of corporations in paper affiliations increased 40% from 36%, but was lower than the 48% recorded in 2008.

With 844 attendees (compared to 551 in 2009), the semiconductor industry proved to be in a strong year. The 345 (compared to 185 in 2009) Professional Development Course (PDC) attendees, 65 exhibitors (compared to 52 in 2009), and 20 sponsors were further proof that the semiconductor industry has been bouncing back from the recession.

On Tuesday, 345 attendees attended 16 professional development courses (PDCs). The courses were organized by the PDC Committee chaired by Kitty Pearsall of IBM.

TUESDAY

The ITRS Assemblies and Packaging Technology Committee meeting took place in parallel to PDCs.

At night, ECTC Panel Discussion on "The Emergence of the Medical Devices Industry through the View-glass of Microelectronic Packaging Innovation" chaired by Rolf Aschenbrenner of Fraunhofer IZM attracted the attention. Conference attendees had an opportunity to listen to Herbert Reichl Fraunhofer IZM,

In addition to technical sessions, the conference was enhanced by PDCs, 10 new exhibitors, luncheons, ruffle drawings, evening receptions, best paper awards, ECTC Panel Discussion chaired by Rolf Aschenbrenner of Fraunhofer IZM, Plenary Session co-chaired by Mark Poliks of Endicott Interconnect Technologies and Jan Vardaman of TechSearch International, and CPMT Seminar co-chaired by Yoshitaka Fukuoka of Westi and Kishio Yokouchi of Fujitsu Interconnect Technologies.

In the evening, students attended the ECTC Student reception hosted by Eric Perfecto of IBM Corporation, where they had an opportunity to learn about how the technical subcommittees work to select the abstracts.

Session chairs and speakers, on the other hand, got together at the General Chair's Reception.

Jan Vardaman of TechSearch International, Dongkai Shangguan of Flextronics, and Robert Hitchcock of University of Utah.

WEDNESDAY

General Chair Jean Trewhella hosted the program subcommittee chairs and assistant chairs in her suite and thanked them for their leadership in selecting the 300+ technical papers out of 600+ abstracts which was the second highest number of abstracts in the ECTC history.

Technical sessions started on Wednesday, and ran through Friday, 8:00 AM to 5:00 PM every day. Speakers and session chairs met at breakfast to prepare for the sessions.

Coffee breaks created the opportunity for networking and exchanging information among the conference attendees.

Dr. Tien Wu, Chief Operating Officer of Advanced Semiconductor Engineering (ASE) gave a talk at the ECTC Luncheon. His presentation is posted at the ECTC web site due to popular demand (www.ectc.net).

In the evening, the exhibitor reception provided another opportunity for networking and exchanging information among the conference attendees.

At night, Mark Poliks of Endicott Interconnect Technologies and Jan Vardaman of TechSearch International co-chaired the Plenary Session titled "The Evolution of Mobile Processing Architectures". Panelists James Baker of RIM, Samuel Chen of ASUSTek, Steve Bezuk of Qualcomm, Lee Smith of Amkor, and Jose Lopez of Texas Instruments discussed the convergence of computing and communications.

THURSDAY

The night ended with the Executive Committee Reception at the General Chair's Suite.

The CPMT Awards were presented at the Luncheon.

Herbert Reichl of Fraunhofer IZM, the leading name of electronics assembly research in Europe, was among the ones that were honored due to their contributions. He received 2010 IEEE CPMT Award. The CPMT ECTC Sustained Contribution award was presented to ECTC volunteers who have served ten and 25 years.

Al Puttlitz received the 25-year award. Ten-year recipients were: Daniel Baldwin, L. J. Ernst, Ceferino Gonzalez, Beth Keser, S. W. Ricky Lee, Li Li, Sylvain Ouimet and Jean Trewhella.

General Chair Jean Trewhella of IBM received her award from CPMT Representative C. P. Wong.

Sixty-five exhibitors took part in the Technology Corner Exhibit which continued on Thursday. Ten of them were new for this year.

In addition to technical sessions that ran throughout the day, the ECTC Program Committee met to prepare for 2011, CPMT Representative C. P. Wong announced that Dr. Senol Pekin of Intel Corporation will serve as the Assistant Program Chair in 2011. Beth Keser of Qualcomm joined the Executive Committee as the new Web Administrator.

Shown in the picture above is the "A-Team" for 2011: (from left to right) Assistant Program Chair Senol Pekin of Intel Corporation, General Chair Rajen Dias of Intel Corporation, Program Chair Wolfgang Sauter of IBM, and Assistant General Chair David McCann of Amkor.

Thursday evening was fun as always at the ECTC, since conference attendees and their spouses got plenty of time to talk at the well-catered ECTC Gala Reception.

FRIDAY

Technical sessions continued till 5 PM. Conference attendees never feel sad at the last day of the conference thanks to the raffle drawings announced by Thomas Reynolds at the luncheon.

The First Call for Papers for 61th ECTC is already out and can be found at www.ectc.net. You are invited to submit a 750-word abstract by October 15, 2010. In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses.

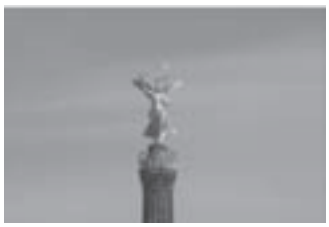
Juha Niitynen of Tampere University of Technology (Finland), who joined the conference for the first time this year to present a paper won a copy of the "Introduction to System-on-Package" book written and donated by Professor Rao Tummala.

See you in at the 61th ECTC in Orlando, Florida, USA next year!

ESTC 2010

in Berlin, September 13–16, Conference Location: Maritim Hotel

We are looking forward to seeing YOU in Berlin in September!



JOIN US IN BERLIN FOR ESTC 2010!

Conference Highlights:

- 160 oral presentations in 5 parallel sessions, 90 posters
- Keynote speeches by Xavier Baraton (ST Microelectronics, Singapore), Eduardo Fernandez, (University Miguel Hernández, Elche, Spain), Reinhard Ploss (Infineon Technologies AG, Munich, Germany) and Masaru Nonomura (Panasonic, Japan)
- A panel discussion on »Challenges and Opportunities for Chip Embedding Technologies«
- A high-level one-day-workshop on 3D wafer level packaging
- Business Session »Managing the Supply Chain in the Medical Electronics Industry«
- A »Chinese Session« on China's contribution to packaging technologies
- Gala Dinner at Meilenwerk, one of the most exciting locations Berlin has to offer

Four half-day tutorials on September 13

- Testing for 1st and 2nd Level Electronics Packaging, K.-J. Wolter, TU Dresden
- Polymers and Nano-Composites for Electronic and Photonic Packaging: Recent Advances on Materials and Process, C. P. Wong, Georgia Tech
- Reliability for System Integration, B. Wunderle, Fraunhofer IZM, Berlin, TU Chemnitz
- Harsh Environment Packaging Using Polymers, K.-F. Becker, Fraunhofer IZM, Berlin

Special: Panel Discussion on Embedding Technologies

Panelists:

- Bernd Appelt (ASE),
- Klaus-Dieter Lang (Fraunhofer IZM)
- Bernd Römer (Infineon)
- Johannes Stahr (AT&S)
- Rao Tummala (Georgia Tech)
- Jan Vardaman (TechSearch)
- Moderator: Chuck Bauer

GMM Fraunhofer IZM iMAPS Europe IEEE

For further information please go to http://www.estc-2010.de

EPTC 2010 Singapore

12th Electronics Packaging Technology Conference
8th – 10th December 2010
Shangri-La Hotel, Singapore

Mark Your Calendar for EPTC 2010

CALL FOR PAPERS

ABOUT EPTC

The 12th Electronics Packaging Technology Conference (EPTC 2010) is an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter and sponsored by IEEE CPMT Society.

EPTC 2010 will feature technical sessions, short courses/forums, an exhibition, social and networking activities. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world.

CONFERENCE TOPICS

You are invited to submit an abstract, presenting new development in the following categories:

- **Advanced Packaging:** Wafer level packaging, 3D integration, TSV (through Silicon Via), embedded passives & actives on substrates, flip chip packaging, RF-ID, 3D SiP, Packaging solutions for MEMS and MOEMS
- **Interconnection Technologies:** wire bonding technology, flip chip technology, solder alternatives (ICP, ACP, ACF, NCP), and TSV
- **Materials & Processes:** Materials and processes for traditional and advanced microelectronic systems, 3D packages, MEMS, solar, green and biomedical packaging
- **Modeling & Simulations:** Electrical modeling & signal integrity, thermal characterization & cooling solutions, mechanical modeling & structural integrity
- **Quality & Reliability:** Component, board and system level reliability assessment, interfacial adhesion, accelerated testing and models, advances in reliability test methods and failure analysis
- **Emerging Technologies:** Packaging technologies in biomedical, bioengineering, biosensors and wearable electronics
- **Printed Electronics:** Printed devices: transistors, batteries and memory, large area printed functional films: lighting, sensors and photovoltaics, solution processing of organic and inorganic materials
- **Wafer/Package Testing and Characterization:** High-speed test architectures and systems, test methodologies, probe card design

IMPORTANT DATES

Submission of abstract	**15th June 2010**
Notification of Acceptance	**1st August 2010**
Submission of manuscript	**1st October 2010**

ABSTRACT AND PAPER SUBMISSION

Abstracts are solicited to describe original and unpublished work. The abstract should be at least 500 words and it must clearly state the purpose, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications and how the work enhances existing knowledge should be included in the abstract as well. Authors can choose between oral or poster presentation.

Authors must designate two appropriate categories (found under CONFERENCE TOPICS) for abstract review. All submissions must be in English and should be made via the online submission system found at http://www.eptc-ieee.net. The required file format is Adobe Acrobat PDF or MS Word in one single file for each submission.

The abstracts must be received by 15th June, 2010. Authors must include their affiliation, mailing address, telephone and fax numbers, and email address. Authors will be notified of paper acceptance and publication instruction by 1st August 2010. The final manuscript for publication in the conference proceedings is due by 1st October 2010. Selected papers will be published in IEEE/CPMT journals.

OUTSTANDING TECHNICAL PAPERS

The conference proceeding is an official IEEE publication. Author(s) of Best Technical Paper (ORAL/POSTER), Outstanding Technical Paper (ORAL) and Best Student Paper will receive an award at the next conference.

CALL FOR SHORT COURSES

The conference program includes short courses which will be conducted by leading experts in the field. Details will be updated in the conference website and available in subsequent mailings. Proposals for short courses can be submitted to techchair@eptc-ieee.net

CALL FOR SPONSORSHIP / EXHIBITION PARTICIPATION

A tabletop exhibition featuring suppliers of materials, equipment, components, software and service providers of the microelectronics and electronic assembly industries will be held during the conference. Potential exhibitors and sponsors may email secretariat@eptc-ieee.net for details.

Organized by

IEEE Reliability/CPMT/ED Singapore Chapter

General Chair:
Dr. Seung Wook YOON, STATS CHIPPAC LTD

Technical Chair:
Dr. Albert LU, SIMTech, A*STAR

Sponsored by

Conference information & contacts: **Website: http://www.eptc-ieee.net** **Email: secretariat@eptc-ieee.net**

The Leading International Symposium on Components, Packaging, and Manufacturing Technology

IEEE CPMT Symposium Japan

(Formerly "VLSI Packaging Workshop in Japan")

Aug. 24-26, 2010

The University of Tokyo, Hongo Campus

Faculty of Engineering Bldg.2 – Sanjo Conference Hall

The VLSI Packaging Workshop in Japan has been held every two years since 1992 in Kyoto, and it has become a well-known international workshop for advanced packaging technologies. Due to ever increasing activities and changing demands, the committee has reviewed its mission; cooperated with the members of IEEE CPMT Japan Chapter, refurbished the workshop, and started the new symposium - IEEE CPMT Symposium Japan. It will provide component, packaging, and manufacturing researchers who are extending their activities beyond borders with opportunities to exchange technical knowledge and perspective. The committee strongly encourages you to attend this symposium and participate in the discussion, to understand the technology trends and find the best targets for your technology / business development. Bring your latest research results and share with the participants who are experts from the industry and the grove of Academe, and discuss with them. Anybody contributing to the achievement of a sustainable society through electronics is very welcome at this symposium.

Features of this symposium are:

- ✓ **Fully supported by IEEE CPMT Society**
- ✓ **Distinguished plenary speakers for the daily topic**
- ✓ **Presented papers will be collected in IEEE Xplore.**
- ✓ **Special offer 50% off of IEEE and CPMT Society membership**
- ✓ **Second day focuses on 3D integration and Interconnection**
- ✓ **Third day focuses on Materials and Optoelectronics**

Online registration starts on July 1, 2010.
Please register online at **http://vlsi-pkg-ws.org/vlsi-pkg.html**
On-site registration will be also available during the symposium. We don't accept registration by mail or FAX. Symposium advance registration fee will be applied if you register online no later than July 31, 2010.

Plenary speakers

Aug. 24, 2010

"Welcome Talk CPMT President"
Rolf Aschenbrenner
President, CPMT Society, IEEE
Fraunhofer IZM

"Advanced Electrical Measurement and Evaluation Technology for 3D LSI Chip Stacking Integration Technology"
Masahiro Aoyagi
President, CPMT Japan Chapter
Advanced industrial science and technology (AIST)

"Materials – Crucial Enabler for Packaging Innovation"
William Chen
Senior Technical Advisor ASE Group
IEEE/CPMT Society
Distinguished Lecturer

"Difficult Challenges and potential solutions for Advanced Packaging"
W. R. Bottoms,
Chair, A&P TWG, ITRS
Chairman, 3MTS

Aug. 25, 2010

"Recent Progress in Surface Activated Bonding Method"
Tadatomo Suga
General Chair, ICPJ 2010
The University of Tokyo

"3D System-in-Package Technologies for Multifunctional Systems"
Klaus-Dieter Lang
Fraunhofer IZM

"3D System Integration - Opportunities and challenges in the supply chain"
Eric Beyne
IMEC

Aug. 26, 2010

"Recent Advances on Nano-materials for Advanced Packaging Applications"
C. P. Wong
Dean of the Faculty of Engineering, The Chinese University of Hong Kong,
On a no pay leave from School of Materials Science and Engineering, Georgia Institute of Technology

More information is provided on the web-site: **http://vlsi-pkg-ws.org/vlsi-pkg.html**

19th IEEE International Conference on
Electrical Performance of Electronic Packaging and Systems
EPEPS 2010
October 24-27, Austin, Texas

Call for Papers

EPEPS is the premier international conference on advanced and emerging issues in electrical modeling, analysis, synthesis and design of electronic interconnections, packages and systems. It also focuses on new methodologies and CAD/design techniques for evaluating and ensuring signal, power and thermal integrity in high-speed designs. EPEPS is jointly sponsored by the IEEE Components, Packaging and Manufacturing Technology Society and IEEE Microwave Theory and Techniques Society. Authors are invited to submit papers describing **new technical contributions related to the broad area of electrical performance of high-speed designs**, covering**:**

1) **Emerging and advanced issues,**
2) **New design techniques and innovative architectures for design and management,**
3) **Novel CAD concepts, methodologies and algorithms for modeling, simulation and optimization,**

with emphasis on:

- System-level, board-level and on-chip interconnects
- High-speed channels, links, backplanes, serial and parallel interconnects, SerDes
- Multiconductor transmission lines
- Memory and DDR interfaces
- Jitter and noise management
- Signal and thermal integrity
- Power integrity and power distribution networks (PDNs)
- Electronic packages and microsystems
- 3D interconnects, 3D packages, TSVs and MCMs
- Nano interconnects and nano structures
- RF/microwave packaging structures, RFICs, mixed signal modules and wireless switches
- Package-chip co-design
- Electromagnetic (EM) and EM interference modeling, simulation algorithms, tools and flows
- Macromodeling and model order reduction as it applies to electrical analysis
- Advanced and parallel CAD techniques for signal, power and thermal integrity analysis
- Measurement and data analysis techniques for system-level and on-chip structures.

Technical Program Committee

Ramachandra Achar, Carlton University; Dale Becker, IBM
Henning Braunisch, Intel; Flavio Canavero, Politecnico di Torino
Moises Cases, IBM (rtd); Paul Franzon, North Carolina State Uni.
Hartmut Grabinski, Uni. of Hannover; Vikram Jandhyala, Uni. of Washington
Michael Lamson, Texas Instruments (rtd); Kathleen Melde, University of Arizona
Michel Nakhla, Carlton University; Dan Oh, Rambus
Christopher Pan, Qualcomm; Albert Ruehli, Emeritus IBM; Missouri U. S&T
Jose Schutt-Aine, University of Illinois; Andreas Weisshaar, Oregon State Uni.
Thomas-Michael Winkel, IBM; Brian Young, Texas Instruments

Submission Deadline: **July 16, 2010, 8pm, PST**

Submission Format: **2 column, 4 page PDF format only.**

Information for authors can be found at www.epeps.org. Submitted manuscripts should be camera ready and compliant with the general standards of the IEEE, including appropriate referencing. Noncompliant manuscripts will not be considered for review.

Location: **Crowne Plaza**, 6121 N. IH-35, Austin, Texas, USA

Tutorials/Workshops: EPEPS offers tutorials or short courses on state-of-the-art topics during the conference. Also on the first day of the conference, a workshop entitled "***Future Directions in Packaging***" may be presented.

Exhibits: EPEPS offers an excellent array of exhibits. EPEPS is an exciting forum for vendors to demonstrate their state-of-the-art-tools to the attendees. Interested vendors can contact the conference administration for more details.

Conference Co-chairs:

Dale Becker, IBM; wbecker@ibm.com

Ramachandra Achar, Carleton University; achar@doe.carleton.ca

For more information please see/contact:

Conference Website:

www.epeps.org **or**

Dale Becker: wbecker@ibm.com **or**

Kelly Sutton: pasutton@email.arizona.edu

IEEE
Institute of Electrical and Electronics Engineers

34th International Electronics Manufacturing Technology Conference (IEMT 2010)

Renaissance Hotel, Melaka, Malaysia
30th Nov – 2nd Dec, 2010

IEEE Component, Packaging and Manufacturing Technology Society

CALL FOR PAPERS - ABSTRACT DEADLINE EXTENDED

Abstract Deadline : July 15th, 2010

About IEMT

The 34th Electronics Manufacturing Technology Conference (IEMT 2010) will be held at Renaissance Hotel, Melaka, Malaysia. It is an international event organized by the IEEE CPMT Malaysia Chapter with co-sponsorship from CPMT society of IEEE, Santa Clara Valley Chapter. IEMT 2010 will feature short courses, 4 parallel technical sessions, and table top exhibition. It aims to provide good coverage of technological developments in all areas of electronics packaging, from design to manufacturing and operation. IEMT 2010 is a major forum, providing opportunities to network and meet leading experts, in addition to exchange of up to date knowledge in the field. Since 1990's, IEMT has gained a reputation as a premier electronics materials and manufacturing technology conference and is well attended by experts in all aspects related to packaging technology from all over the world.

Conference Topics

The topics of interests are specific to manufacturing and test technology, micro systems/MEMS, their packaging, electronics materials, board level assembly and reliability issues. Extended abstracts are being sought from, but not limited to, the following areas:

- Manufacturing Technologies
- Surface Mount Technology
- Advanced/3D Packaging
- Interconnection Technologies
- Emerging Packaging Technologies
- IC Testing Technology
- Materials & Processes
- MEMS & Sensor Packaging
- Electrical Modeling & Signal Integrity
- Thermal Characterization & Cooling Solutions
- Mechanical Modeling & Structural Integrity
- Quality and Reliability
- Chip-Scale Packaging/Flip Chip
- LED Packaging
- Green Package

Important Dates:

Submission of Abstract	**15th July 2010**
Notification of Acceptance	**30th July 2010**
Submission of Manuscript	**15th Sept 2010**

Conference Information and Contacts

IEMT2010 Secretariat
Infineon Technologies (Malaysia) Sdn. Bhd.
FTZ , Batu Berendam, 75350 Melaka, Malaysia
Tel : +6-06-230 3480
Fax : +6-06-231 4233
Email : Tracy.Ow@infineon.com
Conference website: http://ewh.ieee.org/r10/malaysia/cpmt/iemt.htm
Melaka Tourism : http://www.melaka.net/

Extended Abstract and Paper Submission

Extended abstracts are invited to describe original and unpublished works. They should be about 500 words stating clearly the purpose, methodology, results, and conclusions of the work. Key references to prior publications and how the work enhances the existing knowledge should be included in the extended abstract. Authors are requested to designate appropriate areas for the purpose of abstract review. All submissions must be in English and should be made via electronic mail to conference secretariat. Author may send their abstract either in MS Word or Adobe Acrobat© PDF format with only one single file for each submission. The abstracts must be sent to secretariat via email by 15th July, 2010. Authors are requested to include their affiliation, mailing address, telephone and fax numbers, and e-mail address. Authors will be notified of paper acceptance and instruction for preparing final papers by 30th July, 2010. The final manuscript for publication in the conference proceedings is due by 15th September 2010.

Call For Exhibition

A tabletop exhibition from suppliers of materials, equipment, components, software, and service providers of electronics industries will also be held at the venue of the conference. Potential exhibitors and sponsors may email our secretariat for more details.

Conference Best Paper Awards

The conference will present the **"Best paper Award"** to papers in various categories. The overall best paper will receive **RM3000** in cash. Second runner-up will receive **RM2000**. Best poster paper will receive **RM1000**. The conference will also present a cash award of **RM1000** to student best paper.

Free Tour Around The City of Malacca/Cultural Show

We will take the participants for a tour around the historical city of Melaka. They will also be entertained by the local cultural groups while having dinner on various local delicacies. We will make further announcement when more information is available.

Keynotes / Short Courses

The conference will have attractive keynotes and short courses on the latest manufacturing technology and advanced packaging conducted by experts in the field. Please visit our website for more details.

IEEE Components, Packaging and Manufacturing Technology Society
Marsha Tickman, Executive Director
445 Hoes Lane
Piscataway, NJ 08854 USA

Call for Abstracts: IEEE 3DIC 2010

International 3D System Integration Conference

November 16–18, Munich

The IEEE International 3D System Integration Conference (3DIC) will be held at the "Fraunhofer Haus" in Munich in November 16–18, 2010.

This conference combines the previous ASET and IEEE EDS Society sponsored International 3D System Integration Conference, held in Tokyo in 2007 & 2008 and the Fraunhofer and IEEE CPMT sponsored International 3D System Integration Workshop held in 2003 & 2007 in Munich. After the first combined conference in San Francisco 2009, the 2nd IEEE 3D System Integration Conference will be held in Munich in 2010, rotate to Tokyo in 2011 and then rotate back to San Francisco in 2012.

3DIC 2010 will cover all **3D integration** topics, including 3D process technology, materials, equipment, circuits technology, design methodology and applications. The conference invites authors and attendees to submit and interact with 3D researchers from all around the world. Papers are solicited in subject topics, including, but not limited to, the following:

3D Integration Technology: Through Silicon Vias (TSV), wafer thinning, wafer alignment, wafer bonding, wafer dicing, 3D IC process, monolithic 3D integration, heterogeneous 3D integration (e.g. for **MEMS, NEMS**), capacitive coupling, inductive coupling, multilevel epitaxial growth, etc.

3D IC Circuits Technology: 3D SOC, 3D Memory, 3D Processor, 3D DSP, 3D FPGA, 3D RF and microwave/millimeter wave, 3D analog circuits, 3D biomedical circuits etc.

3D Applications: Imaging, memory, processors, communications, networking, wireless, biomedical, MEMS/NEMS etc.

3D Design Methodology: 3D CAD, 3D synthesis, 3D design flows, Signal and power integrity analysis and design in 3D, 3D thermal design and analysis, test and design for test; 3D mechanical stress and reliability design and analysis, etc.

Presentation abstracts and proposals for panels and tutorials should be submitted on the conference web site: **www.3dic-conf.org**. Deadline for papers and proposals is **July 1st, 2010**. Abstracts are to be 500 words in length. Accepted papers will be due **September 15th, 2010**.

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