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THE GLOBAL SOCIETY FOR MICROELECTRONICS SYSTEMS PACKAGING

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President's Column....

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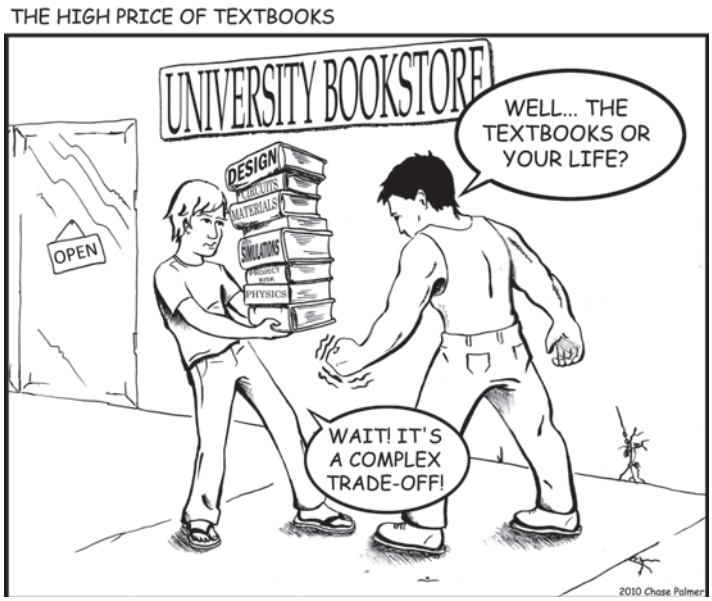
A great deal of my time over the last few months was taken up with organizing ESTC 2010. The conference's five days of presentations and workshops finally took place last week and, exhausted but happy, I can report that the event was a huge success. With 480 participants and an extensive and exciting core and supplementary technical program, I believe we successfully put together a memorable conference for all participants. The feedback so far has been great and, of course, at the end of the day, it was the participation of all the delegates and exhibitors that made the difference.

The 3D WLP workshop was clearly a highlight of the technical program. From the buzz prior to the workshop and the dynamic contributions during its course, it became obvious that 3D packaging is currently the focus of a lot of attention in R&D departments around the world. Architecture, as well as material and equipment, are key topics in 3D WLP and we can definitely expect to hear more on this in the foreseeable future. The panel discussion on "Embedding Technologies" also saw hot discussion. This was only to be expected as the technology is very sensitive to changes in the supply chain. While the discussion highlighted many pressing issues and was a great chance for players in the area to connect, a lot more exchange of ideas on how to tackle challenges in this area will be necessary.

While the weather gods did not smile on us this time, the conference's location in the heart of old Berlin, just around the corner from Checkpoint Charlie, the Tiergarten park and the Brandenburger Gate, was still a great opportunity to explore the city for

(continued on page 3)



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the delegates who managed to tear themselves away from the technical program. I also understand that all enjoyed the supporting program, particularly the gala dinner at Meilenwerk, which was a great opportunity for some quality time not only with the other delegates, but also some outstanding automobile technology. For those of you who could not attend the conference, be sure to check the more detailed overview of ESTC 2010 further on in this newsletter.

The succession of conferences and events continues, with preparation for the 61st ECTC, taking place in Florida, currently underway. As with our events, I encourage you to get involved, and remind you that abstract submissions are still open until mid-October, enough time to package your latest research and hopefully join us next June. ECTC is one of the industry's longest running events, having been held in one form or another since 1950. In June, the joint sponsorship by the IEEE Components, Packaging and Manufacturing Society (CPMT) and the ECA (formerly the EIA) ended with IEEE buying out their long-term partner. This leaves CPMT as the sole sponsor. However, we are working hard to ensure that conference remains the quality event it has traditionally been, and believe that this logistical change should pass unnoticed by both the attendees and the ECTC program committee.

CPMT Society News....

CPMT ELECTION BEGINS ON 24 SEPTEMBER—PLEASE VOTE BY 29 OCTOBER

The IEEE Components, Packaging, and Manufacturing Technology Society Constitution and Bylaws provide that the membership shall elect each year six Members-at-Large to the Society Board of Governors to serve a three-year term.

Members-at-large will be elected to achieve totals proportionate to the geographic distribution of CPMT members. For 2010, this translates as follows:

Regions 1-6, 7 and 9 (US, Canada, South and Central America): **elect 5 members**
Candidates: Xuejun Fan, Ning-Cheng Lee, Debendra Mallik, James Morris, Eric Perfecto, Bahgat Sammakia, Dongkai Shangguan, Jean Trewhella

Region 8 (Europe, Africa, Middle East): **elect 1 member**
Candidates: Jan Felba, Toni Mattila, Gilles Poupon

Region 10 (Asia/Pacific): **no members to be elected**

The six newly-elected Members-at-Large will join continuing Members-at-Large (shown below) on the Board of Governors:

From Regions 1-6, 7 and 9: Vasudeva Atluri, Daniel Donahoe, Paul Franzon, Koneru Ramakrishna, Len Schaper, Patrick Thompson, Paul Wesling,

From Region 8: Chris Bailey, Klaus Jürgen-Wolter

From Region 10: Ricky Lee, Kwang-Lung Lin, Kishio Yokouchi

The Nominations Committee included the CPMT Strategic Program Director, Region 8. The Strategic Program Director worked with volunteer leaders in his Region to identify a high-quality slate of candidates from that Region.

Voting members will elect Members-at-Large from within their respective Region only – that is, members in Region 8 will vote for Members-at-Large from Region 8 only, etc.

This year's election continues to offer the opportunity to cast your ballot electronically. You will need your IEEE Web Account username/password to access the ballot and cast your vote. This is the same account information used to access IEEE online services such as renewing your membership, myIEEE, and Xplore. It is recommended that you test your web account access at **www.ieee.org/myieee** to avoid any potential problems with accessing your ballot. If you do not recall your web account information, you may go to: **www.ieee.org/web/accounts** to recover. You may also email **contactcenter@ieee.org** or call +1 800 678 4333 (USA/Canada) or +1 732 981 0060 (Worldwide).

If you have any questions about the IEEE CPMT Society voting process, please contact **ieee-cpmtvote@ieee.org** or +1 732 562 3904.

JORMA KIVILAHTI FIRST RECIPIENT OF IEEE CPMT REGION 8 AWARD

For establishing the IEEE CPMT Finland Chapter, developing programs to serve local CPMT members and the profession and building strong collaborations and networks within the region.

Professor Jorma Kivilahti became the first recipient of the CPMT Society Regional Contributions Award for Region 8 (Europe, Middle East, Africa). The Award was established to recognize significant and outstanding leadership and contributions to the growth and impact of CPMT programs and activities at the Region level.

The presentation took place at the recent Electronics System Integration Conference (ESTC) in Berlin.

Professor Kivilahti is an IEEE Fellow, a CPMT Distinguished Lecturer, and recipient of the 2006 CPMT "Outstanding Sustained Technical Contribution Award". Professor Kivilahti headed the laboratory of Electronics Production and the Graduate School of Electronics Manufacturing at Helsinki University of Technology, where his R&D primarily covered the integration and reliability of electronics. His numerous major research projects in electronics manufacturing and reliability, hundreds of scientific and technological papers and several patents played a major role in shaping Finland's microelectronics industry.

Professor Kivilahti was extremely active in CPMT and this award recognizes his establishment of the Finland IEEE CPMT Chapter in 1998. He worked hard and closely with the Nordic countries to initiate the Chapter and went on to head it for its first three years. His term was impressive. He was the driving force behind high quality seminars with lecturers worldwide and he established several highly effective networks for the CPMT Society in the Nordics. The Chapter remains strong today thanks to Prof Kivilahti's sustained contribution to CPMT in Region 8.

CALL FOR NOMINATIONS FOR THE 2011 CPMT SOCIETY AWARDS NOMINATIONS DUE BY JANUARY 31, 2011

Hey!! It is that time of year and this is a Call for Action!!!! Don't wait unti the last minute and MISS OUT on a great opportunity to recognize a peer or a co-worker for their contribution to the CPMT Society and/or their technical community. Make a commitment TODAY to put your thinking caps on and think of those individuals that should be recognized! I am sure that you know who has gone above and beyond in their contribution to their technical community and to the CPMT Society. Don't hesitate to put their names forth. The Awards Committee is currently accepting nominations for the 2011 CPMT Awards. All nomination packages are due by January 31, 2011. Winners will be notified by 31 March 2011 and the awards will be presented at the 61th Electronic Components and Technology Conference, May 31st–June 3rd 2011, in Orlando, Florida, USA. A current nomination form can be found on the CPMT web site at the Awards link by accessing the following url http://www.cpmt.org/awards/index.html. We look forward to receiving many nominations in all the categories listed below:

CPMT Society offers the following 5 awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of the CPMT Society.

1) **David Feldman Outstanding Contribution Award:** This award recognizes outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.
   Prize: $2,500 and Certificate
   Basis for Judging: Contributions to the organization or enterprises connected with the field, to CPMT Chapter, Section or Board of Governors activities, and to the fields encompassed by the CPMT Society.
   Eligibility: Recipient must have been a member of IEEE and CPMT for the past five (5) years, including 2010.
2) **Outstanding Sustained Technical Contributions Award:** To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society.
   Prize: $2,500 and Certificate
   Basis for Judging: Technical contributions must be sustained and continuing over a period of at least five (5) and preferably 10 years. One major contribution will not qualify. Contributions must be documented by open literature publications such as papers, patents, books and reports (available to the public).
   Eligibility: Must have been a member of the IEEE and CPMT Society for the past three (3) years, including 2010.
3) **Electronics Manufacturing Technology Award:** To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society.
   Prize: $2,500 and Certificate
   Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Work in the management of CPMT conferences or its BoG may be contributory but not sufficient to receive the award.
   Eligibility: No need to be a member of IEEE and CPMT Society.
4) **Exceptional Technical Achievement Award:** To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the CPMT Society.
   Prize: $2,500 and a Certificate.
   Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important

technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in CPMT's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.

Eligibility: Recipient(s) must have been a member of IEEE and CPMT for the past three (3) years, including 2010. There are no requirements for service to the IEEE or CPMT Society.

5) **Outstanding Young Engineer Award:** To recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.

Prize: $1,500 and Certificate plus one year free membership in CPMT with all CPMT Transactions.

Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the CPMT Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.

Eligibility: Must have been a member of the IEEE and CPMT (member grade or above) for the past three (3) years, including 2009, and must be 35 years of age, or younger, on December 31st, 2010. Please provide Date of Birth (Month/Year) to ensure eligibility.

Guidelines for Nominators:

- Minimum **three** reference letters must be submitted in support of all nominations. Reference letters can be provided by IEEE/CPMT members and non-members.
- Past recipients of an award are not eligible to receive that same award. For list of past awardees, see the CPMT Society Home page (http://www.cpmt.org/awards).
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- It is the responsibility of the nominator to provide quality documentation to assist the Awards Committee in evaluating the candidate.
- Please send nominations to CPMT Society Director, Awards by e-mail or mail:

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Any technologist – **member or non-member** – is welcome to receive alerts when upcoming issues of our CPMT *Transactions* are posted to the IEEE's Xplore database and all the papers are available for downloading. This is a handy way to scan the issue's Table of Contents and quickly learn about novel approaches to packaging, modeling, reliability, materials, assembly and other topics.

The website link is: ieeexplore.ieee.org/xpl/tocalerts_signup.jsp

If you already have an IEEE web account, you may sign in and select those journals you wish to track. If you don't have an account, all it takes is your name and email address! Then simply click the Alert Status box next to the journals you wish to monitor. You will receive an email each quarter when that journal is posted to Xplore.

Similarly, if you prefer to receive information by RSS feed, you may add our journals' feeds to your Reader. You'll get a listing of the papers in that issue, along with full abstracts and a link for downloading the paper. The RSS links are shown on this same web page.

Here are the journals we suggest you select for monitoring:

➥ Advanced Packaging, IEEE Trans on
➥ Components and Packaging Technologies, IEEE Trans on
➥ Electronics Packaging Manufacturing, IEEE Trans on

Publication News....

COMING IN 2011 – NEW OPTIONS FOR SUBSCRIBERS TO CPMT TRANSACTIONS

As previously announced, beginning in January 2011, the CPMT Society will launch the *IEEE Transactions on Components, Packaging, and Manufacturing Technology.* This monthly periodical is a consolidation of the three current CPMT Society Transactions: *Transactions on Advanced Packaging*, *Transactions on Components and Packaging Technologies* and *Transactions on Electronics Packaging Manufacturing.*

Subscribers will now have access to all CPMT archival technical content in one monthly publication (12 issues annually)—with no worry of missing papers of interest that may have been published in one of the other CPMT Transactions to which they didn't subscribe.

Additionally, subscribers will have new options that allow them to manage their subscription fees and the manner in which they receive the new Transactions—by choosing electronic only (online via IEEE Xplore), print only, or combo (electronic and print).

Those who currently subscribe to at least one of the current CPMT Transactions will receive a 2011 IEEE renewal invoice that includes the new *IEEE Transactions on Components, Packaging, and Manufacturing Technology*—which replaces the current CPMT subscription(s).

The default media type for Member subscribers will be combo (electronic and print). Those who prefer print only or electronic only can make this change when they complete their renewal. For Student subscribers, the default media will be electronic only.

The consolidated Transactions, will be published online monthly (12 issues annually). Print issues will be published bimonthly (six issues annually) and combine two months of online issues.

Questions and feedback on these changes are welcome; please forward to cpmt@ieee.org.

HAVE YOU READ THEM? THE MOST DOWNLOADED CPMT PAPERS

What might you be missing in the CPMT literature?

Following is a list of the top CPMT Transactions papers downloaded in July 2010. Subscribers can access these and other papers on IEEE Xplore.

IEEE Transactions on Advanced Packaging

1) **Effects of Warpage on Fatigue Reliability of Solder Bumps: Experimental and Analytical Studies**, Wei Tan; Ume, I.C.; Ying Hung; Wu, C.F.J.; Issue Date: May 2010 Page(s): 314–322

Out-of-plane displacement (warpage) has been a major thermomechanical reliability concern for board-level electronic packages. Printed wiring board (PWB) and component warpage results principally from coefficient of thermal expansion mismatch among the materials that make up the PWB assembly (PWBA). Warpage occurring during surface-mount assembly reflow processes and normal operations may lead to severe solder bump reliability problems. In this research, the effect of initial PWB warpage on the low cycle thermal fatigue reliability of the solder bumps in plastic ball grid array (PBGA) packages was studied using experimental and analytical methods. A real-time projection moireÂ¿ warpage measurement system was used to measure the surface topology of PWBA samples at different temperatures. The thermal fatigue reliability of solder bumps was evaluated from experimental thermal cycling tests and finite element simulation results. Three-dimensional (3-D) models of PWBAs with varying board warpage were used to estimate the solder bump fatigue life for different types of PBGAs mounted on PWBs. In order to improve the accuracy of FE results, the projection moireÂ¿ method was used to measure the initial warpage of PWBs, and this warpage was used as a geometric input to the finite element method. The simulation results were validated and correlated with the experimental results obtained using the projection moireÂ¿ technique and accelerated thermal cycling tests. An advanced prediction model was generated to predict board level solder bump fatigue life based on the initial PWB warpage, package dimensions and locations, and solder bump materials.

2) **Guaranteed Passive Parameterized Admittance-Based Macromodeling** Ferranti, F.; Knockaert, L.; Dhaene, T.; Issue Date: Aug. 2010 Page(s): 623–629

We propose a novel parametric macromodeling technique for admittance and impedance input-output representations parameterized by design variables such as geometrical layout or substrate features. It is able to build accurate multivariate macromodels that are stable and passive in the entire design space. An efficient combination of rational identification and interpolation schemes based on a class of positive interpolation operators, ensures overall stability and passivity of the parametric macromodel. Numerical examples validate the proposed approach on practical application cases

3) **Packaging of Dual-Mode Wireless Communication Module Using RF/Optoelectronic Devices With Shared Functional Components** Jun Liao; Juan Zeng; Shengling Deng; Boryssenko, A.O.; Joyner, V.M.; Huang, Z.R.; Issue Date**:** May 2010 Page(s): 323–332

This paper reports the design, fabrication, and testing of a compact radio-frequency (RF)/ free space optical (FSO) dual mode wireless communication system. A modified split dual-director quasi-Yagi antenna is integrated with optical transmitter and receiver by sharing layout structural components. Bare die vertical-cavity surface-emitting laser (VCSEL) and P-i-N photodiode (PIN) are

placed on antenna director pads and wire bonded to printed circuit board (PCB)-mounted laser driver and transimpedance amplifier (TIA) circuits. Detailed analysis of coupling between RF channel and associated electrical connections for the FSO channel is presented using commercial simulation tools to predict its impact on link degradation. Although crosstalk appears between RF and optical channels, the prototyped system demonstrated dual-mode high-rate communication capability with measured 2.5 Gb/s data rate in FSO link. Variations in RF subsystem features due to coupling from the FSO subsystem is estimated through radiation pattern measurement using near-field scanner.

Transactions on Components and Packaging Technologies

1) **Analytical and Numerical Modeling of the Thermal Performance of Three-Dimensional Integrated Circuits** Jain, A.; Jones, R.E.; Chatterjee, R.; Pozder, S.; Issue Date: March 2010 Page(s): 56–63

Three-dimensional (3D) interconnection technology offers several electrical advantages, including reduced signal delay, reduced interconnect power, and design flexibility. 3D integration relies on through-silicon vias (TSVs) and the bonding of multiple active layers to stack several die or wafers containing integrated circuits (ICs) and provide direct electrical interconnection between the stacked strata. While this approach provides several electrical benefits, it also offers significant challenges in thermal management. While some work has been done in the past in this field, a comprehensive treatment is still lacking. In the current work, analytical and finite-element models of heat transfer in stacked 3D ICs are developed. The models are used to investigate the limits of thermal feasibility of 3D electronics and to determine the improvements required in traditional packaging in order to accommodate 3D ICs. An analytical model for temperature distribution in a multidie stack with multiple heat sources is developed. The analytical model is used to extend the traditional concept of a single-valued junction-to-air thermal resistance in an IC to thermal resistance and thermal sensitivity matrices for a 3D IC. The impact of various geometric parameters and thermophysical properties on thermal performance of a 3D IC is investigated. It is shown that package and heat sink thermal resistances play a more important role in determining temperature rise compared to thermal resistances intrinsic to the multidie stack. The improvement required in package and heat sink thermal resistances for a 3D logic-on-memory implementation to be thermally feasible is quantified. An increase in maximum temperature in a 3D IC compared to an equivalent system-in-package (SiP) is predicted. This increase is found to be mainly due to the reduced chip footprint. The increased memory die temperature in case of memory-on-logic integration compared to a SiP implementation is identified to be a sig- nificant thermal management challenge in the future. The results presented in this paper may be useful in the development of thermal design guidelines for 3D ICs, which are expected to help maximize the electrical benefits of 3D technology without exacerbating thermal management issues when implemented in early-stage electrical design and layout tools.

2) **Dynamic lithium-ion battery model for system simulation** Lijun Gao; Shengyi Liu; Dougal, R.A Issue Date: September 2002 Page(s): 495–505

Presents here a complete dynamic model of a lithium ion battery that is suitable for virtual-prototyping of portable battery-powered systems. The model accounts for nonlinear equilibrium potentials, rate- and temperature-dependencies, thermal effects and response to transient power demand. The model is based on publicly available data such as the manufacturers' data sheets. The Sony US18650 is used as an example. The model output agrees both with manufacturer's data and with experimental results. The model can be easily modified to fit data from different batteries and can be extended for wide dynamic ranges of different temperatures and current rates.

3) **Development of 3-D Silicon Module With TSV for System in Packaging** Khan, N.; Rao, V.S.; Lim, S.; Ho Soon We; Lee, V.; Xiaowu Zhang; Liao, E.B.; Nagarajan, R.; Chai, T.C.; Kripesh, V.; Lau, J.H. Issue Date: March 2010 Page(s): 3–9

Portable electronic products demand multifunctional module comprising of digital, radio frequency and memory functions. Through silicon via (TSV) technology provides a means of implementing complex, multifunctional integration with a higher packing density for a system in package. A 3-D silicon module with TSV has been developed in this paper. Thermo-mechanical analysis has been performed and TSV interconnect design is optimized. Multiple chips representing different functional circuits are assembled using wirebond and flip chip interconnection methods. Silicon carrier is fabricated using via-first approach, the barrier copper via is exposed by the backgrinding process. A two-stack silicon module is developed and module fabrication details are given in this paper. The module reliability has been evaluated under temperature cycling (–40/125Â°C) and drop test.

Transactions on Electronics Packaging Manufacturing

1) **Development of Warpage Measurement System to Simulate Convective Solder Reflow Process** Powell, R.E.; Ume, I.C.; Issue Date: Jan 2008 Page(s): 83–90

In this paper, a warpage measurement system to simulate forced convective reflow is discussed. A warpage measurement system that can simulate convective reflow enables the real-time monitoring of printed wiring boards (PWBs), PWB assemblies (PWBAs), and chip package warpage during the reflow process. This paper will describe the two major parts of the warpage measurement system: the optical measurement part which utilizes the projection Moire method and advanced image processing, as well as the laboratory oven which is used to simulate forced convective reflow. This is the first system that allows PWB/PWBA/chip package warpage to be measured during a simulated convective reflow process. Also, this is the first system that employs automatic image segmentation to separately extract the warpage of the PWB and electronic components from the same measurement. The results will show that when compared to infrared heating which was previously used in this research area, convective heating minimizes thermal gradients on the PWB/PWBA sample. Thermal gradients on the PWB/PWBA sample have the inadvertent effect of inducing warpage into the sample and will interfere with the warpage measurement result. In the first design iteration presented

in this paper, the system can simulate low ramp rate industrial convective reflow profiles and simultaneously measure the warpage of PWBAs. A computational fluid dynamics (CFD) model of the system was developed to determine how to increase the system's heating rate. The CFD model was used to perform a design of simulations (DOS) and regression analysis. The validated regression results will be used to predict oven design parameters to enable the next iteration of the convective system to simulate high ramp rate convective reflow profiles. This paper will show that the presented system is a powerful tool for measuring the warpage of PWBs, PWBAs, and chip packages.

2) **Electron beam lithography in nanoscale fabrication: recent development** Tseng, A.A.; Kuan Chen; Chen, C.D.; Ma, K.J.; Issue Date: April 2003 Page(s): 141–149

Miniaturization is the central theme in modern fabrication technology. Many of the components used in modern products are getting smaller and smaller. In this paper, the recent development of the electron beam lithography technique is reviewed with an emphasis on fabricating devices at the nanometer scale. Because of its very short wavelength and reasonable energy density characteristics, e-beam lithography has the ability to fabricate patterns having nanometer feature sizes. As a result, many nanoscale devices have been successfully fabricated by this technique. Following an introduction of this technique, recent developments in processing, tooling, resist, and pattern controlling are separately examined and discussed. Examples of nanodevices made by several different e-beam lithographic schemes are given, to illustrate the versatility and advancement of the e-beam lithography technique. Finally, future trends in this technique are discussed.

3) **Acid Decapsulation of Epoxy Molded IC Packages With Copper Wire Bonds** Murali, S.; Srikanth, N.; Issue Date: July 2006 Page(s): 179–183

Epoxy molded IC packages with copper wire bonds are decapsulated using mixtures of concentrated sulfuric acid (20%) and fuming nitric acid in an automatic decapping unit and, observed with minimal corrosion of copper wires (0.8-6 mil sizes) and bond interfaces. To attain maximum cross-linking of the molded epoxies, the post mold cured packages (175 degC for 4 h) were further, aged at high temperature of 150 degC for 1000 h. These packages are decapsulated using mixtures of higher ratio of concentrated sulfuric acid (40%) along with fuming nitric acid. The shear strength of copper wire bonds with 1 mil (25 mum) diameter of the decapsulated unit is higher than 5.5 gf/mil2. The present study shows copper stitch bonds to Au, Cu, Pd, and Sn alloy plated surfaces are less affected on decapping, with a few grams of breaking load on stitch pull test, while stitch bonds on silver plated surfaces reveal lifting of wire bonds on decapping

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BOOK REVIEW: PORTABLE CONSUMER ELECTRONICS: PACKAGING, MATERIALS, AND RELIABILITY

By Sridhar Canumalla and Puligandla Viswanadham
Published by PennWell

This book titled "Portable Consumer Electronics: Packaging, Materials, Reliability" is written by two veteran technologists in the industry for engineers working in the field of Portable Consumer Electronics. The authors said in the Preface, "This book is written at a level that assumes only a basic knowledge in the fundamentals of physics, chemistry and engineering at the undergraduate level." It is written for the practicing packaging engineers in the portable electronics sector of our industry. As the title indicates authors have focused their writing on packaging (a la assembly), materials, and reliability. The authors have years of distinguished career in the industry, including the portable consumer electronics industry. They have invested their knowledge and experience in the pages of this book.

The words "Portable Consumer Electronics Products" cover a broad spectrum of electronic products with diverse packaging requirements. However there is a common thread of portability and consumer requirements that sets it apart in Packaging Technology from other electronic products. While much of the technologies are fundamental to all aspects of the packaging industry, it is the focus and practice that distinguish this book from the other packaging technology books.

Chapter 1 introduces the topic of Portable Consumer Electronics with a specific description of what "portability index" means. Chapter 2 articulates the technical challenges in packaging for the portable electronics products. Chapters 3 to 6 cover the topics of PWB technology, first level packaging, 2nd level packaging and board assembly, i.e. the topic of packaging, assembly and materials. Chapters 7 to 9 cover reliability statistics, reliability, and failures and prevention. The last chapter, titled Future Trends in Portable Electronics Products, is devoted to an educated look at what the needs are for future electronic products and what technology and materials are in development to meet those needs. An excellent feature in this book is the reference section at the end of each chapter and suggested reading to help the readers to dig deeper.

I enjoyed reading this book. The three chapters on Reliability Statistics, Reliability of Electronic Assemblies, and Failure and Prevention are particularly valuable for the practicing engineers. These are areas where classroom knowledge is seldom enough as many of us have learned from painful experiences. The authors have lovingly shared their expert knowledge and collective experiences in those pages.

Portable Consumer Electronics is a fast expanding market with rapidly evolving product functions and packaging technologies. This book is a good compelling read for the practicing engineers in the field and a ready relevant reference in their library. It is a very good and worthwhile addition to our literature.

Reviewed by:
William T. Chen
Senior Technical Advisor, ASE US
IEEE CPMT President, 2006-2009

Conference News....

2010 INTERNATIONAL CONFERENCE ON ELECTRONIC PACKAGING AND HIGH DENSITY PACKAGING

Xi'an, China
August 16 – 19, 2010

The 11th International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP 2010) was held in Xi'an, China, from August 16 to 19, 2010. The 11th ICEPT-HDP was organized by the Electronic Manufacturing and Packaging Technology Society of the Chinese Institute of Electronics (CIE-EMPT), and supported by IEEE CPMT. The ICEPT-HDP 2010 was hosted and co-organized by Xidian University. Professor Keyun Bi (Vice Director General of Standing Committee of Chinese Institute of Electronics (CIE); President of Electronic Manufacturing and Packaging Technology Society (EMPT)) served as the General Chair, assisted by five Co-Chairs: Yingtang Tang (Vice President of Xidian University), Rolf Aschenbrenner (President IEEE-CPMT, IZM, Fraunhofer, Germany); William Chen (former President of IEEE-CPMT and Senior Advisor of ASE, USA); Kouchi Zhang (Senior Director and Fellow of Philips Lighting, Professor of Delft University of Technology, Netherlands); and Joahan Liu (Professor of Shanghai University, China, Member of the Royal Swedish Academy of Engineering, Sweden). Dr. Xuejun Fan (Lamar University) serves as Technical Chair.

Gathering at Conference Banquet.

ICEPT-HDP 2010 was an exciting 4-day event, featuring an Executive Wafer Level Packaging Forum, four professional development courses, 17 plenary keynote presentations, 30 technical oral sessions and three poster sessions, a CPMT workshop, a special session on solid state lighting integration and reliability, technical exhibition, and many social and networking activities. These venues covered the latest technological developments in electronic packaging, manufacturing and packaging equipment, and provided opportunities to explore the trends of research and development, as well as business in China. There were more than 400 people in attendance, and was the largest in paper submission and attendance in ICEPT history.

The Wafer Level Packaging (WLP) Executive Forum was one of many highlights of this conference. Wafer Level Chip Scale Packaging (WLCSP) is the most prominent WLP product today. Industry analysis report indicates that inside the top three high-end smart phones, thirty to fifty percent of the components are WLCSPs. New generations of CMOS Image Sensors (CIS) manufactured in wafer level TSV process, are now implemented in cell phones and other mobile products. The most recent wafer level packaging product in high volume production is the fan-out WLCSP. Wafer level MEMs is positioned for a variety of market implementation. The basic technologies and manufacturing infrastructure (fan-in, fan-out, TSV, MEMs, CIS) are expected to serve as building blocks for heterogeneous and 3D integration, and 3D IC architectures for the global market. The WLP Executive Forum invited a group of senior technologists and veteran business executives from around the globe to share their knowledge, experience and vision. The seven speakers are William Chen (on behalf of Bill Bottoms); John Hunt (Engineering Director, ASE Group); Glenn Daves (Packaging Dev Director, Freescale Semiconductor); Bob Forcier (President & CEO, Flip Chip International); Peter Elenius (Consultant, E&G Technology Partners); Jurgen Wolf (Group & Project Manager ASSID, Fraunhofer IZM) ; and Herb Huang (Director of Specialty Technology Development Semiconductor


Prof. Bi (General Chair) with Rolf Aschenbrenner and William Chen.

WLP Executive Forum Speakers and Forum Chair/Co-Chair.

Manufacturing International Corporation (SMIC), Shanghai). The Forum was co-chaired by Drs. William Chen and Wenhui Zhu (CTO, Tian Shui Hua Tian Technology Co. Ltd, China). Each executive presented their perspective, at a high-level, of this very important technology, the global market, product applications and future directions addressing questions such as "what will be the new markets and product applications?" "How will the technologies evolve? What will be the business models and opportunities?" This forum was sponsored by CPMT, ASE Groups and Tianshui Huatian Technology Co.).

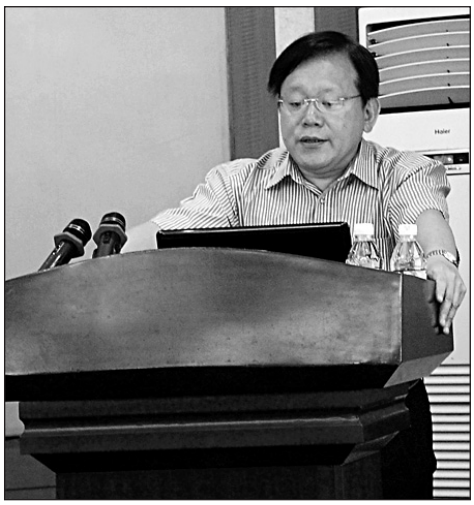
On the opening day of the conference, seventeen distinguished speakers were invited to give keynote presentations. Mr. Rolf Aschenbrenner gave an overview of chip embedding technology for IC packaging. Prof. Zou Shichang of Chinese Academy of Science presented an overview of China's IC industry after the global financial crisis. Dr. Mark Brillhart presented the packaging challenges and technology innovations in high performance networking products. Prof. Kouchi Zhang brought a new perspective and the new technology landscape in solid state lighting.

Thirty technical oral sessions brought the latest technology developments in in electronic packaging, manufacturing and packaging equipment. Many of the sessions focused on 3D/TSV, new materials and reliability challenges. This year three separate poster sessions, each with more than 60 posters, were arranged in dedicated time slots to promote interactive technical discussions. A total of 15 outstanding papers were awarded from both oral and poster sessions.

CPMT workshop was another highlight of the conference. Drs. Kitty Pearsall (VP of CPMT, Member of the Academy of Technology, IBM), and Ricky Lee (Editor-in-Chief of TCPT, Professor of HKUST, Hong Kong) hosted and presented in this workshop. The workshop addressed the importance of the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society in building members career. The workshop also included a presentation about best practices for the generation of "high impact" technical papers, including key attributes of "high impact" papers; a list of "must dos" for authors as they prepare their technical paper for submission; the use of communities of interest to determine which Society transaction is the best one to submit paper to for consideration; and a list of resources.

A special session on solid state lighting (SSL) integration and assembly was organized in this conference. A large attendance joined this special session for technical discussions on the latest developments in packaging, assembly and reliability challenges in SSL system. Philips Lighting sponsored this special session for the selection of the Best SSL Integration Paper Awards.

Cisco sponsored the Best Student Paper Awards. A total of six student papers were selected for the award.



Dr. Ricky Lee at CPMT Workshop.

Cisco Best Student Paper Awards Ceremony.

ESTC 2010 – A RESOUNDING SUCCESS!

With 160 presentations, 4 poster sessions, a 3-day industry exhibition, workshops and short courses, the third Electronics System Integration Technology Conference ESTC 2010 was truly an immersive experience for the almost 500 conference delegates. No matter what your background in micro system packaging, the conference had something for everyone. IEEE-CPMT, IMAPS Germany and Fraunhofer IZM as organizers are particularly pleased that the conference participants, representing 34 different countries, came from industry and academia in equal part and, based on the networking observed on the conference floor and at the social events, it seems everyone went home with new contacts, insights and inspiration.

CPMT president and ESTC chair Rolf Aschenbrenner pointed out that a milestone was achieved in 2010 – ESTC is now undoubtedly Europe's premier packaging conference.

Among the many highlights of the conference the gala dinner at Meilenwerk stood out, with car fans and aesthetes alike marveling at classic cars from bygone eras. It was also a great chance to farewell one of the industry's pioneers, Herbert Reichl, who received a special award for his long-term and significant contributions to micro system packaging. Jorma Kivilahti, who was to be honored with the IEEE Section 8 Award, had unfortunately been taken ill and Mervi Palasto from Aalto University accepted the award in his place.

Our congratulations go to the winners of the Best Paper Award (Yoichiro Kurita et. al. from Renesas Electronics Corporation) on Fan-Out Wafer-Level Packaging with Highly Flexible Design Capability and Best Poster Award (M. Bouchoucha et. al. from STMicroelectronics) on Through Silicon Via Polymer Filling for 3D-WLP Applications.

The organizers would like to thank all participants for ensuring ESTC 2010 was such a resounding success and look forward to what will surely be another standout ESTC in Amsterdam in 2012.

Panel Discussion with the Panel Members.

The Conference Exhibition with Eric Beyne and Chris Bailey.

Plenary Hall during the Keynote Session.

Opening Speech of the General Chair, Rolf Aschenbrenner.

IEEE CPMT SYMPOSIUM JAPAN (10TH VLSI PACKAGE WORKSHOP IN JAPAN)

"IEEE VLSI Package Workshop in Japan" has been held every other year since 1992 and reached the tenth anniversary this year. Based on several considerations, this Workshop has been transformed this year to "IEEE CPMT Symposium Japan" (ICSJ) by the joint effort of IEEE CPMT Japan Chapter and the organizing committee. ICSJ intends to provide researchers and engineers who wish to extend their activities beyond borders with opportunities to exchange technical knowledge and perspective.

ICSJ2010 was held at the University of Tokyo, Japan, from Aug. 24 to 26, 2010—it was the hottest summer in Japan since the Japan Weather Bureau started monitoring climate 113 years ago. As the heat waves at Tokyo smashed the record, in the meanwhile, the number of ICSJ2010 participants also hit the record high of 183, versus the past record of 141. Seventy papers (27 from overseas) out of 86 abstracts were selected and presented in ICSJ2010. IEEE CPMT Society offered the subsidy to the new enrollment fee of IEEE and CPMT Society and received 10 applications during the Symposium.

There were two unique features in ICSJ2010. One is authors' interviews. During the break following the session, the presenters were requested to stay in front of their posters (hardcopies of ppt files) to answer questions from session attendees. Such interviews were proposed to make up the short Q&A time during the session and to promote close interactions between speakers and audience. The other feature was transparent walls between the rooms and the reception hall, which allowed people to see the status of presentations from outside the rooms and lured people from their conversation outside to the sessions inside.

EVENT HIGHLIGHTS

As a pre-conference workshop, ITRS workshop was held on Aug. 23, 2010, by Assembly and Packaging TWG of ITRS and the roadmap committee of Japan Electronics and Information Technology Industries Association (JEITA), with 26 attendees. The agenda included ITRS 2009 brief introduction, ITRS 2010 update, ITRS 2011 activity plan, Japan Jisso Roadmap (JJTR 2009), MEMS roadmap, and the panel discussion about difficult challenges.

On Aug. 24, the Symposium was opened by the remarks from Hirofumi Nakajima, Executive Chair of ICSJ2010, and then the welcome speech from Rolf Aschenbrenner, President of IEEE CPMT Society. Three plenary talks were presented in the morning of the opening day, namely, "Materials – Crucial Enabler for Packaging Innovation" by William Chen (ASE US), "Difficult Challenges and Potential Solutions for Advanced Packaging" by Bill Bottoms (3MTS), and "Recent Advances on Nano-materials for Advanced Packaging Applications" by C. P. Wong (The Chinese University Hong Kong). After the plenary session, people split into three sessions: advanced package, board level reliability, and electrical design, for paper presentations.

On Aug. 25, Ricky Lee, Vice Chair of ICSJ2010, chaired the plenary session. Three keynotes were delivered, namely, "Recent Progress in Surface Activated Bonding Method" by Tadatomo Suga (University of Tokyo), "3D System-in-Package Technologies for Multifunctional Systems" by Klaus-Dieter Lang (Fraunhofer IZM), and "3D System Integration - Opportunities and Challenges in the Supply Chain" by Eric Beyne (IMEC). After the plenary session, people split into three sessions: 3D integration, mechanical design, and optical vs. electrical, for paper presentations.

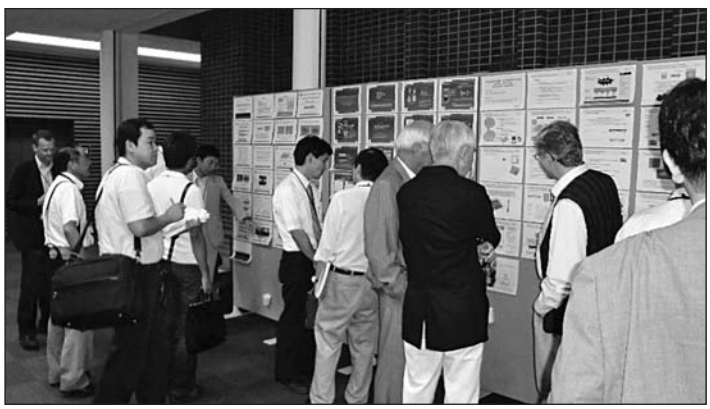
On Aug. 26, Hiroshi Yamada, Vice Chair of ICSJ2010, chaired the plenary session. The keynotes on that day were "3D Packaging Trends: From Stacked Die to 3D ICs with TSV" by Jan Vardaman (TechSearch), and "Advanced Electrical Measurement and Evaluation Technology for 3D LSI Chip Stacking Integration Technology" by Masahiro Aoyagi (AIST). After the plenary session, people split into three sessions: thermal design, materials, and optoelectronics. The materials and optoelectronics sessions had the largest number of papers among sessions, reflecting active industries.

AWARDS

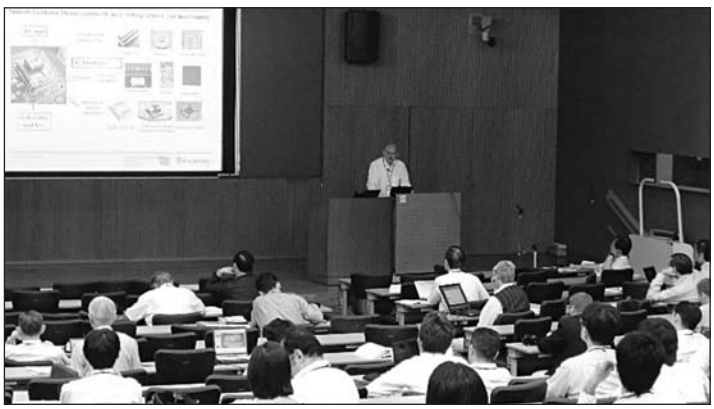
Tadatomo Suga, General Chair of ICSJ2010, awarded the best paper award to Hiroshi Yamada for his paper: "A wafer-level system integration technology for flexible pseudo-SOC incorporates MEMS-CMOS heterogeneous devices"; and the young awards to Jonghyun Cho for his paper: "Guard-Ring Effect for Through Silicon Via (TSV) Coupling Reduction"; and Tatsuya Yamashita for his paper: "Polymeric multi/demultiplexers using light-induced self-written waveguides for cost-effective optical interconnection".

REVIEW AND SURVEY SUMMARY

On the last day, a review meeting was held with CPMT board and organizing committee members over lunch. The main topic



Authors' interview.



ICSJ Plenary session.

of this discussion was the recommendation of transforming ICSJ from a biennial event to an annual event. There have been two biennial events in Japan sponsored by IEEE CPMT Society: VLSI Package Workshop and System Packaging Workshop. The recommendation was to merge these two biennial events to make one annual event, which shall accelerate the growth of both events. a consensus was reached that Kishio Yokouchi, Co-chair of IEEE CPMT Japan Chapter, would look into the possibility of the merger of two events, after resolving the sponsorship issue of IEEE Computer Society to the System Packaging Workshop.

Attendee's survey indicated complete satisfaction to the authors' interview system, which enabled much more interactions and inspiration between speakers and session attendees. Forty percent of participants marked "excellent" on the interviews and 30% on the reception, which was boosted up by the high-spirit talks delivered by the chairs and invited guests. Furthermore, high quality plenary keynotes were another merit commended by ICSJ2010 attendees.

IEEE Semiconductor Wafer Test Workshop

June 6 to 9, 2010 at Rancho Bernardo Inn, San Diego, CA
Submitted by Jerry Broz, Ph.D., General Chair of
IEEE SW Test Workshop and IEEE Senior Member.

The 20th Annual IEEE Semiconductor Wafer Test Workshop (SW Test) was held at the Rancho Bernardo Inn in San Diego, CA, from June 6 to 9, 2010. This annual workshop brings together technologists, engineers, and managers as well as sales and marketing professionals involved with all aspects of probe technology and wafer level testing. SW Test 2010 consisted of a technical program, supplier exhibits (which ARE NOT open during the technical sessions), and a Casino Royale Social Event as well as plenty of time for informal interaction and networking with colleagues. Total conference and EXPO attendance was 270 with approximately 23% international attendees representing 14 countries. This year, SW Test also had a good mix of end-users (~28%) and suppliers (~72%) in attendance.

After the welcome reception on Sunday evening, Jerry Broz, Ph.D., SW Test General Chair, gave a short, "Probe Year In Review" during which he paid tribute to three key probe technologists that passed away during the 12-months – Frank Pietzschmann (Qimonda AG and SW Test Committee Member), Brett Crump (Micron Technology and SW Test Technical Chair), and Bill Mann (founder of SW Test Workshop). Dr. Broz also announced his work with the IEEE Foundation to establish a *William R. Mann Memorial Student Grant Fund*.

Dr. Broz reviewed SIA statistics which highlighted exactly how bad 2009 was for the semiconductor industry, e.g., FAB utilization fell below 60% during the first quarter, etc. Only three of the top twenty semiconductor companies, Samsung, Qualcomm and MediaTek, showed any revenue growth. Interestingly, Qualcomm and MediaTek (which showed growth of +21%) are FAB-less semiconductor companies. Not surprisingly, the bad year was reflected in the VLSI Research probe card market overview released in May. Total probe card revenue was down ~29% (from ~$1.0B in 2008 to ~$700M in 2009). The top three probe card suppliers remained unchanged – (1) FormFactor; (2) Micronics Japan (MJC), and (3) Japan Electronic Materials (JEM); however, all three companies experienced reduced revenue. Microprobe, Inc., moved from 9th to 5th and was the only company in the Top 10 that showed increased revenue.

Dean Freeman, VP of Research at Gartner Research, made the Keynote Presentation entitled, "*What's Going to Rock Your World – Or At Least Push Your Probes*". Mr. Freeman focused on three "hot" technologies that Gartner Research believes will drive semiconductor demand – (1) Cloud Computing, (2) Green Tech/IT, and (3) Social Computing. For Cloud Computing, Gartner expects an infrastructure where the "dumb" terminals will access a more powerful centralized computing resource. Demands for renewable energy will continue to drive Green Tech/IT with the applications for energy generation, reduced consumption, and forms of energy storage. Gartner also predicts that Social Computing demands, such as twitter®, Facebook®, etc., of the "connected" generation will further accelerate and drive adoption of mobile devices with further access to an more "real-time", yet secure, network infrastructure.

Mr. Freeman discussed that chasing Moore's Law will require each IDM to have "extremely deep pockets". In fact, such technology development might only be attained by Intel, Samsung, Toshiba, and large foundries such as TSMC, UMC, or GlobalFoundries. The transition to 450-mm wafers will be a "large" part of the future and has become a constructive dialog such that prototype FABs might be tooling up in 2016 to 2017 and production-level FABs ready as early as 2018 to 2020. Finally, Dean showed that the semiconductor industry seems to be back on track and expects ~27% growth for 2010. It is possible that the semi-market could finally cross the $300B threshold in 2011. The complete version of Dean Freeman's keynote presentation is available for download on the SW Test website (http://www.swtest.org).

On Monday morning Dr. Jerry Broz welcomed attendees to the 20th Annual SW Test Workshop and the technical program had presentations covering every facet of the wafer test process from *Developments for Improved Scribeline Probing* to *Large Area*

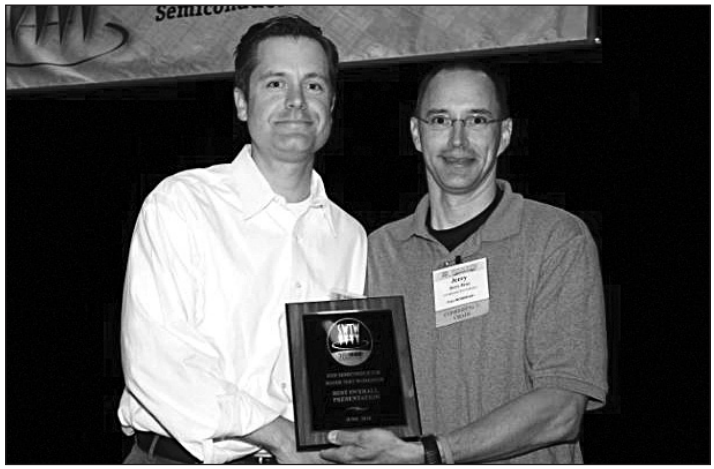
Networking.

Array Probing. Individual highlights from the program included an overview of the benefits of flip chip wafer sort using MEMs multi-site capability by Lo Wee Tick (GlobalFoundries). John Hite (Texas Instruments) discussed standardization of wafer socket spring-pin probe cards for a cost effective approach to chip scale package testing. Ray Robertazzi (IBM Research) outlined an approach for new directions in parametric and defect structure testing. The task of addressing operating challenges needed for full wafer contactors under demanding wafer sort conditions was presented by Keith Breinlinger, Ph.D., from FormFactor. The importance of a correlated probecard analysis and probemark inspection methods for optimizing test cell performance was detailed by Rey Rincon (Freescale) and Jeff Greenberg (Rudolph Technologies). Assessing current carrying capacity using a standard and consistent methodology was detailed by Matt Zeman, Ph.D., (Intel Corporation). Technical hurdles experienced for optimization to reduce cost of ownership were reviewed by Thomas Logue (Seagate – Ireland). Ryan Satrom and Jason Mroczkowski (Multitest | ECT) and Gert Hohenwarter (GateWave Northern) discussed the importance of signal integrity within challenging wafer test environment. Overall, the technical program had 27 podium presentations with 60% from suppliers, 15% from semiconductor manufacturers, and 25% collaborative presentations from both manufacturers and suppliers.

Technical Program 2010.

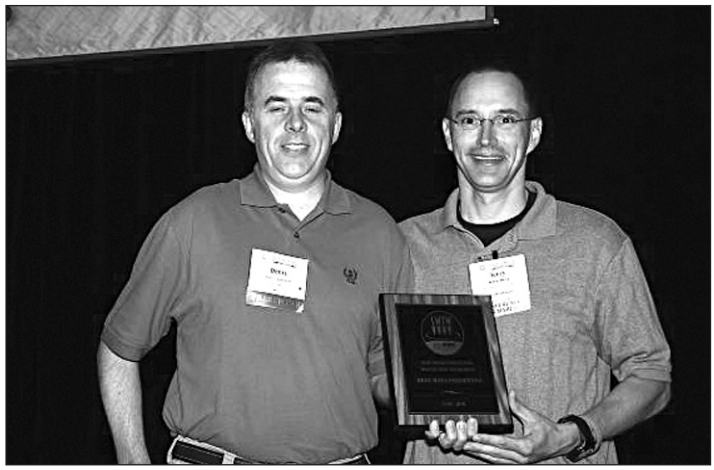
Best Presentation was awarded to Matt Losey, Ph.D., (Touchdown Technologies) for his team's work on "Low-Force MEMS Probe Solution for Full Wafer Single Touch Test"; ***Best Data Presented*** went to Denis Deegan (Analog Devices, Inc.) for his presentation on "Contacting Various Metal Compositions Using ViProbe® Vertical Technology"; ***Best Presentation, Tutorial in Nature***, went to Michael Huebner, Ph.D. (FormFactor, Inc.) for his comprehensive overview on the "High Speed Control Bus for Advanced TRE™"; the ***Most Inspirational Presentation*** was awarded to the two presentations made by SV-Probe Technical Teams of Rehan Kazmi, Ph.D. for work on "Measuring Current Carrying Capability (CCC) of Vertical Probes"; and to Senthil Theppakuttai, Ph.D., for "Probing Assessment on Fine Pitch Copper Pillar Solder Bumps". There were many eligible candidates for the now infamous "***Golden Wheelbarrow Full of Crap for the Poorest Disguised Sales Pitch***"; however, the committee decided to keep the award on the shelf until 2011. All the presentations from 2010 as well as previous workshops (1993 to 2009) are available at the SW Test website (http://www.swtest.org).

Best Presentation



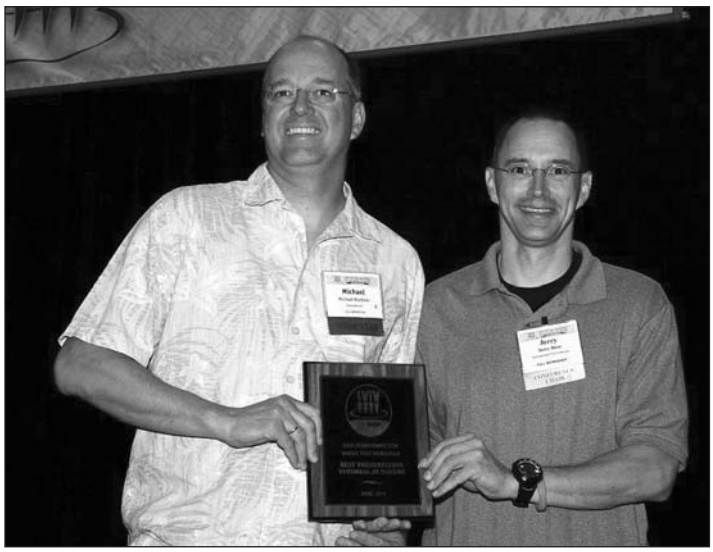
Matt Losey, Ph.D.
(Touchdown Technologies)

Best Data Presented



Denis Deegan
(Analog Devices – Limerick).

Best Presentation, Tutorial in Nature



Michael Huebner, Ph.D.
(FormFactor, Inc.)

Most Inspirational Presentation

Rehan Kazmi, Ph.D. & Senthil Theppakuttai, Ph.D.
(SV-Probe, Inc.)

Technology EXPO 2010.

SW Test EXPO had 28 industry exhibitors and four Corporate Supporters (Acme Technology, Inc., Advanced Probing Systems, International Test Solutions, and JEM America). During the EXPO, all aspects of the wafer sort industry and associated infrastructure suppliers were represented with most probe card vendors, major prober equipment manufacturers, probe card analyzer and probe process metrology companies, companies specializing in probe card cleaning, micro-pogo pin suppliers, and a variety of other probe related service providers.

The 21st Annual IEEE SW Test Workshop and Tech EXPO will be held on *June 12 to 15, 2011* at the Rancho Bernardo Inn, San Diego, CA (http://www.ranchobernardoinn.com). Abstract submission for podium and poster presentations will be open starting January 1, 2011.

IEEE Components, Packaging and Manufacturing Technology Society
Marsha Tickman, Executive Director
445 Hoes Lane
Piscataway, NJ 08854 USA

Upcoming CPMT Society Conferences....

Name: 5th Int'l Microsystems, Packaging, Assembly and Circuits Technology (IMPACT 2010)
Dates: October 20–22, 2010
Location: Taipei, Taiwan
E-mail: service@impact.org.tw
URL: http://www.impact.org.tw/2010/General/

Name: 19th IEEE Conference on Electrical Performance of Electronic Packaging & Systems (EPEPS 2010)
Dates: October 24–27, 2010
Location: Austin, TX, USA
Contact: Kelly Sutton
E-mail: epd@engr.arizona.edu

Name: 4th International Conference on 3D System Integration (3DIC 2010)
Dates: November 16–18, 2010
Location: Munich, Germany
Contact: Peter Ramm, Fraunhofer
E-mail: peter.ramm@emft.fraunhofer.de
URL: http://www.3dic-conf.org/

Name: 34th International Electronics Manufacturing Technology Conference (IEMT)
Dates: Nov. 30–Dec. 2, 2010
Location: Melaka, Malaysia
Contact: Tracy Ow Infineon
E-mail: tracy.ow@infineon.com
URL: http://ewh.ieee.org/r10/malaysia/cpmt/iemt.htm

Name: Electrical Design of Advanced Package & Systems Symposium (EDAPS)
Dates: Dec. 7–9, 2010
Location: Singapore
Contact: Dr. Er-Ping Li, A*STAR
E-mail: erpingli@ieee.org
URL: http://www.edaps2010.org/

Name: 12th Electronics Packaging Technology Conference (EPTC 2010)
Dates: December 8–10, 2010
Location: Singapore
E-mail: secretariat@eptc-ieee.net
URL: http://www.eptc-ieee.net/

Name: 3rd International Conference on Thermal Issues in Emerging Technologies, Theory and Applications (ThETA3)
Dates: December 19–22, 2010
Location: Cairo, Egypt
Contact: Mohamed-Nabil Sabry
E-mail: thetaconf@gmail.com
URL: http://www.thetaconf.org/

Name: 27th Int'l Semiconductor Thermal Modeling, Measurement and Management Symposium (SEMI-THERM)
Dates: March 20–24, 2011
Location: San Jose, CA USA
Contact: Tom Tarter
E-mail: ttarter@semi-therm.org
URL: http://www.semi-therm.org/