Publication News....

COMING IN 2011 – NEW OPTIONS FOR SUBSCRIBERS TO CPMT TRANSACTIONS

As previously announced, beginning in January 2011, the CPMT Society will launch the *IEEE Transactions on Components, Packaging, and Manufacturing Technology.* This monthly periodical is a consolidation of the three current CPMT Society Transactions: *Transactions on Advanced Packaging, Transactions on Components and Packaging Technologies* and *Transactions on Electronics Packaging Manufacturing.*

Subscribers will now have access to all CPMT archival technical content in one monthly publication (12 issues annually)—with no worry of missing papers of interest that may have been published in one of the other CPMT Transactions to which they didn't subscribe.

Additionally, subscribers will have new options that allow them to manage their subscription fees and the manner in which they receive the new Transactions—by choosing electronic only (online via IEEE Xplore), print only, or combo (electronic and print).

Those who currently subscribe to at least one of the current CPMT Transactions will receive a 2011 IEEE renewal invoice that includes the new *IEEE Transactions on Components, Packaging, and Manufacturing Technology*—which replaces the current CPMT subscription(s).

The default media type for Member subscribers will be combo (electronic and print). Those who prefer print only or electronic only can make this change when they complete their renewal. For Student subscribers, the default media will be electronic only.

The consolidated Transactions, will be published online monthly (12 issues annually). Print issues will be published bimonthly (six issues annually) and combine two months of online issues.

Questions and feedback on these changes are welcome; please forward to cpmt@ieee.org.

HAVE YOU READ THEM? THE MOST DOWNLOADED CPMT PAPERS

What might you be missing in the CPMT literature?

Following is a list of the top CPMT Transactions papers downloaded in July 2010. Subscribers can access these and other papers on IEEE Xplore.

IEEE Transactions on Advanced Packaging

1) **Effects of Warpage on Fatigue Reliability of Solder Bumps: Experimental and Analytical Studies**, Wei Tan; Ume, I.C.; Ying Hung; Wu, C.F.J.; Issue Date: May 2010 Page(s): 314–322

Out-of-plane displacement (warpage) has been a major thermomechanical reliability concern for board-level electronic packages. Printed wiring board (PWB) and component warpage results principally from coefficient of thermal expansion mismatch among the materials that make up the PWB assembly (PWBA). Warpage occurring during surface-mount assembly reflow processes and normal operations may lead to severe solder bump reliability problems. In this research, the effect of initial PWB warpage on the low cycle thermal fatigue reliability of the solder bumps in plastic ball grid array (PBGA) packages was studied using experimental and analytical methods. A real-time projection moireÂ¿ warpage measurement system was used to measure the surface topology of PWBA samples at different temperatures. The thermal fatigue reliability of solder bumps was evaluated from experimental thermal cycling tests and finite element simulation results. Three-dimensional (3-D) models of PWBAs with varying board warpage were used to estimate the solder bump fatigue life for different types of PBGAs mounted on PWBs. In order to improve the accuracy of FE results, the projection moireÂ¿ method was used to measure the initial warpage of PWBs, and this warpage was used as a geometric input to the finite element method. The simulation results were validated and correlated with the experimental results obtained using the projection moireÂ¿ technique and accelerated thermal cycling tests. An advanced prediction model was generated to predict board level solder bump fatigue life based on the initial PWB warpage, package dimensions and locations, and solder bump materials.

2) **Guaranteed Passive Parameterized Admittance-Based Macromodeling** Ferranti, F.; Knockaert, L.; Dhaene, T.; Issue Date: Aug. 2010 Page(s): 623–629

We propose a novel parametric macromodeling technique for admittance and impedance input-output representations parameterized by design variables such as geometrical layout or substrate features. It is able to build accurate multivariate macromodels that are stable and passive in the entire design space. An efficient combination of rational identification and interpolation schemes based on a class of positive interpolation operators, ensures overall stability and passivity of the parametric macromodel. Numerical examples validate the proposed approach on practical application cases

3) **Packaging of Dual-Mode Wireless Communication Module Using RF/Optoelectronic Devices With Shared Functional Components** Jun Liao; Juan Zeng; Shengling Deng; Boryssenko, A.O.; Joyner, V.M.; Huang, Z.R.; Issue Date**:** May 2010 Page(s): 323–332

This paper reports the design, fabrication, and testing of a compact radio-frequency (RF)/ free space optical (FSO) dual mode wireless communication system. A modified split dual-director quasi-Yagi antenna is integrated with optical transmitter and receiver by sharing layout structural components. Bare die vertical-cavity surface-emitting laser (VCSEL) and P-i-N photodiode (PIN) are

placed on antenna director pads and wire bonded to printed circuit board (PCB)-mounted laser driver and transimpedance amplifier (TIA) circuits. Detailed analysis of coupling between RF channel and associated electrical connections for the FSO channel is presented using commercial simulation tools to predict its impact on link degradation. Although crosstalk appears between RF and optical channels, the prototyped system demonstrated dual-mode high-rate communication capability with measured 2.5 Gb/s data rate in FSO link. Variations in RF subsystem features due to coupling from the FSO subsystem is estimated through radiation pattern measurement using near-field scanner.

Transactions on Components and Packaging Technologies

1) **Analytical and Numerical Modeling of the Thermal Performance of Three-Dimensional Integrated Circuits** Jain, A.; Jones, R.E.; Chatterjee, R.; Pozder, S.; Issue Date: March 2010 Page(s): 56–63

Three-dimensional (3D) interconnection technology offers several electrical advantages, including reduced signal delay, reduced interconnect power, and design flexibility. 3D integration relies on through-silicon vias (TSVs) and the bonding of multiple active layers to stack several die or wafers containing integrated circuits (ICs) and provide direct electrical interconnection between the stacked strata. While this approach provides several electrical benefits, it also offers significant challenges in thermal management. While some work has been done in the past in this field, a comprehensive treatment is still lacking. In the current work, analytical and finite-element models of heat transfer in stacked 3D ICs are developed. The models are used to investigate the limits of thermal feasibility of 3D electronics and to determine the improvements required in traditional packaging in order to accommodate 3D ICs. An analytical model for temperature distribution in a multidie stack with multiple heat sources is developed. The analytical model is used to extend the traditional concept of a single-valued junction-to-air thermal resistance in an IC to thermal resistance and thermal sensitivity matrices for a 3D IC. The impact of various geometric parameters and thermophysical properties on thermal performance of a 3D IC is investigated. It is shown that package and heat sink thermal resistances play a more important role in determining temperature rise compared to thermal resistances intrinsic to the multidie stack. The improvement required in package and heat sink thermal resistances for a 3D logic-on-memory implementation to be thermally feasible is quantified. An increase in maximum temperature in a 3D IC compared to an equivalent system-in-package (SiP) is predicted. This increase is found to be mainly due to the reduced chip footprint. The increased memory die temperature in case of memory-on-logic integration compared to a SiP implementation is identified to be a sig- nificant thermal management challenge in the future. The results presented in this paper may be useful in the development of thermal design guidelines for 3D ICs, which are expected to help maximize the electrical benefits of 3D technology without exacerbating thermal management issues when implemented in early-stage electrical design and layout tools.

2) **Dynamic lithium-ion battery model for system simulation** Lijun Gao; Shengyi Liu; Dougal, R.A Issue Date: September 2002 Page(s): 495–505

Presents here a complete dynamic model of a lithium ion battery that is suitable for virtual-prototyping of portable battery-powered systems. The model accounts for nonlinear equilibrium potentials, rate- and temperature-dependencies, thermal effects and response to transient power demand. The model is based on publicly available data such as the manufacturers' data sheets. The Sony US18650 is used as an example. The model output agrees both with manufacturer's data and with experimental results. The model can be easily modified to fit data from different batteries and can be extended for wide dynamic ranges of different temperatures and current rates.

3) **Development of 3-D Silicon Module With TSV for System in Packaging** Khan, N.; Rao, V.S.; Lim, S.; Ho Soon We; Lee, V.; Xiaowu Zhang; Liao, E.B.; Nagarajan, R.; Chai, T.C.; Kripesh, V.; Lau, J.H. Issue Date: March 2010 Page(s): 3–9

Portable electronic products demand multifunctional module comprising of digital, radio frequency and memory functions. Through silicon via (TSV) technology provides a means of implementing complex, multifunctional integration with a higher packing density for a system in package. A 3-D silicon module with TSV has been developed in this paper. Thermo-mechanical analysis has been performed and TSV interconnect design is optimized. Multiple chips representing different functional circuits are assembled using wirebond and flip chip interconnection methods. Silicon carrier is fabricated using via-first approach, the barrier copper via is exposed by the backgrinding process. A two-stack silicon module is developed and module fabrication details are given in this paper. The module reliability has been evaluated under temperature cycling (–40/125Â°C) and drop test.

Transactions on Electronics Packaging Manufacturing

1) **Development of Warpage Measurement System to Simulate Convective Solder Reflow Process** Powell, R.E.; Ume, I.C.; Issue Date: Jan 2008 Page(s): 83–90

In this paper, a warpage measurement system to simulate forced convective reflow is discussed. A warpage measurement system that can simulate convective reflow enables the real-time monitoring of printed wiring boards (PWBs), PWB assemblies (PWBAs), and chip package warpage during the reflow process. This paper will describe the two major parts of the warpage measurement system: the optical measurement part which utilizes the projection Moire method and advanced image processing, as well as the laboratory oven which is used to simulate forced convective reflow. This is the first system that allows PWB/PWBA/chip package warpage to be measured during a simulated convective reflow process. Also, this is the first system that employs automatic image segmentation to separately extract the warpage of the PWB and electronic components from the same measurement. The results will show that when compared to infrared heating which was previously used in this research area, convective heating minimizes thermal gradients on the PWB/PWBA sample. Thermal gradients on the PWB/PWBA sample have the inadvertent effect of inducing warpage into the sample and will interfere with the warpage measurement result. In the first design iteration presented

in this paper, the system can simulate low ramp rate industrial convective reflow profiles and simultaneously measure the warpage of PWBAs. A computational fluid dynamics (CFD) model of the system was developed to determine how to increase the system's heating rate. The CFD model was used to perform a design of simulations (DOS) and regression analysis. The validated regression results will be used to predict oven design parameters to enable the next iteration of the convective system to simulate high ramp rate convective reflow profiles. This paper will show that the presented system is a powerful tool for measuring the warpage of PWBs, PWBAs, and chip packages.

2) **Electron beam lithography in nanoscale fabrication: recent development** Tseng, A.A.; Kuan Chen; Chen, C.D.; Ma, K.J.; Issue Date: April 2003 Page(s): 141–149

Miniaturization is the central theme in modern fabrication technology. Many of the components used in modern products are getting smaller and smaller. In this paper, the recent development of the electron beam lithography technique is reviewed with an emphasis on fabricating devices at the nanometer scale. Because of its very short wavelength and reasonable energy density characteristics, e-beam lithography has the ability to fabricate patterns having nanometer feature sizes. As a result, many nanoscale devices have been successfully fabricated by this technique. Following an introduction of this technique, recent developments in processing, tooling, resist, and pattern controlling are separately examined and discussed. Examples of nanodevices made by several different e-beam lithographic schemes are given, to illustrate the versatility and advancement of the e-beam lithography technique. Finally, future trends in this technique are discussed.

3) **Acid Decapsulation of Epoxy Molded IC Packages With Copper Wire Bonds** Murali, S.; Srikanth, N.; Issue Date: July 2006 Page(s): 179–183

Epoxy molded IC packages with copper wire bonds are decapsulated using mixtures of concentrated sulfuric acid (20%) and fuming nitric acid in an automatic decapping unit and, observed with minimal corrosion of copper wires (0.8-6 mil sizes) and bond interfaces. To attain maximum cross-linking of the molded epoxies, the post mold cured packages (175 degC for 4 h) were further, aged at high temperature of 150 degC for 1000 h. These packages are decapsulated using mixtures of higher ratio of concentrated sulfuric acid (40%) along with fuming nitric acid. The shear strength of copper wire bonds with 1 mil (25 mum) diameter of the decapsulated unit is higher than 5.5 gf/mil2. The present study shows copper stitch bonds to Au, Cu, Pd, and Sn alloy plated surfaces are less affected on decapping, with a few grams of breaking load on stitch pull test, while stitch bonds on silver plated surfaces reveal lifting of wire bonds on decapping

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BOOK REVIEW: PORTABLE CONSUMER ELECTRONICS: PACKAGING, MATERIALS, AND RELIABILITY

By Sridhar Canumalla and Puligandla Viswanadham
Published by PennWell

This book titled "Portable Consumer Electronics: Packaging, Materials, Reliability" is written by two veteran technologists in the industry for engineers working in the field of Portable Consumer Electronics. The authors said in the Preface, "This book is written at a level that assumes only a basic knowledge in the fundamentals of physics, chemistry and engineering at the undergraduate level." It is written for the practicing packaging engineers in the portable electronics sector of our industry. As the title indicates authors have focused their writing on packaging (a la assembly), materials, and reliability. The authors have years of distinguished career in the industry, including the portable consumer electronics industry. They have invested their knowledge and experience in the pages of this book.

The words "Portable Consumer Electronics Products" cover a broad spectrum of electronic products with diverse packaging requirements. However there is a common thread of portability and consumer requirements that sets it apart in Packaging Technology from other electronic products. While much of the technologies are fundamental to all aspects of the packaging industry, it is the focus and practice that distinguish this book from the other packaging technology books.

Chapter 1 introduces the topic of Portable Consumer Electronics with a specific description of what "portability index" means. Chapter 2 articulates the technical challenges in packaging for the portable electronics products. Chapters 3 to 6 cover the topics of PWB technology, first level packaging, 2nd level packaging and board assembly, i.e. the topic of packaging, assembly and materials. Chapters 7 to 9 cover reliability statistics, reliability, and failures and prevention. The last chapter, titled Future Trends in Portable Electronics Products, is devoted to an educated look at what the needs are for future electronic products and what technology and materials are in development to meet those needs. An excellent feature in this book is the reference section at the end of each chapter and suggested reading to help the readers to dig deeper.

I enjoyed reading this book. The three chapters on Reliability Statistics, Reliability of Electronic Assemblies, and Failure and Prevention are particularly valuable for the practicing engineers. These are areas where classroom knowledge is seldom enough as many of us have learned from painful experiences. The authors have lovingly shared their expert knowledge and collective experiences in those pages.

Portable Consumer Electronics is a fast expanding market with rapidly evolving product functions and packaging technologies. This book is a good compelling read for the practicing engineers in the field and a ready relevant reference in their library. It is a very good and worthwhile addition to our literature.

Reviewed by:
William T. Chen
Senior Technical Advisor, ASE US
IEEE CPMT President, 2006-2009