

IEEE CPMT SYMPOSIUM JAPAN (10TH VLSI PACKAGE WORKSHOP IN JAPAN)

“IEEE VLSI Package Workshop in Japan” has been held every other year since 1992 and reached the tenth anniversary this year. Based on several considerations, this Workshop has been transformed this year to “IEEE CPMT Symposium Japan” (ICSJ) by the joint effort of IEEE CPMT Japan Chapter and the organizing committee. ICSJ intends to provide researchers and engineers who wish to extend their activities beyond borders with opportunities to exchange technical knowledge and perspective.

ICSJ2010 was held at the University of Tokyo, Japan, from Aug. 24 to 26, 2010—it was the hottest summer in Japan since the Japan Weather Bureau started monitoring climate 113 years ago. As the heat waves at Tokyo smashed the record, in the meanwhile, the number of ICSJ2010 participants also hit the record high of 183, versus the past record of 141. Seventy papers (27 from overseas) out of 86 abstracts were selected and presented in ICSJ2010. IEEE CPMT Society offered the subsidy to the new enrollment fee of IEEE and CPMT Society and received 10 applications during the Symposium.

There were two unique features in ICSJ2010. One is authors’ interviews. During the break following the session, the presenters were requested to stay in front of their posters (hardcopies of ppt files) to answer questions from session attendees. Such interviews were proposed to make up the short Q&A time during the session and to promote close interactions between speakers and audience. The other feature was transparent walls between the rooms and the reception hall, which allowed people to see the status of presentations from outside the rooms and lured people from their conversation outside to the sessions inside.

EVENT HIGHLIGHTS

As a pre-conference workshop, ITRS workshop was held on Aug. 23, 2010, by Assembly and Packaging TWG of ITRS and the roadmap committee of Japan Electronics and Information Technology Industries Association (JEITA), with 26 attendees. The agenda included ITRS 2009 brief introduction, ITRS 2010 update, ITRS 2011 activity plan, Japan Jisso Roadmap (JJTR 2009), MEMS roadmap, and the panel discussion about difficult challenges.

On Aug. 24, the Symposium was opened by the remarks from Hirofumi Nakajima, Executive Chair of ICSJ2010, and then the welcome speech from Rolf Aschenbrenner, President of IEEE

CPMT Society. Three plenary talks were presented in the morning of the opening day, namely, “Materials – Crucial Enabler for Packaging Innovation” by William Chen (ASE US), “Difficult Challenges and Potential Solutions for Advanced Packaging” by Bill Bottoms (3MTS), and “Recent Advances on Nano-materials for Advanced Packaging Applications” by C. P. Wong (The Chinese University Hong Kong). After the plenary session, people split into three sessions: advanced package, board level reliability, and electrical design, for paper presentations.

On Aug. 25, Ricky Lee, Vice Chair of ICSJ2010, chaired the plenary session. Three keynotes were delivered, namely, “Recent Progress in Surface Activated Bonding Method” by Tadatomo Suga (University of Tokyo), “3D System-in-Package Technologies for Multifunctional Systems” by Klaus-Dieter Lang (Fraunhofer IZM), and “3D System Integration - Opportunities and Challenges in the Supply Chain” by Eric Beyne (IMEC). After the plenary session, people split into three sessions: 3D integration, mechanical design, and optical vs. electrical, for paper presentations.

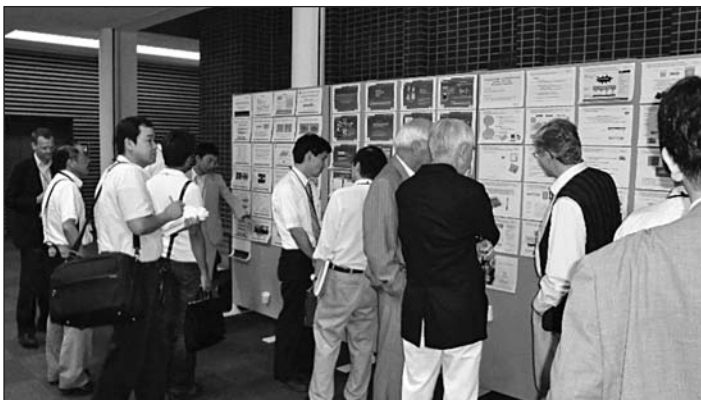
On Aug. 26, Hiroshi Yamada, Vice Chair of ICSJ2010, chaired the plenary session. The keynotes on that day were “3D Packaging Trends: From Stacked Die to 3D ICs with TSV” by Jan Vardaman (TechSearch), and “Advanced Electrical Measurement and Evaluation Technology for 3D LSI Chip Stacking Integration Technology” by Masahiro Aoyagi (AIST). After the plenary session, people split into three sessions: thermal design, materials, and optoelectronics. The materials and optoelectronics sessions had the largest number of papers among sessions, reflecting active industries.

AWARDS

Tadatomo Suga, General Chair of ICSJ2010, awarded the best paper award to Hiroshi Yamada for his paper: “A wafer-level system integration technology for flexible pseudo-SOC incorporates MEMS-CMOS heterogeneous devices”; and the young awards to Jonghyun Cho for his paper: “Guard-Ring Effect for Through Silicon Via (TSV) Coupling Reduction”; and Tatsuya Yamashita for his paper: “Polymeric multi/demultiplexers using light-induced self-written waveguides for cost-effective optical interconnection”.

REVIEW AND SURVEY SUMMARY

On the last day, a review meeting was held with CPMT board and organizing committee members over lunch. The main topic



Authors’ interview.



ICSJ Plenary session.

of this discussion was the recommendation of transforming ICSJ from a biennial event to an annual event. There have been two biennial events in Japan sponsored by IEEE CPMT Society: VLSI Package Workshop and System Packaging Workshop. The recommendation was to merge these two biennial events to make one annual event, which shall accelerate the growth of both events. A consensus was reached that Kishio Yokouchi, Co-chair of IEEE CPMT Japan Chapter, would look into the possibility of the merger of two events, after resolving the spon-

sorship issue of IEEE Computer Society to the System Packaging Workshop.

Attendee's survey indicated complete satisfaction to the authors' interview system, which enabled much more interactions and inspiration between speakers and session attendees. Forty percent of participants marked "excellent" on the interviews and 30% on the reception, which was boosted up by the high-spirit talks delivered by the chairs and invited guests. Furthermore, high quality plenary keynotes were another merit commended by ICSJ2010 attendees.

IEEE Semiconductor Wafer Test Workshop

June 6 to 9, 2010 at Rancho Bernardo Inn, San Diego, CA

Submitted by Jerry Broz, Ph.D., General Chair of
IEEE SW Test Workshop and IEEE Senior Member.

The 20th Annual IEEE Semiconductor Wafer Test Workshop (SW Test) was held at the Rancho Bernardo Inn in San Diego, CA, from June 6 to 9, 2010. This annual workshop brings together technologists, engineers, and managers as well as sales and marketing professionals involved with all aspects of probe technology and wafer level testing. SW Test 2010 consisted of a technical program, supplier exhibits (which ARE NOT open during the technical sessions), and a Casino Royale Social Event as well as plenty of time for informal interaction and networking with colleagues. Total conference and EXPO attendance was 270 with approximately 23% international attendees representing 14 countries. This year, SW Test also had a good mix of end-users (~28%) and suppliers (~72%) in attendance.

After the welcome reception on Sunday evening, Jerry Broz, Ph.D., SW Test General Chair, gave a short, "Probe Year In Review" during which he paid tribute to three key probe technologists that passed away during the 12-months – Frank Pietzschmann (Qimonda AG and SW Test Committee Member), Brett Crump (Micron Technology and SW Test Technical Chair), and Bill Mann (founder of SW Test Workshop). Dr. Broz also announced his work with the IEEE Foundation to establish a *William R. Mann Memorial Student Grant Fund*.

Dr. Broz reviewed SIA statistics which highlighted exactly how bad 2009 was for the semiconductor industry, e.g., FAB utilization fell below 60% during the first quarter, etc. Only three of the top twenty semiconductor companies, Samsung, Qualcomm and MediaTek, showed any revenue growth. Interestingly, Qualcomm and MediaTek (which showed growth of +21%) are FAB-less semiconductor companies. Not surprisingly, the bad year was reflected in the VLSI Research probe card market overview released in May. Total probe card revenue was down ~29% (from ~\$1.0B in 2008 to ~\$700M in 2009). The top three probe card suppliers remained unchanged – (1) FormFactor; (2) Micronics Japan (MJC), and (3) Japan Electronic Materials (JEM); however, all three companies experienced reduced revenue. Microprobe, Inc., moved from 9th to 5th and was the only company in the Top 10 that showed increased revenue.

Dean Freeman, VP of Research at Gartner Research, made the Keynote Presentation entitled, "*What's Going to Rock Your World*

– *Or At Least Push Your Probes*". Mr. Freeman focused on three "hot" technologies that Gartner Research believes will drive semiconductor demand – (1) Cloud Computing, (2) Green Tech/IT, and (3) Social Computing. For Cloud Computing, Gartner expects an infrastructure where the "dumb" terminals will access a more powerful centralized computing resource. Demands for renewable energy will continue to drive Green Tech/IT with the applications for energy generation, reduced consumption, and forms of energy storage. Gartner also predicts that Social Computing demands, such as twitter®, Facebook®, etc., of the "connected" generation will further accelerate and drive adoption of mobile devices with further access to an more "real-time", yet secure, network infrastructure.

Mr. Freeman discussed that chasing Moore's Law will require each IDM to have "extremely deep pockets". In fact, such technology development might only be attained by Intel, Samsung, Toshiba, and large foundries such as TSMC, UMC, or GlobalFoundries. The transition to 450-mm wafers will be a "large" part of the future and has become a constructive dialog such that prototype FABs might be tooling up in 2016 to 2017 and production-level FABs ready as early as 2018 to 2020. Finally, Dean showed that the semiconductor industry seems to be back on track and expects ~27% growth for 2010. It is possible that the semi-market could finally cross the \$300B threshold in 2011. The complete version of Dean Freeman's keynote presentation is available for download on the SW Test website (<http://www.swtest.org>).

On Monday morning Dr. Jerry Broz welcomed attendees to the 20th Annual SW Test Workshop and the technical program had presentations covering every facet of the wafer test process from *Developments for Improved Scribeline Probing to Large Area*



Networking.