of this discussion was the recommendation of transforming ICSJ from a biennial event to an annual event. There have been two biennial events in Japan sponsored by IEEE CPMT Society: VLSI Package Workshop and System Packaging Workshop. The recommendation was to merge these two biennial events to make one annual event, which shall accelerate the growth of both events. a consensus was reached that Kishio Yokouchi, Co-chair of IEEE CPMT Japan Chapter, would look into the possibility of the merger of two events, after resolving the sponsorship issue of IEEE Computer Society to the System Packaging Workshop.

Attendee's survey indicated complete satisfaction to the authors' interview system, which enabled much more interactions and inspiration between speakers and session attendees. Forty percent of participants marked "excellent" on the interviews and 30% on the reception, which was boosted up by the high-spirit talks delivered by the chairs and invited guests. Furthermore, high quality plenary keynotes were another merit commended by ICSJ2010 attendees.

IEEE Semiconductor Wafer Test Workshop

June 6 to 9, 2010 at Rancho Bernardo Inn, San Diego, CA
Submitted by Jerry Broz, Ph.D., General Chair of
IEEE SW Test Workshop and IEEE Senior Member.

The 20th Annual IEEE Semiconductor Wafer Test Workshop (SW Test) was held at the Rancho Bernardo Inn in San Diego, CA, from June 6 to 9, 2010. This annual workshop brings together technologists, engineers, and managers as well as sales and marketing professionals involved with all aspects of probe technology and wafer level testing. SW Test 2010 consisted of a technical program, supplier exhibits (which ARE NOT open during the technical sessions), and a Casino Royale Social Event as well as plenty of time for informal interaction and networking with colleagues. Total conference and EXPO attendance was 270 with approximately 23% international attendees representing 14 countries. This year, SW Test also had a good mix of end-users (~28%) and suppliers (~72%) in attendance.

After the welcome reception on Sunday evening, Jerry Broz, Ph.D., SW Test General Chair, gave a short, "Probe Year In Review" during which he paid tribute to three key probe technologists that passed away during the 12-months – Frank Pietzschmann (Qimonda AG and SW Test Committee Member), Brett Crump (Micron Technology and SW Test Technical Chair), and Bill Mann (founder of SW Test Workshop). Dr. Broz also announced his work with the IEEE Foundation to establish a *William R. Mann Memorial Student Grant Fund*.

Dr. Broz reviewed SIA statistics which highlighted exactly how bad 2009 was for the semiconductor industry, e.g., FAB utilization fell below 60% during the first quarter, etc. Only three of the top twenty semiconductor companies, Samsung, Qualcomm and MediaTek, showed any revenue growth. Interestingly, Qualcomm and MediaTek (which showed growth of +21%) are FAB-less semiconductor companies. Not surprisingly, the bad year was reflected in the VLSI Research probe card market overview released in May. Total probe card revenue was down ~29% (from ~$1.0B in 2008 to ~$700M in 2009). The top three probe card suppliers remained unchanged – (1) FormFactor; (2) Micronics Japan (MJC), and (3) Japan Electronic Materials (JEM); however, all three companies experienced reduced revenue. Microprobe, Inc., moved from 9th to 5th and was the only company in the Top 10 that showed increased revenue.

Dean Freeman, VP of Research at Gartner Research, made the Keynote Presentation entitled, "*What's Going to Rock Your World – Or At Least Push Your Probes*". Mr. Freeman focused on three "hot" technologies that Gartner Research believes will drive semiconductor demand – (1) Cloud Computing, (2) Green Tech/IT, and (3) Social Computing. For Cloud Computing, Gartner expects an infrastructure where the "dumb" terminals will access a more powerful centralized computing resource. Demands for renewable energy will continue to drive Green Tech/IT with the applications for energy generation, reduced consumption, and forms of energy storage. Gartner also predicts that Social Computing demands, such as twitter®, Facebook®, etc., of the "connected" generation will further accelerate and drive adoption of mobile devices with further access to an more "real-time", yet secure, network infrastructure.

Mr. Freeman discussed that chasing Moore's Law will require each IDM to have "extremely deep pockets". In fact, such technology development might only be attained by Intel, Samsung, Toshiba, and large foundries such as TSMC, UMC, or GlobalFoundries. The transition to 450-mm wafers will be a "large" part of the future and has become a constructive dialog such that prototype FABs might be tooling up in 2016 to 2017 and production-level FABs ready as early as 2018 to 2020. Finally, Dean showed that the semiconductor industry seems to be back on track and expects ~27% growth for 2010. It is possible that the semi-market could finally cross the $300B threshold in 2011. The complete version of Dean Freeman's keynote presentation is available for download on the SW Test website (http://www.swtest.org).

On Monday morning Dr. Jerry Broz welcomed attendees to the 20th Annual SW Test Workshop and the technical program had presentations covering every facet of the wafer test process from *Developments for Improved Scribeline Probing* to *Large Area*

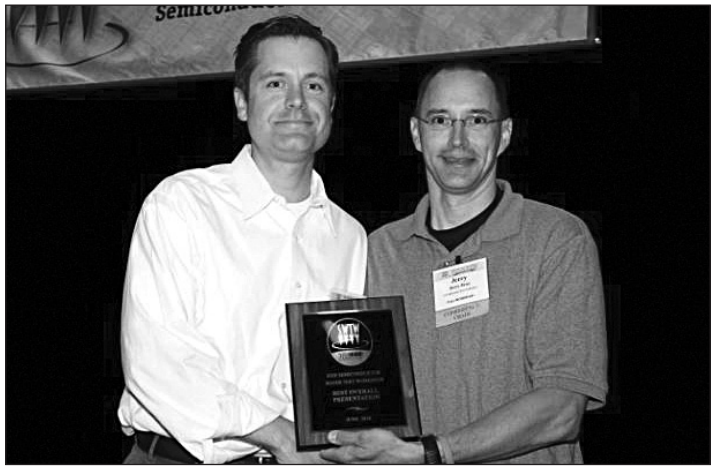
Networking.

Array Probing. Individual highlights from the program included an overview of the benefits of flip chip wafer sort using MEMs multi-site capability by Lo Wee Tick (GlobalFoundries). John Hite (Texas Instruments) discussed standardization of wafer socket spring-pin probe cards for a cost effective approach to chip scale package testing. Ray Robertazzi (IBM Research) outlined an approach for new directions in parametric and defect structure testing. The task of addressing operating challenges needed for full wafer contactors under demanding wafer sort conditions was presented by Keith Breinlinger, Ph.D., from FormFactor. The importance of a correlated probecard analysis and probemark inspection methods for optimizing test cell performance was detailed by Rey Rincon (Freescale) and Jeff Greenberg (Rudolph Technologies). Assessing current carrying capacity using a standard and consistent methodology was detailed by Matt Zeman, Ph.D., (Intel Corporation). Technical hurdles experienced for optimization to reduce cost of ownership were reviewed by Thomas Logue (Seagate – Ireland). Ryan Satrom and Jason Mroczkowski (Multitest | ECT) and Gert Hohenwarter (GateWave Northern) discussed the importance of signal integrity within challenging wafer test environment. Overall, the technical program had 27 podium presentations with 60% from suppliers, 15% from semiconductor manufacturers, and 25% collaborative presentations from both manufacturers and suppliers.

Technical Program 2010.

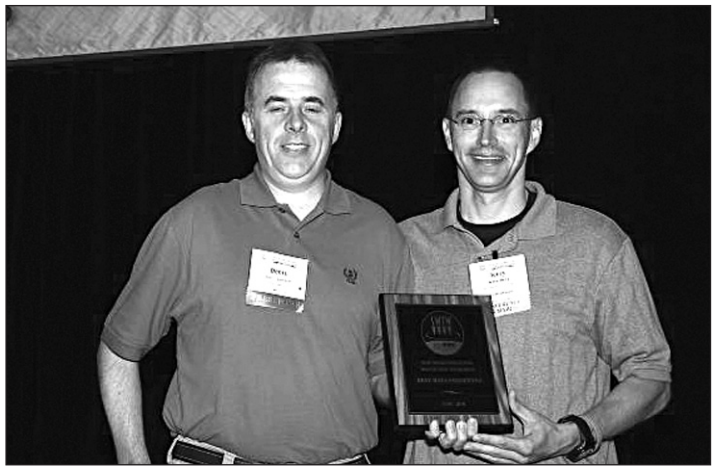
Best Presentation was awarded to Matt Losey, Ph.D., (Touchdown Technologies) for his team's work on "Low-Force MEMS Probe Solution for Full Wafer Single Touch Test"; ***Best Data Presented*** went to Denis Deegan (Analog Devices, Inc.) for his presentation on "Contacting Various Metal Compositions Using ViProbe® Vertical Technology"; ***Best Presentation, Tutorial in Nature***, went to Michael Huebner, Ph.D. (FormFactor, Inc.) for his comprehensive overview on the "High Speed Control Bus for Advanced TRE™"; the ***Most Inspirational Presentation*** was awarded to the two presentations made by SV-Probe Technical Teams of Rehan Kazmi, Ph.D. for work on "Measuring Current Carrying Capability (CCC) of Vertical Probes"; and to Senthil Theppakuttai, Ph.D., for "Probing Assessment on Fine Pitch Copper Pillar Solder Bumps". There were many eligible candidates for the now infamous "***Golden Wheelbarrow Full of Crap for the Poorest Disguised Sales Pitch***"; however, the committee decided to keep the award on the shelf until 2011. All the presentations from 2010 as well as previous workshops (1993 to 2009) are available at the SW Test website (http://www.swtest.org).

Best Presentation



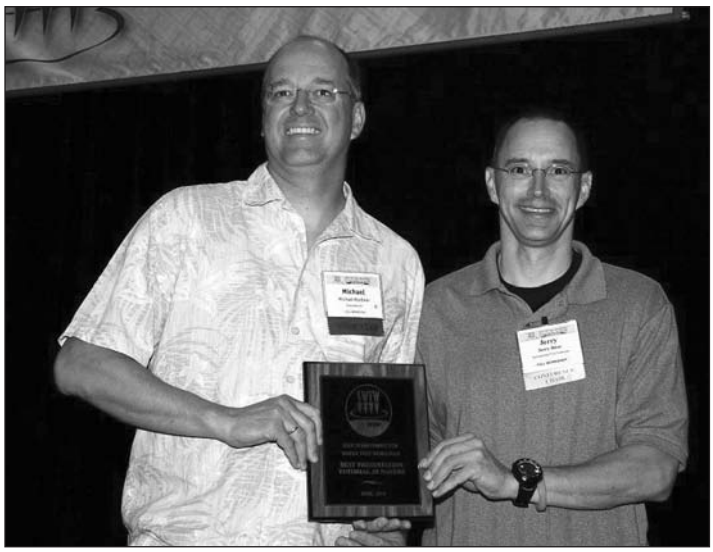
Matt Losey, Ph.D.
(Touchdown Technologies)

Best Data Presented



Denis Deegan
(Analog Devices – Limerick).

Best Presentation, Tutorial in Nature



Michael Huebner, Ph.D.
(FormFactor, Inc.)

Most Inspirational Presentation

Rehan Kazmi, Ph.D. & Senthil Theppakuttai, Ph.D.
(SV-Probe, Inc.)

Technology EXPO 2010.

SW Test EXPO had 28 industry exhibitors and four Corporate Supporters (Acme Technology, Inc., Advanced Probing Systems, International Test Solutions, and JEM America). During the EXPO, all aspects of the wafer sort industry and associated infrastructure suppliers were represented with most probe card vendors, major prober equipment manufacturers, probe card analyzer and probe process metrology companies, companies specializing in probe card cleaning, micro-pogo pin suppliers, and a variety of other probe related service providers.

The 21st Annual IEEE SW Test Workshop and Tech EXPO will be held on *June 12 to 15, 2011* at the Rancho Bernardo Inn, San Diego, CA (http://www.ranchobernardoinn.com). Abstract submission for podium and poster presentations will be open starting January 1, 2011.
