Stack Die CSP Interconnect Challenges

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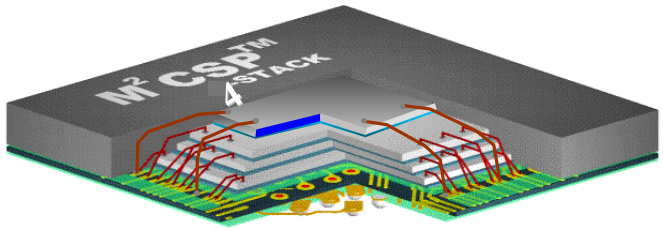
IEEE/CPMT Seminar

Overview



- Stacked die Chip Scale Packages (CSPs) enable more device functionality in a given package area/volume:
  - Economical: the price of a two die stack package is less than two separate packages.
  - Most stacked die packaging solution are wirebond based.
  - Driven primarily by applications requiring miniaturization such as next generation cell phones, portable electronics, etc.
  - Today, 5 die can be stacked in 1.4mm BGA CSP package.

- Stacked die packaging presents many interconnect challenges:
  - Low loop and reverse wirebond formation
  - Wirebonding on thin die, wirebonding on "overhang".
  - Staggered wirebonding

Stacked Die Packaging Trends

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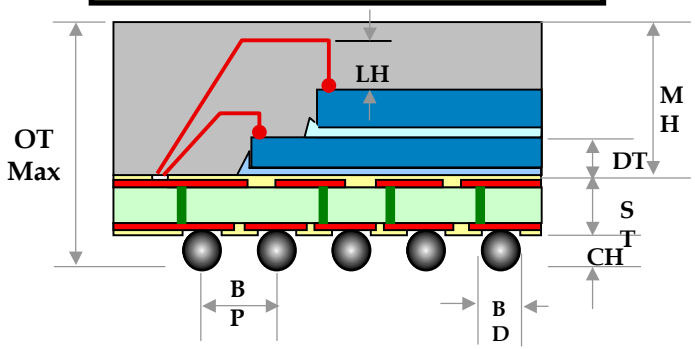
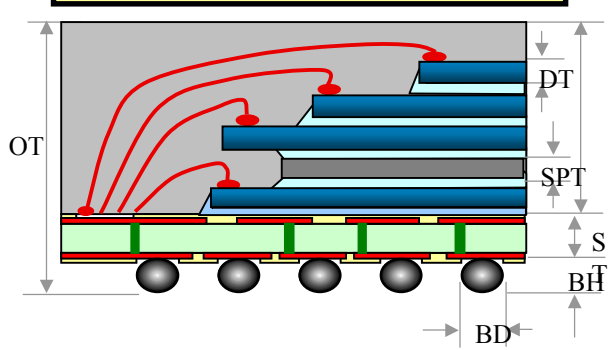
- More die stacked in a typical 1.4mm max CSP package:
  - More memory intensive applications/displays are driving die stacks from typical 2 to 4+.
- Same/Similar Die Stack Capability:
  - Example: 2 X 16M Flash can be stacked in same package to compete with 1 X 32M Flash or Logic and Memory can be stacked in same package.

2 die Stack 1.4mm



	Sym	Description	Type	Dimension (mm) / Package Heigh 1.4mm
Mold Cap	DT	Die Thickness	Max	0.175
	LH	Loop Height	Max	0.175 (fwd)
	MH	Mold Height	Nom	0.700
Substrate	ST	Subst. Th. (2L)	Nom	0.260
Ball	BD	Ball Diam	Nom	0.400
	CH	Collapse Ht	Min	0.250
Status				Avail CPK/CPS

4 + 1 die Stack 1.4mm



	Sym	Description	Type	Dimension (mm) / Package Heigh 1.4mm
Mold Cap	DT	Die Thickness	Max	0.107
	LH	Loop Height	Max	0.089 (rvs)
	MH	Mold Height	Nom	0.830
Substrate	ST	Subst. Th. (2L)	Nom	0.210
Ball	BD	Ball Diam	Nom	0.400
	CH	Collapse Ht	Min	0.230
Status				Avail CPK

Die Thickness Trends

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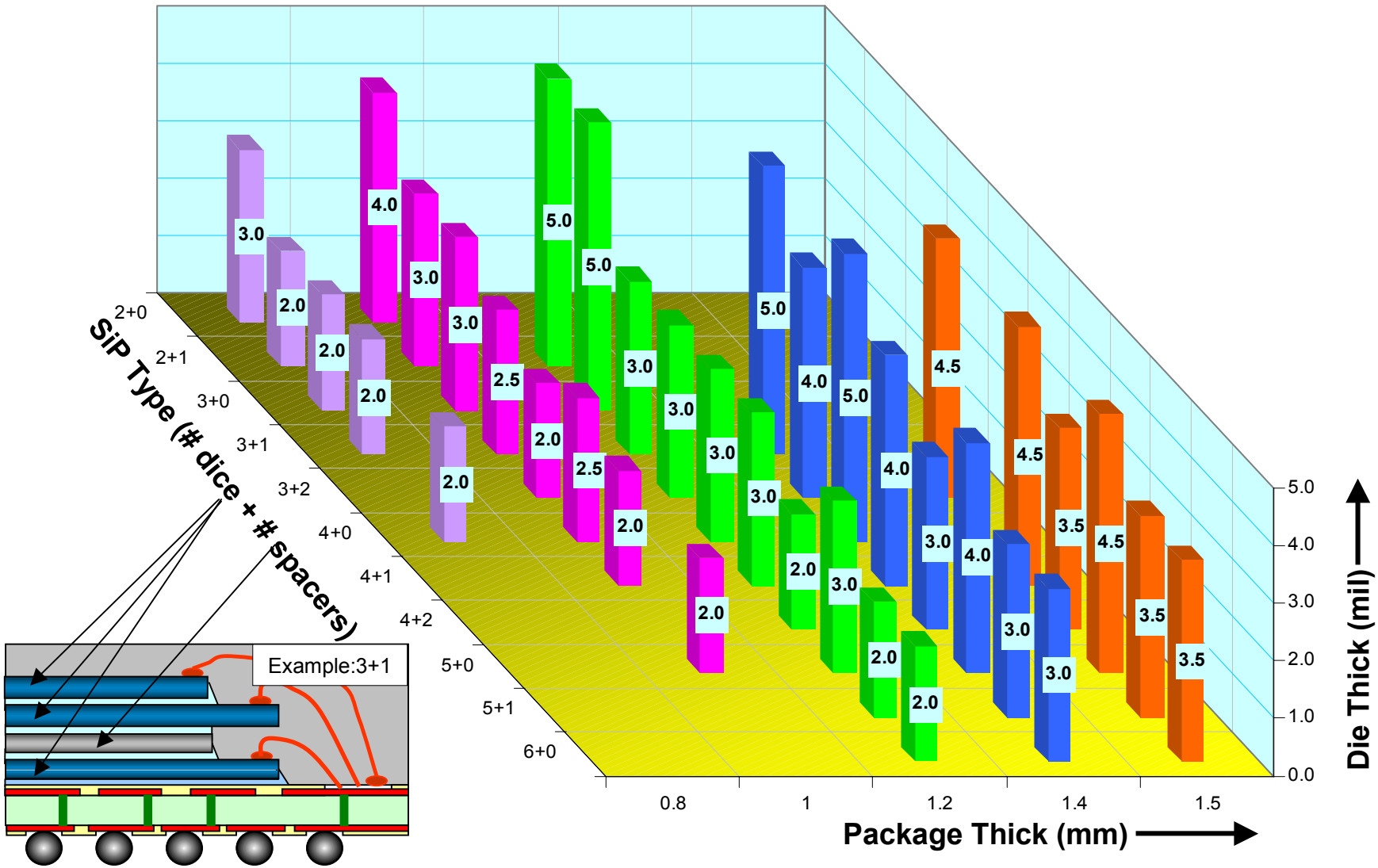

Thin, stacked die packages require very thin die

Die Thickness Roadmap

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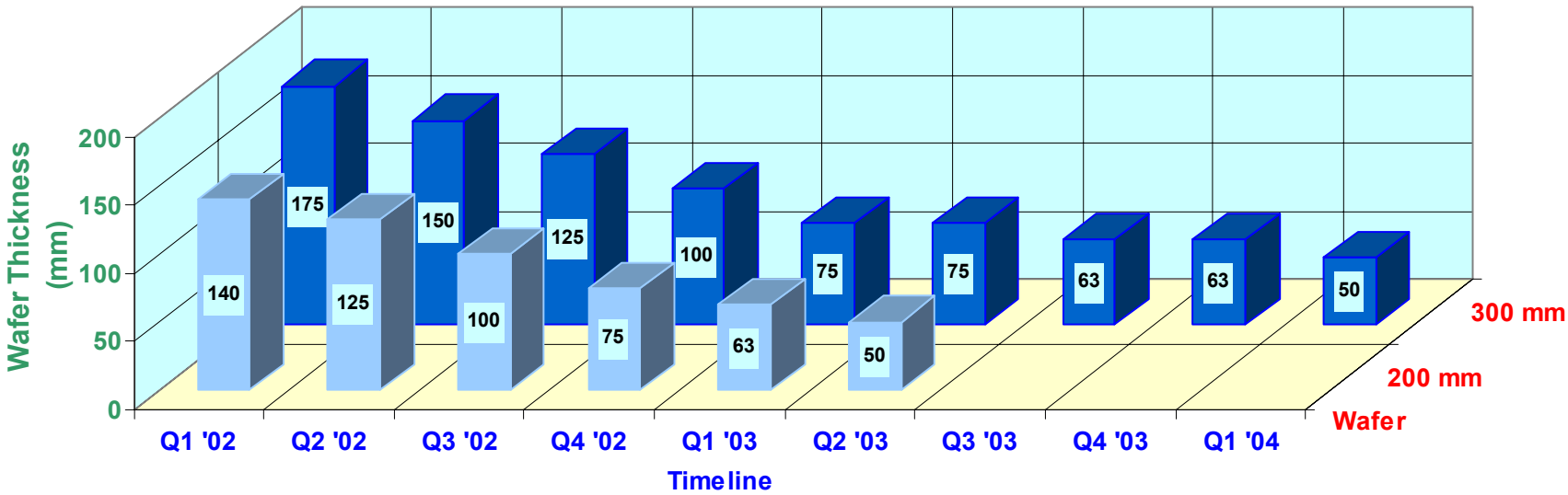

- Wafer thinning available for 200mm and 300mm wafers.
- Wafer thinning is key enabler to stacked die CSP.
- Wafer polishing necessary for <120um thick 200 mm and for <150um thick 300 mm wafers in order to relieve wafer backside grinding stress and warpage.
- In-line processing used from wafer backgrind to saw tape ring mount and backgrind tape removal to minimize wafer handling and breakage.

Stacked Die Bonding Methods

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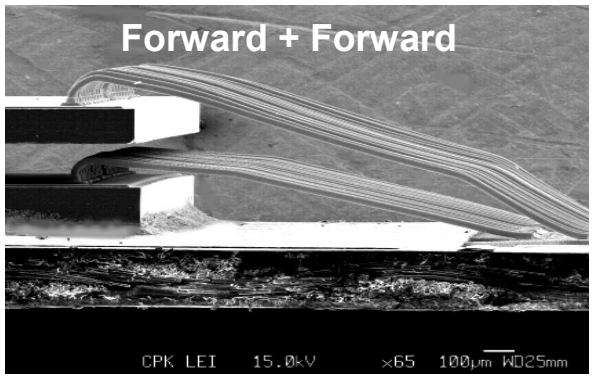
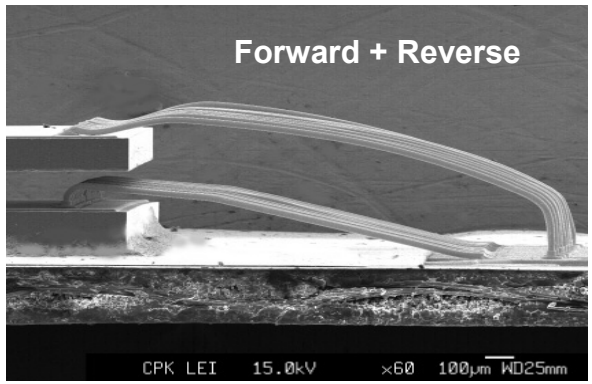
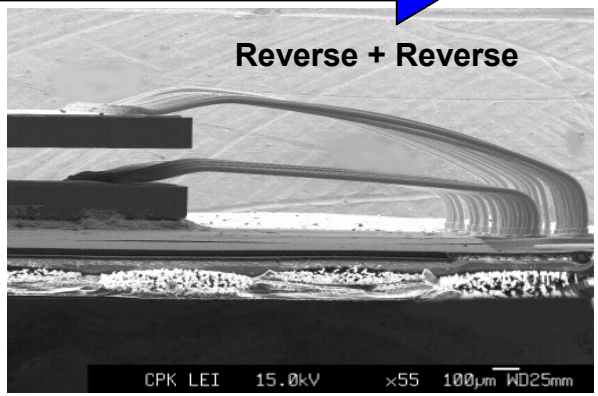
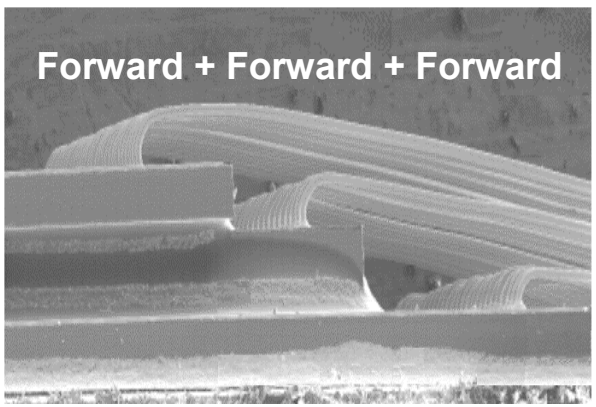
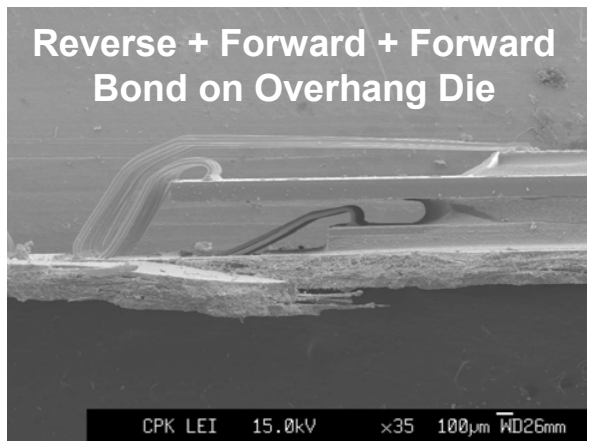
Thinner or More Die Pkg Trend = Lower Wire Loop = More Reverse Bond

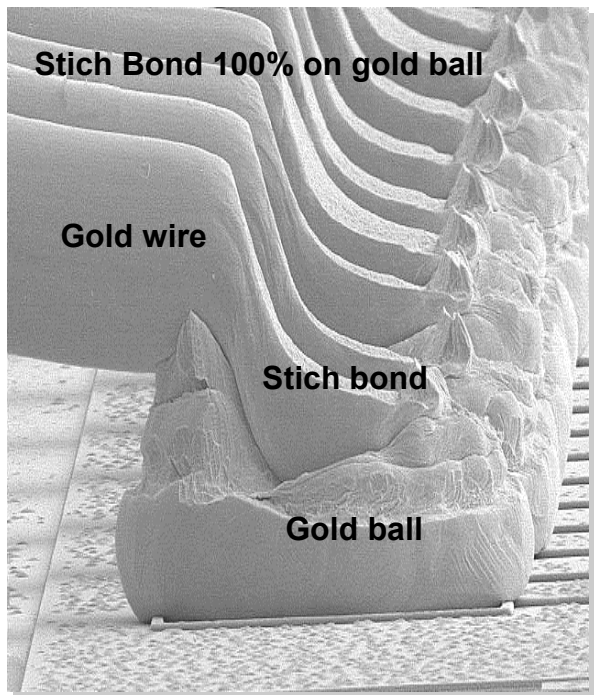












Forward Bond Pitch

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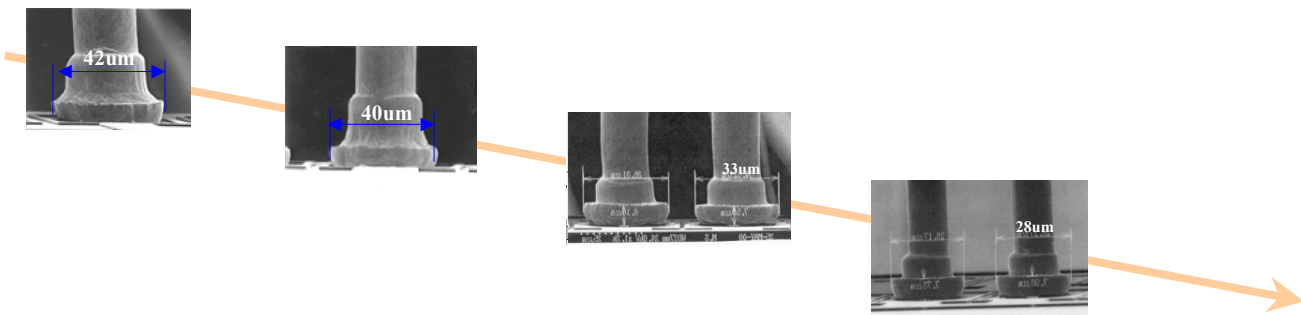
- Even for Stacked Die CSP, Forward Wirebond Pitch is same roadmap as fine pitch BGA:

Single In-line Pad

PAD PITCH	55um	50um		45um		40um	35um
Pad Pitch @ Corner	100um	100um		90um		80um	70um
Open Pad	48um	43um		38um		34um	29um
Wire Dia	23um	20um	23um	18um	20um	15um	15um
Wire Length	170mil	150mil	170mil	130mil	150mil	100mil	100mil
DEVELOP	Done	Done	Q3 '02	Done	Q2 '02	Q3 '02	Q1 '03
PRODUCTION	HVM	Qual	Q1 '02	Qual	Q3 '02	Q1 '03	Q3 '03

Ball Size 45um
40um
35um
30um
25um



* Wire Angle : max 45 degree for all pitch

Reverse Bond Pitch

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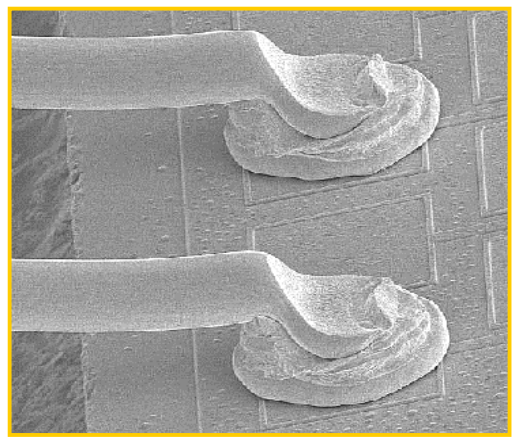
- For Reverse Wirebond, allowance must be made for stitch bond on ball which decreases the fine pitch capability
  - Usually not an issue for typical Memory Die Stack application (pitch typically >80um)

PAD PITCH		70um	65um	60um	55um	50um
Pad Opening (um)		60	55	50	48	44
Wire Diam.(um)		25	25	23	20	20
Wire Length	Max(mil)	160	160	150	120	130
	Min(mil)	15	15	12	12	7
Min Loop Height(mil)		3.5	3.5	3.0	2.5	2.5

- **Standard aluminum pad**
- **65um pitch 4mm max wire length for 25um wire**
- **Wire Loop Height is decreasing to 3.5mil Max for 25um wire**



Wire Bonding on Overhang

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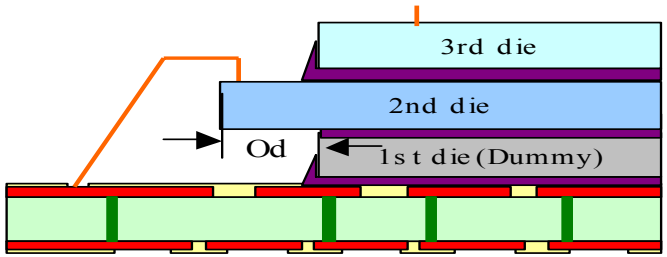
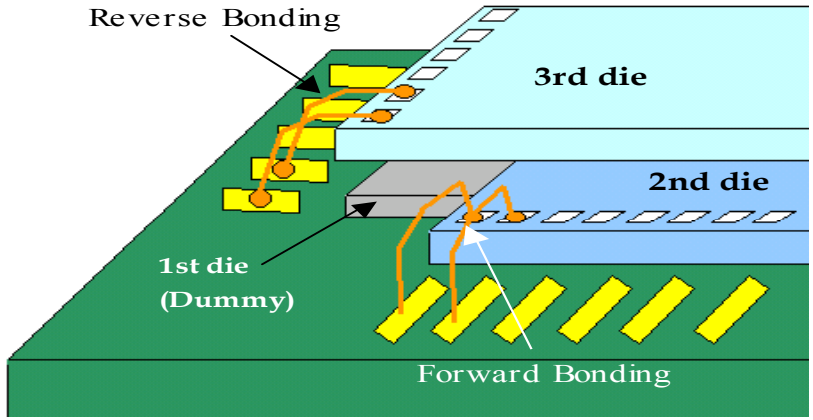
- Capability to bond on overhang determines stacked die configuration capability
  - Overhang distance is determined by die thickness and bonding method



Notes) W/B Methodology
- Forward Bonding for 2nd die overhang
- Reverse Bonding for 3rd die overhang
- "Od" : Overhang distance



Die Thickness		Bonding Method		Overhang Distance		Status
mm	mils	Fwd	Rvs	mm	mils	
0.150+	6+	X	X	2	80	In Production
0.138	5.5	X	X	2	80	In Production
0.125	5	X	X	2	80	In Production
0.113	4.5	X	X	1.5	60	Under Qualification
0.100	4	X		1	40	Under Qualification and Optimization to Extend
			X	0.75	30	
0.075	3	X		0.75	30	Under Further Optimization to Extend
			X	0.5	20	

Wire Bonding on Overhang

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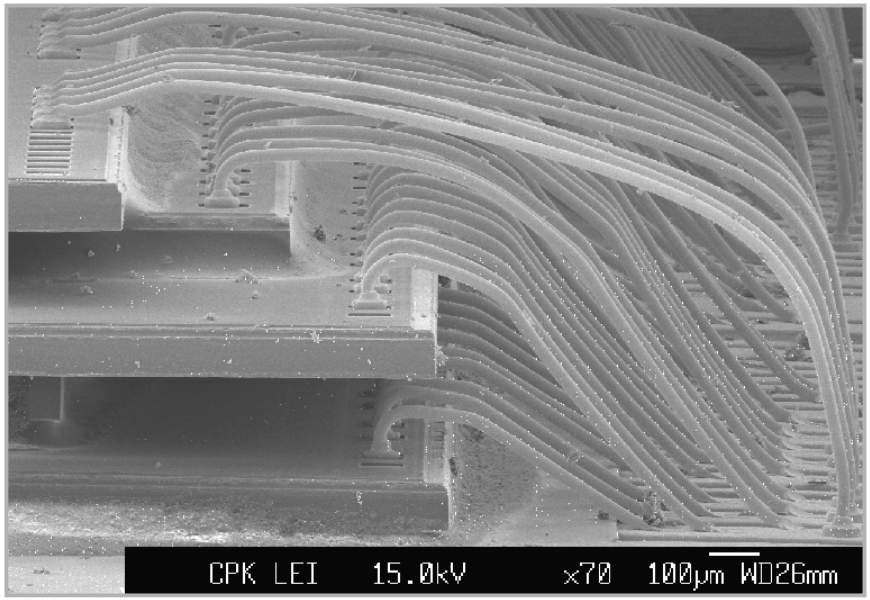
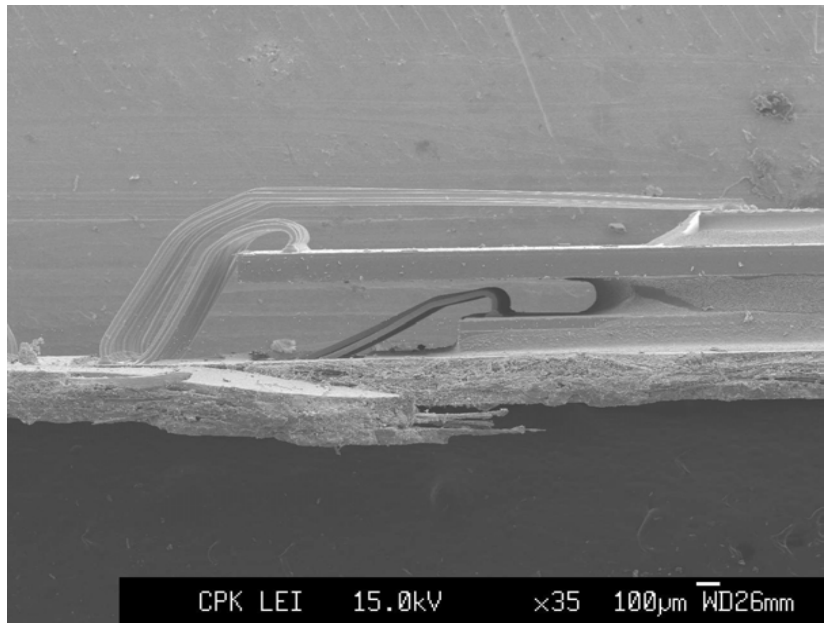
- Examples of wirebonding on overhang:



Forward bond 100um die, ~0.8mm overhang
- 4 + 1 die stack 1.4mm max CSP BGA
- Good test yield and reliability

Forward bond 125um die, ~1.6mm overhang
- 3 + 1 die stack 1.4mm max CSP BGA
- Good test yield and reliability
- Note long reverse bond on top die



Staggered Wirebonding

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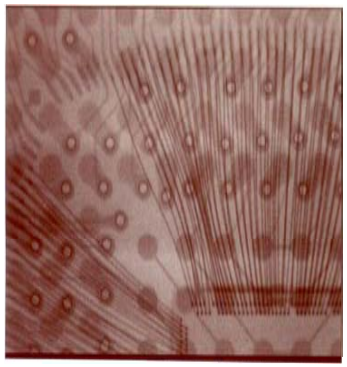
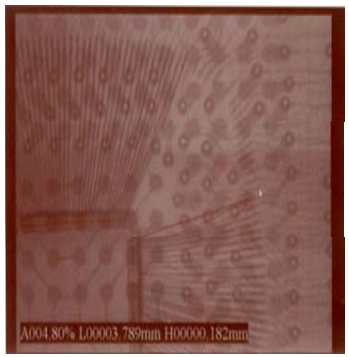
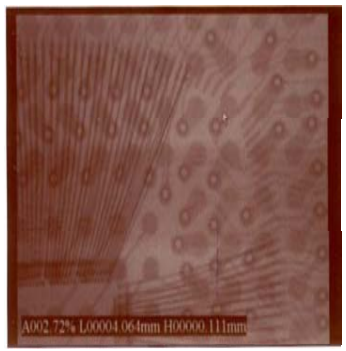
- Die stack with ASIC or Logic device, which is becoming more common, drives staggered wirebonding in stacked die package
  - Typical staggered wirebond in finepitch BGA package has >12mil wireloop height
  - Prove capability to wirebond staggered with low loop height

Die	0.5T mold cap	0.6T mold cap	0.7T mold cap
4.5x 4.5			

Die size	Mold cap	Wire sweep		
		Min	Max	Avg
4.5x4.5	0.5T	4.19	5.89	4.928
	0.6T	2.72	4.8	3.896
	0.7T	1.89	3.95	3.186
5x5	0.5T	1.86	5.42	3.815
	0.6T	2.12	5.01	3.703
	0.7T	1.27	3.25	2.339
5.5x5.5	0.5T	2.29	4.41	3.601
	0.6T	2.36	4.51	3.417
	0.7T	2.3	3.75	3.143

Leg #	Die	Wire short or Special issue on W/B (O/X)			Die size	Wire length	Loop height
		0.5T/6.7mil	0.6T/6.7mil	0.7T/6.7mil			
S1	Staggered	X	X	X	5.5sqmm	139 / 127	8.5 / 5.5
S2	Staggered	X	X	X	5.0sqmm	157 / 145	8.5 / 5.5
S3	Staggered	X	X	X	4.5sqmm	177 / 164	8.5 / 5.5

- **<u>Conclusion</u>: All legs are feasible, even 170 mil long staggered wirebond in 0.5mm Mold Cap**

Staggered Wirebonding

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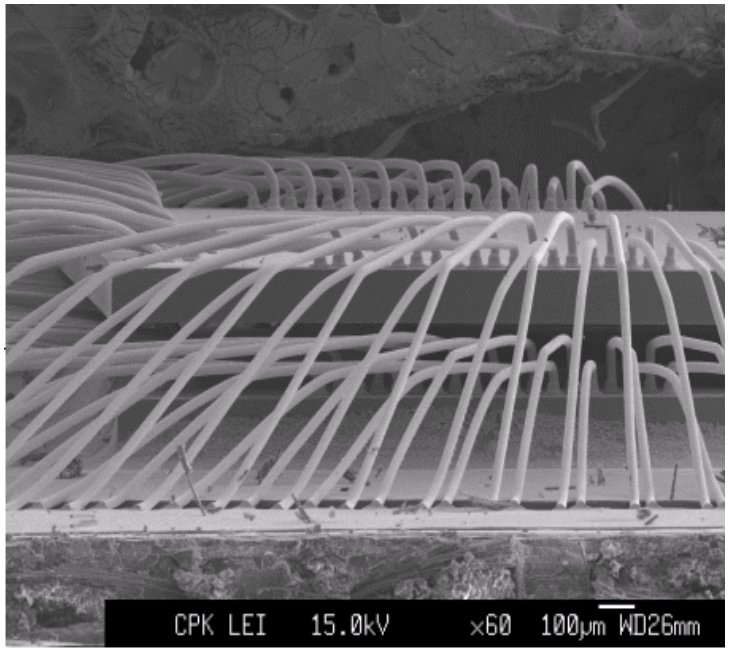
- 2 + 1 Die Stack 1.4mm CSP BGA with Staggered Wirebonding is Available:

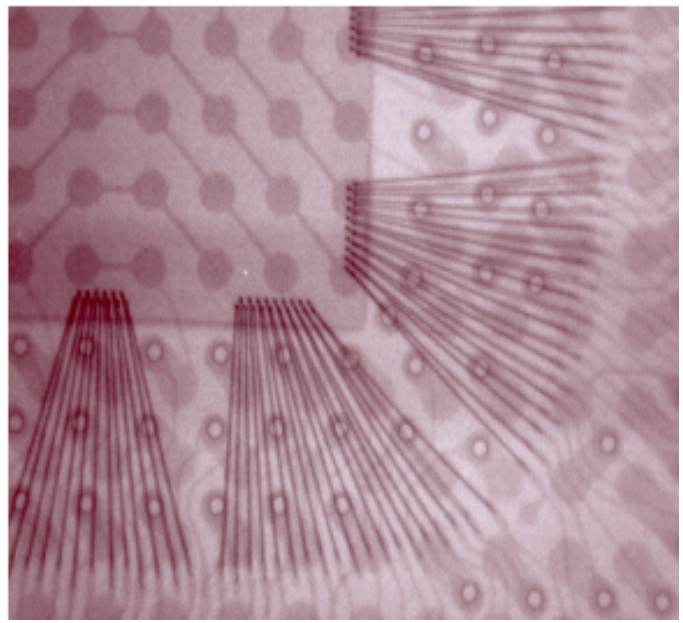


Loop Height (mils):

	Bottom Wires		Top Wires	
	Inner(Lower)	Outer	Inner	Outer
Avg.	3.01	4.95	2.98	5.00
Max.	3.20	5.10	3.13	5.03
Min.	2.87	4.71	2.82	4.89
STD	0.10	0.12	0.10	0.04

Wire Sweep:

Leg #	Min	Max	Avg	W/B option
Leg 1	0.90%	2.10%	1.52%	Bottom : In-line, Top : Staggered.
Leg 2	0.70%	2.20%	1.57%	Bottom /Top : Staggered.



Summary and Conclusion

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- Stacked Die Packaging is evolving into a standard package type for applications where an economical way to increase package functionality per area is sought.
- Trend in Stacked Die Packaging is more die in a given thickness and capability to stack same or similar die.
  - Reverse bonding becomes necessary to lower loop height.
  - Bonding on overhang with thin die becomes necessary which limits die configurations that can be packaged.
  - Staggered wirebonding becomes necessary for ASIC and logic die stacks.
- Future areas of focus.
  - Lowering loop height for both forward and reverse bonding.
  - Improving wire sweep for reverse low loop.
  - Increasing reverse bond fine pitch capability.
  - Proliferation of staggered wirebonding in stacked die packaging.