COMPASS TECHNOLOGY COMPANY LIMITED

# High Density Interconnect on Flexible Substrate

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Compass Technology Co., Ltd
Shatin, HK

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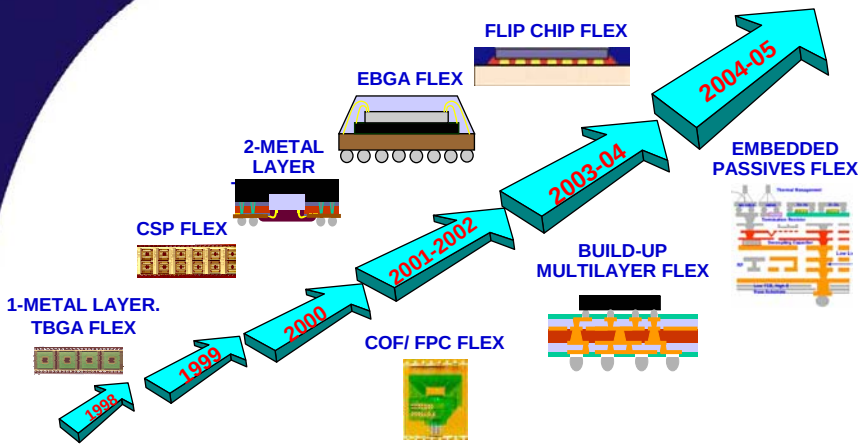
SCV CPMT
Society Chapter
Meeting

## Compass Technology Co Ltd

- **Founded:** June, 1997
  Will be listed in Singapore, in June 2004
- **Paid-up Capital:** US$ 65M
- **Area:** HK-150,000ft$^2$ (13,935m$^2$)
  China-21,528ft$^2$ (2,000m$^2$)
- **No of Employee:** HK: 440
  China: 300
- **Major Investors:** GEMS
  General Oriental Investments (HK) Ltd.
  Temasek Holdings Ltd.
  Value Partners
- **Business:** Flexible substrates (CSP/TBGA/EBGA/COF/camera module, etc) in IC/RF/Optical packaging, LCD display, Connectors
- **Process:** Reel-to-Reel Tape, 35mm, 48mm and 70mm

# Compass Product Roadmap




# Compass Technology Roadmap

| Design | | 2002 | 2003 | 2004 | 2005 |
|---|---|---|---|---|---|
| Signal Layer | Line/Space @Cu | 12/25@8 | 12/23@8 | 15/15@8 | 10/15@8 |
| Ground Layer (for 2-ML) | Line/Space @Cu | 35/35@18 | 30/30@15 | 25/25@12 | 15/15@10 |
| PI Thickness | um | 25, 50 | 25, 38, 50 | 25, 38, 50, 75 | 12.5, 25, 38, 50, 75 |
| Solder Mask | Registration | ±50 | ±50<br>±15 (Laser) | ±25<br>±15 (Laser) | ±25<br>±15 (Laser) |
| Blind Via | Via diameter | 75 | 50 | 20 | 15 |
| | Via Registration | 50 | 50 | 25 | 25 |
| New Metallization | Metal finish | ENIG<br>Immersion Sn, OSP | -- | | Immersion Ag |
| Technology | Update | Lead-/halogen-free<br>Semi-additive | UV Yag laser via<br>Multi-layer<br>Embedded Resistor | Multi-layer<br>Embedded Passive | Embedded Passive |
| Product | Applications | TBGA/CSP/FC/<br>COF/FPC | TBGA/CSP/FC<br>COF/FPC/MEMS | TBGA/CSP/FC<br>COF/FPC/MEMS/<br>RF | TBGA/CSP/FC<br>COF/FPC/MEMS/<br>RF/MCM |

# Rigid vs Flex

## The Gap is becoming "Gray"

- Thin 50um core BT material is available
- Thin Cu with carrier in market
- Multi-layer substrate on flex is emerging

- Flexible substrate
  - Variable base material: Adhesive and adhesiveless (CCL, casting, sputtered)
  - Variable process: Panel, roll-to-roll/panel, reel-to-reel
  - Flexible, bendable, and able to rigid

- Tape is a flex made in TAB reel-to-reel process, which provides higher trace density with small area and constant etching speed.

# Circuit Density Development

# Trace Density

## International Technology Roadmap Semiconductor (ITRS)-2003

*Table 100 Flip Chip Substrate Top-side Fan-out Potential Solutions*

| *Year of Production* | *2003* | *2004* | *2005* | *2006* | *2007* | *2008* | *2009* | *2012* | *2015* | *2018* |
|---|---|---|---|---|---|---|---|---|---|---|
| *Technology Node* | | *hp90* | | | *hp65* | | | | | |
| *DRAM ½ Pitch (nm)* | *100* | *90* | *80* | *70* | *65* | *57* | *50* | *35* | *25* | *18* |
| *MPU/ASIC ½ Pitch (nm)* | *107* | *90* | *80* | *70* | *65* | *57* | *50* | *35* | *25* | *18* |
| *MPU Printed Gate Length (nm)* | *65* | *53* | *45* | *40* | *35* | *32* | *28* | *20* | *14* | *10* |
| *MPU Physical Gate Length (nm)* | *45* | *37* | *32* | *28* | *25* | *22* | *20* | *14* | *10* | *7* |
| Flip chip pad pitch (µm) | 150 | 150 | 130 | 130 | 120 | 110 | 100 | 90 | 80 | 70 |
| Pad size (µm)* | 75 | 75 | 65 | 65 | 60 | 55 | 50 | 45 | 40 | 35 |
| *Chip Size (mm/size)* | | | | | | | | | | |
| Cost-performance | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 |
| High-performance | 17 | 17 | 17 | 17 | 17 | 17 | 17 | 17 | 17 | 17 |
| *Array Size = # pads along chip edge* | | | | | | | | | | |
| Cost-performance (maximum) | 79 | 79 | 91 | 91 | 99 | 108 | 119 | 132 | 149 | 170 |
| High-performance (maximum) | 112 | 112 | 129 | 129 | 140 | 153 | 169 | 187 | 211 | 241 |
| *Wiring Substrate (Three lines replacing one depopulated pad accessing 2.0 rows per fan-out layer)* | | | | | | | | | | |
| Line width (µm) | 32.1 | 32.1 | 27.8 | 27.8 | 25.7 | 23.5 | 21.4 | 19.2 | 17.1 | 15 |
| Line spacing (µm) | 32.1 | 32.1 | 27.9 | 27.9 | 25.7 | 23.6 | 21.4 | 19.3 | 17.1 | 15 |
| *Wiring Substrate (Five lines replacing one depopulated pad accessing 3.0 rows per fan-out layer)* | | | | | | | | | | |
| Line width (µm) | 20.4 | 20.4 | 17.7 | 17.7 | 16.3 | 15 | 13.6 | 12.2 | 10.9 | 9.5 |
| Line spacing (µm) | 20.5 | 20.5 | 17.7 | 17.7 | 16.4 | 15 | 13.6 | 12.3 | 10.9 | 9.5 |
| *Wiring Substrate (Three lines between adjacent pads accessing 4.0 rows per fan-out layer)* | | | | | | | | | | |
| Line width (µm) | 10.7 | 10.7 | 9.2 | 9.2 | 8.5 | 7.8 | 7.1 | 6.4 | 5.7 | 5 |
| Line spacing (µm) | 10.7 | 10.7 | 9.2 | 9.3 | 8.6 | 7.9 | 7.1 | 6.4 | 5.7 | 5 |

** The pad size is assumed as 50% of pad pitch. It is usually different at different fan-out layers, e.g. from 30% to 60%*

- **High trace density on substrate is demanding**

# Trace Density

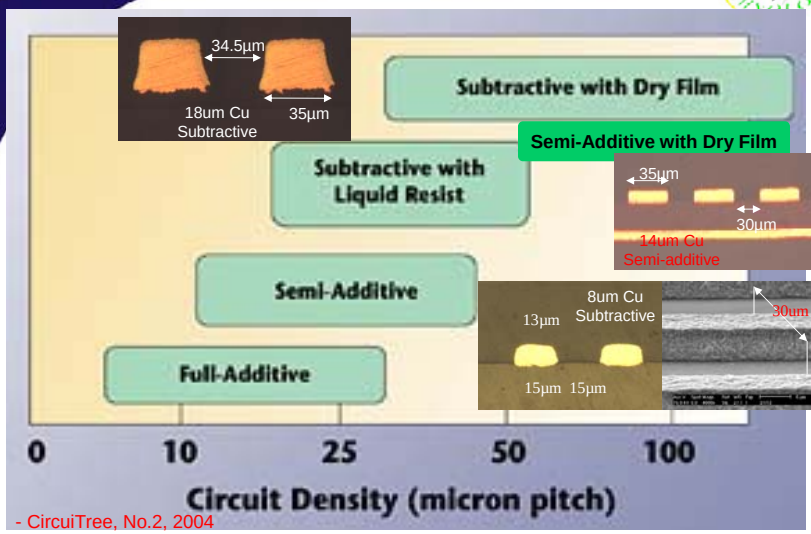
| Year | 1999 | 2000 | 2005 | 2010 | |
|---|---|---|---|---|---|
| Dielectric Tg | 160~180 | | 180~200 | 200~220 | (℃) |
| Dielectric Constant | 4.4~4.6 | | 3.0~3.5 | < 3.0 | (1MHz) |
| Via Formation | 150 | 100 | 50 | 25 | (㎛) |
| | $CO_2$ Laser → | | | | |
| | | | UV Laser → | | |
| | | | | Photo via → | |
| Fine Lines | 75 | | 50 30 | 20~10 | (㎛) |

| | *Line Width* | *Line Pitch* | *Via Diameter* | *Pad Diameter* | *Ball Pitch* |
|---|---|---|---|---|---|
| ***Std. PWB*** | 125 | 250 | 300 | 500 | 1.3mm |
| ***Adv. PWB*** | 75 | 150 | 200 | 400 | 1.0mm |
| ***Std. Substrate*** | 65 | 130 | 150 | 350 | 1.0mm |
| ***Adv. Substrate*** | 45 | 80 | 50 | 100 | 0.8mm |
| ***Leading Substrate*** | 25 | 50 | 30 | 55 | 0.4mm |
| ***Std. Tape*** | 25 | 50 | 100 | 200 | 0.4mm |
| ***Adv. Tape*** | 15 | 30 | 20 | 80 | 0.4mm |
| ***Next generation*** | 10 | 20 | 30 | Pad-less | 0.4mm |

- Part of data are from “Substrate Packaging Trends”, R. Huemoeller, Amkor Technology

- **Tape flexible substrate has a higher trace density than rigid substrate.**

# Trace Density



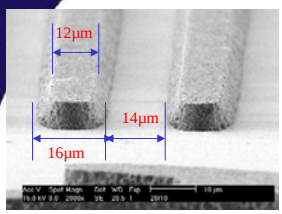

- CircuiTree, No.2, 2004

• **Tape flexible substrate achieves 25-30um trace pitch by subtractive.**

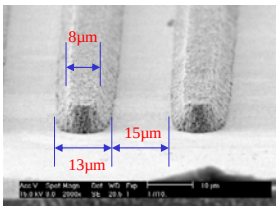
# Trace Density

## Trace Pitch Development

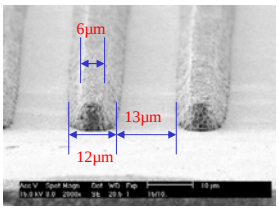
### 8um copper/Subtractive



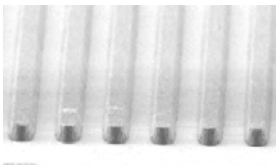

T/B Ratio=75%

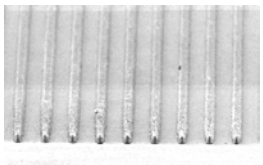


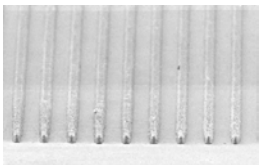

T/B Ratio=61.5%



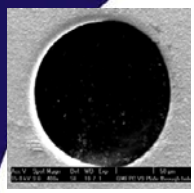

T/B Ratio=50%

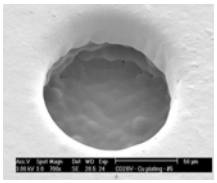


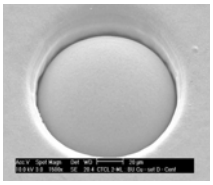


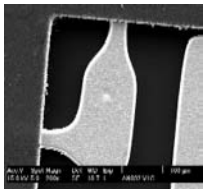


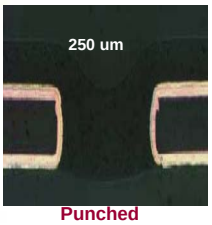
# Vias for Interconnect



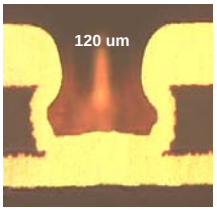




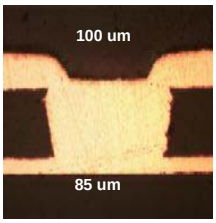


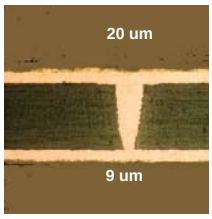



Punched




$CO_2$ Laser



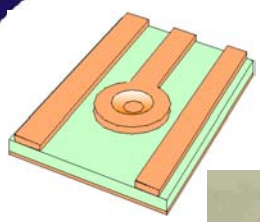




UV YAG Laser

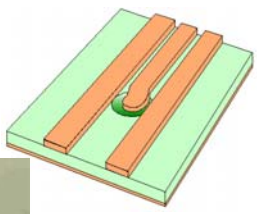
- Via size is reduced with Cu fully filled.

# Padless?

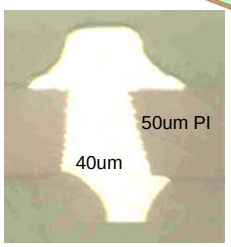
## Cu Filled Blind Via



Conventional



Padless



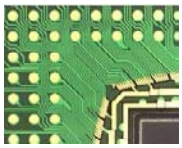

- Padless structure could be achieved with Cu fully filled via.

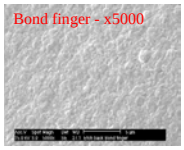
# Semi-Additive Bussless

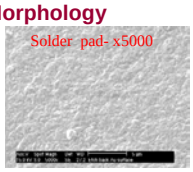
## For Non-Plating Buss Lines

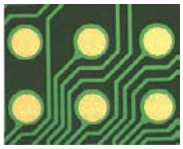
- **Material Selection/Applications**
  - → **Adhesiveless Materials**
  - → **1-ML and 2-ML tapes**

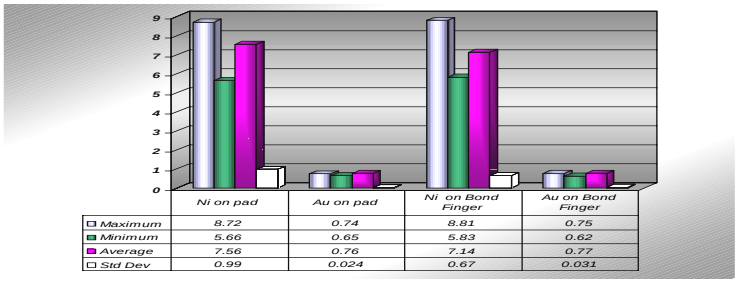
**Surface Morphology**





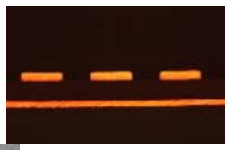



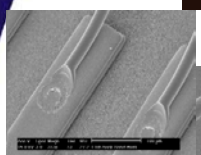


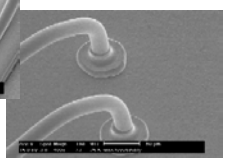

| | Ni on pad | Au on pad | Ni on Bond Finger | Au on Bond Finger |
|---|---|---|---|---|
| Maximum | 8.72 | 0.74 | 8.81 | 0.75 |
| Minimum | 5.66 | 0.65 | 5.83 | 0.62 |
| Average | 7.56 | 0.76 | 7.14 | 0.77 |
| Std Dev | 0.99 | 0.024 | 0.67 | 0.031 |

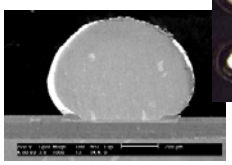

# Semi-Additive Bussless

## For Non-Plating Buss Lines







- **Negligible Cu under-cut was observed.**
- **Good wire bondability and Solderability were examined.**
- **TBGA (35x35mm) meets the reliability in MST-level3 (260$^{o}$C) + PCT and HTS.**

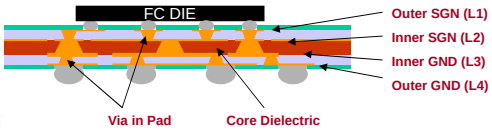
# Multi-Layer Flex Development

## Build-up 4-ML Tape Development

| | Unit | Inner Layer | Outer Layer |
|---|---|---|---|
| *Min. Trace Width/Spacing (Signal layer)* | um | 30/30 | 25/25 |
| *Min. diameter of blind via hole (entry/Exit)* | um | 20/10 | 75/55 |
| *Min. diameter of blind via Capture Pad* | um | 70 | 125 |
| *Conductor Thickness* | um | 12 | 9 Min. |
| *Dielectric Layer Thickness* | um | 50 | 40 |
| *Soldermask thickness* | Um | -- | 20 |
| *Registration accuracy* | um | +/-25 | +/-25 |
| *Total substrate thickness* | um | 185+/-10% | |

| Build-up Dielectric Material | |
|---|---|
| Dielectric constant: 3.4 at 1 GHz: | Tg: 153°C(TMA), 180°C(DMA) |
| Dissipation factor: 0.023 at 1 GHz | Dielectric strength: 2,200 V/mil |

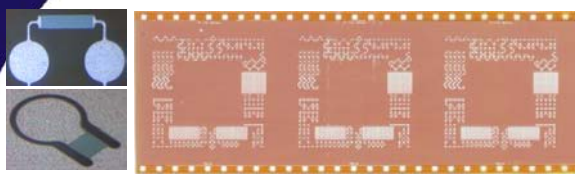
**Layer Construction : 1+2+1**




# Embedded Passives

## Embedded Etched Thin Film Resistor

### Ohmega-Ply RCM Ni-P resistor



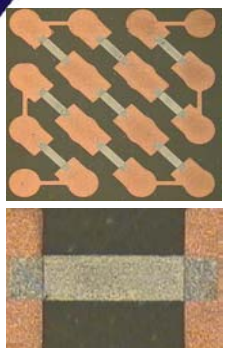
| *No of Sq (L x W) $R_{design}$ (Ω)* | *0.5 (100X200) 12.5* | *1 (200X200) 25.0* | *1.5 (300X200) 37.5* | *2 (400X200) 50.0* | *3 (600X200) 75.0* | *4 (800X200) 100* |
|---|---|---|---|---|---|---|
| $R_{MAX}$ (Ω) | 72.7 | 54.6 | 55.6 | 64.0 | 86.4 | 118.1 |
| $R_{Min}$ (Ω) | 16.6 | 27.3 | 37.3 | 48.2 | 73.5 | 95.6 |
| Tolerance (%) | 141% | 56% | 26% | 19% | 10% | 13% |
| $R_{Mean}$ (Ω) $_6$ 1σ (%) | $30.1_6$ 21.8% | $35.1_6$ 11.1% | $44.1_6$ 6.6% | $53.8_6$ 4.2% | $78.4_6$ 2.9% | $104.6_6$ 3.2% |
| $\Delta R/R_{design}$ (%) | +141% | +40.4% | +17.7% | +7.7% | +4.6% | +4.6% |

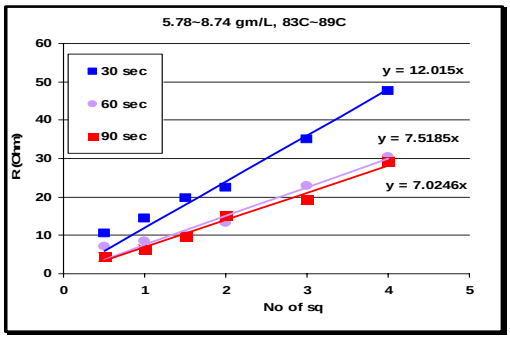
- **Etched tolerance will be significantly increased when the dimension of resistor is below 200um.**

# Embedded Passives

## Embedded Plated Thin Film Resistor

### Shipley Ni-P plating solution



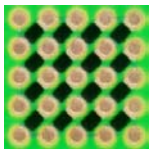


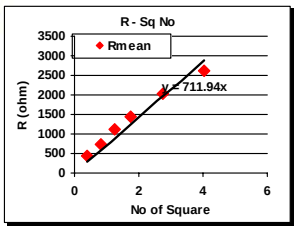

- Resistors with high ratio of L/W (>2) have lower resistance tolerance and better linearity.

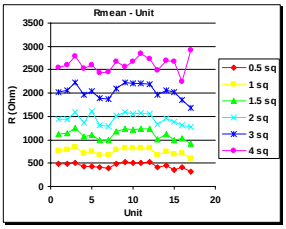
# Embedded Passives

## Embedded Thick Film Resistor

### PTF Carbon ink





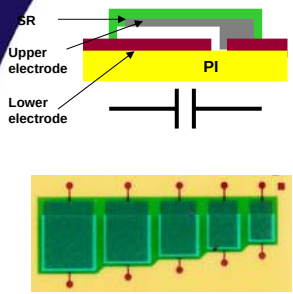

| Reliability Test Items | ΔR(%) |
|---|---|
| MSL-3 + PCT | -10% |
| Temperature Cycle | -12% |
| Humidity Storage 300 Hrs (after baking) | +11% (+2.4%) |

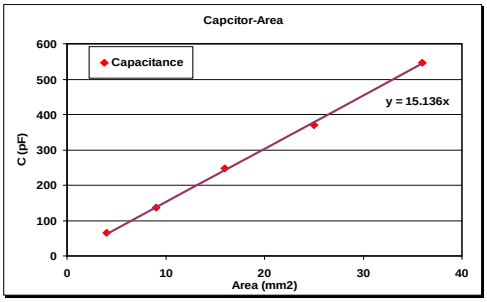
- Resistors with high ratio of L/W (>2) has lower resistance tolerance (<20%) and better linearity.

# Embedded Passives

## Embedded Capacitor

### Electrapolymers thick film dielectric paste (k=16)



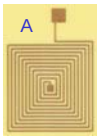



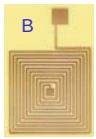

- Capacitance density reaches 15.1 pF/mm$^2$ with a low tolerance (<5%) and good linearity.

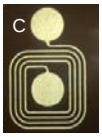
# Embedded Passives

## Embedded Inductor

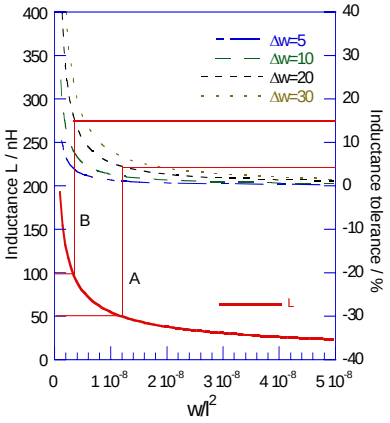
### Planar Inductor formed by Cu pattern




| Design | A | B | C |
|---|---|---|---|
| Design rule | | | |
| Base film thickness (um) | 50 | 50 | 50 |
| Trace width/space (um) | 250/250 | 250/150 | 50/50 |
| Coil Turns | 11 | 11 | 4 |
| Outer Diameter (mm) | 11.75 | 10 | 1.5 |
| Inner Diameter (mm) | 1.75 | 1.6 | 1.0 |
| Testing Result (f = 1 MHz) | | | |
| Inductance (nH) | 511 | 476 | 33.1 |
| Q factor | 20 | 3.6 | 3.99 |
| Serial Resistance (Ω) | 1.6 | 0.8 | 0.294 |

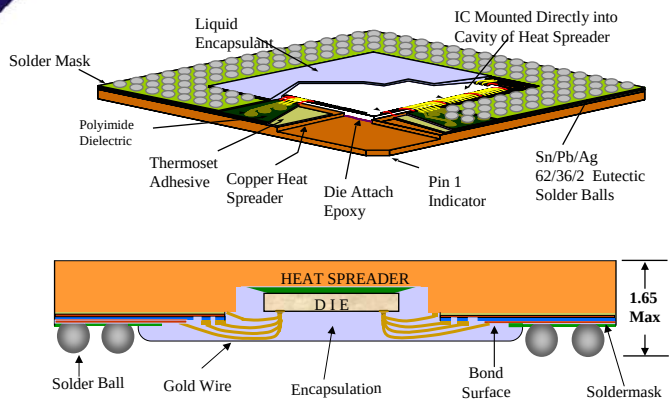



- Planar Inductor on flex achieved a tolerance of <3%.

# Flexible Substrates Development in IC Packaging

## Tape Ball Grid Array (TBGA)

### Package with High Thermal Performance

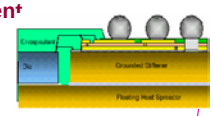


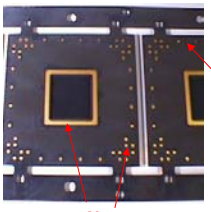

- **High thermal dissipation at Theta Ja down to 7.8°C/W.**
- **1-ML, 2-ML and multi-layer metal substrates are available for ASIC, MPU, etc.**

# Close Loop TBGA

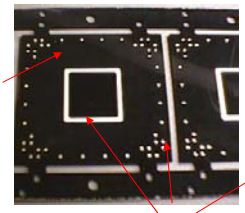
## Applications

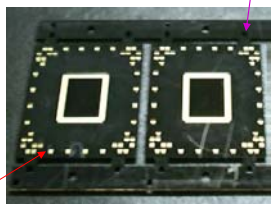
- Increasing the circuit density with grounded heatsink
- One additional metal layer for electrical requirement





Black oxide





Ni/Au

Ag

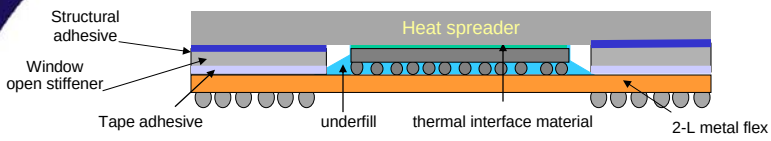
1.27mm Ball Pitch

1.00 mm Ball Pitch

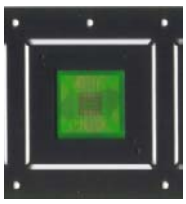
- Capability is demonstrated to be 0.2 mm space between spots for 1mm ball pitch with the tolerance of ±50um on spot diameter.

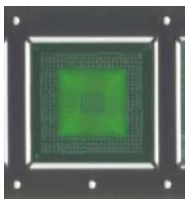
# Flip Chip Tape BGA

- Thermal performance: > 6W
- Electrical performance: > 2.5GHz




Chip side





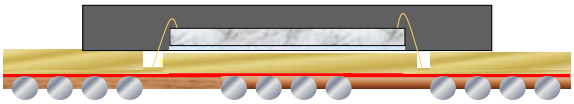
SMT side

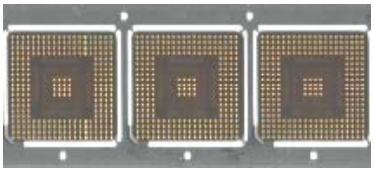
- Flip chip TBGA with multi-layer flexible substrate will be for high pin-count packages.

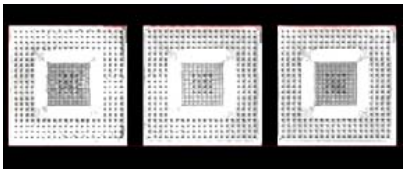
# Cavity-UP Enhanced BGA

## Applications

- Alternative solution with Thermal performance to PBGA





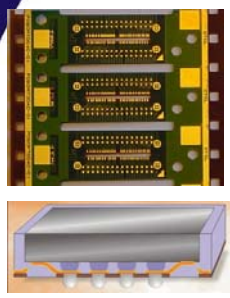


- It is proven for lead-free and halogen-free applications with a Theta Ja of ~17°C/W at zero air flow for the thermal performance.
- Transfer molding is applicable with the same assembly process to PBGA.

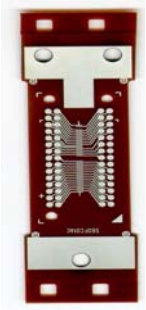
# Chip Scale Package (CSP)

## Wire bonding and Flip chip CSP

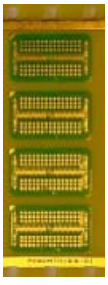
- 1-ML or 2-ML tape
- Different interconnects

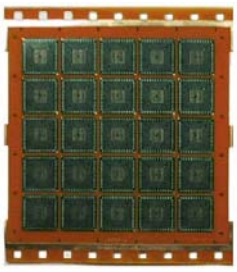


TAB or wire bonding



Sn/Au bonding

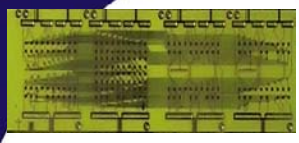


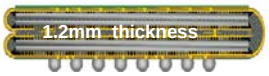


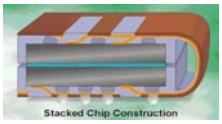
Solder joint

- CSP is one of the main application for flexible substrates.

# Stacked Chip Scale Package (CSP)

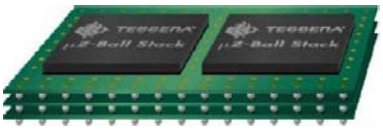




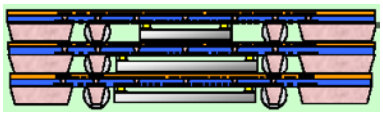





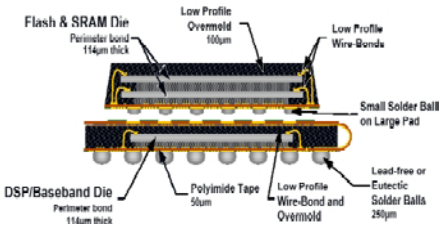
**Folded flex CSP – Tessera design**



**UZM MCP Ball Stacked CSP**



**North NMTI design**




**UZ Folded-over Tape with Memory Stacked CSP (1.4mm thick)**

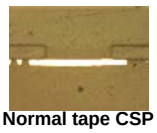
# Land Grid Array (LGA) For CSP

## Advantages of LGA CSP vs normal tape CSP

» **Improved board level reliability**

» **Better for ≤ 0.4mm ball pitch**

**Via Hole Structure for Solder Ball in CSP**



**Normal tape CSP**

**Land grid array/Stud grid array**

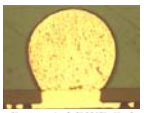


*Table 99 BGA and FBGA/CSP Package Potential PWB Solutions*

| *Year of Production* | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2012 | 2015 | 2018 |
|---|---|---|---|---|---|---|---|---|---|---|
| *Technology Node* | | hp90 | | | hp65 | | | | | |
| *DRAM ½ Pitch (nm)* | 100 | 90 | 80 | 70 | 65 | 57 | 50 | 35 | 25 | 18 |
| *MPU/ASIC ½ Pitch (nm)* | 107 | 90 | 80 | 70 | 65 | 57 | 50 | 35 | 25 | 18 |
| *MPU Printed Gate Length (nm)* | 65 | 53 | 45 | 40 | 35 | 32 | 28 | 20 | 14 | 10 |
| *MPU Physical Gate Length (nm)* | 45 | 37 | 32 | 28 | 25 | 22 | 20 | 14 | 10 | 7 |
| FBGA/CSP solder ball pad pitch (mm) | 0.4 | 0.4 | 0.3 | 0.3 | 0.2 | 0.2 | 0.2 | 0.15 | 0.15 | 0.1 |
| Pad size (µm) | 160 | 160 | 120 | 120 | 80 | 80 | 80 | 60 | 60 | 40 |
| Line width (µm) | 48 | 48 | 36 | 36 | 24 | 24 | 24 | 18 | 18 | 12 |
| Line spacing (µm) | 48 | 48 | 36 | 36 | 24 | 24 | 24 | 18 | 18 | 12 |
| Number of rows accessed | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |

–ITRS 2003

• **Cu build-up height in via holes can be controlled in the range of 20-50 ± 5µm.**

# Lead-Free and Halogen-Free Products

## Recommended Material Sets

| *Material set* | *1-ML TBGA* | *2-ML TBGA* | *CSP Tape* |
|---|---|---|---|
| *PI Base*# | Any type | Any type | Any type |
| *Tape adhesive* | Tomegawa-X# Toray 8600# | --- | Tomegawa-X# Toray 8600# |
| *Signal solder mask* | AUS-5, AUS-11, AUS-21# | | |
| *Ground solder mask* | --- | AR-7100# or Bare Cu | AUS-11, AUS-21# |
| *Heatsink adhesive* | TSA-14#, TSA-51#, TSA-67# | TSA-51#, TSA-67# | --- |

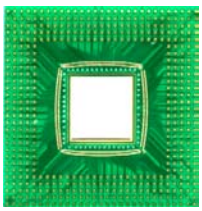
*Note* *#: Halogen-free material*
*All solder mask are over Cu.*

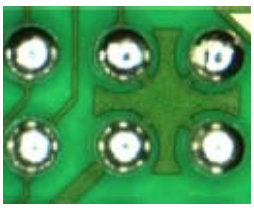
# Liquid Crystal Polymer (LCP) Base Material

## Characteristics of LCP over PI

» Stable/low Dk at 2.9 and Df at 0.002 (1-10GHz) for high speed and high frequency

» Low moisture absorption at <0.4%





- Adhesiveless LCP TBGA has similar wire bondability and solderability performance to PI TBGA.
- Passed the reliability tests at substrate level for 1-ML and 2-ML LCP TBGA
  - » MST-level 3 at 238°C and 260°C.
  - » MST-level 3 at 238°C + PCT for 168 hrs

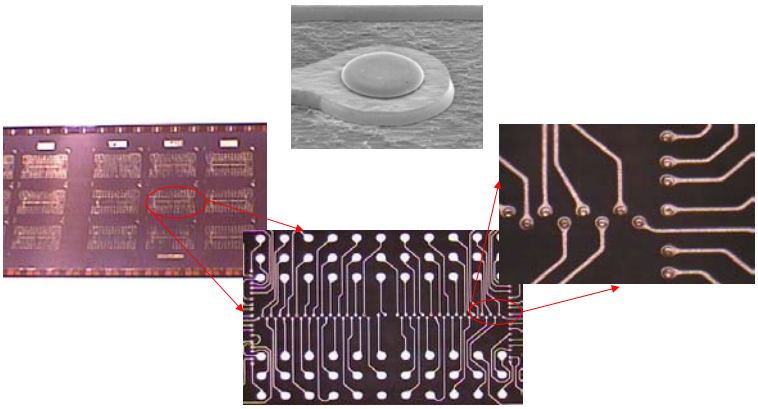
# Cu Bumped Tape

## Specifications

Ni/Au or Sn finish

75um bump diameter/160um bump pitch

bump height: 20-40 ± 2 um



# Solder Bumped Tape

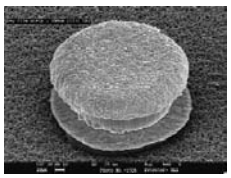
## Solder Bumping on Substrate

Eutectic, high Pb, and lead-free (Sn-Cu, Sn-Ag) solder bumping

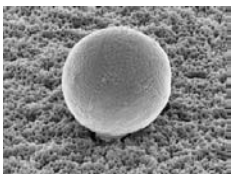
75um bump diameter/125um bump pitch

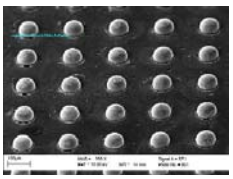
bump height: 80um ± 5um

Printing or plating



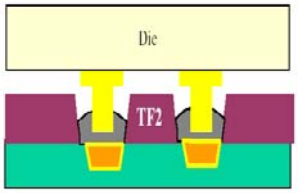
After Sn-Cu plating
and dry film stripping

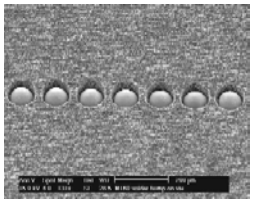


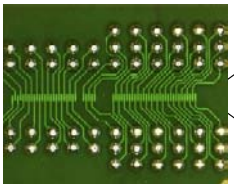


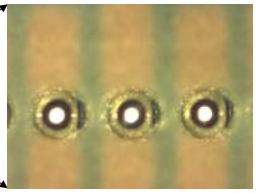
After solder reflow
and flux residue cleaning

# Fine Bump Pitch For Direct Flip Chip



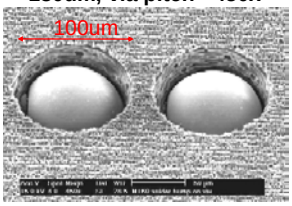




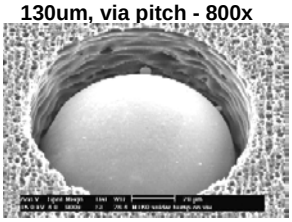
- Eutectic/ lead-free (Sn-Cu-Ag) solder bumping
- 50um bump diameter/70um bump pitch
- Au or Cu stud bumps on die
- Fluxless process

# Fine Bump Pitch For Direct Flip Chip

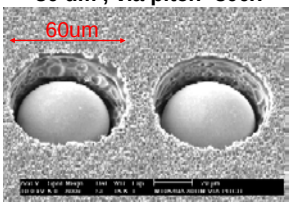
130um, via pitch - 450x



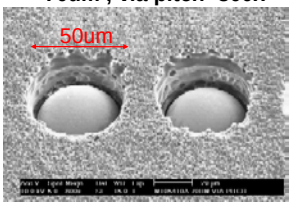

130um, via pitch - 800x



80 um , via pitch- 800x

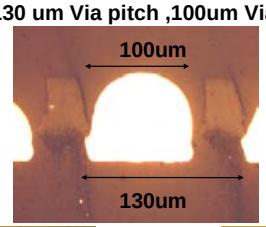


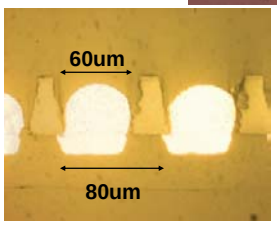

70um , via pitch- 800x



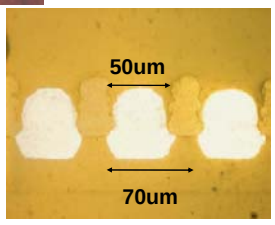
# Fine Bump Pitch For Direct Flip Chip

130 um Via pitch ,100um Via size




80 um Via pitch ,60 um Via size




70 um Via pitch ,50 um Via size

# Fine Bump Pitch For Direct Flip Chip

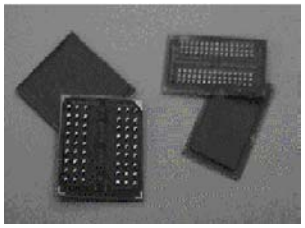
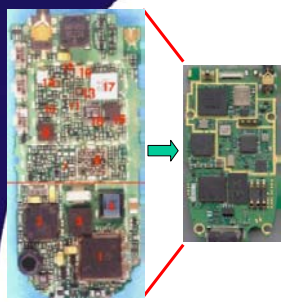


Table 5: Package reliability base on continuity resistance for 8x9mm package

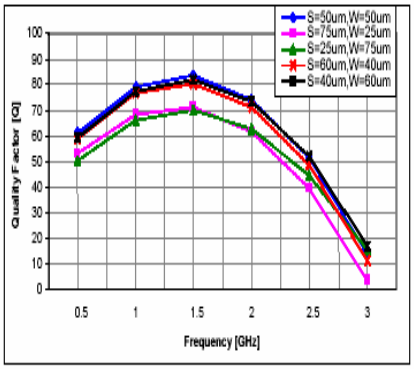
| No | Test Description | Reliability Result |
|---|---|---|
| 1 | MST L2 85°C/60% RH with 3IR reflow 260°C based on J-STD-020 | 0/15 |
| 2 | MST L3 30°C/60% RH with 3IR reflow 260°C based on J-STD-020 | 0/15 |
| 3 | Temperature cycling condition A –40 to 85°C for 1000 cycles based on EIA/JESD22-A105-B | 0/15 |
| 4 | Temperature cycling condition B –40 to 125°C for 1000 cycles based on EIA/JESD22-A105-B | 0/15 |
| 5 | Thermal Shock Condition D –65 to 150°C for 700 cycles based on JESD22-A106-A | 0/15 |
| 6 | Accelerated Moisture Resistance – Unbiased autoclave condition C 121°C/100% RH 96hrs based on JESD22-A102-B | 0/15 |

– TK Lee, et al ECTC, June 2004

# Tape Substrate for RF Wireless



MOTOROLA V3688
DUAL-BAND GSM PHONE




Tessera, 2002

- ± 10 μm manufacturing tolerance of trace spacing and width variations resulted in less than ± 5 % variations on Q values.
- ± 25 μm manufacturing tolerance of trace spacing and width variations resulted in around ± 15 ~ 20 % variations on Q values.

**• Reel-to-reel tape process provides ± 5-7um tolerance in line width/space and 5% tolerance in thickness, good for RF.**

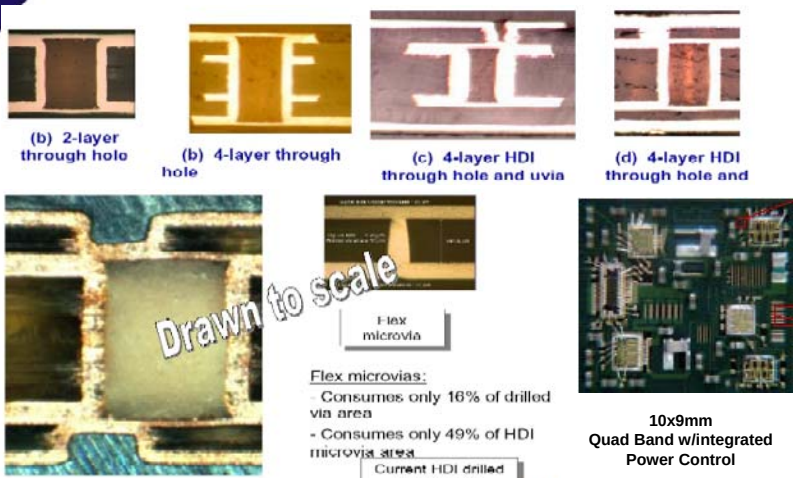
# Tape Substrate for RF Wireless

## Comparison in Substrate Materials for RF

| Property | Unit | FR4 | GETEK | LTCC | PI Flex | Leadframe |
|---|---|---|---|---|---|---|
| **Electrical** | | | | | | |
| Dielectric Constant, k | | 3.0~4.5@ 1GHz | 3.82~4.2@ 1GHz | 5.6~10@ 10MHz | 3.6@ 2GHz | |
| Loss Tangent | % | 0.017~0.025 @1GHz | 0.0093 @1GHz | 0.001~0.002 @10MHz | 0.006 @2GHz | |
| **Mechanical & Thermal** | | | | | | |
| Young's Modulus | | 3 ~3.5 mpsi | 980 kpsi | 150-300GPa | 800 kpsi | |
| CTE | Ppm/ºC | 14 -17 | 12 -15 | 5.8 - 7 | 16 | 17 |
| Tg | ºC | 135 | 180 | - | >350 | - |
| Thermal conductivity | W/mK | 0.25 | 0.31 | 2 ~ 4.4 | 0.35 | |
| Metal | | Cu | Cu | W/Ag | Cu | |
| **Processing** | | | | | | |
| Min. L/S (HDI) | μm | 100/100 (75/75) | 100/100 (75/75) | 100/100 (75/75) | 40/40 (25/25) | 150/150 |
| Min.via / land (HDI) | μm | 200/350 (100/250) | 200/350 (100/250) | 200/250 (100/200) | 30/100 | N/A |
| Metal thickness | μm | < 35 | < 35 | < 15 | < 35 | 150 |
| Process precision | | Medium | Medium | Low | High | Medium |
| Cavity capability | | Routing | Routing | Punch | Punch | Etch |

# Tape Substrate for RF Wireless

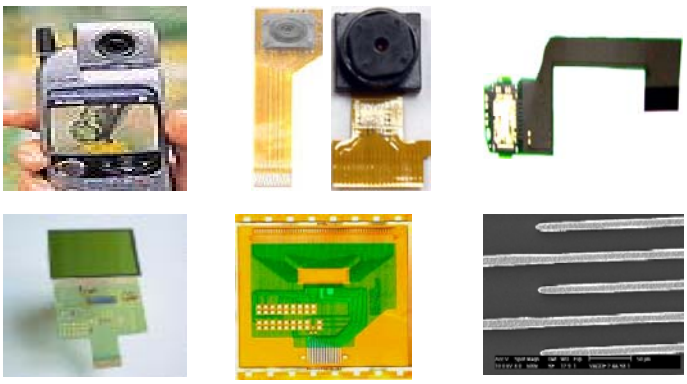
## Vias in GETEK laminate for RF wireless




**10x9mm**
**Quad Band w/integrated Power Control**

# COF For LCD Display

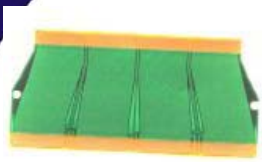
- **Current Fine pitch COF Production (L/S = 15/15)**
- **Camera module demand for cell phone**

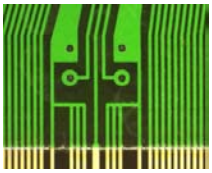


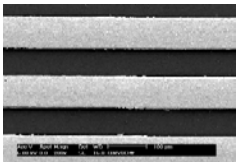
- **Flex/tape is exclusive choice for bending and dynamic applications.**

# Impedance-Controllable Flex

## Reel-to-reel process for impedance control







| Simulated Impedance (Ohm) | | Trace Width (um) | Trace Thickness (um) | Trace Space (um) | PI Thickness (um) | SM Thickness (um) | Measured Differential Impedance (Ohm) | |
|---|---|---|---|---|---|---|---|---|
| Nominal | Differential | | | | | | Sample 1 | Sample 2 |
| 100 | 95.3 | 50 | 18 | 40 | 50 | 30 | Min. 102.1 | Min. 102.2 |
| 100 | 94.4 | 25 | 12 | 25 | 25 | 30 | Max. 107.5 | Max. 107.5 |

- Reel-to-Reel process easily produces controlled differential impedance at tight tolerances with better line width control.

# Summary

## Flexible substrate provides

- Finer trace pitch and blind via, providing HDI for IC Packages
- Well adapt to cavity packages and exclusive to the bending requirement
- Multi-layer and embedded passives to narrow the gap to HDI laminate
- Good solution for driving small form factor
- Good process for high volume/low cost in roll-to-roll & reel-to-reel format
- New base materials, such as LCP etc, will widen the applications of flexible substrate