High Density Interconnect on Flexible Substrate

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Compass Technology Co., Ltd
Shatin, HK

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SCV CPMT
Society Chapter Meeting

Compass Technology Co Ltd

Founded: June, 1997
Will be listed in Singapore, in June 2004

- Paid-up Capital: US$ 65M
- Area:
  - HK: 150,000ft² (13,935m²)
  - China: 21,528ft² (2,000m²)
- No of Employee:
  - HK: 440
  - China: 300
- Major Investors:
  - GEMS
  - General Oriental Investments (HK) Ltd.
  - Temasek Holdings Ltd.
  - Value Partners
- Business:
  - Flexible substrates (CSP/TBGA/EBGA/COF/camera module, etc) in IC/RF/Optical packaging, LCD display, Connectors
- Process:
  - Reel-to-Reel Tape, 35mm, 48mm and 70mm
Rigid vs Flex

The Gap is becoming “Gray”

- Thin 50um core BT material is available
- Thin Cu with carrier in market
- Multi-layer substrate on flex is emerging

- Flexible substrate
  - Variable base material: Adhesive and adhesiveless (CCL, casting, sputtered)
  - Variable process: Panel, roll-to-roll/panel, reel-to-reel
  - Flexible, bendable, and able to rigid

- Tape is a flex made in TAB reel-to-reel process, which provides higher trace density with small area and constant etching speed.

Circuit Density Development
Trace Density

**Table 109: Flip Chip Substrate Top-side Fan-out and Potential Solutions**

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology Notes</td>
<td>ITRS</td>
<td>ITRS</td>
<td>ITRS</td>
<td>ITRS</td>
<td>ITRS</td>
<td>ITRS</td>
<td>ITRS</td>
<td>ITRS</td>
<td>ITRS</td>
</tr>
<tr>
<td></td>
<td>Apr 03</td>
<td>Apr 04</td>
<td>Apr 05</td>
<td>Apr 06</td>
<td>Apr 07</td>
<td>Apr 08</td>
<td>Apr 09</td>
<td>Apr 10</td>
<td>Apr 11</td>
</tr>
<tr>
<td>TAIW: &amp; Pack (mm)</td>
<td>100</td>
<td>90</td>
<td>80</td>
<td>70</td>
<td>60</td>
<td>50</td>
<td>40</td>
<td>30</td>
<td>20</td>
</tr>
<tr>
<td>APAC: &amp; Pack (mm)</td>
<td>80</td>
<td>70</td>
<td>60</td>
<td>50</td>
<td>40</td>
<td>30</td>
<td>20</td>
<td>10</td>
<td>5</td>
</tr>
<tr>
<td>EUP: &amp; Pack (mm)</td>
<td>60</td>
<td>50</td>
<td>40</td>
<td>30</td>
<td>20</td>
<td>10</td>
<td>5</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>EUP: &amp; Pack (mm)</td>
<td>25</td>
<td>20</td>
<td>15</td>
<td>10</td>
<td>7</td>
<td>5</td>
<td>2</td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>Ref. Pad: pitch (um)</td>
<td>150</td>
<td>150</td>
<td>130</td>
<td>130</td>
<td>120</td>
<td>100</td>
<td>90</td>
<td>70</td>
<td>50</td>
</tr>
<tr>
<td>Ref. Pad: pitch (um)</td>
<td>75</td>
<td>75</td>
<td>65</td>
<td>65</td>
<td>60</td>
<td>55</td>
<td>50</td>
<td>45</td>
<td>40</td>
</tr>
</tbody>
</table>

**Trace Density**

- Part of data are from “Substrate Packaging Trends”, R. Huemoeller, Amkor Technology

- Tape flexible substrate has a higher trace density than rigid substrate.
Tape flexible substrate achieves 25-30um trace pitch by subtractive.
Vias for Interconnect

- Via size is reduced with Cu fully filled.

Padless?

Cu Filled Blind Via

- Padless structure could be achieved with Cu fully filled via.
Semi-Additive Bussless
For Non-Plating Buss Lines

- Material Selection/Applications
  - Adhesiveless Materials
  - 1-ML and 2-ML tapes

> Surface Morphology

- Negligible Cu under-cut was observed.
- Good wire bondability and Solderability were examined.
- TBGA (35x35mm) meets the reliability in MST-level3 (260°C) + PCT and HTS.
### Multi-Layer Flex Development

**Build-up 4-ML Tape Development**

<table>
<thead>
<tr>
<th>Unit</th>
<th>Inner Layer</th>
<th>Outer Layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min. Trace Width/Spacing (Signal layer)</td>
<td>um</td>
<td>30/30</td>
</tr>
<tr>
<td>Min. diameter of blind via hole (entry/Exit)</td>
<td>um</td>
<td>20/10</td>
</tr>
<tr>
<td>Min. diameter of blind via Capture Pad</td>
<td>um</td>
<td>70</td>
</tr>
<tr>
<td>Conductor Thickness</td>
<td>um</td>
<td>12</td>
</tr>
<tr>
<td>Dielectric Layer Thickness</td>
<td>um</td>
<td>50</td>
</tr>
<tr>
<td>Soldermask thickness</td>
<td>Um</td>
<td>--</td>
</tr>
<tr>
<td>Registration accuracy</td>
<td>um</td>
<td>+/-25</td>
</tr>
<tr>
<td>Total substrate thickness</td>
<td>um</td>
<td>185 +/-10%</td>
</tr>
</tbody>
</table>

**Build-up Dielectric Material**
- Dielectric constant: 3.4 at 1 GHz
- **Tg**: 153°C (TMA), 180°C (DMA)
- Dissipation factor: 0.023 at 1 GHz
- Dielectric strength: 2,200 V/mil

**Layer Construction:** 1+2+1
- FC DIE
- Outer SGN (L1)
- Inner SGN (L2)
- Inner GND (L3)
- Outer GND (L4)
- Via in Pad
- Core Dielectric

### Embedded Passives

**Embedded Etched Thin Film Resistor**

<table>
<thead>
<tr>
<th>No of Sq</th>
<th>0.5 (100X200)</th>
<th>1 (200X200)</th>
<th>1.5 (300X300)</th>
<th>2 (400X200)</th>
<th>3 (600X200)</th>
<th>4 (800X200)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rmin (Ω)</td>
<td>12.5</td>
<td>25.0</td>
<td>37.5</td>
<td>50.0</td>
<td>75.0</td>
<td>100</td>
</tr>
<tr>
<td>Rmax (Ω)</td>
<td>72.7</td>
<td>54.6</td>
<td>55.6</td>
<td>64.0</td>
<td>86.4</td>
<td>118.1</td>
</tr>
</tbody>
</table>

**Tolerance (%)**
- Rmin (Ω): 12.5 - 25.0: ±141%
- Rmax (Ω): 72.7 - 118.1: ±4.6%

- Etched tolerance will be significantly increased when the dimension of resistor is below 200um.
Embedded Passives

Embedded Plated Thin Film Resistor
Shipley Ni-P plating solution

- Resistors with high ratio of L/W (>2) have lower resistance tolerance and better linearity.

![Graph showing resistance values over time and square number]

- Equations:
  1. \( y = 12.015x \)
  2. \( y = 7.5185x \)
  3. \( y = 7.0246x \)

Embedded Thick Film Resistor
PTF Carbon ink

- Resistors with high ratio of L/W (>2) has lower resistance tolerance (<20%) and better linearity.

![Graph showing resistance values over time and square number]

- Reliability Test Items:
  - MSL-3 + PCT: -10%
  - Temperature Cycle: -12%
  - Humidity Storage: +11%
  - 300 Hrs (after baking): (+2.4%)
Embedded Capacitor
Electropolymers thick film dielectric paste (k=16)

- Capacitance density reaches 15.1 pF/mm² with a low tolerance (<5%) and good linearity.

Embedded Inductor
Planar Inductor formed by Cu pattern

- Planar Inductor on flex achieved a tolerance of <3%.
Flexible Substrates Development in IC Packaging

Tape Ball Grid Array (TBGA)

Package with High Thermal Performance

- High thermal dissipation at Theta Ja down to 7.8°C/W.
- 1-ML, 2-ML and multi-layer metal substrates are available for ASIC, MPU, etc.
Close Loop TBGA

Applications
- Increasing the circuit density with grounded heatsink
- One additional metal layer for electrical requirement

- Capability is demonstrated to be 0.2 mm space between spots for 1mm ball pitch with the tolerance of ±50um on spot diameter.

1.27mm Ball Pitch 1.00 mm Ball Pitch

Ni/Au Black oxide Ag

Flip Chip Tape BGA

- Thermal performance: > 6W
- Electrical performance: > 2.5GHz

- Flip chip TBGA with multi-layer flexible substrate will be for high pin-count packages.
Cavity-UP Enhanced BGA

Applications
- Alternative solution with Thermal performance to PBGA

- It is proven for lead-free and halogen-free applications with a Theta Ja of ~17°C/W at zero air flow for the thermal performance.
- Transfer molding is applicable with the same assembly process to PBGA.

Chip Scale Package (CSP)

Wire bonding and Flip chip CSP

- 1-ML or 2-ML tape
- Different interconnects

- TAB or wire bonding
- Sn/Au bonding
- Solder joint

- CSP is one of the main application for flexible substrates.
Stacked Chip Scale Package (CSP)

Stacked Chip Scale Package (CSP)

Folded flex CSP – Tessera design

UZM MCP Ball Stacked CSP

North NMTI design

UZ Folded-over Tape with Memory
Stacked CSP (1.4mm thick)

Advantages of LGA CSP vs normal tape CSP

» Improved board level reliability
» Better for ≤ 0.4mm ball pitch

Via Hole Structure for Solder Ball in CSP

Normal tape CSP

Land grid array/Stud grid array

Cu build-up height in via holes can be controlled in the range of 20-50 ± 5µm.

Table 96 - BGA and FPCA/CSP Package Potential PWB Solutions

<table>
<thead>
<tr>
<th></th>
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<th></th>
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<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Through-Pass (µm)</td>
<td>640</td>
<td>630</td>
<td>620</td>
<td>610</td>
<td>600</td>
<td>590</td>
<td>580</td>
<td>570</td>
<td>560</td>
<td>550</td>
<td>540</td>
</tr>
<tr>
<td>Through-Pass (µm)</td>
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<td>630</td>
<td>620</td>
<td>610</td>
<td>600</td>
<td>590</td>
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<td>620</td>
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</tr>
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<td>630</td>
<td>620</td>
<td>610</td>
<td>600</td>
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<td>600</td>
<td>590</td>
<td>580</td>
<td>570</td>
<td>560</td>
<td>550</td>
<td>540</td>
</tr>
<tr>
<td>Through-Pass (µm)</td>
<td>640</td>
<td>630</td>
<td>620</td>
<td>610</td>
<td>600</td>
<td>590</td>
<td>580</td>
<td>570</td>
<td>560</td>
<td>550</td>
<td>540</td>
</tr>
</tbody>
</table>

• Cu build-up height in via holes can be controlled in the range of 20-50 ± 5µm.

ITRS 2003
Lead-Free and Halogen-Free Products

Recommended Material Sets

<table>
<thead>
<tr>
<th>Material set</th>
<th>1-ML TBGA</th>
<th>2-ML TBGA</th>
<th>CSP Tape</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PI Base</strong></td>
<td>Any type</td>
<td>Any type</td>
<td>Any type</td>
</tr>
<tr>
<td><strong>Tape adhesive</strong></td>
<td>Tomegawa-X(^a) Toray 8600(^a)</td>
<td>---</td>
<td>Tomegawa-X(^a) Toray 8600(^a)</td>
</tr>
<tr>
<td><strong>Signal solder mask</strong></td>
<td>AUS-5, AUS-11, AUS-21(^a)</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td><strong>Ground solder mask</strong></td>
<td>---</td>
<td>AR-7100(^a) or Bare Cu</td>
<td>AUS-11, AUS-21(^a)</td>
</tr>
<tr>
<td><strong>Heatsink adhesive</strong></td>
<td>TSA-14(^a), TSA-51(^a), TSA-67(^a)</td>
<td>TSA-51(^a), TSA-67(^a)</td>
<td>---</td>
</tr>
</tbody>
</table>

Note: #: Halogen-free material
All solder mask are over Cu.

Liquid Crystal Polymer (LCP) Base Material

Characteristics of LCP over PI
- Stable low Dk at 2.9 and Df at 0.002 (1-10GHz) for high speed and high frequency
- Low moisture absorption at <0.4%

- Adhesiveless LCP TBGA has similar wire bondability and solderability performance to PI TBGA.
- Passed the reliability tests at substrate level for 1-ML and 2-ML LCP TBGA
  » MST-level 3 at 238°C and 260°C.
  » MST-level 3 at 238°C + PCT for 168 hrs
Cu Bumped Tape

Specifications
Ni/Au or Sn finish
75um bump diameter/160um bump pitch
bump height: 20-40 ± 2 um

Solder Bumped Tape

Solder Bumping on Substrate
Eutectic, high Pb, and lead-free (Sn-Cu, Sn-Ag) solder bumping
75um bump diameter/125um bump pitch
bump height: 80um ± 5um
Printing or plating

After Sn-Cu plating and dry film stripping  After solder reflow and flux residue cleaning
• Eutectic/ lead-free (Sn-Cu-Ag) solder bumping
• 50um bump diameter/70um bump pitch
• Au or Cu stud bumps on die
• Fluxless process
Fine Bump Pitch For Direct Flip Chip

130 um Via pitch, 100um Via size

80 um Via pitch, 60 um Via size

70 um Via pitch, 50 um Via size

Table 5: Package reliability based on continuity resistance for 8x8mm package

<table>
<thead>
<tr>
<th>No</th>
<th>Test Description</th>
<th>Reliability Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MIST L2 85°C/60% RH with 3R reflow 300°C based on I-STD-720</td>
<td>0/15</td>
</tr>
<tr>
<td>2</td>
<td>MIST L3 30°C/60% RH with 3R reflow 260°C based on I-STD-720</td>
<td>0/15</td>
</tr>
<tr>
<td>3</td>
<td>Temperature cycling condition A -40 to 85°C for 1000 cycles based on J/IS/322-A/05-0</td>
<td>0/15</td>
</tr>
<tr>
<td>4</td>
<td>Temperature cycling condition B -40 to 125°C for 1000 cycles based on J/IS/322-A/05-0</td>
<td>0/15</td>
</tr>
<tr>
<td>5</td>
<td>Thermal Shock Condition D -65 to 150°C for 20 cycles based on J/IS/322-A/05-0</td>
<td>0/15</td>
</tr>
<tr>
<td>6</td>
<td>Accelerated Moisture Resistance - Unbaked automotive condition C 122°C/100% RH 96hrs based on J/SS022-A/05-0</td>
<td>0/15</td>
</tr>
</tbody>
</table>

– TK Lee, et al ECTC, June 2004
Tape Substrate for RF Wireless

• Reel-to-reel tape process provides ±5-7μm tolerance in line width/space and 5% tolerance in thickness, good for RF.

<table>
<thead>
<tr>
<th>Property</th>
<th>Unit</th>
<th>FR4</th>
<th>GETEK</th>
<th>LTCC</th>
<th>PI Flex</th>
<th>Leadframe</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielectric constant, k</td>
<td></td>
<td>3.0~4.5@1GHz</td>
<td>3.82~4.2@1GHz</td>
<td>5.6~10@10MHz</td>
<td>3.6@2GHz</td>
<td></td>
</tr>
<tr>
<td>Loss Tangent</td>
<td>%</td>
<td>0.017~0.025@1GHz</td>
<td>0.0095@1GHz</td>
<td>0.001~0.002@10MHz</td>
<td>0.006@2GHz</td>
<td></td>
</tr>
<tr>
<td>Mechanical &amp; Thermal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Young’s Modulus</td>
<td></td>
<td>3~3.5 mpsi</td>
<td>980 kpsi</td>
<td>150-300GPa</td>
<td>800 kpsi</td>
<td></td>
</tr>
<tr>
<td>CTE</td>
<td>Ppm/°C</td>
<td>14~17</td>
<td>12~15</td>
<td>5.8~7</td>
<td>16</td>
<td>17</td>
</tr>
<tr>
<td>Tg</td>
<td>°C</td>
<td>135</td>
<td>180</td>
<td>-</td>
<td>&gt;350</td>
<td>-</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>W/mK</td>
<td>0.25</td>
<td>0.31</td>
<td>2~4.4</td>
<td>0.35</td>
<td></td>
</tr>
<tr>
<td>Metal</td>
<td>Cu</td>
<td>Cu</td>
<td>W/Ag</td>
<td>Cu</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Processing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Min. L/S (HDI)</td>
<td>μm</td>
<td>100/100 (75/75)</td>
<td>100/100 (75/75)</td>
<td>100/100 (75/75)</td>
<td>40/40 (25/25)</td>
<td>150/150</td>
</tr>
<tr>
<td>Min. via / land (HDI)</td>
<td>μm</td>
<td>200/350 (100/250)</td>
<td>200/350 (100/250)</td>
<td>200/250 (100/200)</td>
<td>30/100</td>
<td>N/A</td>
</tr>
<tr>
<td>Metal thickness</td>
<td>μm</td>
<td>&lt; 35</td>
<td>&lt; 35</td>
<td>&lt; 15</td>
<td>&lt; 35</td>
<td>150</td>
</tr>
<tr>
<td>Process precision</td>
<td></td>
<td>Medium</td>
<td>Medium</td>
<td>Low</td>
<td>High</td>
<td>Medium</td>
</tr>
<tr>
<td>Cavity capability</td>
<td></td>
<td>Routing</td>
<td>Routing</td>
<td>Punch</td>
<td>Punch</td>
<td>Etch</td>
</tr>
</tbody>
</table>
Tape Substrate for RF Wireless

Vias in GETEK laminate for RF wireless

- 2-layer through hole
- 4-layer through hole
- 4-layer HDI through hole and via
- 4-layer HDI through hole and

Flex microvias:
- Consumes only 16% of drilled via area
- Consumes only 49% of HDI microvias area

10x9mm Quad Band w/integrated Power Control

COF For LCD Display

- Current Fine pitch COF Production (L/S = 15/15)
- Camera module demand for cell phone

- Flex/tape is exclusive choice for bending and dynamic applications.
Impedance-Controllable Flex

Reel-to-reel process for impedance control

<table>
<thead>
<tr>
<th>Simulated Impedance (Ohm)</th>
<th>Trace Width (um)</th>
<th>Trace Thickness (um)</th>
<th>PI Thickness (um)</th>
<th>SM Thickness (um)</th>
<th>Measured Differential Impedance (Ohm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal Differential</td>
<td>Sample 1</td>
<td>Sample 2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>96.3</td>
<td>50</td>
<td>18</td>
<td>40</td>
<td>Min. 102.1</td>
</tr>
<tr>
<td>100</td>
<td>94.4</td>
<td>25</td>
<td>12</td>
<td>25</td>
<td>Max. 107.5</td>
</tr>
</tbody>
</table>

• Reel-to-Reel process easily produces controlled differential impedance at tight tolerances with better line width control.

Summary

Flexible substrate provides

• Finer trace pitch and blind via, providing HDI for IC Packages
• Well adapt to cavity packages and exclusive to the bending requirement
• Multi-layer and embedded passives to narrow the gap to HDI laminate
• Good solution for driving small form factor
• Good process for high volume/low cost in roll-to-roll & reel-to-reel format
• New base materials, such as LCP etc, will widen the applications of flexible substrate